Winbond Electronics Corp.

150MHZ CLOCK FOR WHITNEY CHIPSET

1.0 GENERAL DESCRIPTION

The W83194AR-73 is a Clock Synthesizer for Intel Whitney chipset. W83194AR-73 provides all clocks required for high-speed RISC or CISC microprocessor and also provides 32 different frequencies of CPU, SDRAM, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

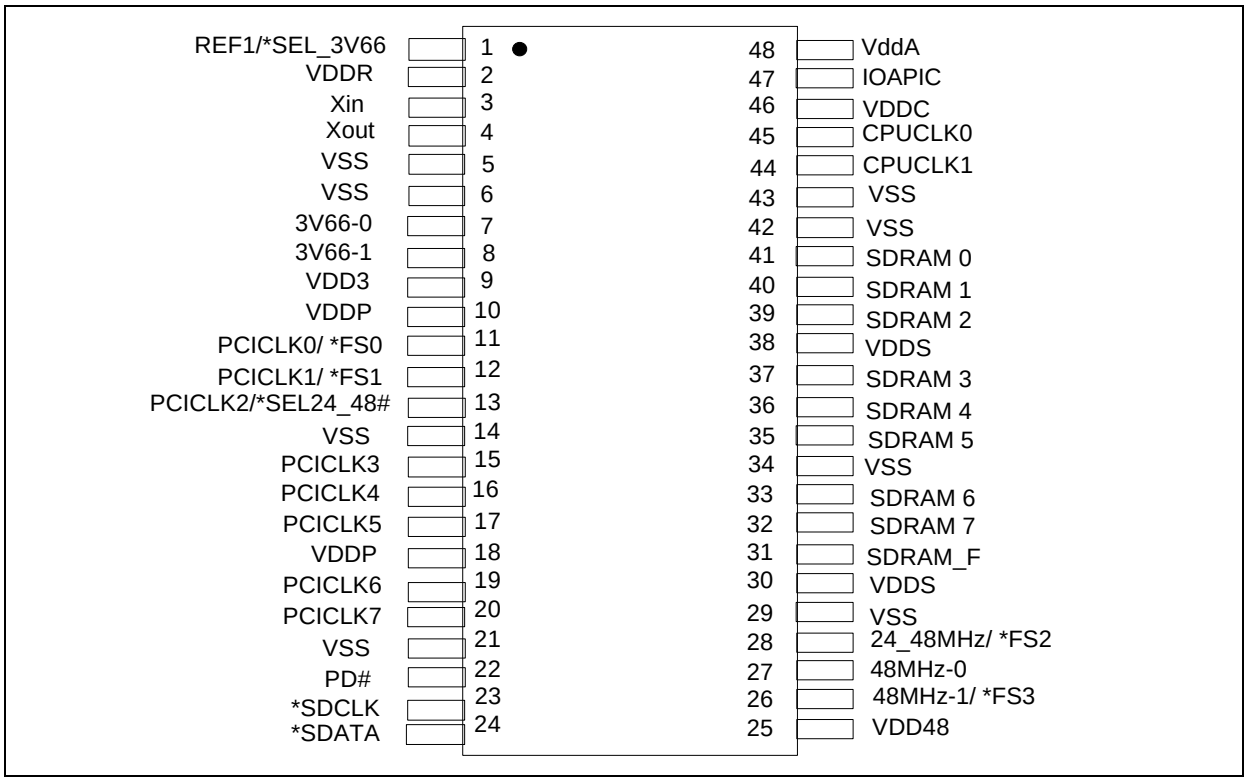
The W83194AR-73 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.25% center and 0-0.5% down type spread spectrum to reduce EMI.

The W83194AR-73 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50¡Ó 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

1.0 PRODUCT FEATURES

- 2 CPU clocks
- 9 SDRAM clocks for 2 DIMMs
- 8 PCI synchronous clocks.
- Optional single or mixed supply:
  (VDDR = VDDP=VDDS = VDD48 = VDD3 = 3.3V, VDDA=VDDC=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 150MHz
- I^2C 2-Wire serial interface and I^2C read back
- 0.25% center and 0-0.5% down type spread spectrum
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 48-pin SSOP

3.0 PIN CONFIGURATION



4.0 FREQUENCY SELECTION BY HARDWARE

FS3	FS2	FS1	FS0	CPU(MHz)	SDRAM (MHz)	3V66 (MHz)		PCI(MHz)	IOAPIC (MHz)
						SEL_3V66=0	SEL_3V66=1		
0	0	0	0	100.23	100.23	66.82	**66.82**	33.41	16.71
0	0	0	1	100.9	100.9	67.26	67.26	33.63	16.815
0	0	1	0	105	105	70	70	35	17.5
0	0	1	1	66.89	100.33	66.89	66.89	33.44	16.72
0	1	0	0	120	120	64	80	40	20.00
0	1	0	1	124	124	64	82.66	41.33	20.67
0	1	1	0	133.3	133.3	**66.65**	88.86	44.43	22.22
0	1	1	1	**133.6**	**100.2**	**66.65**	**66.65**	33.32	16.66
1	0	0	0	140	140	70	70	35	17.5
1	0	0	1	150	150	64	75	37.50	18.75
1	0	1	0	114.99	114.99	64	76.66	38.33	19.17
1	0	1	1	70	105	70	70	35	17.5
1	1	0	0	75	112.5	64	75	37.5	18.75
1	1	0	1	83.31	124.96	64	83.31	41.65	20.825
1	1	1	0	90	90	60	60	30	15
1	1	1	1	95	95	63.33	63.33	31.67	15.84

5.0 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

5.1 Register 0: CPU Frequency Select Register

Bit	@PowerUp	Pin	Description
7	0	-	0 = ¡ó0.25% Center type Spread Spectrum Modulation 1 = 0~ 0.5% Down type Spread Spectrum Modulation
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit (2, 6:4), **Register1 Bit1**
2	0	-	SSEL3 (Frequency table selection by software via I^2C)
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	0 = Running 1 = Tristate all outputs

5.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	**X**	**-**	**FS3#**
6	**X**	**-**	**FS0#**
5	**X**	**-**	**FS2#**
4	1	28	24_48MHz(Active / Inactive)
3	1	27	48MHz-0(Active / Inactive)
2	1	26	48MHz-1(Active / Inactive)
1	**1**	**-**	**SEL_3V66(Frequency table selection by software via I^2C)**
0	1	31	SDRAM_F(Active / Inactive)

5.3 Register 2: SDRAM Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	32	SDRAM7 (Active / Inactive)
6	1	33	SDRAM6 (Active / Inactive)
5	1	35	SDRAM5 (Active / Inactive)
4	1	36	SDRAM4 (Active / Inactive)
3	1	37	SDRAM3 (Active / Inactive)
2	1	39	SDRAM2 (Active / Inactive)
1	1	40	SDRAM1 (Active / Inactive)
0	1	41	SDRAM0 (Active / Inactive)

5.4 Register 3: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	20	PCICLK7 (Active / Inactive)
6	1	19	PCICLK6 (Active / Inactive)
5	1	17	PCICLK5 (Active / Inactive)
4	1	16	PCICLK4 (Active / Inactive)
3	1	15	PCICLK3 (Active / Inactive)
2	1	13	PCICLK2 (Active / Inactive)
1	1	12	PCICLK1 (Active / Inactive)
0	1	11	PCICLK0 (Active / Inactive)

5.5 Register 4: Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	**X**	**-**	**SEL_3V66#**
6	1	8	3V66_1(Active / Inactive)
5	1	7	3V66_0(Active / Inactive)
4	**0**	**-**	**Reserve**
3	1	47	IOAPIC (Active / Inactive)
2	**X**	**-**	**FS1#**
1	1	44	CPUCLK1(Active / Inactive)
0	1	45	CPUCLK0(Active / Inactive)

5.6 Register 5: Reserve Register

Bit	@PowerUp	Pin	Description
7	0	-	Reserve
6	0	-	Reserve
5	0	-	Reserve
4	0	-	Reserve
3	0	-	Reserve
2	0	-	Reserve
1	0	-	Reserve
0	0	-	Reserve

5.7 Register 6: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	1	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	1	-	Winbond Chip ID
0	0	-	Winbond Chip ID

5.8 Register 7: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	1	-	Winbond Chip ID
0	0	-	Winbond Chip ID

6.0 SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V_{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

6.2 AC CHARACTERISTICS

VddR=Vdd3=VddP=VddS=3.3V – 5 %, VddC = VddA= 2.375V~2.9V , T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	t_{OFF}	1		4	ns	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	t_{SKEW}			250	ps	15 pF Load Measured at 1.5V
CPU/SDRAM Cycle to Cycle Jitter	t_{CCJ}			¡Ó250	ps	
CPU/SDRAM Absolute Jitter	t_{JA}			500	ps	
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time	t_{TLH} t_{THL}	0.4		1.6	ns	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	V_{over}	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	Ring Back must not enter this range.

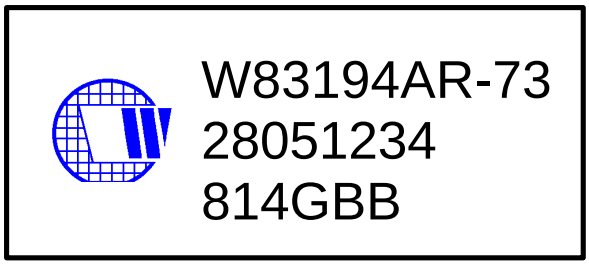
6.3 DC CHARACTERISTICS

VddR=Vdd3=VddP=VddS=3.3V – 5 %, VddC = VddA= 2.375V~2.9V , T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input Low Voltage	V_{IL}	Vss-0.3		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		Vdd +0.3	V_{dc}	
Input Low Current (no pull-up Resistors)	I_{IL}	-5	2.0		µA	
Input Low Current (pull-up Resistors)	I_{IL}	-200	-100		µA	
Input High Current	I_{IH}	-5		5	µA	
Operating Current	I_{DD}		60	100	mA	@66M
Power Down Current	I_{DDPD}		400	600	µA	C_L= 0pF
Input Frequency	Fi		14.318		MHz	Vdd=3.3V
Pin Inductance	Lpin		7		nH	
Input Capacitance	C_{IN}			5	pF	Logic Inputs
	C_{OUT}		6		pF	Output pins capacitance
	C_{INX}	13.5		22.5	pF	X1 & X2 pins
Transition Time	T_{Tra}			3	mS	
Disable/Enable Delay	T	1		10	nS	
Clock stabilization	T_{STA}			3	mS	

7.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194AR-73	48 PIN SSOP	Commercial, 0°C to +70°C

8.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194AR-73

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

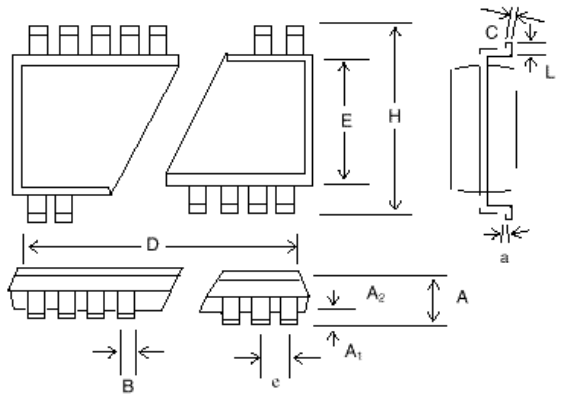
814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

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9.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668

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