W7500P Reference Manual

Version 1.0.3

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1 Documentation conventions

1.1 Glossary

ARP	Address Resolution Protocol
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
AFC	Alternate Function Controller
ADC	Analog-to-Digital Converter
BOD	BrownOut Detection
CPU	Central Processing Unit
CRG	Clock Reset generator
DMA	Direct Memory Access
EOP	End Of Packet
EXTINT	External Interrupt
GPIO	General Purpose Input/Output
IrDA	Infrared Data Association
I/O	Input/Output
ICMP	Internet Control Message Protocol
IGMP	Internet Group Management Protocol
IPv4	Internet Protocol version 4
IRQ	interrupt request
NMI	NonMaskable Interrupt
PADCON	Pad Controller
PLL	Phase-Locked Loop
PHY	Physical Layer
PPPoE	Point-to-Point Protocol over Ethernet
POR	Power Of Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
RNG	Random number generator
SR	Status Register
SSP	Synchronous Serial Port

SYSCFG	System configuration controller
TOE	TCPIPCore Offload Engine
TTL	Transistor-Transistor Logic
TCP	Transmission Control Protocol
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UDP	User Datagram Protocol
WOL	Wake On Lan
WDT	Watchdog Timer

1.2 Register Bit Conventions

Each register is shown with a key indicating the accessibility of the each individual bit, and the initial condition:

Key	Bit Accessibility
rw	Read/Write
r	Read Only
r0	Read as 0
r1	Read as 1
W	Write Only

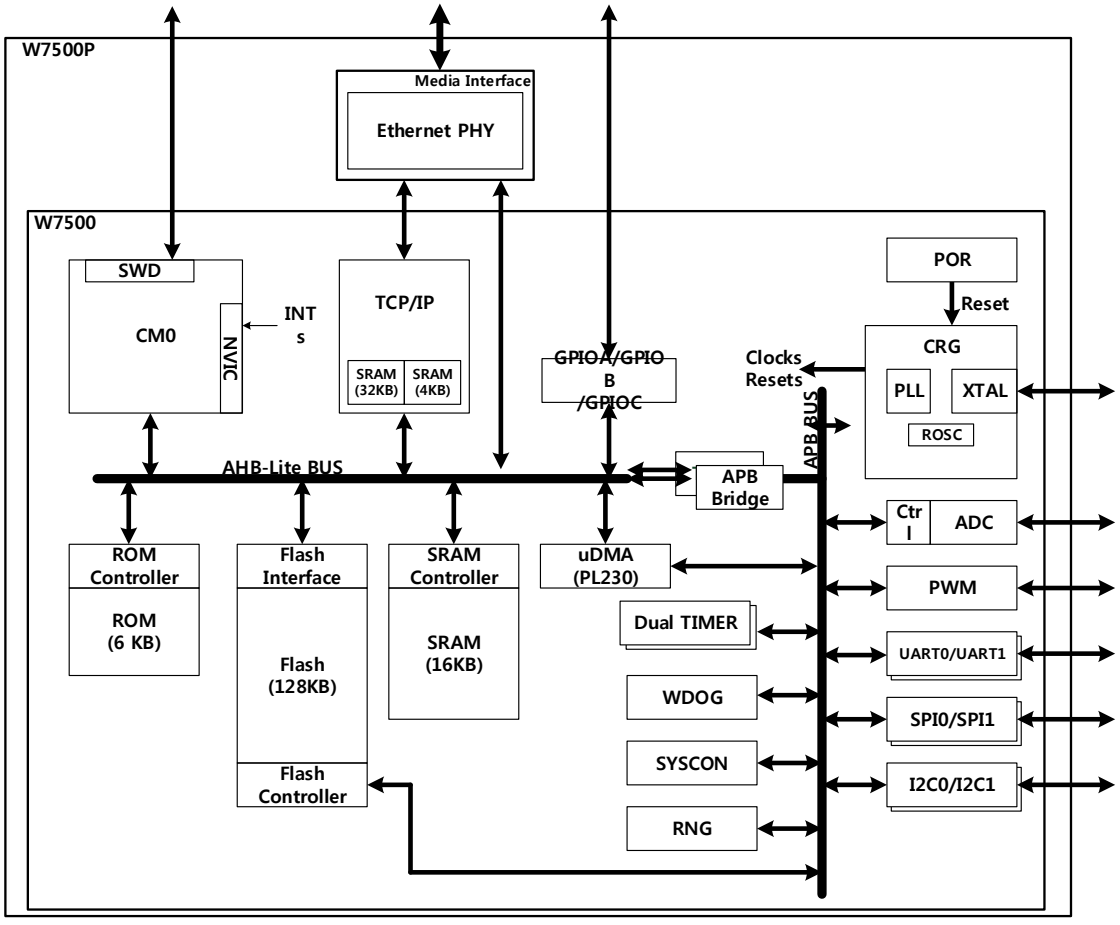
2 System and memory overview

2.1 System architecture

Main system consists of :

- Ethernet :
  - IP101G
- Two masters :
  - Cortex-M0 core
  - uDMAC (PL230, 6channel)
- Ten slaves :
  - Internal BOOT ROM
  - Internal SRAM
  - Internal Flash memory
  - Two AHB2APB bridge which connects all APB peripherals
  - Four AHB dedicated to 16bit GPIOs
  - TCPIP Hardware core

System architecture and AHB-Lite bus architecture shown in



.

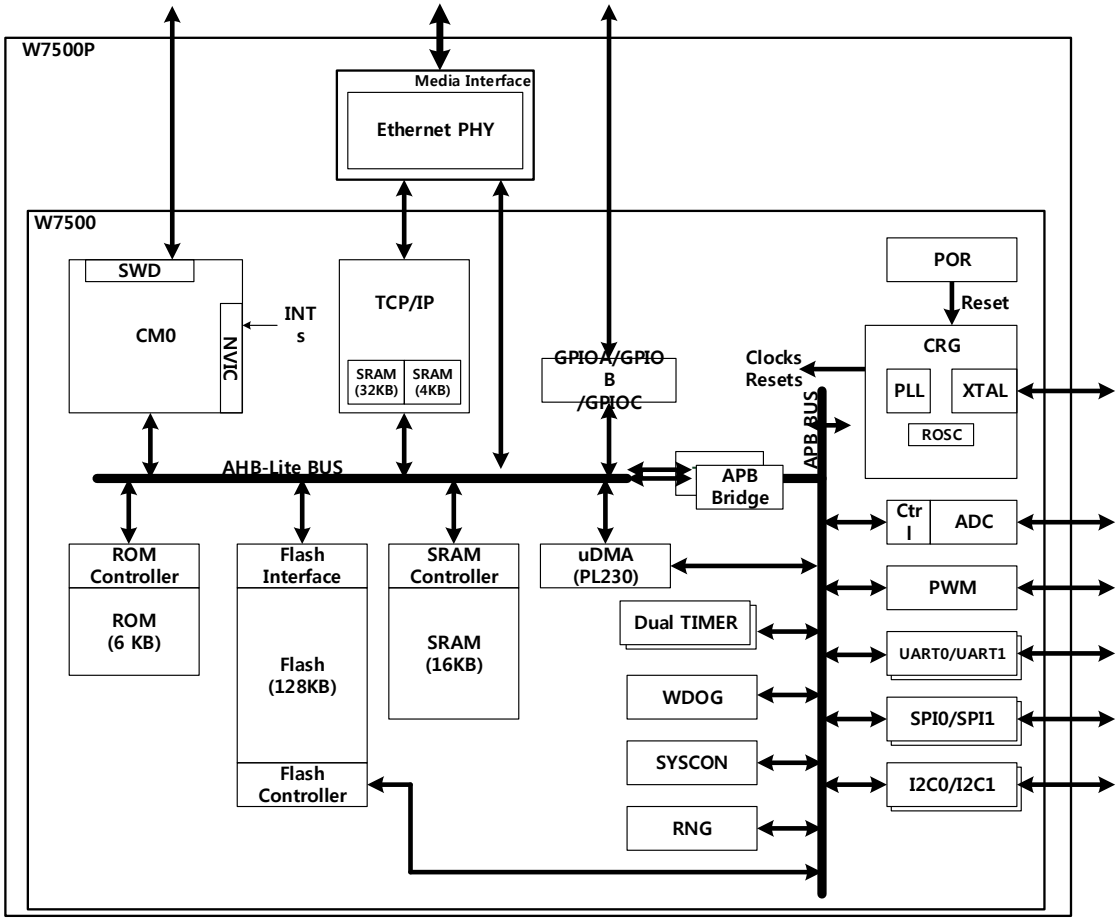


Figure 1 W7500P System Architecture

AHB-Lite BUS

- This bus connects the two masters (Cortex-M0 and uDMAC) and ten AHB slaves.

Two APB BUSs

- These buses connect Seventeen APB peripherals (Watchdog, two dual timers, pwm, two UARTs, simple UART, two I2Cs, two SSPs, random number generator, real time clock, 12bits analog digital converter, clock controller, IO configuration, PAD MUX controller)

2.2 Memory organization

2.2.1 Introduction

Program memory, data memory, registers and I/O ports are organized within the same linear 4-Gbyte address space.

The bytes are coded in memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

2.2.2 Memory map

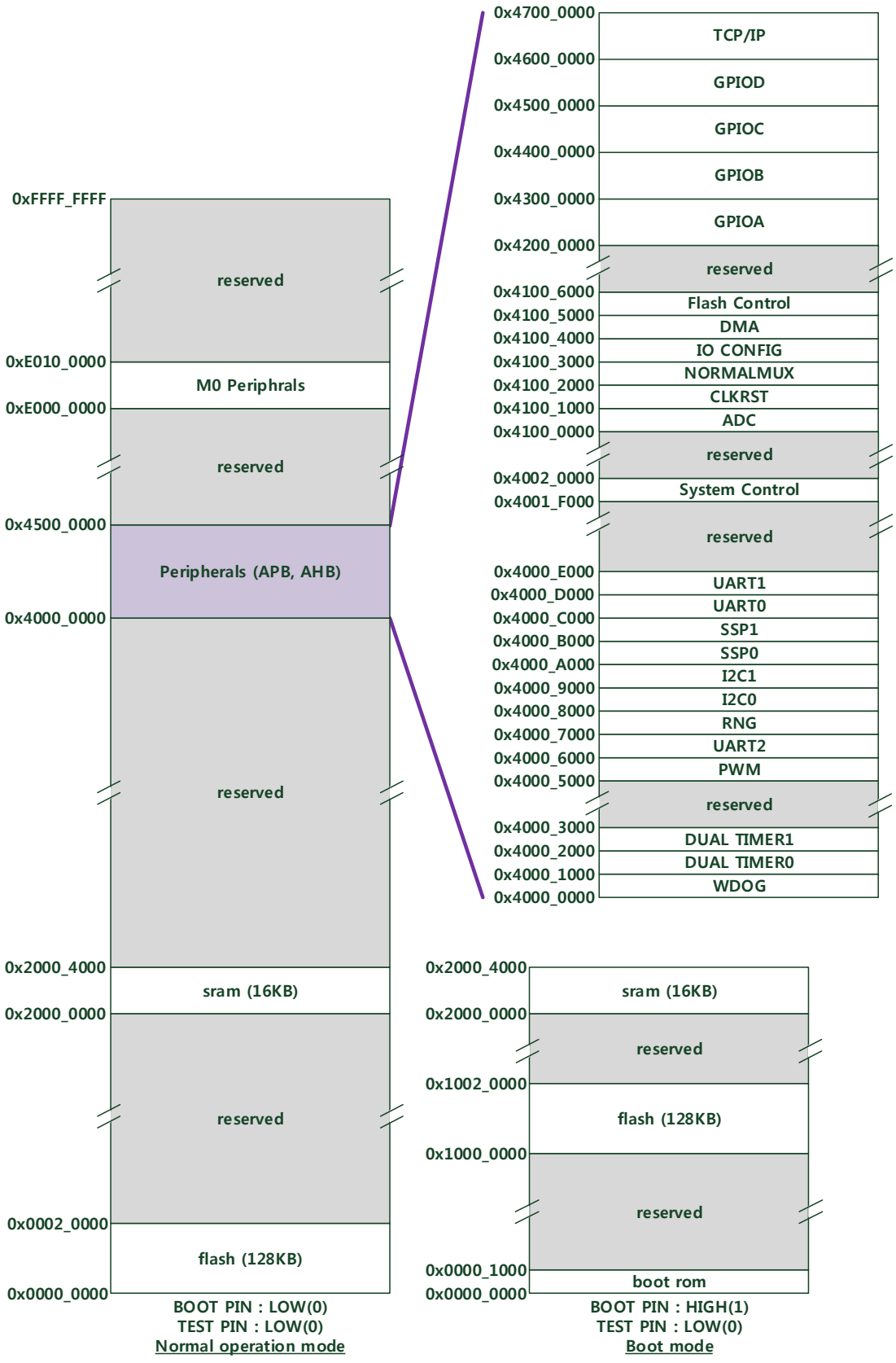


Figure 2 W7500P memory map

3 System configuration controller (SYSCFG)

3.1 Introduction

Main purposes of the system configuration controller are the following

- Control of the memory remap feature
- The ability to enable an automatic reset if the system locks up
- Information about the cause of the last reset

3.2 Registers (Base address : 0x4001_F000)

3.2.1 REMAP register

Address offset : 0x000

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	REMAP	
														R/W	

[1:0] REMAP – Memory mapping selection bits

These bits are written by S/W to set memory mapping at address 0x0000_0000. These bits are only updated after CM0 executes system reset command.

And REMAP is restored to reset value (01) automatically after WDOG Reset.

00 : Flash memory mapped at 0x0000_0000

01 : Boot rom mapped at 0x0000_0000

10 : reserved

11 : Noting mapped at 0x0000_0000

3.2.2 RESETOP register

Address offset : 0x008

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RESETOP
															R/W

[0] RESETOP – Enable the reset controller to generate a system reset automatically if the system locks up.

This bit is written by S/W.

0 : Does not automatically generate reset when the processor is in the LOCKUP state.

1 : Automatically generates system reset if the processor is in the LOCKUP state.

3.2.3 RSTINFO register

Address offset : 0x010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	RSTINFO		
													R/CW1		

[2:0] RSTINFO – Information register about the cause of the last reset.

These bits are written by S/W; write 1 to each bit to clear

[0] : if 1, SYSRESETREQ caused the reset.

[1] : if 1, Watchdog caused the reset.

[2] : if 1, processor LOCKUP caused the reset.

4 Interrupt and events

4.1 Introduction

W7500P contains interrupt service and event service as below

- 26ea interrupt request (IRQ) lines.
- One NonMaskable Interrupt (NMI).
- One event signal

4.2 Interrupt assignments

Table 1 describes the W7500P interrupt assignments.

Table 1 W7500P interrupt assignments

IRQ/NMI	Device	Description	Address
NMI	Watchdog	Watchdog interrupt	0x0000_0008
IRQ[0]	SSP0	SSP0 global interrupt	0x0000_0040
IRQ[1]	SSP1	SSP1 global interrupt	0x0000_0044
IRQ[2]	UART0	UART0 global interrupt	0x0000_0048
IRQ[3]	UART1	UART1 global interrupt	0x0000_004C
IRQ[4]	UART2	UART2 global interrupt	0x0000_0050
IRQ[5]	I2C0	I2C0 global interrupt	0x0000_0054
IRQ[6]	I2C1	I2C1 global interrupt	0x0000_0058
IRQ[7]	GPIO0	GPIOA global interrupt	0x0000_005C
IRQ[8]	GPIO1	GPIOB global interrupt	0x0000_0060
IRQ[9]	GPIO2	GPIOC global interrupt	0x0000_0064
IRQ[10]	GPIO3	GPIOD global interrupt	0x0000_0068
IRQ[11]	DMA	DMA channel 1 ~ channel 5 interrupt	0x0000_006C
IRQ[12]	Dualtimer0	Dualtimer0 global interrupt	0x0000_0070
IRQ[13]	Dualtimer1	Dualtimer1 global interrupt	0x0000_0074
IRQ[14]	PWM0	PWM0 global interrupt	0x0000_0078
IRQ[15]	PWM1	PWM1 global interrupt	0x0000_007C
IRQ[16]	PWM2	PWM2 global interrupt	0x0000_0080
IRQ[17]	PWM3	PWM3 global interrupt	0x0000_0084
IRQ[18]	PWM4	PWM4 global interrupt	0x0000_0088
IRQ[19]	PWM5	PWM5 global interrupt	0x0000_008C
IRQ[20]	PWM6	PWM6 global interrupt	0x0000_0090
IRQ[21]	PWM7	PWM7 global interrupt	0x0000_0094
IRQ[22]	reserved		0x0000_0098
IRQ[23]	ADC	ADC acquisition end interrupt	0x0000_009C
IRQ[24]	TCPIP	TCPIP global interrupt	0x0000_00A0
IRQ[25]	EXT_INT	External pin interrupt	0x0000_00A4
IRQ[26]	reserved		0x0000_00A8
IRQ[27]	reserved		0x0000_00AC
IRQ[28]	reserved		0x0000_00B0
IRQ[29]	reserved		0x0000_00B4
IRQ[30]	reserved		0x0000_00B8
IRQ[31]	reserved		0x0000_00BC

4.3 Event

W7500P is able to handle internal events in order to wake up the core(WFE). The wakeup event can be generated by

- When after DMA process finished

5 Power supply

5.1 Introduction

W7500P embeds a voltage regulator in order to supply the internal 1.5V digital power domain.

- Require a 2.7V ~ 5.5V operating supply voltage (VDD)
- ADC ref voltage is same as VDD

5.2 Voltage regulator

The voltage regulator is always enabled after Reset and works in only one mode.

- In Run mode, the regulator supplies full power to the 1.5V domain.
- There is no power down or sleep mode

5.3 Power supply supervisor

W7500P has an integrated reset (POR) circuit which is always active and ensures proper operation above a threshold of 0.6V

- The POR monitors only the VDD supply voltage. During the startup phase VDD must arrive first and be greater or equal to 0.6V

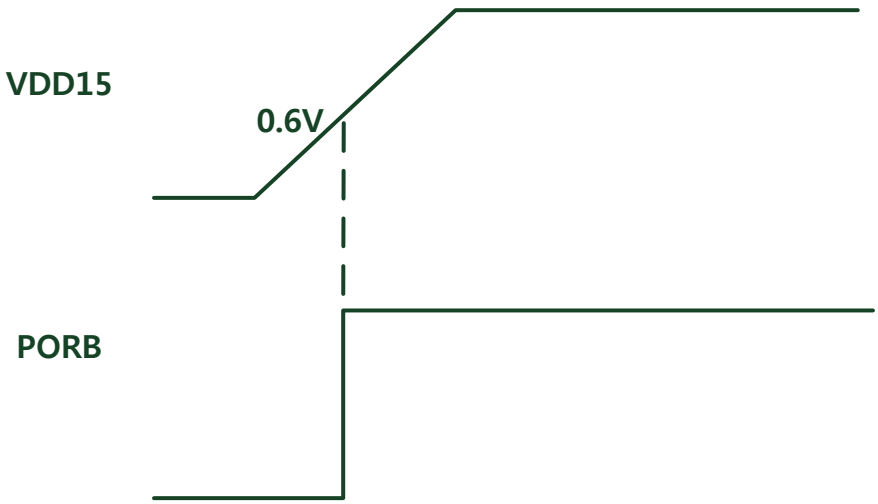


Figure 3 POR reset waveform

5.4 Low-power modes

W7500P is in RUN mode after a system or power reset. There are two low power modes to save power when the CPU does not need to be kept running. These modes are useful for instances like when the CPU is waiting for an external interrupt. Please note that there is no power-off mode for W7500P.

The device features two low-power modes:

- Sleep mode
- Deep Sleep mode

Additionally, the power consumption can be reducing by following method:

- User can slow down the system clocks
- User can gate the clocks to the peripherals when they are unused.

5.4.1 Sleep mode

W7500P has two kinds of sleep modes. One is Sleep mode and the other is Deep sleep mode. Two of them are almost the same except the clock gated peripherals kinds. Table 2 shows the Sleep mode summary.

Table 2 W7500P sleep mode summary

Mode	Entry	Wakeup	Effect on clocks
Sleep mode	DEEPSLEEP = 0 Enable WFI	Any interrupt	CPU clock OFF APB Bus Clock ON AHB Bus clock ON Memory clocks ON
	DEEPSLEEP = 0 Enable WFE	Wakeup event	
Deep Sleep mode	DEEPSLEEP = 1 Enable WFI	Any interrupt	CPU clock OFF APB Bus Clock OFF AHB Bus clock OFF Memory clocks OFF
	DEEPSLEEP = 1 Enable WFE	Wakeup event	

5.4.2 Peripheral clock gating

In Run mode, individual clocks can be stopped at any time to reduce power.

Peripheral clock gating is controlled by the CRG block.

Below is the list of clocks which can be gating in CRG block.

- ADC clock (ADCCLK)
- SSP0, SSP1 clock (SSPCLK)

- UART0, UART1 clock (UARTCLK)
- Two Timer clocks (TIMCLK0, TIMCLK1)
- 8ea PWM clocks (PWMCLK0 ~ PWMCLK7)
- WDOG clock (WDOGCLK)
- Random number generator clock (RNGCLK)

6 System tick timer

6.1 Introduction

System tick timer(SysTick) is part of the ARM Cortex-M0 core

6.2 Features

Simple 24bit timer.

Clocked internally by the system clock or the system clock/2.

6.3 Functional description

The SysTick timer is an integral part of Cortex-M0. The SysTick timer is intended to generated a fixed 10 millisecond interrupt for use by an operating system or other system management software.

Since the SysTick timer is a part of the Cortex-M0, it facilitates porting of software by providing a standard timer that is available on Cortex-M0 based devices. The SysTick timer can be used for :

- An RTOS tick timer which fires at a programmable rate (for example 100 Hz) and invokes a SysTick routine.
- A high-speed alarm timer using the core clock.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

6.4 Registers (Base : 0xE000_E000)

6.4.1 System Timer control and status register (SYST_CSR)

Address Offset : 0x010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CNTFLAG
															R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TICKINT	ENABLE
														R/W	R/W

[0] ENABLE – Enables the counter

0 : Counter disabled

1 : Counter enabled

[1] TICKINT – Enables SysTick exception request

O : Counting down to zero does not assert the SysTick exception request

1 : Counting down to zero to asserts the SysTick exception request

[16] COUNTFLAG – Returns 1 if timer counted to 0 since the last read of this register.

6.4.2 SysTick Reload Value Register (SYST_RVR)

Address Offset : 0x014

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	RELOAD[23:16]							
								R							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RELOAD[15:0]															
R															

[23:0] RELOAD – Value to load into the SYST_CVR when the counter is enabled and when it reaches 0

- The RELOAD value can be any value in the range 0x0000_0001 – 0x00FFFFFF. You can program a value of 0, but this has no effect because the SysTick exception request and COUNTFLAG are activated when count from 1 to 0.

- To generate a multi-short timer with a period of N processor clock cycles, use a RELOAD value of N-1. For example, if the SysTick interrupt is required every 100 clock pulses, set RELOAD to 99.

6.4.3 SysTick Current Value Register (SYST_CVR)

Address Offset : 0x018

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	CURRENT[23:16]							
								R/W							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT [15:0]															
R/W															

[23:0] CURRENT – Reads return the current value of the SysTick counter.

A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.

6.4.4 SysTick Calibration Value Register (SYST_CALIB)

Address Offset : 0x01C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NORF	SKEW	res	res	res	res	res	res	TENMS[23:16]							
R	R							R							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TENMS [15:0]															
R															

[23:0] TENMS - Reads as zero. Indicates calibration value is not known.

[30] SKEW - Reads as one. Calibration value for the 10ms inexact timing is not known because TENMS is not known. This can affect the suitability of SysTick as a software real time clock.

[31] NOREF - Reads as one. Indicates that no separate reference clock is provided.

7 TCPIPCore Offload Engine (TOE)

7.1 Introduction

The TCP/IPCore Offlead Engine (TOE) is a Hardwired TCP/IP embedded Ethernet controller that provides easier Internet connection to embedded systems. TOE enables users to have Internet connectivity in their applications by using the TCP/IP stack.

WIZnet's Hardwired TCP/IP is the market-proven technology that supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE protocols. TOE embeds the 32Kbyte internal memory buffer for the Ethernet packet processing. Using TOE allows users to implement the Ethernet application by adding the simple socket program. It's faster and easier than using any other Embedded Ethernet solutions. 8 independent hardware sockets can be used simultaneously.

TOE also provides WOL (Wake on LAN) to reduce power consumption of the system.

7.2 Features

- Supports Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Supports 8 independent sockets simultaneously
- Supports Power down mode
- Supports Wake on LAN over UDP
- Internal 32Kbytes Memory for TX/RX Buffers
- Not supports IP Fragmentation

7.3 Functional description

Figure 4 shows the TOE block diagram.

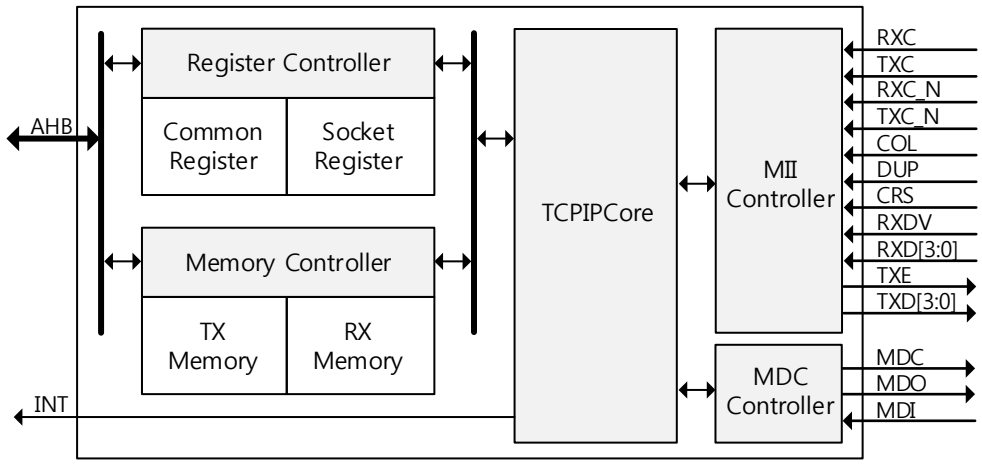


Figure 4 TOE block diagram

7.4 TOE Memory map

TOE has one Common Register Block, eight Socket Register Blocks, and TX/RX Buffer Blocks allocated to each Socket. Figure 5 shows the selected block by the base address and the available offset address range of Socket TX/RX Buffer Blocks. Each Socket's TX Buffer Block physically exists in one 16KB TX memory and is initially allocated with 2KB. Also, Each Socket's RX Buffer Block physically exists in one 16KB RX Memory and is initially allocated with 2KB.

Regardless of the allocated size of each Socket TX/RX Buffer, it can be accessible within the 16 bits offset address range (From 0x0000 to 0xFFFF).

Refer to 'Chapter 7.4.3' for more information about 16KB TX/RX Memory organization and access method.

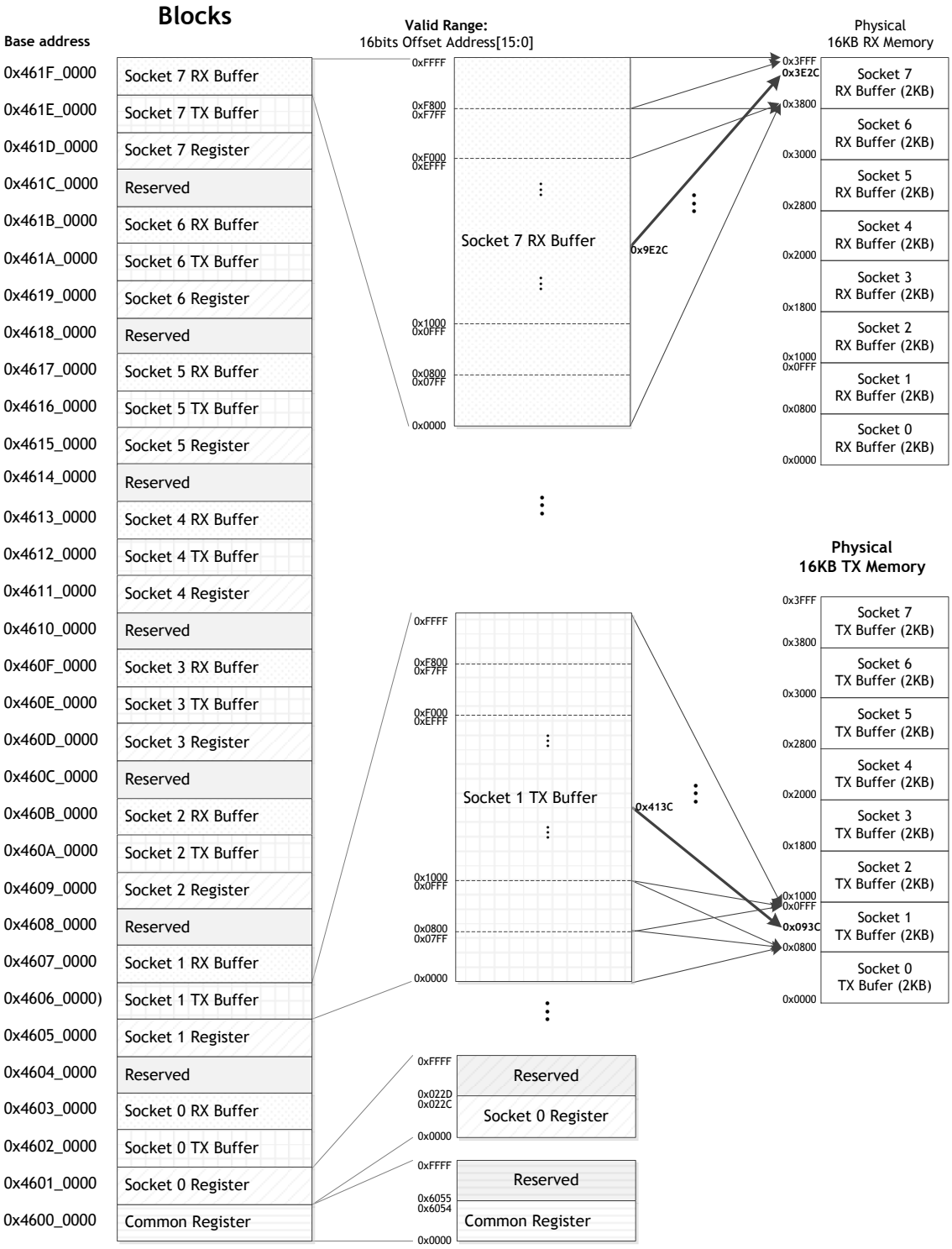


Figure 5. Register & Memory Organization

7.4.1 Common register map

Common Register Block configures the general information of TOE such as IP and MAC address. <Table 3> defines the offset address of registers in this block. Refer to 'Chapter7.5' for more details about each register.

Table 3. Offset Address for Common Register

Address	Register
0x0000	TOE Version (VERSIONR)
0x2000	TICKCLOK (TCLKR)
0x2100	Interrupt (IR)
0x2104	Interrupt Mask (IMR)
0x2108	Interrupt Clear (IRCR)
0x2110	Socket Interrupt (SIR)
0x2114	Socket Mask (SIMR)
0x2300	Mode (MR)
0x2400	PPP Timer (PTIMER)
0x2404	PPP Magic (PMAGIC)
0x2408	PPP Destination MAC Address (PHAR1)
0x240C	PPP Destination MAC address (PHAR0)
0x2410	PPP Session Identification (PSIDR)
0x2414	PPP Maximum Segment Size (PMSS)
0x6000	Source Hardware Address (SHAR1)
0x6004	Source Hardware Address (SHAR0)
0x6008	Gateway Address (GA)
0x600C	Subnet Mask (SUB)
0x6010	Source IP Address (SIP)
0x6020	Network Configuration Lock (NCONFL)
0x6040	Retry Time (RTR)
0x6044	Retry Counter (RCR)
0x6050	Unreachable IP Address (UIP)
0x6054	Unreachable Port Address (UPORT)

7.4.2 Socket register map

TOE supports 8 Sockets for communication channel. Each Socket is controlled by Socket n Register (n = 0,…,7 ,where n is socket number). <Table 2> defines the 16bits Offset Address of registers in Socket n Register Block.

Refer to 'Chapter 7.4.2' for more details about each register.

Table 4. Offset Address in Socket n Register Block (n = 0,…,7, where n is Socket number)

Offset	Register
0x0000	Socket Mode (Sn_MR)
0x0010	Socket Command (Sn_CR)
0x0020	Socket Interrupt (Sn_IR)
0x0024	Socket Interrupt Mask (Sn_IMR)
0x0028	Socket Interrupt Clear (Sn_ICR)
0x0030	Socket Status (Sn_SR)
0x0100	Socket Protocol Number (Sn_PNR)
0x0104	Socket IP Type of Service (Sn_TOS)
0x0108	Socket TTL (Sn_TTLR)
0x010C	Socket Fragment Offset (Sn_FRAG)
0x0110	Socket Maximum Segment (Sn_MSSR)
0x0114	Socket Port Number (Sn_PORTR)
0x0118	Socket Destination Hardware address0 (Sn_DHAR0)
0x011C	Socket Destination Hardware address1 (Sn_DHAR1)
0x0120	Socket Destination Port Number (Sn_DPORTR)
0x0124	Socket Destination IP Address (Sn_DIPR)
0x0180	Socket Keep Alive Timer (Sn_KATMR)
0x0184	Socket Retry Time (Sn_RTR)
0x0188	Socket Retry Counter (Sn_RCR)
0x0200	Socket TX Memory Size (Sn_TXBUF_SIZE)
0x0204	Socket TX Free Size (Sn_TX_FSR)
0x0208	Socket TX Read Pointer (Sn_TX_RD)
0x020C	Socket TX Write Pointer (Sn_TX_WR)
0x0220	Socket RX Memory Size (Sn_RXBUF_SIZE)
0x0224	Socket RX Received Size (Sn_RX_RSR)
0x0228	Socket RX Read Pointer (Sn_RX_RD)
0x022C	Socket RX Write Pointer (Sn_RX_WR)

7.4.3 Memory

TOE has one 16KB TX memory for Socket n TX Buffer Blocks and one 16KB RX memory for Socket n RX buffer Blocks.

16KB TX memory is initially allocated in 2KB size for each Socket TX Buffer Block (2KB X 8 = 16KB). The initial allocated 2KB size of Socket n TX Buffer can be re-allocated by using ‘Socket n TX Buffer Size Register (Sn_TXBUF_SIZE)’.

Once all Sn_TXBUF_SIZE registers have been configured, Socket TX Buffer is allocated with the configured size of 16KB TX Memory and is assigned sequentially from Socket 0 to Socket 7. Its physical memory address is automatically determined in 16KB TX memory. Therefore, the total sum of Sn_TXBUF_SIZE should not exceed 16 in case of error in data transmission.

The 16KB RX memory allocation method is the same as the 16KB TX memory allocation method. 16KB RX memory is initially allocated into 2KB size for each Socket RX Buffer Block (2KB X 8 = 16KB). The initial allocated 2KB size of Socket n RX Buffer can be re-allocated by using 'Socket n RX Buffer Size Register (Sn_RXBUF_SIZE)'.

When all Sn_RXBUF_SIZE registers have been configured, the Socket RX Buffer is allocated with the configured size in 16KB RX Memory and is assigned sequentially from Socket 0 to Socket 7. The physical memory address of the Socket RX Buffer is automatically determined in 16KB RX memory. Therefore, the total sum of Sn_RXBUF_SIZE should not exceed 16 or data reception error will occur.

For 16KB TX/RX memory allocation, refer to Sn_TXBUF_SIZE & Sn_RXBUF_SIZE in 'Chapter 7.4.2'. The Socket n TX Buffer Block allocated in 16KB TX memory is buffer for saving data to be transmitted by host. The 16bits Offset Address of Socket n TX Buffer Block has 64KB address space ranged from 0x0000 to 0xFFFF, and is configured with reference to 'Socket n TX Write Pointer Register (Sn_TX_WR)' & 'Socket n TX Read Pointer Register(Sn_RX_RD)'. However, the 16bits Offset Address automatically converts into the physical address to be accessible in 16KB TX memory such as Figure 5. Refer to 'Chapter 7.4.2' for Sn_TX_WR & Sn_TX_RD.

The Socket n RX Buffer Block allocated in 16KB RX memory is buffer for saving the received data through the Ethernet. The 16bits Offset Address of Socket n RX Buffer Block has 64KB address space ranged from 0x0000 to 0xFFFF, and is configured with reference to 'Socket n RX RD Pointer Register (Sn_RX_RD)' & 'Socket n RX Write Pointer Register (Sn_RX_WR)'. However, the 16bits Offset Address automatically converts into the physical address to be accessible in 16KB RX memory such as Figure 5. Refer to 'Chapter 7.4.2' for Sn_RX_RD & Sn_RX_WR.

7.5 Common register (Base : 0x4600_0000)

7.5.1 VERSIONR (TOE Version Register)

Address Offset : 0x0000

Reset value : 0x0000_0005

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	Res	res	res	res	res	res	VERSION[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[7:0] VERSION - indicates the TOE version as 0x05.

7.5.2 TCKCNTR (Ticker Counter Register)

Address Offset : 0x2000

Reset value : 0x0000_07D0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCKCNT[15:0]															
R/W															

[15:0] TCKCNT – Ticker counter register is used Tick counter of 100usec. for internal timer of TOE. The unit of tick is HCLK.

Ex) HCLK is 20MHz,

0.0001sec./ (1sec./HCLK (=20000000)) = 2000(dec) = 0x7DC

7.5.3 IR (Interrupt Register)

Address Offset : 0x2100

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	Res	res	res	res	res	res	res	res	res	res	es	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	IR[7:4]				res	res	res	res
								R	R	R	R				

IR indicates the interrupt status. If IR is not equal to ‘0x00’, INTn PIN is asserted low until it is ‘0x00’.

[4] WOL – Magic Packet

When WOL mode is enabled and receives the magic packet over UDP, this bit is set.

[5] PPPoE – PPPoE Close

When PPPoE is disconnected during PPPoE mode, this bit is set.

[6] UNREACH – Destination unreachable

When receiving the ICMP (Destination port unreachable) packet, this bit is set as '1'. When this bit is '1', Destination Information such as IP address and Port number may be checked with the corresponding UIPR & UPORTR.

[7] Conflict – IP Conflict

Bit is set as '1' when own source IP address is same with the sender IP address in the received ARP request.

7.5.4 IMR (Interrupt Mask Register)

Address Offset : 0x2104

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	IMR[7:4]				res	res	res	res
								R/W							

IMR is used to mask interrupts. Each bit of IMR corresponds to each bit of IR. When a bit of IMR is '1' and the corresponding bit of IR is '1', an interrupt will be issued. In other words, if a bit of IMR is '0', an interrupt will not be issued even if the corresponding bit of IR is '1'.

[4] Magic Packet

0: Disable Magic Packet Interrupt

1: Enable Magic Packet Interrupt

[5] PPPoE Close Interrupt Mask

0: Disable PPPoE Close Interrupt

1: Enable PPPoE Close Interrupt

[6] Destination unreachable Interrupt Mask

0: Disable Destination unreachable Interrupt

1: Enable Destination unreachable Interrupt

[7] IP Conflict Interrupt Mask

0: Disable IP Conflict Interrupt

1: Enable IP Conflict Interrupt

7.5.5 IRCR (Interrupt Clear Register)

Address Offset : 0x2108

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	IRC[8:4]				res	res	res	res
								*R/C_W1							

IRCR is used to clear interrupts. Each bit of IR can be cleared when the host writes '1' value to each bit of IRCR corresponding to each bit of IR.

** ReadClearWrite1 (R/C_W1) : Software can read as well as clear this bit by writing '1'. Writing '0' has no effect on the bit value.*

[4] Magic Packet Interrupt Clear

[5] PPPoE Close Interrupt Clear

[6] Destination unreachable Interrupt Clear

[7] IP Conflict Interrupt Clear

7.5.6 SIR (Socket Interrupt Register)

Address Offset : 0x2110

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	S7	S6	S5	S4	S3	S2	S1	S0
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SIR indicates the interrupt status of Socket. Each bit of SIR be still '1' until Sn_IR is cleared by the host. If Sn_IR is not equal to '0x00', the n-th bit of SIR is '1' and INTn PIN is asserted until SIR is '0x00'

[7:0] SIR - When the interrupt of Socket n occurs, the n-th bit of SIR becomes '1'.

7.5.7 SIMR (Socket Interrupt Mask Register)

Address Offset : 0x2114

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	S7	S6	S5	S4	S3	S2	S1	S0
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Each bit of SIMR corresponds to each bit of SIR. When a bit of SIMR is '1' and the corresponding bit of SIR is '1', Interrupt will be issued. In other words, if a bit of SIMR is '0', an interrupt will be not issued even if the corresponding bit of SIR is '1'.

[7:0] SIR - Socket n Interrupt Mast

0: Disable Socket n Interrupt

1: Enable Socket n Interrupt

7.5.8 MD (Mode Register)

Address Offset : 0x2300

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	RST	res	WOL	PB	PPP	res	FA	res
								R/W		R/W	R/W	R/W		R/W	

MR is used for S/W reset, ping block mode and PPPoE mode

[3] PPP – PPPoE

If you use ADSL, this bit should be '1'.

0: Disable PPPoE mode

1: Enable PPPoE mode

[4] PB – Ping Block

If the bit is '1', it blocks the response to a ping request.

0: Disable Ping block

1: Enable Ping block

[5] WOL – Wake on Lan

If WOL mode is enabled and the received magic packet over UDP has been normally processed, the Interrupt PIN (INTn) asserts to low. When using WOL mode, the UDP Socket should be opened with any source port number. (Refer to Socket n Mode Register (Sn_MR) for opening Socket.)

Notice: The magic packet over UDP supported by TOE consists of 6 bytes synchronization stream ('0xFFFFFFFFFFFF') and 16 times Target MAC address stream in UDP payload. The options such like password are ignored. You can use any UDP source port number for WOL mode.

0: Disable WOL mode

1: Enable WOL mode

[7] RST – Software Reset

If this bit is '1', All internal registers will be initialized. It will be automatically cleared as '0' after S/W reset.

7.5.9 PTIMER (PPP Link Control Protocol Request Timer Register)

Address Offset : 0x2400

Reset value : 0x0000_0028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	Res	res	res	res	res	PTIME[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[7:0] PTIME configures the time for sending LCP echo request. The unit of time is 25ms

Ex) in case that PTIMER is 200,

200 * 25(ms) = 5000(ms) = 5 seconds

7.5.10 PMAGICR (PPP Link Control Protocol Magic number Register)

Address Offset : 0x2404

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	Res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	Res	res	res	res	res	PMAGIC[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMAGICR configures the 4bytes magic number to be used in LCP echo request.

[7:0] PMAGIC

Ex) PMAGIC = 0x01

0x001D

0x01

LCP Magic number = 0x01010101

7.5.11 PHAR (Destination Hardware Address Register in PPPoE)

Address Offset : 0x2408

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHAR[31:24]								PHAR1[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHAR[15:8]								PHAR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address Offset : 0x240C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHAR[31:24]								PHAR[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res								res							

PHAR should be written to the PPPoE server hardware address acquired in PPPoE connection process.

PHAR0 and PHAR1 – configures Destination hardware address

Ex) In case that destination hardware address is 00:08:DC:12:34:56

PHAR0[32:24]	PHAR0[23:16]	PHAR0[15:8]	PHAR0[32:24]	PHAR1[32:24]	PHAR1[23:16]
0x00	0x08	0xDC	0x12	0x34	0x56

7.5.12 PSIDR (Session ID Register in PPPoE)

Address Offset : 0x2410

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	Res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSID[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:0] PSID - should be written to the PPPoE sever session ID acquired in PPPoE connection process.

7.5.13 PMRUR (Maximum Receive Unit Register in PPPoE)

Address Offset : 0x2414

Reset value : 0x0000_FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	Res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMSS[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:0] PMRUR configures the maximum receive unit of PPPoE.

Ex) in case that maximum receive unit in PPPoE is 0x1234

PMSS[15:8]	PMSS[7:0]
0x12	0x34

7.5.14 SHAR (Source Hardware Address Register)

Address Offset : 0x6000

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHAR0[31:24]								SHAR0[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHAR0[15:8]								SPHAR0[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address Offset : 0x6004

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHA1[31:24]								SHAR1[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res								res							

SHAR configures the source hardware address.

Ex) In case of “00.08.DC.12.34.56”

SHAR0[32:24]	SHAR0[23:16]	SHAR0 [15:8]	SHAR0 [32:24]	SHAR1 [32:24]	SHAR2 [23:16]
0x00	0x08	0xDC	0x12	0x34	0x56

7.5.15 GAR (Gateway Address)

Address Offset : 0x6008

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GA[31:24]								GA[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GA[15:8]								GA[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GAR[31:0] – configures the default gateway address

Ex) In case of “192.168.0.1”

GA[31:24]	GA[23:16]	GA[15:8]	GA[7:0]
192 (0xC0)	168 (0xA8)	0 (0x00)	1 (0x01)

7.5.16 SUBR (Subnet Mask Register)

Address Offset : 0x600C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUB[31:24]								SUB[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBR[15:8]								SUBR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SUBR configures the subnet mask address.

Ex) In case of “255.255.255.0”

SUB[31:24]	SUB[23:16]	SUB[15:8]	SUB[7:0]
255 (0xFF)	255 (0xFF)	255 (0xFF)	0 (0x00)

7.5.17 SIPR (Source IP address Register)

Address Offset : 0x6010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIPR[31:24]								SIPR[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIPR[15:8]								SIPR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SIPR configures the source IP address.

Ex) In case of “192.168.0.2”

SIPR[31:24]	SIPR[23:16]	SIPR[15:8]	SPIR[7:0]
192 (0xC0)	168 (0xA8)	0 (0x00)	2 (0x02)

7.5.18 NCONFLR (Network Configuration Lock Register)

Address Offset : 0x6020

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NCONFL[31:24]								NCONFL [23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCONFL [15:8]								NCONFL [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NCONFLR is used to unlock and lock the network configuration registers which are SIR, SUBR, GAR and SHAR. When LOCK is ‘ON’, the protected registers are not able to access. In this case a value of 0x01ACCE55 is written to NCONFLR. When LOCK is ‘OFF’, the protected registers are allowed to access. In this case any value except 0x01ACCE55 is written.

Ex) In case of ‘LOOK is ON’

NCONFL[31:24]	NCONFL [23:16]	NCONFL [15:8]	NCONFL [7:0]
1 (0x01)	172 (0xAC)	206 (0xCE)	85 (0x55)

7.5.19 RTR (Retry Time Register)

Address Offset : 0x6040

Reset value : 0x0000_07D0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTR[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTR configures the retransmission timeout period. The unit of timeout period is 100us and the default of RTR is ‘0x07D0’ or ‘2000’. And so the default timeout period is 200ms(100us X 2000).

During the time configured by RTR, WZTOE waits for the peer response to the packet that is transmitted by Sn_CR(CONNECT, DISCON, CLOSE, SEND, SEND_MAC, SEND_KEEP command). If the peer does not respond within the RTR time, WZTOE retransmits the packet or issues timeout.

When RTR is not '0x0000_0000, RTR is used to configure the timeout period of all socket. When RTR is '0x0000_0000', the timeout period of each socket could set by using Socket n Retry Time Register (Sn_RTR).

Ex) When timeout-period is set as 400ms, RTR = (400ms / 1ms) X 10 = 4000(0x0FA0)

RTR[15:8]
0x0F

7.5.20 RCR (Retry Counter Register)

Address Offset : 0x6044

Reset value : 0x0000_0008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res								res							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res								RC[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RCR configures the number of time of retransmission. When retransmission occurs as many as 'RCR+1', Timeout interrupt is issued (Sn_IR[TIMEOUT] = '1').

When RCR is not '0x0000_0000, RCR is used to configure the timeout period of all socket. When RCR is '0x0000_0000', the timeout period of each socket could set by using Socket n Retry Counter Register (Sn_RCR).

Ex) RCR = 0x0007

RC[7:0]
0x07

The timeout of WZTOE can be configurable with RTR and RCR. WZTOE has two kind timeout such as Address Resolution Protocol (ARP) and TCP retransmission.

At the ARP (Refer to RFC 826, http://www.ietf.org/rfc.html) retransmission timeout, WZTOE automatically sends ARP-request to the peer's IP address in order to acquire MAC address information (used for communication of IP, UDP, or TCP). While waiting for ARP-response from

the peer, if there is no response during the configured RTR time, a temporary timeout is occurred and ARP-request is retransmitted. It is repeated as many as 'RCR + 1' times. Even after the ARP-request retransmissions are repeated as 'RCR+1' and there is no response to the ARP-request, the final timeout is occurred and Sn_IR(TIMEOUT) becomes '1'. The time of final timeout (ARP_{TO}) of ARP-request is as below.

$$ARP_{TO} = (RTR \times 0.1ms) \times (RCR + 1)$$

At the TCP packet retransmission timeout, WZTOE transmits TCP packets (SYN, FIN, RST, DATA packets) and waits for the acknowledgement (ACK) during the configured RTR time and RCR. If there is no ACK from the peer, a temporary timeout occurs and the TCP packet is retransmitted. The retransmission is repeated as many as 'RCR+1'. Even after TCP retransmission is repeated as 'RCR+1' and there is no response to the TCP retransmission, the final timeout is occurred and Sn_IR(TIMEOUT) becomes '1'. The time of final timeout (TCPTO) of TCP retransmission is as below.

$$TCP_{TO} = \left(\sum_{N=0}^{M}(RTR \times 2^N) \quad + \quad \left((RCR - M) \times RTR_{MAX}\right)\right) \times 0.1ms$$

N : Retransmission count, $0 \le N \le M$

M : Minimum value when RTR x $2^{(M+1)}$ > 65535 and $0 \le M \le RCR$

RTRMAX : RTR x 2^M

Ex) When RTR = 2000(0x07D0), RCR = 8(0x0008),

ARP_{TO} = 2000 X 0.1ms X 9 = 1800ms = 1.8s

TCP_{TO} = (0x07D0+0x0FA0+0x1F40+0x3E80+0x7D00+0xFA00+0xFA00+0xFA00+0xFA00) X 0.1ms

= (2000 + 4000 + 8000 + 16000 + 32000 + ((8 - 4) X 64000)) X 0.1ms

= 318000 X 0.1ms = 31.8s

7.5.21 UIPR (Unreachable IP address Register)

Address Offset : 0x6050

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UIP[31:24]								UIPR[23:16]							

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UIPR[15:8]								UIPR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TOE receives an ICMP packet(Destination port unreachable) when data is sent to a port number which socket is not open and UNREACH bit of IR becomes '1' and UIPR indicates the destination IP address.

Ex) In case of "192.168.0.11"

UIP[31:24]	UIP[23:16]	UIP[15:8]	UIP[7:0]
192 (0xC0)	168 (0xA8)	0 (0x00)	11 (0x0E)

7.5.22 UPORTR (Unreachable Port Register)

Address Offset : 0x6054

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPORT[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TOE receives an ICMP packet(Destination port unreachable) when data is sent to a port number which socket is not open and UNREACH bit of IR becomes '1' and UPORTR indicates the destination port number.

[15 :0] UPORT – Destination port number bits

Ex) In case of "0x1234"

UPORT[15:8]	UPORT[7:0]
18 (0x12)	52(0x34)

7.6 Socket register (Base : 0x4601_0000 + 0x0004_000 x n)[n=0,…7, where n is socket number]

7.6.1 Sn_MR (Socket n Mode Register)

Address Offset : 0x0000

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res	Sn_MR[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_MR configures the option or protocol type of Socket n.

[3:0] These bits configures the protocol mode of Socket n as follows

Sn_MR[3:0]				Meaning
0	0	0	0	Closed
0	0	0	1	TCP
0	0	1	0	UDP
0	1	0	0	MACRAW

- MACRAW mode should be only used in Socket 0.

[4] UNICAST Blocking and IPv6 packet Blocking

UNICAST Blocking in UDP mode

0 : disable Unicast Blocking

1 : enable Unicast Blocking

This bit blocks receiving the unicast packet during UDP mode(P[3:0] = ‘0010’) and MULTI = ‘1’.

IPv6 packet Blocking in MACRAW mode

0 : disable IPv6 Blocking

1 : enable IPv6 Blocking

This bit is applied only during MACRAW mode (P[3:0] = ‘0100’). It blocks to receiving the IPv6 packet.

[5] **Use No Delayed ACK, Multicast and Multicast Blocking mode**

Use No Delayed ACK

0 : Disable No Delayed ACK option

1 : Enable No Delayed ACK option

This bit is applied only during TCP mode (P[3:0] = '0001').When this bit is '1', It sends the ACK packet without delay as soon as a

Multicast

0 : using IGMP version 2

1 : using IGMP version 1

This bit is applied only during UDP mode(P[3:0] = '0010') and MULTI = '1'. It configures the version for IGMP messages (Join/Leave/Report).

Multicast Blocking in MACRAW mode

0 : disable Multicast Blocking

1 : enable Multicast Blocking

This bit is applied only when MACRAW mode(P[3:0] = '0100'). It blocks to receive the packet with multicast MAC address.

[6] **Broadcast Blocking in MACRAW and UDP mode**

0 : disable Broadcast Blocking

1 : enable Broadcast Blocking

This bit blocks to receive broadcasting packet during UDP mode(P[3:0] = '0010'). In addition, This bit does when MACRAW mode(P[3:0] = '0100') Data packet is received from a peer. When this bit is '0', It sends the ACK packet after waiting for the timeout time configured by RTR.

[7] **Multicasting and MAC Filter Enable mode**

Multicasting in UDP mode

0 : disable Multicasting

1 : enable Multicasting

This bit is applied only during UDP mode(P[3:0] = '0010').To use multicasting, Sn_DIPR & Sn_DPORT should be respectively configured with the multicast group IP address & port number before Socket n is opened by OPEN command of Sn_CR

MAC Filter Enable in MACRAW mode

0 : disable MAC Filtering

1 : enable MAC Filtering

This bit is applied only during MACRAW mode(P[3:0] = '0100').When set as '1', WZTOE can only receive broadcasting packet or packet sent to itself. When this bit is '0', WZTOE can receive all packets on Ethernet. If user wants to implement Hybrid TCP/IP stack, it is recommended that this bit is set as '1' for reducing host overhead to process the all received packets.

7.6.2 Sn_CR (Socket n Command Register)

Address Offset : 0x0010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res	Sn_CR[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This is used to set the command for Socket n such as OPEN, CLOSE, CONNECT, LISTEN, SEND, and RECEIVE. After WZTOE accepts the command, the Sn_CR register is automatically cleared to 0x00. Even though Sn_CR is cleared to 0x00, the command is still being processed. To check whether the command is completed or not, please check the Sn_IR or Sn_SR.

<table>
<tr><th>Value</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0x01</td><td>OPEN</td><td>Socket n is initialized and opened according to the protocol selected in Sn_MR (P3:P0). The table below shows the value of Sn_SR corresponding to Sn_MR.

<table>
<tr><th>Sn_MR (P[3:0])</th><th>Sn_SR</th></tr>
<tr><td>Sn_MR_CLOSE ('0000')</td><td>-</td></tr>
<tr><td>Sn_MR_TCP ('0001')</td><td>SOCK_INIT (0x13)</td></tr>
<tr><td>Sn_MR_UDP ('0010')</td><td>SOCK_UDP (0x22)</td></tr>
<tr><td>S0_MR_MACRAW ('0100')</td><td>SOCK_MACRAW (0x02)</td></tr>
</table>
</td></tr>
<tr><td>0x02</td><td>LISTEN</td><td>This is valid only in TCP mode (Sn_MR(P3:P0) = Sn_MR_TCP). In this mode, Socket n operates as a 'TCP server' and waits for connection-request (SYN packet) from any 'TCP client'.

The Sn_SR changes the state from SOCK_INIT to SOCKET_LISTEN.</td></tr>
</table>

		When a 'TCP client' connection request is successfully established, the Sn_SR changes from SOCK_LISTEN to SOCK_ESTABLISHED and the Sn_IR(0) becomes '1'. But when a 'TCP client' connection request is failed, Sn_IR(3) becomes '1' and the status of Sn_SR changes to SOCK_CLOSED.
0x04	CONNECT	This is valid only in TCP mode and operates when Socket n acts as 'TCP client'. To connect, a connect-request (SYN packet) is sent to 'TCP server' configured by Sn_DIPR & Sn_DPORT(destination address & port). If the connect-request is successful, the Sn_SR is changed to SOCK_ESTABLISHED and the Sn_IR(0) becomes '1'. The connect-request fails in the following three cases. 1. When a ARP_{TO} occurs (Sn_IR(3)='1') because the destination hardware address is not acquired through the ARP-process. 2. When a SYN/ACK packet is not received and TCP_{TO} (Sn_IR(3) = '1) 3. When a RST packet is received instead of a SYN/ACK packet. In these cases, Sn_SR is changed to SOCK_CLOSED.
0x08	DISCON	Valid only in TCP mode. Regardless of 'TCP server' or 'TCP client', the DISCON command processes the disconnect-process ('Active close' or 'Passive close'). **Active close**: it transmits disconnect-request(FIN packet) to the connected peer **Passive close**: When FIN packet is received from peer, a FIN packet is replied back to the peer. When the disconnect-process is successful (that is, FIN/ACK packet is received successfully), Sn_SR is changed to SOCK_CLOSED. Otherwise, TCP_{TO} occurs (Sn_IR(3)='1)= and then Sn_SR is changed to SOCK_CLOSED. cf> If CLOSE is used instead of DISCON, only Sn_SR is changed to SOCK_CLOSED without disconnect-process. If a RST packet is received from a peer during communication, Sn_SR is unconditionally changed to SOCK_CLOSED.
0x10	CLOSE	Close Socket n. Sn_SR is changed to SOCK_CLOSED.

0x20	SEND	SEND transmits all the data in the Socket n TX buffer. For more details, please refer to Socket n TX Free Size Register (Sn_TX_FSR), Socket n, TX Write Pointer Register (Sn_TX_WR), and Socket n TX Read Pointer Register(Sn_TX_RD).
0x21	SEND_MAC	Valid only in UDP mode. The basic operation is same as SEND. Normally SEND transmits data after destination hardware address is acquired by the automatic ARP-process(Address Resolution Protocol). But SEND_MAC transmits data without the automatic ARP-process. In this case, the destination hardware address is acquired from Sn_DHAR configured by host, instead of APR-process.
0x22	SEND_KEEP	Valid only in TCP mode. It checks the connection status by sending 1byte keep-alive packet. If the peer cannot respond to the keep-alive packet during timeout time, the connection is terminated and the timeout interrupt will occur.
0x40	RECV	RECV completes the processing of the received data in Socket n RX Buffer by using a RX read pointer register (Sn_RX_RD). For more details, refer to Socket n RX Received Size Register (Sn_RX_RSR), Socket n RX Write Pointer Register (Sn_RX_WR), and Socket n RX Read Pointer Register (Sn_RX_RD).

7.6.3 Sn_IR (Socket n Interrupt Register)

Address Offset : 0x0020

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	Res	res	res	res	res	res	Sn_IR[4:0]				
											R	R	R	R	R

Sn_IR indicates the status of Socket Interrupt such as establishment, termination, receiving data, timeout). When an interrupt occurs and the corresponding bit of Sn_IMR is '1', the corresponding bit of Sn_IR becomes '1'.

[0] **CONNECT Interrupt -** This is issued one time when the connection with peer is successful and then Sn_SR is changed to SOCK_ESTABLISHED

[1] **DISCONNECT Interrupt -** This is issued when FIN or FIN/ACK packet is received.

[2] **RECV Interrupt -** This is issued whenever data is received from a peer.

[3] **TIMEOUT Interrupt -** This is issued when ARP_{TO} or TCP_{TO} occurs.

[4] **SENDOK Interrupt -** This is issued when SEND command is completed

7.6.4 Sn_IMR (Socket n Interrupt Mask Register)

Address Offset : 0x0024

Reset value: 0x0000_00FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res	res	res	res	Sn_IMR[4:0]				
											R/W	R/W	R/W	R/W	R/W

Sn_IMR is used to mask interrupts. Each bit of Sn_IMR corresponds to each bit of Sn_IR. When a bit of Sn_IMR is '1' and the corresponding bit of Sn_IR is '1', an interrupt will be issued. In other words, if a bit of Sn_IMR is '0', an interrupt will not be issued even if the corresponding bit of Sn_IR is '1'.

[0] **CONNECT Interrupt** Mask

0: Disable CONNECT Interrupt

1: Enable CONNECT Interrupt

[1] **DISCONNECT Interrupt** Mask

0: Disable DISCONNECT Interrupt

1: Enable DISCONNECT Interrupt

[2] **RECV Interrupt** Mask

0: Disable RECV Interrupt

1: Enable RECV Interrupt

[3] **TIMEOUT Interrupt** Mask

0: Disable TIMEOUT Interrupt

1: Enable TIMEOUT Interrupt

[4] **SENDOK Interrupt Mask**

0: Disable SENDOK Interrupt

1: Enable SENDOK Interrupt

7.6.5 Sn_ICR (Socket n Interrupt Clear Register)

Address Offset : 0x0028

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res								
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_ICR is used to clear interrupts. Each bit of Sn_IR can be cleared when the host writes '1' value to each bit of Sn_ICR corresponding to each bit of Sn_IR.

[0] CONNECT Interrupt Clear

[1] DISCONNECT Interrupt Clear

[2] RECV Interrupt Mask

[3] TIMEOUT Interrupt Mask

[4] SENDOK Interrupt Mask

** ReadClearWrite1 (R/C_W1) : Software can read as well as clear this bit by writing 1. Writing '0' has no effect on the bit value.*

7.6.6 Sn_SR (Socket n Status Register)

Address Offset : 0x0030

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res								
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_SR indicates the status of Socket n. The status of Socket n is changed by Sn_CR or some special control packet as SYN, FIN packet in TCP.

Value	Symbol	Description
0x00	SOCK_CLOSED	This indicates that Socket n is released.

		When DISCON, CLOSE command is ordered, or when a timeout occurs, it is changed to SOCK_CLOSED regardless of previous status.
0x13	SOCK_INIT	This indicates Socket n is opened with TCP mode. It is changed to SOCK_INIT when Sn_MR (P[3:0]) = '0001' and OPEN command is ordered. After SOCK_INIT, user can use LISTEN /CONNECT command.
0x14	SOCK_LISTEN	This indicates Socket n is operating as 'TCP server' mode and waiting for connection-request (SYN packet) from a peer ('TCP client'). It will change to SOCK_ESTALBLISHED when the connection-request is successfully accepted. Otherwise it will change to SOCK_CLOSED after TCPTO occurred (Sn_IR(TIMEOUT) = '1').
0x17	SOCK_ESTABLISHED	This indicates the status of the connection of Socket n. It changes to SOCK_ESTABLISHED when the 'TCP SERVER' processed the SYN packet from the 'TCP CLIENT' during SOCK_LISTEN, or when the CONNECT command is successful. During SOCK_ESTABLISHED, DATA packet can be transferred using SEND or RECV command.
0x1C	SOCK_CLOSE_WAIT	This indicates Socket n received the disconnect-request (FIN packet) from the connected peer. This is half-closing status, and data can be transferred. For full-closing, DISCON command is used. But For just-closing, CLOSE command is used.
0x22	SOCK_UDP	This indicates Socket n is opened in UDP mode(Sn_MR(P[3:0]) = '0010'). It changes to SOCK_UDP when Sn_MR(P[3:0]) = '0010') and OPEN command is ordered. Unlike TCP mode, data can be transfered without the connection-process.
0x42	SOCK_MACRAW	This indicates Socket 0 is opened in MACRAW mode (S0_MR(P[3:0]) = '0100')and is valid only in Socket 0. It changes to SOCK_MACRAW when S0_MR(P[3:0] = '0100' and OPEN command is ordered. Like UDP mode socket, MACRAW mode Socket 0 can transfer a MAC packet (Ethernet frame) without the connection-process.

The following table shows a temporary status indicated during changing the status of Socket n.

Value	Symbol	Description
0x15	SOCK_SYNSENT	This indicates Socket n sent the connect-request packet (SYN packet) to a peer. It is temporarily shown when Sn_SR is changed from SOCK_INIT to SOCK_ESTABLISHED by CONNECT command. If connect-accept(SYN/ACK packet) is received from the peer at SOCK_SYNSENT, it changes to SOCK_ESTABLISHED. Otherwise, it changes to SOCK_CLOSED after TCPTO (Sn_IR[TIMEOUT] = '1') is occurred.
0x16	SOCK_SYNRECV	It indicates Socket n successfully received the connect-request packet (SYN packet) from a peer. If socket n sends the response (SYN/ACK packet) to the peer successfully, it changes to SOCK_ESTABLISHED. If not, it changes to SOCK_CLOSED after timeout occurs (Sn_IR[TIMEOUT] = '1').
0x18	SOCK_FIN_WAIT	These indicate Socket n is closing. These are shown in disconnect-process such as active-close and passive-close. When Disconnect-process is successfully completed, or when timeout occurs, these change to SOCK_CLOSED.
0x1A	SOCK_CLOSING	
0X1B	SOCK_TIME_WAIT	
0X1D	SOCK_LAST_ACK	This indicates Socket n is waiting for the response (FIN/ACK packet) to the disconnect-request (FIN packet) by passive-close. It changes to SOCK_CLOSED when Socket n received the response successfully, or when timeout occurs (Sn_IR[TIMEOUT] = '1').

7.6.7 Sn_PNR (Socket n Protocol Number Register)

Address Offset : 0x0100

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res	Sn_PNR[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This IP Protocol Register is user to set up the Protocol Field of IP Header at the IP layer RAW mode. There are several protocol number defined in advance by registering to IANA. For the overall list of upper level protocol identification number that IP is using, refer to online documents of IANA (http://www.iana.org/assignments/protocol-numbers).

Ex) Internet Control Message Protocol (ICMP) = 0x01, Internet Group Management Protocol = 0x02

7.6.8 Sn_TOSR (Socket n IP Type of Service Register)

Address Offset : 0x0104

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res	Sn_ROS[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_TOSR configures the TOS(Type Of Service field in IP Header) of Socket n. It is set before OPEN command.

For more the details, refer to http://www.iana.org/assignments/ip-parameters.

7.6.9 Sn_TTLR (Socket n TTL Register)

Address Offset : 0x0108

Reset value : 0x0000_0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res	Sn_TTL[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_TTL configures the TTL(Time To Live field in IP Header) of Socket n. It is set before OPEN command.

For more the details, refer to http://www.iana.org/assignments/ip-parameters.

7.6.10 Sn_FRAGR (Socket n Fragment offset Register)

Address Offset : 0x010C

Reset value : 0x0000_4000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_FRAG[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:0] Sn_FRAG configures the FRAG(Fragment field in IP header)

Ex) Sn_FRAGR = 0x0000 (Don't Fragment)

Sn_FRAG[15:8]	Sn_FRAG[7:0]
0x00	0x00

7.6.11 Sn_MSSR (Socket n Maximum Segment Register)

Address Offset : 0x0110

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	Res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_MSS[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register is used for MSS (Maximum Segment Size) of TCP, and the register displays MSS set by the other party when TCP is activated in Passive Mode.

Ex) In case of Socket 0 MSS = 1460 (0x05B4), configure as below,

0x4101_0110
0x05B4

7.6.12 Sn_PORTR (Socket n Source Port Register)

Address Offset : 0x0114

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_SPROT[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_PORTR configures the source port number of Socket n. It is valid when Socket n is used in TCP/UDP mode. It should be set before OPEN command is ordered.

Ex) In case of Socket 0 Port = 5000(0x1388), configure as below,

0x4101_0114

0x1388

7.6.13 Sn_DHAR (Socket n Destination Hardware address Register)

Address Offset : 0x0118

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Sn_DHAR0[31:24]								Sn_DHAR0 [23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_DHAR0 [15:8]								Sn_DHAR0 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address Offset : 0x011C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Sn_DHAR1 [31:24]								Sn_DHAR1 [23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res								res							

Sn_DHAR configures the destination hardware address of Socket n when using SEND_MAC command in UDP mode or it indicates that it is acquired in ARP-process by CONNECT/SEND command.

Ex) In case of "00.08.DC.12.34.56"

Sn_DHAR0 [32:24]	Sn_DHAR0 [23:16]	Sn_DHAR0 [15:8]	Sn_DHAR0 [32:24]	Sn_DHAR1 [32:24]	Sn_DHAR1 [23:16]
0x00	0x08	0xDC	0x12	0x34	0x56

7.6.14 Sn_DPORTR (Socket n Destination Port Number Register)

Address Offset : 0x0120

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_DPROT[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_DPORT configures or indicates the destination port number of Socket n. It is valid when Socket n is used in TCP/UDP mode.

In TCP client mode, it configures the listen port number of 'TCP server' before CONNECT command.
In TCP server mode, it indicates the port number of 'TCP client' after successfully establishing connection.
In UDP mode, it configures the port number of peer to be transmitted the UDP packet by SEND/SEND_MAC command.

Ex) In case of Socket 0 Destination Port = 5000(0x1388), configure as below,

0x4101_0120
0x1388

7.6.15 Sn_DIPR (Socket n Destination IP address Register)

Address Offset : 0x0124

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Sn_DIPR[31:24]								Sn_DIPR [23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_DIPR [15:8]								Sn_DIPR [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_DIPR configures or indicates the destination IP address of Socket n. It is valid when Socket n is used in TCP/UDP mode.

In TCP client mode, it configures an IP address of 'TCP server' before CONNECT command.

In TCP server mode, it indicates an IP address of 'TCP client' after successfully establishing connection.

In UDP mode, it configures an IP address of peer to be received the UDP packet by SEND or SEND_MAC command.

Ex) In case of "192.168.0.2"

Sn_DIPR[31:24]	Sn_DIPR [23:16]	Sn_DIPR [15:8]	Sn_DIPR [7:0]
192 (0xC0)	168 (0xA8)	0 (0x00)	2 (0x02)

7.6.16 Sn_KATMR (Socket n Keep Alive Timer Register)

Address Offset : 0x0180

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res	Sn_KATM[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_KPALVTR configures the transmitting timer of 'KEEP ALIVE(KA)' packet of SOCKETn. It is valid only in TCP mode, and ignored in other modes. The time unit is 5s.

KA packet is transmittable after Sn_SR is changed to SOCK_ESTABLISHED and after the data is transmitted or received to/from a peer at least once. In case of 'Sn_KPALVTR > 0', WZTOE automatically transmits KA packet after time-period for checking the TCP connection (Auto-keepalive-process). In case of 'Sn_KPALVTR = 0', Auto-keep-alive-process will not operate, and KA packet can be transmitted by SEND_KEEP command by the host (Manual-keep-alive-process). Manual-keep-alive-process is ignored in case of 'Sn_KPALVTR > 0'.

Ex) Sn_KPALVTR = 10 (Keep Alive packet will be transmitted every 50 seconds.)

Sn_KATM[7:0]
0x0A

7.6.17 Sn_RTR (Socket n Retry Time Register)

Address Offset : 0x0184

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_RTR[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_RTR configures the retransmission timeout period of Socket n. When Retry Counter Register(RTR) is zero, Sn_RTR is valid. The unit of timeout period is 100us.

During the time configured by Sn_RTR, WZTOE waits for the peer response to the packet that is transmitted by Sn_CR(CONNECT, DISCON, CLOSE, SEND, SEND_MAC, SEND_KEEP command). If the peer does not respond within the RTR time, WZTOE retransmits the packet or issues timeout.

Ex) When timeout-period is set as 400ms, RTR = (400ms / 1ms) X 10 = 4000(0x0FA0)

RTR[15:0]
0x0FA0

7.6.18 Sn_RCR (Socket n Retry Counter Register)

Address Offset : 0x0188

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

res								Res							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res								Sn_RC[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_RCR configures the number of time of retransmission of Socket n. When Retry Counter Register(RCR) is zero, Sn_RCR is valid. When retransmission occurs as many as 'Sn_RCR+1', Timeout interrupt is issued (Sn_IR[TIMEOUT] = '1').

Ex) Sn_RCR = 0x0007

Sn_RC[7:0]
0x07

7.6.19 Sn_TXBUF_SIZE (Socket n TX Buffer Size Register)

Address Offset : 0x0200

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res	Sn_TMS[7:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_TXBUF_SIZE configures the TX Buffer size of Socket n. Socket n TX Buffer size can be configured with 0,1,2,4,8 and 16 Kbytes. If a different size is configured, the data can't be normally transmitted to a peer.

Although Socket n TX Buffer size is initially configured to 2Kbytes, user can be re-configure its size using Sn_TXBUF_SIZE. The total sum of Sn_TXBUF_SIZE cannot be exceed 16Kbytes. When exceeded, the data transmission error is occurred.

When all Sn_TXBUF_SIZE have been configured, Socket n TX Buffer is allocated with the configured size in 16KB TX Buffer and is assigned sequentially from Socket 0 to Socket 7.

Socket n TX Buffer can be accessible with 16bits Offset Address ranged from 0x0000 to 0xFFFF regardless of the configured size. (Refer to Sn_TX_WR & Sn_TX_RD).

Value (dec)	0	1	2	4	8	16
Buffer size	0KB	1KB	2KB	4KB	8KB	16KB

Ex) Socket 0 TX Buffer Size = 4KB

0x4600_0200

0x04

7.6.20 Sn_TX_FSR (Socket n TX Free Size Register)

Address Offset : 0x0204

Reset value : 0x0000_0800

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	Res	res	res	res	res	res								
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_TX_FSR indicates the free size of Socket n TX Buffer. It is initialized to the configured size by Sn_TX_SIZE. Data bigger than Sn_TX_SIZE should not be saved in the Socket n TX Buffer because the bigger data overwrites the previous saved data not yet sent. Therefore, check before saving the data to the Socket n TX Buffer, and if data is equal or smaller than its checked size, transmit the data with SEND/SEND_MAC command after saving the data in Socket n TX Buffer. But, if data is bigger than its checked size, transmit the data after dividing into the checked size and saving in the Socket n TX Buffer.

If Sn_MR(P[3:0]) is not TCP mode('0001'), it is automatically calculated as the difference between 'Socket n TX Write Pointer (Sn_TX_WR)' and 'Socket n TX Read Pointer (Sn_TX_RD)'. If Sn_MR(P[3:0]) is TCP mode('0001'), it is automatically calculated as the difference between Sn_TX_WR and the internal ACK pointer which indicates the point of data is received already by the connected peer.

Ex) In case of 2048(0x0800) in S0_TX_FSR,

0x4600_0204

0x0800

Note) Because this register for representing the size information is 16 bits, it is impossible to read all bytes at the same time. Before 16 bit-read operation is not completed, the value may be changed.

Therefore, it is recommended that you read all 16-bits twice or more until getting the same value.

7.6.21 Sn_TX_RD (Socket n TX Read Pointer Register)

Address Offset : 0x0208

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_TXRP[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_TX_RD is initialized by OPEN command. However, if Sn_MR(P[3:0]) is TCP mode('0001'), it is re-initialized while connecting with TCP.

After its initialization, it is auto-increased by SEND command. SEND command transmits the saved data from the current Sn_TX_RD to the Sn_TX_WR in the Socket n TX Memory. After transmitting the saved data, the SEND command increases the Sn_TX_RD as same as the Sn_TX_WR. If its increment value exceeds the maximum value 0xFFFF, (greater than 0x10000 and the carry bit occurs), then the carry bit is ignored and will automatically update with the lower 16bits value.

7.6.22 Sn_TX_WR (Socket n TX Write Pointer Register)

Address Offset : 0x020C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_TXWP[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_TX_WR is initialized by OPEN command. However, if Sn_MR(P[3:0]) is TCP mode('0001'), it is re-initialized while connecting with TCP.

It should be read or to be updated like as follows.

1. Read the starting address for saving the transmitting data.
2. Save the transmitting data from the starting address of Socket n TX buffer.
3. After saving the transmitting data, update Sn_TX_WR to the increased value as many as transmitting data size. If the increment value exceeds the maximum value 0xFFFF(greater than 0x10000 and the carry bit occurs), then the carry bit is ignored and will automatically update with the lower 16bits value.
4. Transmit the saved data in Socket n TX Buffer by using SEND/SEND command

7.6.23 Sn_RXBUF_SIZE (Socket n RX Buffer Size Register)

Address Offset : 0x0220

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	res	res	res	res	res	Sn_RXMS[15:0]							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_RXBUF_SIZE configures the RX Buffer size of Socket n. Socket n RX Buffer size can be configured with 1,2,4,8, and 16 Kbytes. If a different size is configured, the data cannot be normally received from a peer.

Although Socket n RX Buffer size is initially configured to 2Kbytes, user can re-configure its size using Sn_RXBUF_SIZE. The total sum of Sn_RX_SIZE cannot be exceed 16Kbytes. When exceeded, the data reception error is occurred.

When all Sn_RXBUF_SIZE have been configured, Socket n RX Memory is allocated with the configured size in 16KB RX Memory and is assigned sequentially from Socket 0 to Socket 7.

Socket n RX Buffer Block can be accessible with the 16bits Offset Address ranged from 0x0000 to 0xFFFF regardless of the configured size. (Refer to Sn_RX_RD & Sn_RX_WR).

Value (dec)	0	1	2	4	8	16
Buffer size	0KB	1KB	2KB	4KB	8KB	16KB

Ex) Socket 0 RX Buffer Size = 8KB

0x4101_0220

0x08

7.6.24 Sn_RX_RSR (Socket n RX Received Size Register)

Address Offset : 0x0224

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_RX_RSR[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_RX_RSR indicates the data size received and saved in Socket n RX Buffer. Sn_RX_RSR does not exceed the Sn_RXBUF_SIZE and is calculated as the difference between 'Socket n RX Write Pointer (Sn_RX_WR)' and 'Socket n RX Read Pointer (Sn_RX_PD)'.

Ex) In case of 2048(0x0800) in S0_RXSR,

0x4101_0224

0x0800

Note) Because this register for representing the size information is 16 bits, it is impossible to read all bytes at the same time. Before 16 bit-read operation is not completed, the value may be changed.

Therefore, it is recommended that you read all 16-bits twice or more until getting the same value.

7.6.25 Sn_RX_RD (Socket n RX Read Pointer Register)

Address Offset : 0x0228

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_RXRP[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_RX_RD is initialized by OPEN command. Make sure to be read or updated as follows.

1. Read the starting save address of the received data
2. Read data from the starting address of Socket n RX Buffer.
3. After reading the received data, Update Sn_RX_RD to the increased value as many as the reading size. If the increment value exceeds the maximum value 0xFFFF, that is, is greater than 0x10000 and the carry bit occurs, update with the lower 16bits value ignored the carry bit.
4. Order RECV command is for notifying the updated Sn_RX_RD to TOE.

Ex) In case of 2048(0x0800) in S0_RX_RD,

0x4101_0228

0x08

7.6.26 Sn_RX_WR (Socket n RX Write Pointer Register)

Address Offset : 0x022C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sn_RX_WR[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sn_RX_WR is initialized by OPEN command and it is auto-increased by the data reception.
If the increased value exceeds the maximum value 0xFFFF, (greater than 0x10000 and the carry bit occurs), then the carry bit is ignored and will automatically update with the lower 16bits value.

Ex) In case of 2048(0x0800) in S0_RX_WR,

0x4101_022C

0x0800

8 Booting Sequence

W7500P has three different boot modes that can be selected through the BOOT pin and TEST pin as shown in Table 5.

Table 5 operation of mode selection

Mode selection		Mode	Aliasing
TEST	BOOT		
0	0	APP	User code execute in Main Flash memory.
0	1	ISP	In this mode,W7500P can support ISP function in order to control flash using serial interface.

When W7500P is reset by hardware, it will be operated as below in embedded boot code.

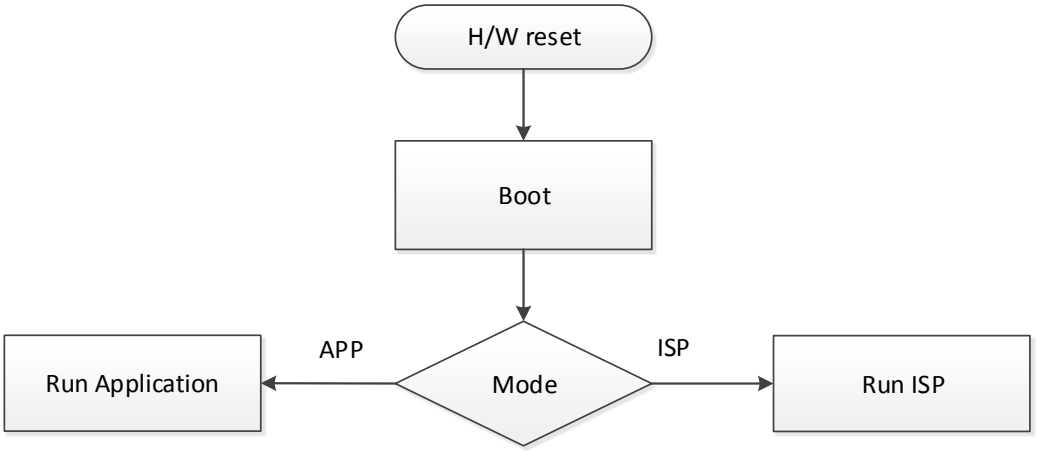


Figure 6. operation of boot code

9 Embedded Flash memory

9.1 Flash main features

- Up to 128Kbytes of Flash memory
- Memory organization:
  - Main Flash memory block:
    Up to 128Kbytes

- Information block:
  Up to 512bytes
  Information block is read only
- Data block:
  Up to 512bytes

• Flash memory interface features:
  - Read interface with prefetch buffer(1 x 32-bit words)
  - Flash Program / Erase operation
  - Read / Write protection

9.2 Flash memory functional description

9.2.1 Flash memory organization

The Flash memory is organized of 32-bit wide memory cells that can be used for storing both code and data constants.

The memory organization is based on a main Flash memory block containing 512 sectors of 256byte or 32 blocks of 4Kbyte. The block and sector provides read/write protection.

Table 6 description of Flash memory

Flash area	Flash memory address	Size (bytes)	Name	Description
Main Flash memory	0x0000 0000 ~ 0x0000 00FF	256	Sector 0	Block 0
	0x0000 0100 ~ 0x0000 01FF	256	Sector 1	
	0x0000 0200 ~ 0x0000 02FF	256	Sector 2	
	0x0000 0300 ~ 0x0000 03FF	256	Sector 3	
	⋮	⋮	⋮	⋮
	0x0000 7000 ~ 0x0000 70FF	256	Sector112	Block 7
	0x0000 7100 ~ 0x0000 71FF	256	Sector113	
	0x0000 7200 ~ 0x0000 72FF	256	Sector114	
	0x0000 7300 ~ 0x0000 73FF	256	Sector115	
	⋮	⋮	⋮	⋮
	0x0001 FC00 ~ 0x0001 FCFF	256	Sector509	Block 32
	0x0001 FD00 ~ 0x0001 FDFF	256	Sector510	
	0x0001 FE00 ~ 0x0001 FEFF	256	Sector511	
	0x0001 FF00 ~ 0x0001 FFFF	256	Sector512	
Information block	0x0003 FC00 ~ 0x0003 FCFF	256		Lock info
	0x0003 FD00 ~ 0x0003 FDFF	Reserved		

Data block	0x0003 FE00 ~ 0x0003 FEFF	256		Data0
	0x0003 FF00 ~ 0x0003 FFFF	256		Data1
Flash memory Interface register	0x4100 5000 ~ 0x4100 5003	4		FACCR
	0x4100 5004 ~ 0x4100 5007	4		FADDR
	0x4100 5008 ~ 0x4100 500B	4		FDATAR
	0x4100 500C ~ 0x4100 500F	4		FCTRLR
	0x4100 5010 ~ 0x4100 5013	4		FSTATR
	0x4100 5014 ~ 0x4100 5017	4		FLOCKR0
	0x4100 5018 ~ 0x4100 501B	4		FLOCKR1
	0x4100 5030 ~ 0x4100 5033	4		FKEYR0
	0x4100 5034 ~ 0x4100 5037	4		FKEYR1
	0x4100 5038 ~ 0x4100 503B	4		BSADDR0
	0x4100 503C ~ 0x4100 503F	4		BSADDR1

The W7500P embedded Flash memory can be programmed using in-circuit programming or in-application programming.

The **in-circuit programming (ICP)** method is used to update the entire contents of the Flash memory using the SWD protocol or the boot loader to load the user application into the microcontroller. ICP offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices.

In contrast to the ICP method, **in-application programming (IAP)** can use any communication interface supported by the microcontroller (I/Os, UART, I2C, SPI, etc.) to download programming data into memory. IAP allows the user to re-program the Flash memory while the application is running. Nevertheless, part of the application has to have been previously programmed in the Flash memory using ICP.

The program and erase operations can be performed over the whole product voltage range.

They are managed through the following seven Flash registers:

- Flash access control register (FACCR)
- Flash address register (FADDR)
- Flash data register (FDATAR)
- Flash control register (FCTRLR)
- Flash status register (FSTATR)
- Flash lock register (FLOCKR0/R1)
- Flash key register (FKEYR0/R1)

Unlocking the Flash access Control register (FACCR)

After reset, the Flash memory is protected against unwanted write or erase operations. The FACCR register is not accessible in write mode. An unlocking sequence should be written to

the FKEYR0/R1 register to open the access to the FACCR register. This sequence consists of two write operations:

- Write KEY 0 (FKEYR0) = 0x52537175
- Write KEY 1 (FKEYR1) = 0xA91875FC

Any wrong sequence locks up the FACCR register.

The FACCR register can be locked again by finishing flash control operation.

9.2.2 Read operations

The embedded Flash module can be addressed directly as a common memory space. The instruction fetch and the data access are both done through the same AHB bus. Read accesses can be performed with the following options managed through the Flash control register. (FCTRLR)

The Flash reading sequence using FCTRLR register is as below:

1. Check that no main Flash memory operation is ongoing by checking the RDY bit in the FSTATR register.
2. Set KEY in FKEYR0/R1 for setting FACCR register.
3. Set FEN and CTRL bits in the FACCR register.
4. Write main Flash memory address or Data block address to FADDR register.
5. Set RDI or RD bit in FACTRLR to 1. If use RDI bit, don’t need to set FADDR again due to increase automatically by SZ bit in FACCR register.
6. Read data from FDATAR register.
7. Wait until the RDY bit is 1 in the FSTATR register.(it is set when the programming operation has succeeded)
8. Set KEY in FKEYR0/R1 for clearing FACCR register.
9. Clear FEN and CTRL bits in the FACCR register

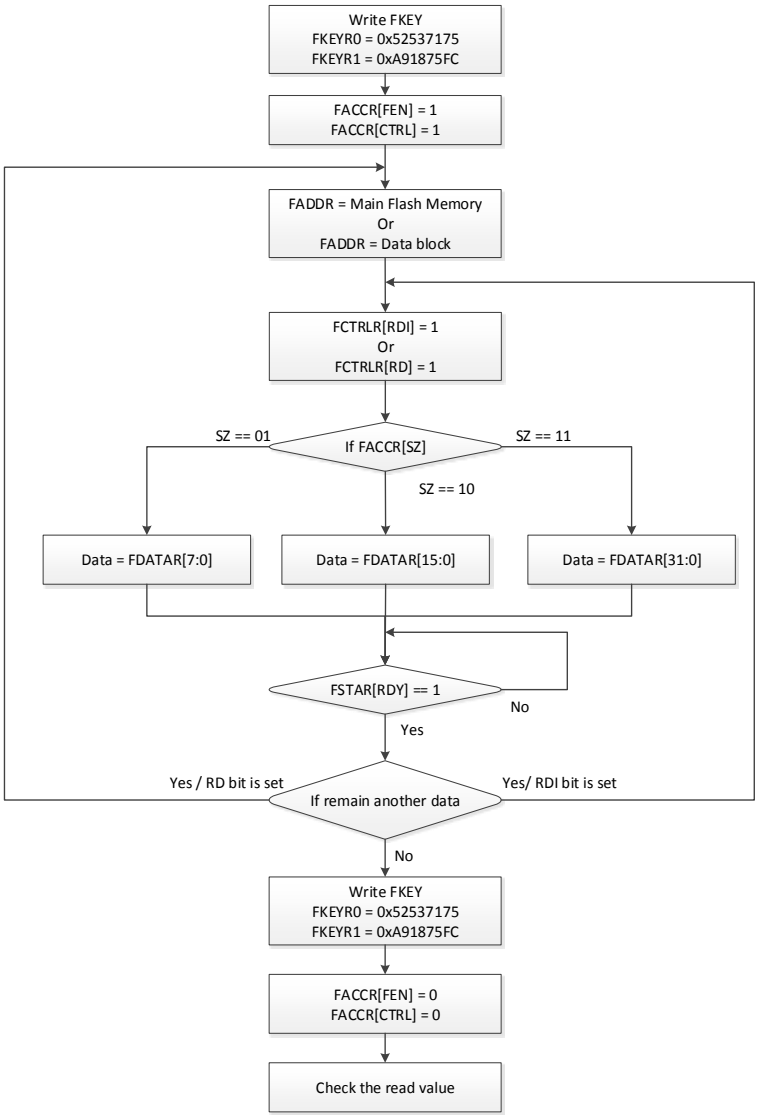


Figure 7. Flash reading sequence

9.2.3 Flash erase operations

Sector Erase

Follow the procedure below to erase a sector:

1. Check that no Flash memory operation is ongoing by checking the RDY bit in the FSTATR register.
2. Set KEY in FKEYR0/R1 for setting FACCR register.
3. Set FEN and CTRL bits in the FACCR register.
4. Write main Flash memory address to FADDA register to erase.
5. Set SER bit in FACTRLR to 1.
6. Wait until the RDY bit is 1 in the FSTATR register.
7. Set KEY in FKEYR0/R1 for clearing FACCR register.
8. Clear FEN and CTRL bits in the FACCR register

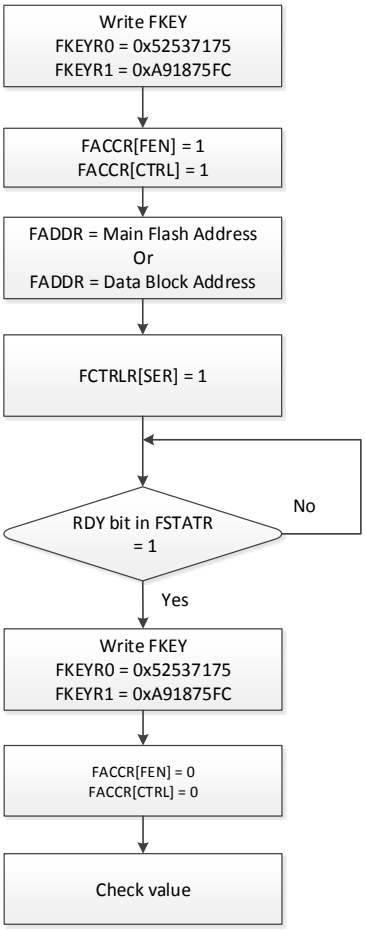


Figure 8. Flash erase operations

Block Erase

To erase a block, set BER bit in FACTRLR to 1. All other procedures are the same as the sector erase sequence.

Chip Erase (All main Flash memory erase)

To erase chip (Main Flash memory), Set CER bit in FACTRLR to 1. All other procedures are the same as the sector erase sequence.

Mass Erase (All main Flash memory erase + Data block erase)

To erase mass (Main Flash memory + Data block), Set MER bit in FACTRLR to 1. All other procedures are the same as the sector erase sequence.

9.2.4 Flash program operation

The main Flash memory can be programmed word, half word, or 1 byte at a time by SZ bit of FACCR. The program operation is started when the CPU writes a data into a main Flash memory address with the WRI or WR bit of FCTRLR register set.

The main Flash memory programming sequence in standard mode is as below:

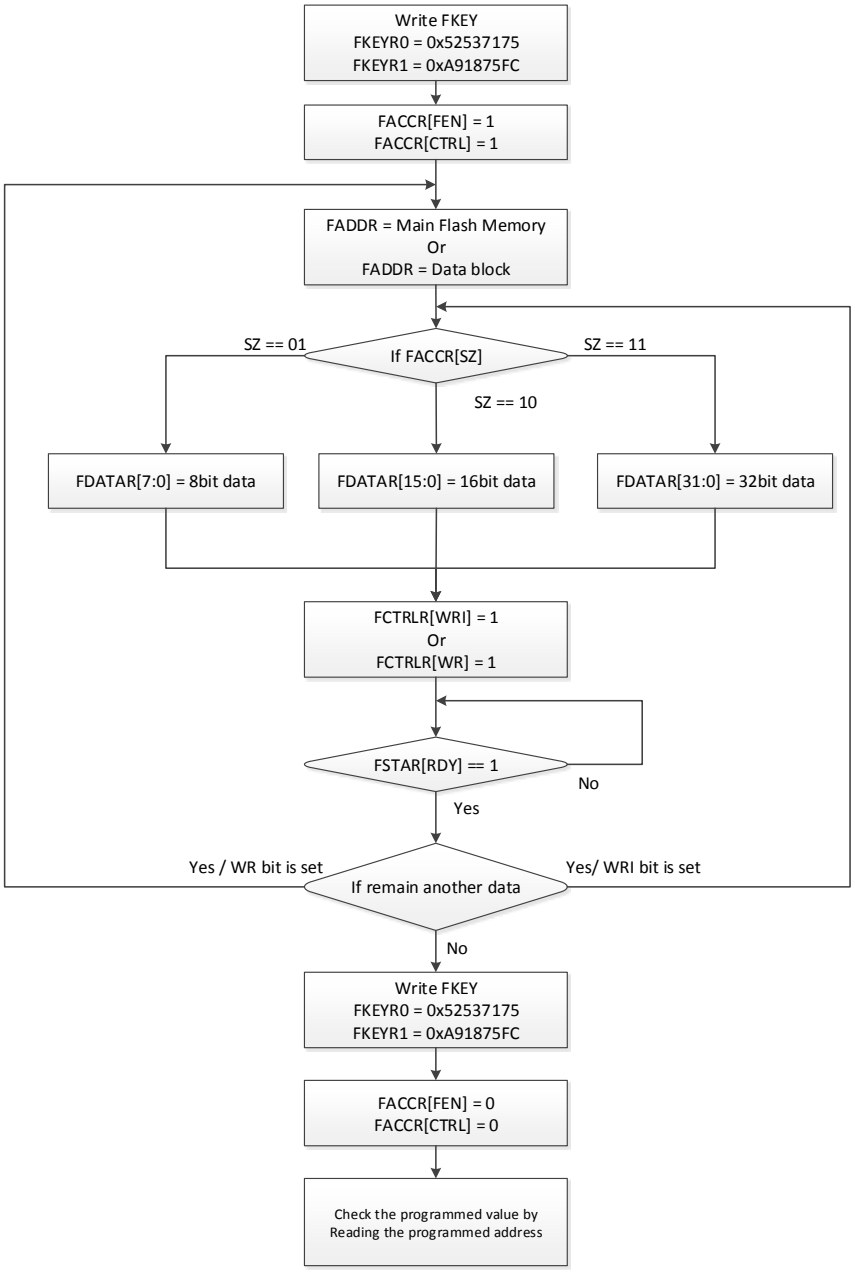


Figure 9. main Flash memory programming sequence

1. Check that no main Flash memory operation is ongoing by checking the RDY bit in the FSTATR register.

2. Set KEY in FKEYR0/R1 for setting FACCR register.
3. Set FEN and CTRL bits in the FACCR register.
4. Write main Flash memory address or Data block address to FADDR register.
5. Write data to FDATAR register.
6. Set WRI or WR bit in FACTRLR to 1. If use WRI bit, don't need to set FADDR again due to increase automatically by SZ bit in FACCR register.
7. Wait until the RDY bit is 1 in the FSTATR register.(it is set when the programming operation has succeeded)
8. Set KEY in FKEYR0/R1 for clearing FACCR register.
9. Clear FEN and CTRL bits in the FACCR register

9.3 Memory protection

The user area of the Flash memory can be protected against read by untrusted code. The blocks of the Flash memory can also be protected against unwanted write due to loss of program counter contexts. The write-protection granularity is one block (4Kbyte).

9.3.1 Read protection

The read protection is activated by DRL bit and CRL bit in FLOCKR0 register.

- DRL0 : read protection to Data0 area in Data block.
- DRL1 : read protection to Data1 area.in Data block
- CRL : read protection to main Flash memory

9.3.2 Write protection

The write protection is implemented with a granularity of one block. It is activated by configuring the FLOCKR1 register or DWL bit, CABWL bit in FLOCKR0 register.

- FLOCKR1 : write protection to main Flash memory with a granularity of one block.
- DWL0 : write protection to Data0 area in Data block.
- DWL1 : write protection to Data1 area in Data block.
- CABWL : write protection to main Flash memory all block.

10 Clock Reset generator (CRG)

10.1 Introduction

CRG is clock reset generator block for W7500P System. It provides every clock/reset for all other block include CPU and peripherals. CRG includes PLL and POR.

10.2 Features

10.2.1 Reset

- Three types of reset – external reset, Power reset, system reset
- External reset is generated by low level on the RSTn pin (external reset)
- Power reset is generated by Power-on reset (POR)
- Power on reset is generated by POR
- System reset is generated when one of the following events occurs
  - Watchdog event
  - After remapping
  - Software reset (SYSRESETREQ bit in Cortex-M0. Refer to the Cortex-M0 technical reference manual for more detail)
- Power reset sets all registers to their reset values.
- System reset sets all registers to their reset values except the CRG block registers and remap register to protect remap value

10.2.2 Clock

Two clock sources can be used to drive the system clock.

- External oscillator clock (8MHz ~ 24MHz) (OCLK)
- Internal 8MHz RC oscillator clock (RCLK)

One additional clock source

- 32.768KHz low speed external crystal which derives the real time clock.

There is a PLL

One PLL is integrated

- Input clock range is from 8MHz to 24MHz
- Frequency can be generated by M/N/OD registers. (refer register description)
- Bypass option enabled

There are many generated clocks for independent operating with system clock

- System clock (FCLK)
- ADC clock (ADCCLK)
- SSP0, SSP1 clock (SSPCLK)
- UART0, UART1 clock (UARTCLK)

- Two Timer clocks (TIMCLK0, TIMCLK1)
- 8ea PWM clocks (PWMCLK0 - PWMCLK7)
- Real time clock (RTCCLK)
- WDOG clock (WDOGCLK)
- Random number generator clock (RNGCLK)

RNGCLK have only one source (pll output) and no prescaler

Some of the generated clocks turn off automatically when CPU enters sleep mode.

- ADCCLK, RNGCLK

Generate two Hardware TCPIP Clocks (MII_RXC, MII_TXC) are from external PADs.

Hardware TCPIP Clocks can be gated by register control.

All clocks generated from CRG can be monitored.

10.3 Functional description

Figure 10 shows the CRG block diagram.

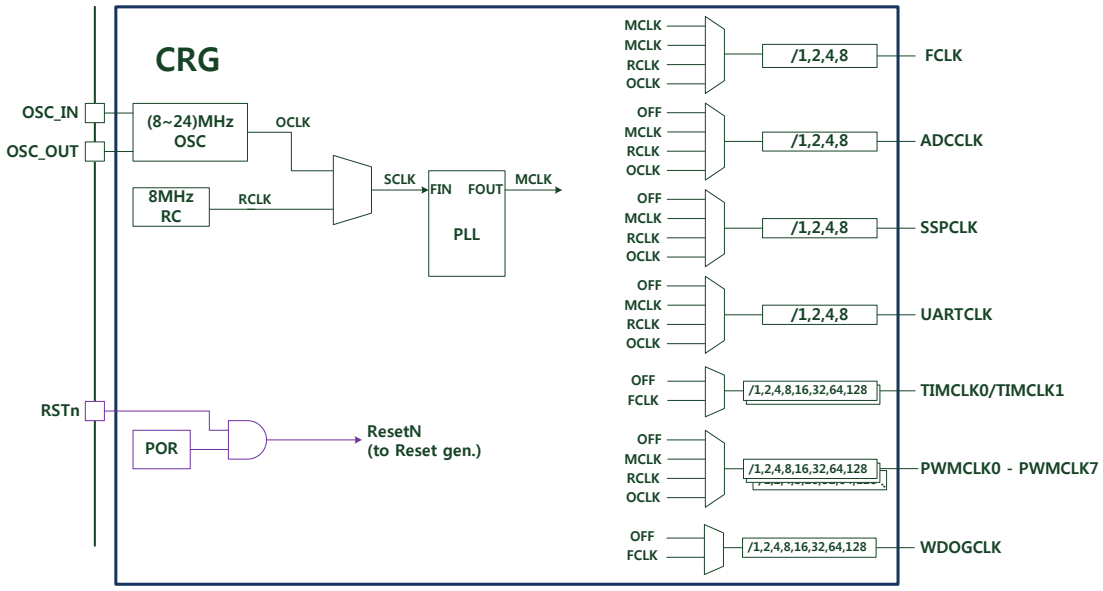


Figure 10 CRG block diagram

10.3.1 External Oscillator Clock

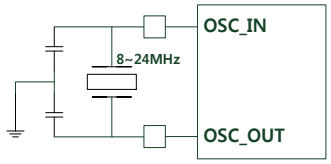
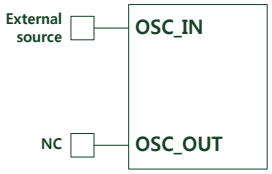
External oscillator clock (OCLK) can be generated from two possible clock source

- External crystal/ceramic resonator (8 to 24MHz external oscillator)
- User external clock

Table 7 shows the two clock sources of external oscillator clock

Table 7 External oscillator clock sources

	External clock	Crystal/

		Ceramic resonators
Schematic		

10.3.2RC oscillator clock

RC oscillator clock (RCLK) signal is generated from an internal 8MHz RC oscillator.
RC oscillator has the advantage of providing a clock source at low cost (no external components). However the RC oscillator is less accurate than the external crystal or ceramic resonator.

- Accuracy : 1% at T_A= 25ºC (User don't need to calibration)

10.3.3PLL

The internal PLL can be used to multiply the External Oscillator Clock (OCLK) or RC Oscillator Clock (RCLK). PLL input can be selected by register.
PLL output clock can be generated by following the equations below.

- FOUT = FIN x M / N x 1 / OD
- Where:
- $M = M[5] \times 2^5 + M[4] \times 2^4 + M[3] \times 2^3 + M[2] \times 2^2 + M[1] \times 2 + M[0] \times 1$
- $N = N[5] \times 2^5 + N[4] \times 2^4 + N[3] \times 2^3 + N[2] \times 2^2 + N[1] \times 2 + N[0] \times 1$
- $OD = 2^{(2 \times OD[1])} \times 2^{(1 \times OD[0])}$

10.3.4Generated clock

Each generated clock source can be selected among 3 clock source as independent by each clock source select register.

- PLL output clock (MCLK)
- Internal 8MHz RC oscillator clock (RCLK)
- External oscillator clock (8MHz ~ 24MHz) (OCLK)

Each generated clock has own prescaler which can be selected individually by each prescale value register.

- FCLK, ADCCLK, SSPCLK, UARTCLK : 1/1, 1/2, 1/4, 1/8
  - TIMCLK0, TIMCLK1, PWMCLK0 – PWMCLK7, RTCCLK, WDOGCLK : 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128

10.4 Registers (Base address : 0x4100_1000)

10.4.1OSC power down register (OSC_PDR)

Address offset : 0x000

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OSCPD
															R/W

[0] OSCPD – Internal 8MHz RC oscillator power down register

This bit written by S/W to RCOSC enter sleep mode or not

0 : normal operation

1 : power down (enter sleep mode)

10.4.2PLL power down register (PLL_PDR)

Address offset : 0x010

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PLLPD
															R/W

[0] PLLPD – PLL power down register

This bit written by S/W to PLL power down or not

0 : power down

1 : normal operation

10.4.3PLL frequency calculating register (PLL_FCR)

Address offset : 0x014

Reset value : 0x0005_0200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	M					

										R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	N						res	res	res	res	res	res	OD	
		R/W												R/W	

[1:0] OD

[13:8] N

[21:16] M

These bits are written by S/W to set frequency of PLL output.

PLL output frequency FOUT is calculated by the following equations:

FOUT = FIN x M / N x 1 / OD

Where:

M = M[5] x 32 + M[4] x 16 + M[3] x 8 + M[2] x 4 + M[1] x 2 + M[0] x 1 (2 ~ 63)

N = N[5] x 32 + N[4] x 16 + N[3] x 8 + N[2] x 4 + N[1] x 2 + N[0] x 1 (1 ~ 63)

OD = $2^{(2 \times OD[1])} \times 2^{(1 \times OD[0])}$

10.4.4PLL output enable register (PLL_OER)

Address offset : 0x018

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PLLOEN
															R/W

[0] PLLOEN – output enable register of PLL

This bit written by S/W to control output enable of PLL

0 : Clock out is disable. VCO is working but FOUT is low only.

1 : Clock out is enable.

10.4.5PLL bypass register (PLL_BPR)

Address offset : 0x01c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PLLBP
															R/W

[0] PLLBP – bypass register of PLL

This bit written by S/W to control bypass or not of PLL

0 : bypass disable. Normal operation

1 : bypass enable. Clock out is clock input

10.4.6PLL input clock source select register (PLL_IFSR)

Address offset : 0x020

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PLLIS
															R/W

[0] PLLIS – select register of PLL input clock source

This bit written by S/W to select

0 : Internal 8MHz RC oscillator clock (RCLK)

1 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.7FCLK source select register (FCLK_SSR)

Address offset : 0x030

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	FCKSRC	
														R/W	

[1:0] FCKSRC – select register of FCLK clock source

These bits are written by S/W to select

00, 01 : output clock of PLL (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.8FCLK prescale value select register (FCLK_PVSR)

Address offset : 0x034

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	FCKPRE	
														R/W	

[1:0] FCKPRE – select prescale value of FCLK clock

These bits are written by S/W to select

00 : 1/1 (bypass)

01 : 1/2

10 : 1/4

11 : 1/8

10.4.9SSPCLK source select register (SSPCLK_SSR)

Address offset : 0x040

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	SSPCSS	
														R/W	

[1:0] SSPCSS – SSPCLK clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.10 SSPCLK prescale value select register (SSPCLK_PVSR)

Address offset : 0x044

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	SSPCP	
														R/W	

[1:0] SSPCP – select prescale value of SSPCLK clock

These bits are written by S/W to select

00 : 1/1 (bypass)

01 : 1/2

10 : 1/4

11 : 1/8

10.4.11 ADCCLK source select register (ADCCLK_SSR)

Address offset : 0x060

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	ADCSS	
														R/W	

[1:0] ADCSS – ADCCLK clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.12 ADCCLK prescale value select register (ADCCLK_PVSR)

Address offset : 0x064

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	ADCCP	
														R/W	

[1:0] ADCCP – select prescale value of ADCCLK clock

These bits are written by S/W to select

00 : 1/1 (bypass)

01 : 1/2

10 : 1/4

11 : 1/8

10.4.13 TIMER0CLK source select register (TIMER0CLK_SSR)

Address offset : 0x070

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	T0CSS
															R/W

[0] T0CSS – TIMCLK0 clock source select register.

These bits are written by S/W to select clock source

0 : disable clock

1 : FCLK

10.4.14 TIMER0CLK prescale value select register (TIMER0CLK_PVSR)

Address offset : 0x074

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	T0CPS		
													R/W		

[2:0] T0CPS – select prescale value of TIM0CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.15 TIMER1CLK source select register (TIMER1CLK_SSR)

Address offset : 0x080

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	T1CSS
															R/W

[0] T1CSS – TIMCLK1 clock source select register.

These bits are written by S/W to select clock source

0 : disable clock

1 : FCLK

10.4.16 TIMER1CLK prescale value select register (TIMER1CLK_PVSR)

Address offset : 0x084

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	T1CPS		
													R/W		

[2:0] T1CPS – select prescale value of TIM1CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.17 PWM0CLK source select register (PWM0CLK_SSR)

Address offset : 0x0b0

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	P0CSS	
														R/W	

[1:0] P0CPS – PWMCLK0 clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.18 PWM0CLK prescale value select register (PWM0CLK_PVSR)

Address offset : 0x0b4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	P0CPS		
													R/W		

[2:0] P0CPS – select prescale value of PWM0CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.19 PWM1CLK source select register (PWM1CLK_SSR)

Address offset : 0x0c0

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	P1CSS	
														R/W	

[1:0] P1CSS – PWMCLK1 clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.20 PWM1CLK prescale value select register (PWM1CLK_PVSR)

Address offset : 0x0c4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	P1CPS		
													R/W		

[2:0] P1CPS – select prescale value of PWM1CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.21 PWM2CLK source select register (PWM2CLK_SSR)

Address offset : 0x0d0

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	P2CSS	
														R/W	

[1:0] P2CSS – PWMCLK2 clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.22 PWM2CLK prescale value select register (PWM2CLK_PVSR)

Address offset : 0x0d4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	P2CPS		
													R/W		

[2:0] PWM2CLK_PRE – select prescale value of PWM2CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.23 PWM3CLK source select register (PWM3CLK_SSR)

Address offset : 0x0e0

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	P3CSS	
														R/W	

[1:0] P3CSS – PWMCLK3 clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.24 PWM3CLK prescale value select register (PWM3CLK_PVSR)

Address offset : 0x0e4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	P3CPS		
													R/W		

[2:0] P3CPS – select prescale value of PWM3CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.25 PWM4CLK source select register (PWM4CLK_SSR)

Address offset : 0x0f0

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	P4CSS	
														R/W	

[1:0] P4CSS – PWMCLK4 clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.26 PWM4CLK prescale value select register (PWM4CLK_PVSR)

Address offset : 0x0f4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	P4CPS		
													R/W		

[2:0] P4CPS – select prescale value of PWM4CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.27 PWM5CLK source select register (PWM5CLK_SSR)

Address offset : 0x100

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	P5CSS	
														R/W	

[1:0] P5CSS – PWMCLK5 clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.28 PWM5CLK prescale value select register (PWM5CLK_PVSR)

Address offset : 0x104

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	P5CPS		
													R/W		

[2:0] P5CPS – select prescale value of PWM5CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.29 PWM6CLK source select register (PWM6CLK_SSR)

Address offset : 0x110

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	P6CSS	
														R/W	

[1:0] P6CSS – PWMCLK6 clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.30 PWM6CLK prescale value select register (PWM6CLK_PVSR)

Address offset : 0x114

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	P6CPS		
													R/W		

[2:0] P6CPS – select prescale value of PWM6CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.31 PWM7CLK source select register (PWM7CLK_SSR)

Address offset : 0x120

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	P7CSS	
														R/W	

[1:0] P7CSS – PWMCLK7 clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.32 PWM7CLK prescale value select register (PWM7CLK_PVSR)

Address offset : 0x124

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	P7CPS		
													R/W		

[2:0] P7CPS – select prescale value of PWM7CLK clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.33 WDOGCLK High Speed source select register (WDOGCLK_HS_SSR)

Address offset : 0x140

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	WDHS
															R/W

[1:0] WDHS – WDOGCLK_hs clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.34 WDOGCLK High Speed prescale value select register (WDOGCLK_HS_PVSR)

Address offset : 0x144

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	WDPRE		
													R/W		

[2:0] WDPRE – select prescale value of WDOGCLK_hs clock

These bits are written by S/W to select

000 : 1/1 (bypass)

001 : 1/2

010 : 1/4

011 : 1/8

100 : 1/16

101 : 1/32

110 : 1/64

111 : 1/128

10.4.35 UARTCLK source select register (UARTCLK_SSR)

Address offset : 0x150

Reset value : 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	UCSS	
														R/W	

[1:0] UCSS – UARTCLK clock source select register.

These bits are written by S/W to select clock source

00 : disable clock

01 : PLL output clock (MCLK)

10 : Internal 8MHz RC oscillator clock (RCLK)

11 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

10.4.36 UARTCLK prescale value select register (UARTCLK_PVSR)

Address offset : 0x154

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	UCP	
														R/W	

[1:0] UCP – select prescale value of UARTCLK clock

These bits are written by S/W to select

00 : 1/1 (bypass)

01 : 1/2

10 : 1/4

11 : 1/8

10.4.37 MIICLK enable control register (MIICLK_ECR)

Address offset : 0x160

Reset value : 0x0000_0003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIITEN	MIIREN
														R/W	R/W

[0] MIIREN – MII RX Clock source enable register

This bit is written by S/W to set enable or disable

0 : Disable MII_RCK and MII_RCK_N

1 : Enable MII_RCK and MII_RCK_N

[1] MIITEN – MII TX Clock source enable register

This bit is written by S/W to set enable or disable

0 : Disable MII_TCK and MII_TCK_N

1 : Enable MII_TCK and MII_TCK_N

10.4.38 Monitoring Clock source select register (MONCLK_SSR)

Address offset : 0x170

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	CLKMON_SEL				
											R/W				

[4:0] CLKMON_SEL – Select clock source for monitoring (monitoring pin : PA_02)

This bit is written by S/W to set enable or disable

00000 : PLL output clock (MCLK)

00001 : FCLK

00010 : Internal 8MHz RC oscillator clock (RCLK)

00011 : External oscillator clock (OCLK, 8MHz ~ 24MHz)

00100 : ADCCLK

00101 : SSPCLK

00110 : TIMCLK0

00111 : TIMCLK1

01000 : PWMCLK0

01001 : PWMCLK1

01010 : PWMCLK2

01011 : PWMCLK3

01100 : PWMCLK4

01101 : PWMCLK5

01110 : PWMCLK6

01111 : PWMCLK7

10000 : UARTCLK

10001 : MII_RCK

10010 : MII_TCK

10011 : RTCCLK

10.5 Register map

The following Table 8 summarizes the CRG registers.

Table 8 CRG register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	OSC_PDR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OSCPD
	reset value																																0
0x010	PLL_PDR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PLLPD
	reset value																																0
0x014	PLL_FCR	res	res	res	res	res	res	res	res	res	res	M						res	res	N						res	res	res	res	res	res	res	OD
	reset value											0	0	0	1	0	1			0	0	0	0	1	0							0	0
0x018	PLL_OER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PLLOEN
	reset value																																1
0x01c	PLL_BPR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PLLBP
	reset value																																0
0x020	PLL_IFSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PLLIS
	reset value																																0
0x030	FCLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	FCKSRC
	reset value																															0	1
0x034	FCLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	FCKPRE
	reset value																															0	0
0x040	SSPCLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	SSPCSS
	reset value																															0	1
0x044	SSPCLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	SSPCP
	reset value																															0	0
0x060	ADCCLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ADCSS
	reset value																															0	1
0x064	ADCCLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ADCCP
	reset value																															0	0
0x070	TIMER0CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	T0CSS
	reset value																															0	1
0x074	TIMER0CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	T0CPS		
	reset value																														0	0	0
0x080	TIMER1CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	T1CSS
	reset value																															0	1
0x084	TIMER1CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	T1CPS		
	reset value																														0	0	0
0x0b0	PWM0CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P0CSS
	reset value																															0	1
0x0b4	PWM0CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P0CPS		
	reset value																														0	0	0

0x0c0	PWM1CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P1CSS	
	reset value																															0	1
0x0c4	PWM1CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P1CPS		
	reset value																														0	0	0
0x0d0	PWM2CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P2CSS	
	reset value																															0	1
0x0d4	PWM2CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P2CPS		
	reset value																														0	0	0
0x0e0	PWM3CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P3CSS	
	reset value																															0	1
0x0e4	PWM3CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P3CPS		
	reset value																														0	0	0
0x0f0	PWM4CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P4CSS	
	reset value																															0	1
0x0f4	PWM4CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P4CPS		
	reset value																														0	0	0
0x100	PWM5CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P5CSS	
	reset value																															0	1
0x104	PWM5CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P5CPS		
	reset value																														0	0	0
0x110	PWM6CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P6CSS	
	reset value																															0	1
0x114	PWM6CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P6CPS		
	reset value																														0	0	0
0x120	PWM7CLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P7CSS	
	reset value																															0	1
0x124	PWM7CLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	P7CPS		
	reset value																														0	0	0
0x140	WDOGCLK_HS_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	WDHS	
	reset value																															0	1
0x144	WDOGCLK_HS_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	WDPRE		
	reset value																														0	0	0
0x150	UARTCLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UCSS	
	reset value																															0	1
0x154	UARTCLK_PVSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UCP	
	reset value																															0	0
0x160	MIICLK_ECR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIITEN	MIIREN
	reset value																															1	1
0x170	MONCLK_SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CLKMON_SEL				
	reset value																												0	0	0	0	0

11 Random number generator (RNG)

11.1 Introduction

RNG is a 32bit random number generator. RNG generates power on random number when power on reset. RNG can run/stop by software. RNG seed value and polynomial of RNG can be modified by software.

11.2 Features

- 32bit pseudo random number generator
- Formula of pseudo random number generator (polynomial) can be modified.
- Seed value of random generator can be modified.
- Support power on reset random value.
- Random value can be obtains by control start/stop by software.

11.3 Functional description

Figure 11 shows the RNG block diagram.

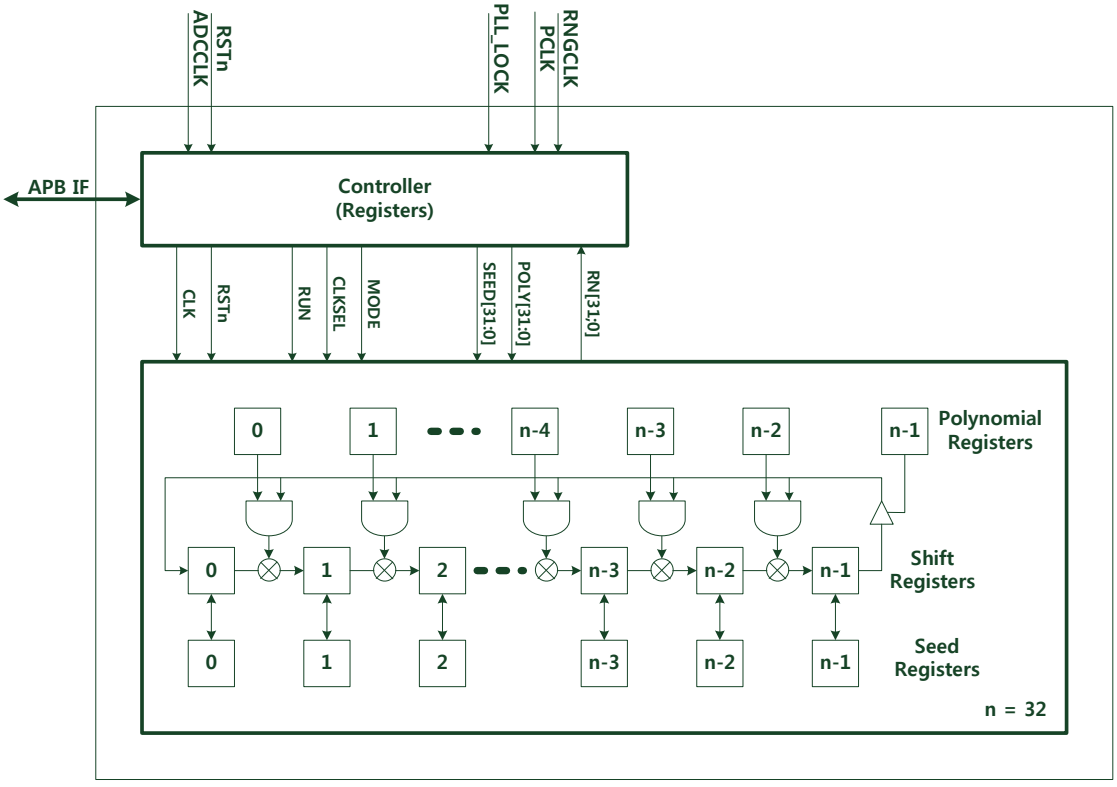


Figure 11. Random Number Generator block diagram

11.3.1 Operation RNG

Figure 12 shows the flowchart of RNG operation.

A random number is automatically generated after powering on reset,

Follow the procedure below to manually generate a random number.

1. Change MODE to start/stop by register.
2. Change clock source / seed value / polynomial value if need.
3. Run and Stop the RNG.
4. Read Random value.

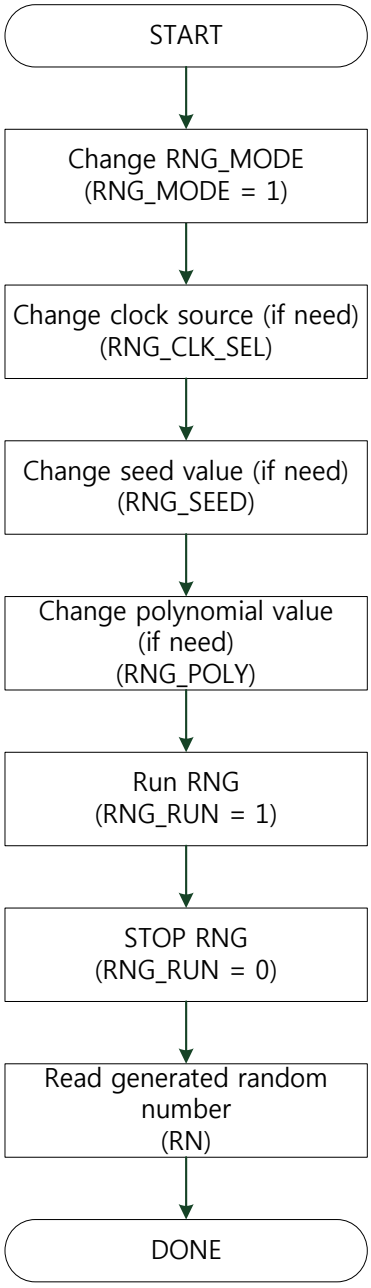


Figure 12. Flow chart of RNG operation

11.4 Registers (Base address : 0x4000_7000)

11.4.1 RNG run register (RNG_RUN)

Address offset : 0x000

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RUN
															R/W

[0] RUN – run RNG shift register

This bit written by S/W to run or stop RNG

0 : stop random number generator shift register

1 : run random number generator shift register

11.4.2 RNG SEED register (RNG_SEED)

Address offset : 0x004

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEED[31:16]															
R/W															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEED[15:0]															
R/W															

[31:0] SEED – seed value of random number generator shift register

These bits written by S/W to set seed value of RNG before start(run) RNG shift register

11.4.3 RNG clock select register (RNG_CLKSEL)

Address offset : 0x008

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CLKSEL
															R/W

[0] CLKSEL – select clock source register of RNG shift register

This bit written by S/W to select clock source of RNG shift register

0 : RNG clock (refer to clock generator block)

1 : PCLK

11.4.4 RNG manual mode select register (RNG_MODE)

Address offset : 0x00c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MODE
															R/W

[0] MODE – RNG run mode select register

This bit written by S/W to select which mode

0 : run/stop by PLL_LOCK signal (which is for power on random number)

1 : run/stop by RNG_RUN register (refer 1.4.1)R

11.4.5 RNG random number value register (RNG_RN)

Address offset : 0x010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RN[31:16]															
R															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RN[15:0]															

R

[31:0] RN – random number of RNG shift register

These bits are read only registers.

11.4.6 RNG polynomial register (RNG_POLY)

Address offset : 0x014

Reset value : 0xE000_0202

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POLY[31:16]															
R/W															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLY[15:0]															
R/W															

[31:0] POLY – 32bit polynomial of random number generator

These bits are written by S/W to modify the formula of random number generator

Default polynomial: $F(x) = x^{31} + x^{30} + x^{29} + x^{9} + x$

11.5 Register map

The following Table 9 summarizes the RNG registers.

Table 9 RNG register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	RNG_RUN	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RUN
	reset value																																0
0x004	RNG_SEED	SEED																															
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x008	RNG_CLKSEL	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CLKSEL
	reset value																																0
0x00C	RNG_MODE	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MODE
	reset value																																0
0x010	RNG_RN	RN																															
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x014	RNG_POLY	POLY																															
	reset value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	

12 Alternate Function Controller (AFC)

12.1 Introduction

Each functional PADs have several functions.

Users can select a function in Alternate Function Controller block.

12.2 Features

Each functional pad has 2 ~ 4 functions.

Pads can be selected by each registers individually.

Each pad can be used as an external interrupt source.

12.3 Functional description

Table 10 shows the function table of each functional pad.

Table 10 functional description table

		function selection register value			
		00 (reset value)	01	10	11
PAD	PIN	Normal Function	2nd Function	3rd Function	4th Function
PA_00	27	GPIO1_0	GPIO1_0	PWM6/CAP6	
PA_01	28	GPIO1_1	GPIO1_1	PWM7/CAP7	
PA_02	29	GPIO1_2	GPIO1_2	CLKOUT	
PA_03	30	SWCLK	GPIO1_3		PWM0/CAP0
PA_04	31	SWDIO	GPIO1_4		
PA_05	19	SSEL0	GPIO1_5	SCL1	PWM2/CAP2
PA_06	20	SCLK0	GPIO1_6	SDA1	
PA_07	21	MISO0	GPIO1_7	U_CTS1	PWM4/CAP4
PA_08	22	MOSI0	GPIO1_8	U_RTS1	PWM5/CAP5
PA_09	23	SCL0	GPIO1_9	U_TXD1	PWM6/CAP6
PA_10	24	SDA0	GPIO1_10	U_RXD1	PWM7/CAP7
PA_11	41	U_CTS0	GPIO1_11	SSEL1	
PA_12	42	U_RTS0	GPIO1_12	SCLK1	
PA_13	43	U_TXD0	GPIO1_13	MISO1	
PA_14	44	U_RXD0	GPIO1_14	MOSI1	
PB_00	45	SSEL1	GPIO2_0	U_CTS0	
PB_01	46	SCLK1	GPIO2_1	U_RTS0	
PB_02	47	MISO1	GPIO2_2	U_TXD0	
PB_03	48	MOSI1	GPIO2_3	U_RXD0	

PB_06	15	DUP	GPIO2_6		
PC_00	53	U_CTS1	GPIO3_0	PWM0/CAP0	
PC_01	54	U_RTS1	GPIO3_1		
PC_02	55	U_TXD1	GPIO3_2	PWM2/CAP2	
PC_03	56	U_RXD1	GPIO3_3		
PC_04	57	SCL1	GPIO3_4	PWM4/CAP4	
PC_05	58	SDA1	GPIO3_5	PWM5/CAP5	
PC_06	11	GPIOC_6	GPIO3_6	U_TXD2	
PC_08	1	PWM0/CAP0	GPIO3_8	SCL0	AIN7
PC_09	2	PWM1/CAP1	GPIO3_9	SDA0	AIN6
PC_10	3	U_TXD2	GPIO3_10	PWM2/CAP2	AIN5
PC_11	4	U_RXD2	GPIO3_11	PWM3/CAP3	AIN4
PC_12	5	AIN3	GPIO3_12	SSEL0	AIN3
PC_13	6	AIN2	GPIO3_13	SCLK0	AIN2
PC_14	7	AIN1	GPIO3_14	MISO0	AIN1
PC_15	8	AIN0	GPIO3_15	MOSI0	AIN0

12.4 Registers (Base address : 0x4100_2000)

12.4.1 PA_00 pad alternate function select register (PA_00_AFR)

Address offset : 0x000

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA00AF	
														R/W	

[1:0] PA00AF – PA_00 Pad alternate function selection register.

These bits are written by S/W.

00 : GPIOA_0

01 : GPIOA_0

10 : PWM6/CAP6

11 : None

12.4.2 PA_01 pad alternate function select register (PA_01_AFR)

Address offset : 0x004

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA01AF	
														R/W	

[1:0] PA01AF – PA_01 Pad function selection register.

These bits are written by S/W.

00 : GPIOA_1

01 : GPIOA_1

10 : PWM7/CAP7

11 : None

12.4.3 PA_02 pad alternate function select register (PA_02_AFR)

Address offset : 0x008

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA02AF	
														R/W	

[1:0] PA02AF – PA_02 Pad function selection register.

These bits are written by S/W.

00 : GPIOA_2

01 : GPIOA_2

10 : CLKOUT

11 : None

12.4.4 PA_03 pad alternate function select register (PA_03_AFR)

Address offset : 0x00c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA03AF	
														R/W	

[1:0] PA03AF – PA_03 Pad function selection register.

These bits are written by S/W.

00 : SWCLK

01 : GPIOA_3

10 : None

11 : PWM0/CAP0

12.4.5 PA_04 pad alternate function select register (PA_04_AFR)

Address offset : 0x010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA04AF	
														R/W	

[1:0] PA04AF – PA_04 Pad function selection register.

These bits are written by S/W.

00 : SWDIO

01 : GPIOA_4

10 : None

11 : PWM1/CAP1

12.4.6 PA_05 pad alternate function select register (PA_05_AFR)

Address offset : 0x014

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA05AF	
														R/W	

[1:0] PA05AF – PA_05 Pad function selection register.

These bits are written by S/W.

00 : SSEL0

01 : GPIOA_5

10 : SCL1

11 : PWM2/CAP2

12.4.7 PA_06 pad alternate function select register (PA_06_AFR)

Address offset : 0x018

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA06AF	
														R/W	

[1:0] PA06AF – PA_06 Pad function selection register.

These bits are written by S/W.

00 : SCLK0

01 : GPIOA_6

10 : SDA1

11 : PWM3/CAP3

12.4.8 PA_07 pad alternate function select register (PA_07_AFR)

Address offset : 0x01c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA07AF	
														R/W	

[1:0] PA07AF – PA_07 Pad function selection register.

These bits are written by S/W.

00 : MISO0

01 : GPIOA_7

10 : CTS1

11 : PWM4/CAP4

12.4.9 PA_08 pad alternate function select register (PA_08_AFR)

Address offset : 0x020

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA08AF	
														R/W	

[1:0] PA08AF – PA_08 Pad function selection register.

These bits are written by S/W.

00 : MOSI0

01 : GPIOA_8

10 : RTS1

11 : PWM5/CAP5

12.4.10 PA_09 pad alternate function select register (PA_09_AFR)

Address offset : 0x024

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA09AF	
														R/W	

[1:0] PA09AF – PA_09 Pad function selection register.

These bits are written by S/W.

00 : SCL0

01 : GPIOA_9

10 : TXD1

11 : PWM6/CAP6

12.4.11 PA_10 pad alternate function select register (PA_10_AFR)

Address offset : 0x028

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA10AF	
														R/W	

[1:0] PA10AF – PA_10 Pad function selection register.

These bits are written by S/W.

00 : SDA0

01 : GPIOA_10

10 : RXD1

11 : PWM7/CAP7

12.4.12 PA_11 pad alternate function select register (PA_11_AFR)

Address offset : 0x02c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA11AF	
														R/W	

[1:0] PA11AF – PA_11 Pad function selection register.

These bits are written by S/W.

00 : CTS0

01 : GPIOA_11

10 : SSEL1

11 : None

12.4.13 PA_12 pad alternate function select register (PA_12_AFR)

Address offset : 0x030

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA12AF	
														R/W	

[1:0] PA12AF – PA_12 Pad function selection register.

These bits are written by S/W.

00 : RTS0

01 : GPIOA_12

10 : SCLK1

11 : None

12.4.14 PA_13 pad alternate function select register (PA_13_AFR)

Address offset : 0x034

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA13AF	
														R/W	

[1:0] PA13AF – PA_13 Pad function selection register.

These bits are written by S/W.

00 : TXD0

01 : GPIOA_13

10 : MISO1

11 : None

12.4.15 PA_14 pad alternate function select register (PA_14_AFR)

Address offset : 0x038

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA14AF	
														R/W	

[1:0] PA14AF – PA_14 Pad function selection register.

These bits are written by S/W.

00 : RXD0

01 : GPIOA_14

10 : MOSI1

11 : None

12.4.16 PB_00 pad alternate function select register (PB_00_AFR)

Address offset : 0x040

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB00AF	
														R/W	

[1:0] PB00AF – PB_00 Pad function selection register.

These bits are written by S/W.

00 : SSEL1

01 : GPIOB_0

10 : CTS0

11 : None

12.4.17 PB_01 pad alternate function select register (PB_01_AFR)

Address offset : 0x044

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB01AF	
														R/W	

[1:0] PB01AF – PB_01 Pad function selection register.

These bits are written by S/W.

00 : SCLK1

01 : GPIOB_1

10 : RTS0

11 : None

12.4.18 PB_02 pad alternate function select register (PB_02_AFR)

Address offset : 0x048

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB02AF	
														R/W	

[1:0] PB02AF – PB_02 Pad function selection register.

These bits are written by S/W.

00 : MISO1

01 : GPIOB_2

10 : TXD0

11 : None

12.4.19 PB_03 pad alternate function select register (PB_03_AFR)

Address offset : 0x04c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB03AF	
														R/W	

[1:0] PB03AF – PB_03 Pad function selection register.

These bits are written by S/W.

00 : MOSI1

01 : GPIOB_3

10 : RXD0

11 : None

12.4.20 PB_06 pad alternate function select register (PB_06_AFR)

Address offset : 0x058

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB06AF	
														R/W	

[1:0] PB06AF – PB_06 Pad function selection register.

These bits are written by S/W.

00 : DUP spare

01 : None

10 : None

11 : None

12.4.21 PC_00 pad alternate function select register (PC_00_AFR)

Address offset : 0x080

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC00AF	
														R/W	

[1:0] PC00AF – PC_00 Pad function selection register.

These bits are written by S/W.

00 : CTS1

01 : GPIOC_0

10 : PWM0/CAP0

11 : None

12.4.22 PC_01 pad alternate function select register (PC_01_AFR)

Address offset : 0x084

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC01AF	
														R/W	

[1:0] PC01AF – PC_01 Pad function selection register.

These bits are written by S/W.

00 : RTS1

01 : GPIOC_1

10 : PWM1/CAP1

11 : None

12.4.23 PC_02 pad alternate function select register (PC_02_AFR)

Address offset : 0x088

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC02AF	
														R/W	

[1:0] PC02AF – PC_02 Pad function selection register.

These bits are written by S/W.

00 : TXD1

01 : GPIOC_2

10 : PWM2/CAP2

11 : None

12.4.24 PC_03 pad alternate function select register (PC_03_AFR)

Address offset : 0x08c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC03AF	
														R/W	

[1:0] PC03AF – PC_03 Pad function selection register.

These bits are written by S/W.

00 : RXD1

01 : GPIOC_3

10 : PWM3/CAP3

11 : None

12.4.25 PC_04 pad alternate function select register (PC_04_AFR)

Address offset : 0x090

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC04AF	
														R/W	

[1:0] PC04AF – PC_04 Pad function selection register.

These bits are written by S/W.

00 : SCL1

01 : GPIOC_4

10 : PWM4/CAP4

11 : None

12.4.26 PC_05 pad alternate function select register (PC_05_AFR)

Address offset : 0x094

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC05AF	
														R/W	

[1:0] PC05AF – PC_05 Pad function selection register.

These bits are written by S/W.

00 : SDA1

01 : GPIOC_5

10 : PWM5/CAP5

11 : None

12.4.27 PC_06 pad alternate function select register (PC_06_AFR)

Address offset : 0x098

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC06AF	
														R/W	

[1:0] PC06AF – PC_06 Pad function selection register.

These bits are written by S/W.

00 : GPIOC_6

01 : GPIOC_6

10 : TXD2

11 : None

12.4.28 PC_08 pad alternate function select register (PC_08_AFR)

Address offset : 0x0a0

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC08AF	
														R/W	

[1:0] PC08AF – PC_08 Pad function selection register.

These bits are written by S/W.

00 : PWM0/CAP0

01 : GPIOC_8

10 : SCL0

11 : ADC_IN7

12.4.29 PC_09 pad alternate function select register (PC_09_AFR)

Address offset : 0x0a4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC09AF	
														R/W	

[1:0] PC09AF – PC_09 Pad function selection register.

These bits are written by S/W.

00 : PWM1/CAP1

01 : GPIOC_9

10 : SDA0

11 : ADC_IN6

12.4.30 PC_10 pad alternate function select register (PC_10_AFR)

Address offset : 0x0a8

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC10AF	
														R/W	

[1:0] PC10AF – PC_10 Pad function selection register.

These bits are written by S/W.

00 : TXD2

01 : GPIOC_10

10 : PWM2/CAP2

11 : ADC_IN5

12.4.31 PC_11 pad alternate function select register (PC_11_AFR)

Address offset : 0x0ac

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC11AF	
														R/W	

[1:0] PC11AF – PC_11 Pad function selection register.

These bits are written by S/W.

00 : RXD2

01 : GPIOC_11

10 : PWM3/CAP3

11 : ADC_IN4

12.4.32 PC_12 pad alternate function select register (PC_12_AFR)

Address offset : 0x0b0

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC12AF	
														R/W	

[1:0] PC12AF – PC_12 Pad function selection register.

These bits are written by S/W.

00 : ADC_IN3

01 : GPIOC_12

10 : SSEL0

11 : ADC_IN3

12.4.33 PC_13 pad alternate function select register (PC_13_AFR)

Address offset : 0x0b4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC13AF	
														R/W	

[1:0] PC13AF – PC_13 Pad function selection register.

These bits are written by S/W.

00 : ADC_IN2

01 : GPIOC_13

10 : SCLK0

11 : ADC_IN2

12.4.34 PC_14 pad alternate function select register (PC_14_AFR)

Address offset : 0x0b8

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC14AF	
														R/W	

[1:0] PC14AF – PC_14 Pad function selection register.

These bits are written by S/W.

00 : ADC_IN1

01 : GPIOC_14

10 : MISO0

11 : ADC_IN1

12.4.35 PC_15 pad alternate function select register (PC_15_AFR)

Address offset : 0x0bc

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC15AF	
														R/W	

[1:0] PC15AF – PC_15 Pad function selection register.

These bits are written by S/W.

00 : ADC_IN0

01 : GPIOC_15

10 : MOSI0

11 : ADC_IN0

12.5 Register map

The following Table 11 summarizes the AFC registers.

Table 11 AFC register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	PA_00_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA00AF	
	reset value																															0	0
0x004	PA_01_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA01AF	
	reset value																															0	0
0x008	PA_02_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA02AF	
	reset value																															0	0
0x00C	PA_03_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA03AF	
	reset value																															0	0
0x010	PA_04_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA04AF	
	reset value																															0	0
0x014	PA_05_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA05AF	
	reset value																															0	0
0x018	PA_06_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA06AF	
	reset value																															0	0
0x01C	PA_07_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA07AF	
	reset value																															0	0
0x020	PA_08_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA08AF	
	reset value																															0	0
0x024	PA_09_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA09AF	
	reset value																															0	0
0x028	PA_10_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA10AF	
	reset value																															0	0
0x02C	PA_11_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA11AF	
	reset value																															0	0
0x030	PA_12_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA12AF	
	reset value																															0	0
0x034	PA_13_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA13AF	
	reset value																															0	0
0x038	PA_14_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA14AF	
	reset value																															0	0
0x040	PB_00_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB00AF	
	reset value																															0	0
0x044	PB_01_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB01AF	
	reset value																															0	0

0x048	PB_02_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB02AF	
	reset value																															0	0
0x04C	PB_03_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB03AF	
	reset value																															0	0
0x058	PB_06_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB06AF	
	reset value																															0	0
0x080	PC_00_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC00AF	
	reset value																															0	0
0x084	PC_01_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC01AF	
	reset value																															0	0
0x088	PC_02_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC02AF	
	reset value																															0	0
0x08C	PC_03_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC03AF	
	reset value																															0	0
0x090	PC_04_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC04AF	
	reset value																															0	0
0x094	PC_05_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC05AF	
	reset value																															0	0
0x098	PC_06_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC06AF	
	reset value																															0	0
0x0A0	PC_08_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC08AF	
	reset value																															0	0
0x0A4	PC_09_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC09AF	
	reset value																															0	0
0x0A8	PC_10_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC10AF	
	reset value																															0	0
0x0AC	PC_11_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC11AF	
	reset value																															0	0
0x0B0	PC_12_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC12AF	
	reset value																															0	0
0x0B4	PC_13_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC13AF	
	reset value																															0	0
0x0B8	PC_14_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC14AF	
	reset value																															0	0
0x0BC	PC_15_AFR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC15AF	
	reset value																															0	0

13 External Interrupt (EXTI)

13.1 Introduction

Each functional pads are connected to the external interrupt(EXTINT) source.

13.2 Features

- All functional pads can be used as an external interrupt source regardless of any set of pad function.
- External Interrupt controller has the following functions and can be controlled by registers.
    - Interrupt mask (enable or disable, default : disable)
    - Interrupt polarity (rising or falling, default : rising)

13.3 Functional description

All pads are connected to the control register individually. (External interrupt mask register and External Interrupt polarity register)

External interrupt working as following expression:

- Each pad interrupt = Interrupt mask & (Interrupt polarity ^ Pad input)
- EXTINT = any Each pad interrupt

Figure 13 shows the External Interrupt diagram.

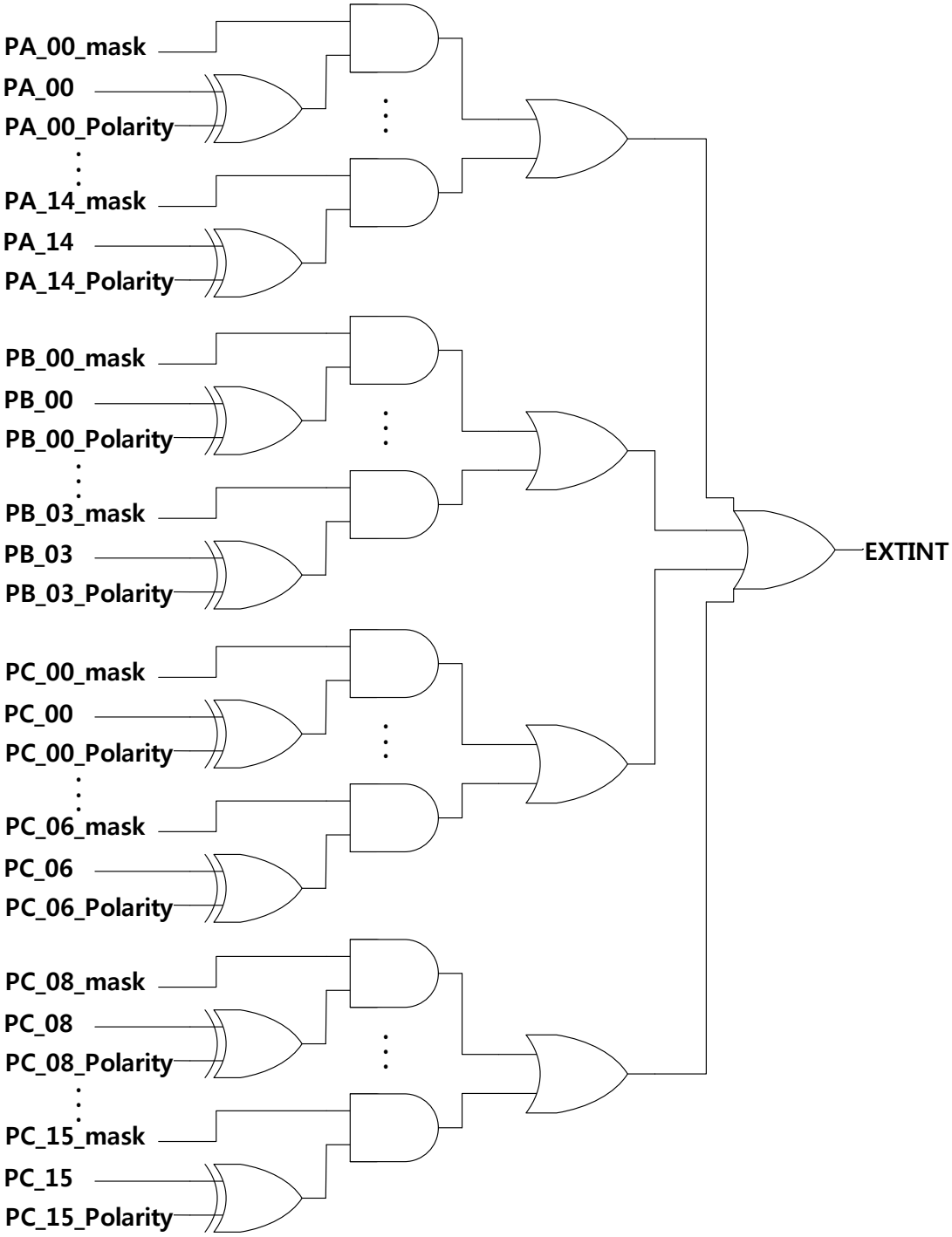


Figure 13. External Interrupt diagram

13.4 Registers (Base address : 0x4100_2000)

13.4.1 PA_00 external interrupt enable register (PA_00_EXTINT)

Address offset : 0x200

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA00IEN	PA00POL
														R/W	R/W

[0] PA00POL – External interrupt polarity selection register of PA_00 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA00IEN – External interrupt enable register of PA_00 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.2 PA_01 external interrupt enable register (PA_01_EXTINT)

Address offset : 0x204

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA01IEN	PA01POL
														R/W	R/W

[0] PA01POL - External interrupt polarity selection register of PA_01 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA01IEN – External interrupt enable register of PA_01 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.3 PA_02 external interrupt enable register (PA_02_EXTINT)

Address offset : 0x208

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA02IEN	PA02POL
														R/W	R/W

[0] PA02POL - External interrupt polarity selection register of PA_02 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA02IEN – External interrupt enable register of PA_02 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.4 PA_03 external interrupt enable register (PA_03_EXTINT)

Address offset : 0x20c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA03IEN	PA03POL
														R/W	R/W

[0] PA03POL - External interrupt polarity selection register of PA_03 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA03IEN – External interrupt enable register of PA_03 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.5 PA_04 external interrupt enable register (PA_04_EXTINT)

Address offset : 0x210

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA04IEN	PA04POL
														R/W	R/W

[0] PA04POL - External interrupt polarity selection register of PA_04 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA04IEN – External interrupt enable register of PA_04 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.6 PA_05 external interrupt enable register (PA_05_EXTINT)

Address offset : 0x214

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA05IEN	PA05POL
														R/W	R/W

[0] PA05POL - External interrupt polarity selection register of PA_05 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA05IEN – External interrupt enable register of PA_05 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.7 PA_06 external interrupt enable register (PA_06_EXTINT)

Address offset : 0x218

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA06IEN	PA06POL
														R/W	R/W

[0] PA06POL - External interrupt polarity selection register of PA_06 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA06IEN – External interrupt enable register of PA_06 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.8 PA_07 external interrupt enable register (PA_07_EXTINT)

Address offset : 0x21c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA07IEN	PA07POL
														R/W	R/W

[0] PA07POL - External interrupt polarity selection register of PA_07 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA07IEN – External interrupt enable register of PA_07 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.9 PA_08 external interrupt enable register (PA_08_EXTINT)

Address offset : 0x220

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA08IEN	PA08POL
														R/W	R/W

[0] PA08POL - External interrupt polarity selection register of PA_08 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA08IEN – External interrupt enable register of PA_08 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.10 PA_09 external interrupt enable register (PA_09_EXTINT)

Address offset : 0x224

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA09IEN	PA09POL
														R/W	R/W

[0] PA09POL - External interrupt polarity selection register of PA_09 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA09IEN – External interrupt enable register of PA_09 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.11 PA_10 external interrupt enable register (PA_10_EXTINT)

Address offset : 0x228

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA10IEN	PA10POL
														R/W	R/W

[0] PA10POL - External interrupt polarity selection register of PA_10 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA10IEN – External interrupt enable register of PA_10 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.12 PA_11 external interrupt enable register (PA_11_EXTINT)

Address offset : 0x22c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA11IEN	PA11POL
														R/W	R/W

[0] PA11POL - External interrupt polarity selection register of PA_11 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA11IEN – External interrupt enable register of PA_11 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.13 PA_12 external interrupt enable register (PA_12_EXTINT)

Address offset : 0x230

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA12IEN	PA12POL
														R/W	R/W

[0] PA12POL - External interrupt polarity selection register of PA_12 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA12IEN – External interrupt enable register of PA_12 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.14 PA_13 external interrupt enable register (PA_13_EXTINT)

Address offset : 0x234

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA13IEN	PA13POL
														R/W	R/W

[0] PA13POL - External interrupt polarity selection register of PA_13 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA13IEN – External interrupt enable register of PA_13 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.15 PA_14 external interrupt enable register (PA_14_EXTINT)

Address offset : 0x238

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PA14TIEN	PA14POL
														R/W	R/W

[0] PA14POL - External interrupt polarity selection register of PA_14 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PA14IEN – External interrupt enable register of PA_14 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.16 PB_00 external interrupt enable register (PB_00_EXTINT)

Address offset : 0x240

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PB00IEN	PB00POL
														R/W	R/W

[0] PB00POL - External interrupt polarity selection register of PB_00 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PB00IEN – External interrupt enable register of PB_00 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.17 PB_01 external interrupt enable register (PB_01_EXTINT)

Address offset : 0x244

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PB01IEN	PB01POL
														R/W	R/W

[0] PB01POL - External interrupt polarity selection register of PB_01 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PB01IEN – External interrupt enable register of PB_01 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.18 PB_02 external interrupt enable register (PB_02_EXTINT)

Address offset : 0x248

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PB02IEN	PB02POL
														R/W	R/W

[0] PB02POL - External interrupt polarity selection register of PB_02 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PB02IEN – External interrupt enable register of PB_02 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.19 PB_03 external interrupt enable register (PB_03_EXTINT)

Address offset : 0x24c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PB03IEN	PB03POL
														R/W	R/W

[0] PB03POL - External interrupt polarity selection register of PB_03 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PB03IEN – External interrupt enable register of PB_03 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.20 PC_00 external interrupt enable register (PC_00_EXTINT)

Address offset : 0x280

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC00IEN	PC00POL
														R/W	R/W

[0] PC00POL - External interrupt polarity selection register of PC_00 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC00IEN – External interrupt enable register of PC_00 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.21 PC_01 external interrupt enable register (PC_01_EXTINT)

Address offset : 0x284

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC01IEN	PC01POL

														R/W	R/W

[0] PC01POL - External interrupt polarity selection register of PC_01 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC01IEN – External interrupt enable register of PC_01 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.22 PC_02 external interrupt enable register (PC_02_EXTINT)

Address offset : 0x288

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC02IEN	PC02POL
														R/W	R/W

[0] PC02POL - External interrupt polarity selection register of PC_02 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC02IEN – External interrupt enable register of PC_02 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.23 PC_03 external interrupt enable register (PC_03_EXTINT)

Address offset : 0x28c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC03IEN	PC03POL
														R/W	R/W

[0] PC03POL - External interrupt polarity selection register of PC_03 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC03IEN – External interrupt enable register of PC_03 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.24 PC_04 external interrupt enable register (PC_04_EXTINT)

Address offset : 0x290

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC04IEN	PC04POL
														R/W	R/W

[0] PC04POL - External interrupt polarity selection register of PC_04 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC04IEN – External interrupt enable register of PC_04 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.25 PC_05 external interrupt enable register (PC_05_EXTINT)

Address offset : 0x294

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC05IEN	PC05POL
														R/W	R/W

[0] PC05POL - External interrupt polarity selection register of PC_05 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC05IEN – External interrupt enable register of PC_05 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.26 PC_06 external interrupt enable register (PC_06_EXTINT)

Address offset : 0x298

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC06IEN	PC06POL
														R/W	R/W

[0] PC06POL - External interrupt polarity selection register of PC_06 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC06IEN – External interrupt enable register of PC_06 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.27 PC_08 external interrupt enable register (PC_08_EXTINT)

Address offset : 0x2a0

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC08IEN	PC08POL
														R/W	R/W

[0] PC08POL - External interrupt polarity selection register of PC_08 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC08IEN – External interrupt enable register of PC_08 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.28 PC_09 external interrupt enable register (PC_09_EXTINT)

Address offset : 0x2a4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC09IEN	PC09POL
														R/W	R/W

[0] PC09POL - External interrupt polarity selection register of PC_09 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC09IEN – External interrupt enable register of PC_09 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.29 PC_10 external interrupt enable register (PC_10_EXTINT)

Address offset : 0x2a8

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC10IEN	PC10POL
														R/W	R/W

[0] PC10POL - External interrupt polarity selection register of PC_10 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC10IEN – External interrupt enable register of PC_10 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.30 PC_11 external interrupt enable register (PC_11_EXTINT)

Address offset : 0x2ac

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC11IEN	PC11POL
														R/W	R/W

[0] PC11POL - External interrupt polarity selection register of PC_11 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC11IEN – External interrupt enable register of PC_11 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.31 PC_12 external interrupt enable register (PC_12_EXTINT)

Address offset : 0x2b0

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC12IEN	PC12POL
														R/W	R/W

[0] PC12POL - External interrupt polarity selection register of PC_12 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC12IEN – External interrupt enable register of PC_12 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.32 PC_13 external interrupt enable register (PC_13_EXTINT)

Address offset : 0x2b4

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC13IEN	PC13POL
														R/W	R/W

[0] PC13POL - External interrupt polarity selection register of PC_13 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC13IEN – External interrupt enable register of PC_13 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.33 PC_14 external interrupt enable register (PC_14_EXTINT)

Address offset : 0x2b8

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC14IEN	PC14POL
														R/W	R/W

[0] PC14POL - External interrupt polarity selection register of PC_14 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC14IEN – External interrupt enable register of PC_14 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.4.34 PC_15 external interrupt enable register (PC_15_EXTINT)

Address offset : 0x2bc

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	Res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

res	res	res	res	res	res	res	res	res	res	res	Res	res	res	PC15IEN	PC15POL
														R/W	R/W

[0] PC15POL - External interrupt polarity selection register of PC_15 PAD

These bits are written by S/W.

0 : interrupt occurs when pad detect HIGH level signal

1 : interrupt occurs when pad detect LOW level signal

[1] PC15IEN – External interrupt enable register of PC_15 PAD

These bits are written by S/W.

0 : external interrupt disable

1 : external interrupt enable

13.5 Register map

The following Table 12 summarizes the EXTINT registers.

Table 12 EXTINT register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x200	PA_00_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA00IEN	PA00POL
	reset value																															0	0
0x204	PA_01_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA01IEN	PA01POL
	reset value																															0	0
0x208	PA_02_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA02IEN	PA02POL
	reset value																															0	0
0x20C	PA_03_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA03IEN	PA03POL
	reset value																															0	0
0x210	PA_04_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA04IEN	PA04POL
	reset value																															0	0
0x214	PA_05_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA05IEN	PA05POL
	reset value																															0	0
0x218	PA_06_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA06IEN	PA06POL
	reset value																															0	0
0x21C	PA_07_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA07IEN	PA07POL
	reset value																															0	0
0x220	PA_08_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA08IEN	PA08POL
	reset value																															0	0
0x224	PA_09_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA09IEN	PA09POL
	reset value																															0	0
0x228	PA_10_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA10IEN	PA10POL
	reset value																															0	0
0x22C	PA_11_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA11IEN	PA11POL
	reset value																															0	0
0x230	PA_12_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA12IEN	PA12POL
	reset value																															0	0
0x234	PA_13_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA13IEN	PA13POL
	reset value																															0	0
0x238	PA_14_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA14IEN	PA14POL
	reset value																															0	0
0x240	PB_00_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB00IEN	PB00POL
	reset value																															0	0

0x244	PB_01_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB01IEN	PB01POL
	reset value																															0	0
0x248	PB_02_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB02IEN	PB02POL
	reset value																															0	0
0x24C	PB_03_EXTINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB03IEN	PB03POL
	reset value																															0	0
0x280	PC_00_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC00IEN	PC00POL
	reset value																															0	0
0x284	PC_01_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC01IEN	PC01POL
	reset value																															0	0
0x288	PC_02_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC02IEN	PC02POL
	reset value																															0	0
0x28C	PC_03_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC03IEN	PC03POL
	reset value																															0	0
0x290	PC_04_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC04IEN	PC04POL
	reset value																															0	0
0x294	PC_05_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC05IEN	PC05POL
	reset value																															0	0
0x298	PC_06_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC06IEN	PC06POL
	reset value																															0	0
0x2A0	PC_08_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC08IEN	PC08POL
	reset value																															0	0
0x2A4	PC_09_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC09IEN	PC09POL
	reset value																															0	0
0x2A8	PC_10_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC10IEN	PC10POL
	reset value																															0	0
0x2AC	PC_11_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC11IEN	PC11POL
	reset value																															0	0
0x2B0	PC_12_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC12IEN	PC12POL
	reset value																															0	0
0x2B4	PC_13_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC13IEN	PC13POL
	reset value																															0	0
0x2B8	PC_14_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC14IEN	PC14POL
	reset value																															0	0
0x2BC	PC_15_EXINT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC15IEN	PC15POL
	reset value																															0	0

14 Pad Controller (PADCON)

14.1 Introduction

Pads of W7500P are controllable. User can control pad's characteristic.

14.2 Features

- W7500P has digital I/O pads and digital/analog mux I/O pads
- Controllable characteristics of pads are pull-up, pull-down, driving strength, input enable, and CMOS/Schmitt trigger input buffer
- Each pad can be controlled individually by register.

14.3 Functional description

Figure 14 shows the function schematic of digital I/O pad of W7500P.

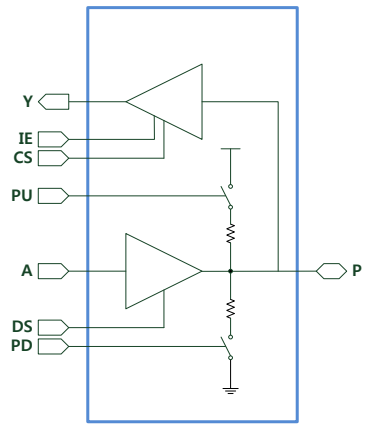


Figure 14. function schematic of digital I/O pad

Figure 15 shows the function schematic of digital/analog mux IO pad of W7500P

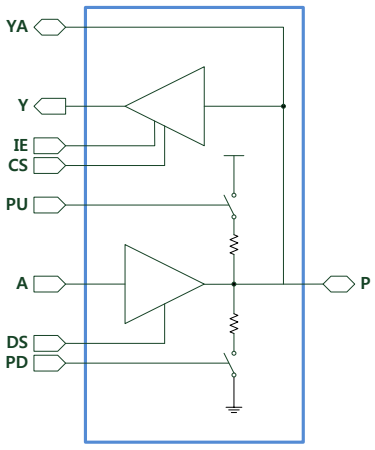


Figure 15. function schematic of digital/analog mux IO pad

Initials of Pad diagram is same as below.

P - PAD

YA – Analog Input (connect to ADC input)

Y – Digital Input

IE – Input buffer enable

Condition		A	Y	P
Input buffer enable (IE = 1)	Output mode	OUT	OUT	OUT
	Input mode	No use	IN	IN
Input buffer disable (IE = 0)	Output mode	OUT	Low (0)	OUT
	Input mode	No use	IN	IN

CS – CMOS/Schmitt trigger input buffer select

PU – Pull-up enable

A – Digital Output

DS – Driving strength select

Condition		Rise/Fall Time (nSec)		Propagation Delay (nSec)	
Driving Strength	Capacitance loading	Min	Max	Min	Max
High (DS = 1)	25pF	4	18	7	27
	100pF	11	53	11	44
Low (DS = 0)	25pF	1	8	4	16
	100pF	4	23	7	24

PD – Pull-down enable

User can set pad condition with IE, CS, PU/PD, DS by register.

And pads are can be controlled individually.

14.4 Registers (Base address : 0x4100_3000)

14.4.1PA_00 pad control register

Address offset : 0x000

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA00_CS	PA00_IE	res	res	PA00_DS	PA00_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA00_PUPD – Pull-up, Pull-down selection register of Pad PA_00

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA00_DS – Driving strength selection register of Pad PA_00

0 : Low driving strength

1 : High driving strength

[5] PA00_IE : Input buffer enable selection register of Pad PA_00

0 : Input buffer disable

1 : Input buffer enable

[6] PA00_CS – CMOS input or Summit trigger input selection register of Pad PA_00

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.2PA_01 pad control register

Address offset : 0x004

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA01_CS	PA01_IE	res	res	PA01_DS	PA01_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA01_PUPD – Pull-up, Pull-down selection register of Pad PA_01

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA01_DS – Driving strength selection register of Pad PA_01

0 : Low driving strength

1 : High driving strength

[5] PA01_IE : Input buffer enable selection register of Pad PA_01

0 : Input buffer disable

1 : Input buffer enable

[6] PA01_CS – CMOS input or Summit trigger input selection register of Pad PA_01

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.3PA_02 pad control register

Address offset : 0x008

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA02_CS	PA02_IE	res	res	PA02_DS	PA02_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA02_PUPD – Pull-up, Pull-down selection register of Pad PA_02

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA02_DS – Driving strength selection register of Pad PA_02

0 : Low driving strength

1 : High driving strength

[5] PA02_IE : Input buffer enable selection register of Pad PA_02

0 : Input buffer disable

1 : Input buffer enable

[6] PA02_CS – CMOS input or Summit trigger input selection register of Pad PA_02

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.4PA_03 pad control register

Address offset : 0x00c

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA03_CS	PA03_IE	res	res	PA03_DS	PA03_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA03_PUPD – Pull-up, Pull-down selection register of Pad PA_03

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA03_DS – Driving strength selection register of Pad PA_03

0 : Low driving strength

1 : High driving strength

[5] PA03_IE : Input buffer enable selection register of Pad PA_03

0 : Input buffer disable

1 : Input buffer enable

[6] PA03_CS – CMOS input or Summit trigger input selection register of Pad PA_03

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.5PA_04 pad control register

Address offset : 0x010

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA04_CS	PA04_IE	res	res	PA04_DS	PA04_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA04_PUPD – Pull-up, Pull-down selection register of Pad PA_04

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA04_DS – Driving strength selection register of Pad PA_04

0 : Low driving strength

1 : High driving strength

[5] PA04_IE : Input buffer enable selection register of Pad PA_04

0 : Input buffer disable

1 : Input buffer enable

[6] PA04_CS – CMOS input or Summit trigger input selection register of Pad PA_04

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.6PA_05 pad control register

Address offset : 0x014

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA05_CS	PA05_IE	res	res	PA05_DS	PA05_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA05_PUPD – Pull-up, Pull-down selection register of Pad PA_05

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA05_DS – Driving strength selection register of Pad PA_05

0 : Low driving strength

1 : High driving strength

[5] PA05_IE : Input buffer enable selection register of Pad PA_05

0 : Input buffer disable

1 : Input buffer enable

[6] PA05_CS – CMOS input or Summit trigger input selection register of Pad PA_05

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.7PA_06 pad control register

Address offset : 0x018

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA06_CS	PA06_IE	res	res	PA06_DS	PA06_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA06_PUPD – Pull-up, Pull-down selection register of Pad PA_06

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA06_DS – Driving strength selection register of Pad PA_06

0 : Low driving strength

1 : High driving strength

[5] PA06_IE : Input buffer enable selection register of Pad PA_06

0 : Input buffer disable

1 : Input buffer enable

[6] PA06_CS – CMOS input or Summit trigger input selection register of Pad PA_06

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.8PA_07 pad control register

Address offset : 0x01c

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA07_CS	PA07_IE	res	res	PA07_DS	PA07_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA07_PUPD – Pull-up, Pull-down selection register of Pad PA_07

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA07_DS – Driving strength selection register of Pad PA_07

0 : Low driving strength

1 : High driving strength

[5] PA07_IE : Input buffer enable selection register of Pad PA_07

0 : Input buffer disable

1 : Input buffer enable

[6] PA07_CS – CMOS input or Summit trigger input selection register of Pad PA_07

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.9PA_08 pad control register

Address offset : 0x020

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA08_CS	PA08_IE	res	res	PA08_DS	PA08_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA08_PUPD – Pull-up, Pull-down selection register of Pad PA_08

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA08_DS – Driving strength selection register of Pad PA_08

0 : Low driving strength

1 : High driving strength

[5] PA08_IE : Input buffer enable selection register of Pad PA_08

0 : Input buffer disable

1 : Input buffer enable

[6] PA08_CS – CMOS input or Summit trigger input selection register of Pad PA_08

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.10 PA_09 pad control register

Address offset : 0x024

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA09_CS	PA09_IE	res	res	PA09_DS	PA09_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA09_PUPD – Pull-up, Pull-down selection register of Pad PA_09

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA09_DS – Driving strength selection register of Pad PA_09

0 : Low driving strength

1 : High driving strength

[5] PA09_IE : Input buffer enable selection register of Pad PA_09

0 : Input buffer disable

1 : Input buffer enable

[6] PA09_CS – CMOS input or Summit trigger input selection register of Pad PA_09

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.11 PA_10 pad control register

Address offset : 0x028

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA10_CS	PA10_IE	res	res	PA10_DS	PA10_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA10_PUPD – Pull-up, Pull-down selection register of Pad PA_10

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA10_DS – Driving strength selection register of Pad PA_10

0 : Low driving strength

1 : High driving strength

[5] PA10_IE : Input buffer enable selection register of Pad PA_10

0 : Input buffer disable

1 : Input buffer enable

[6] PA10_CS – CMOS input or Summit trigger input selection register of Pad PA_10

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.12 PA_11 pad control register

Address offset : 0x02c

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA11_CS	PA11_IE	res	res	PA11_DS	PA11_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA11_PUPD – Pull-up, Pull-down selection register of Pad PA_11

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA11_DS – Driving strength selection register of Pad PA_11

0 : Low driving strength

1 : High driving strength

[5] PA11_IE : Input buffer enable selection register of Pad PA_11

0 : Input buffer disable

1 : Input buffer enable

[6] PA11_CS – CMOS input or Summit trigger input selection register of Pad PA_11

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.13 PA_12 pad control register

Address offset : 0x030

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA12_CS	PA12_IE	res	res	PA12_DS	PA12_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA12_PUPD – Pull-up, Pull-down selection register of Pad PA_12

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA12_DS – Driving strength selection register of Pad PA_12

0 : Low driving strength

1 : High driving strength

[5] PA12_IE : Input buffer enable selection register of Pad PA_12

0 : Input buffer disable

1 : Input buffer enable

[6] PA12_CS – CMOS input or Summit trigger input selection register of Pad PA_12

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.14 PA_13 pad control register

Address offset : 0x034

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA13_CS	PA13_IE	res	res	PA13_DS	PA13_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA13_PUPD – Pull-up, Pull-down selection register of Pad PA_13

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA13_DS – Driving strength selection register of Pad PA_13

0 : Low driving strength

1 : High driving strength

[5] PA13_IE : Input buffer enable selection register of Pad PA_13

0 : Input buffer disable

1 : Input buffer enable

[6] PA13_CS – CMOS input or Summit trigger input selection register of Pad PA_13

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.15 PA_14 pad control register

Address offset : 0x038

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PA14_CS	PA14_IE	res	res	PA14_DS	PA14_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PA14_PUPD – Pull-up, Pull-down selection register of Pad PA_14

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PA14_DS – Driving strength selection register of Pad PA_14

0 : Low driving strength

1 : High driving strength

[5] PA14_IE : Input buffer enable selection register of Pad PA_14

0 : Input buffer disable

1 : Input buffer enable

[6] PA14_CS – CMOS input or Summit trigger input selection register of Pad PA_14

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.16 PB_00 pad control register

Address offset : 0x040

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PB00_CS	PB00_IE	res	res	PB00_DS	PB00_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PB00_PUPD – Pull-up, Pull-down selection register of Pad PB_00

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PB00_DS – Driving strength selection register of Pad PB_00

0 : Low driving strength

1 : High driving strength

[5] PB00_IE : Input buffer enable selection register of Pad PB_00

0 : Input buffer disable

1 : Input buffer enable

[6] PB00_CS – CMOS input or Summit trigger input selection register of Pad PB_00

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.17 PB_01 pad control register

Address offset : 0x044

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PB01_CS	PB01_IE	res	res	PB01_DS	PB01_PUPD	

									R/W	R/W			R/W	R/W

[1:0] PB01_PUPD – Pull-up, Pull-down selection register of Pad PB_01

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PB01_DS – Driving strength selection register of Pad PB_01

0 : Low driving strength

1 : High driving strength

[5] PB01_IE : Input buffer enable selection register of Pad PB_01

0 : Input buffer disable

1 : Input buffer enable

[6] PB01_CS – CMOS input or Summit trigger input selection register of Pad PB_01

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.18 PB_02 pad control register

Address offset : 0x048

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PB02_CS	PB02_IE	res	res	PB02_DS	PB02_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PB02_PUPD – Pull-up, Pull-down selection register of Pad PB_02

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PB02_DS – Driving strength selection register of Pad PB_02

0 : Low driving strength

1 : High driving strength

[5] PB02_IE : Input buffer enable selection register of Pad PB_02

0 : Input buffer disable

1 : Input buffer enable

[6] PB02_CS – CMOS input or Summit trigger input selection register of Pad PB_02

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.19 PB_03 pad control register

Address offset : 0x04c

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PB03_CS	PB03_IE	res	res	PB03_DS	PB03_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PB03_PUPD – Pull-up, Pull-down selection register of Pad PB_03

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PB03_DS – Driving strength selection register of Pad PB_03

0 : Low driving strength

1 : High driving strength

[5] PB03_IE : Input buffer enable selection register of Pad PB_03

0 : Input buffer disable

1 : Input buffer enable

[6] PB03_CS – CMOS input or Summit trigger input selection register of Pad PB_03

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.20 PB_06 pad control register

Address offset : 0x058

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PB06_CS	PB06_IE	res	res	PB06_DS	PB06_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PB06_PUPD – Pull-up, Pull-down selection register of Pad PB_06

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PB06_DS – Driving strength selection register of Pad PB_06

0 : Low driving strength

1 : High driving strength

[5] PB06_IE : Input buffer enable selection register of Pad PB_06

0 : Input buffer disable

1 : Input buffer enable

[6] PB06_CS – CMOS input or Summit trigger input selection register of Pad PB_06

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.21 PC_00 pad control register

Address offset : 0x080

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC00_CS	PC00_IE	res	res	PC00_DS	PC00_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC00_PUPD – Pull-up, Pull-down selection register of Pad PC_00

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC00_DS – Driving strength selection register of Pad PC_00

0 : Low driving strength

1 : High driving strength

[5] PC00_IE : Input buffer enable selection register of Pad PC_00

0 : Input buffer disable

1 : Input buffer enable

[6] PC00_CS – CMOS input or Summit trigger input selection register of Pad PC_00

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.22 PC_01 pad control register

Address offset : 0x084

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC01_CS	PC01_IE	res	res	PC01_DS	PC01_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC01_PUPD – Pull-up, Pull-down selection register of Pad PC_01

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC01_DS – Driving strength selection register of Pad PC_01

0 : Low driving strength

1 : High driving strength

[5] PC01_IE : Input buffer enable selection register of Pad PC_01

0 : Input buffer disable

1 : Input buffer enable

[6] PC01_CS – CMOS input or Summit trigger input selection register of Pad PC_01

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.23 PC_02 pad control register

Address offset : 0x088

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC02_CS	PC02_IE	res	res	PC02_DS	PC02_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC02_PUPD – Pull-up, Pull-down selection register of Pad PC_02

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC02_DS – Driving strength selection register of Pad PC_02

0 : Low driving strength

1 : High driving strength

[5] PC02_IE : Input buffer enable selection register of Pad PC_02

0 : Input buffer disable

1 : Input buffer enable

[6] PC02_CS – CMOS input or Summit trigger input selection register of Pad PC_02

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.24 PC_03 pad control register

Address offset : 0x08C

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC03_CS	PC03_IE	res	res	PC03_DS	PC03_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC03_PUPD – Pull-up, Pull-down selection register of Pad PC_03

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC03_DS – Driving strength selection register of Pad PC_03

0 : Low driving strength

1 : High driving strength

[5] PC03_IE : Input buffer enable selection register of Pad PC_03

0 : Input buffer disable

1 : Input buffer enable

[6] PC03_CS – CMOS input or Summit trigger input selection register of Pad PC_03

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.25 PC_04 pad control register

Address offset : 0x090

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC04_CS	PC04_IE	res	res	PC04_DS	PC04_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC04_PUPD – Pull-up, Pull-down selection register of Pad PC_04

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC04_DS – Driving strength selection register of Pad PC_04

0 : Low driving strength

1 : High driving strength

[5] PC04_IE : Input buffer enable selection register of Pad PC_04

0 : Input buffer disable

1 : Input buffer enable

[6] PC04_CS – CMOS input or Summit trigger input selection register of Pad PC_04

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.26 PC_05 pad control register

Address offset : 0x094

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC05_CS	PC05_IE	res	res	PC05_DS	PC05_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC05_PUPD – Pull-up, Pull-down selection register of Pad PC_05

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC05_DS – Driving strength selection register of Pad PC_05

0 : Low driving strength

1 : High driving strength

[5] PC05_IE : Input buffer enable selection register of Pad PC_05

0 : Input buffer disable

1 : Input buffer enable

[6] PC05_CS – CMOS input or Summit trigger input selection register of Pad PC_05

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.27 PC_06 pad control register

Address offset : 0x098

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC06_CS	PC06_IE	res	res	PC06_DS	PC06_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC06_PUPD – Pull-up, Pull-down selection register of Pad PC_06

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC06_DS – Driving strength selection register of Pad PC_06

0 : Low driving strength

1 : High driving strength

[5] PC06_IE : Input buffer enable selection register of Pad PC_06

0 : Input buffer disable

1 : Input buffer enable

[6] PC06_CS – CMOS input or Summit trigger input selection register of Pad PC_06

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.28 PC_08 pad control register

Address offset : 0x0A0

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC08_CS	PC08_IE	res	res	PC08_DS	PC08_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC08_PUPD – Pull-up, Pull-down selection register of Pad PC_08

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC08_DS – Driving strength selection register of Pad PC_08

0 : Low driving strength

1 : High driving strength

[5] PC08_IE : Input buffer enable selection register of Pad PC_08

0 : Input buffer disable

1 : Input buffer enable

[6] PC08_CS – CMOS input or Summit trigger input selection register of Pad PC_08

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.29 PC_09 pad control register

Address offset : 0x0A4

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC09_CS	PC09_IE	res	res	PC09_DS	PC09_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC09_PUPD – Pull-up, Pull-down selection register of Pad PC_09

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC09_DS – Driving strength selection register of Pad PC_09

0 : Low driving strength

1 : High driving strength

[5] PC09_IE : Input buffer enable selection register of Pad PC_09

0 : Input buffer disable

1 : Input buffer enable

[6] PC09_CS – CMOS input or Summit trigger input selection register of Pad PC_09

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.30 PC_10 pad control register

Address offset : 0x0A8

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC10_CS	PC10_IE	res	res	PC10_DS	PC10_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC10_PUPD – Pull-up, Pull-down selection register of Pad PC_10

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC10_DS – Driving strength selection register of Pad PC_10

0 : Low driving strength

1 : High driving strength

[5] PC10_IE : Input buffer enable selection register of Pad PC_10

0 : Input buffer disable

1 : Input buffer enable

[6] PC10_CS – CMOS input or Summit trigger input selection register of Pad PC_10

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.31 PC_11 pad control register

Address offset : 0x0AC

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC11_CS	PC11_IE	res	res	PC11_DS	PC11_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC11_PUPD – Pull-up, Pull-down selection register of Pad PC_11

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC11_DS – Driving strength selection register of Pad PC_11

0 : Low driving strength

1 : High driving strength

[5] PC11_IE : Input buffer enable selection register of Pad PC_11

0 : Input buffer disable

1 : Input buffer enable

[6] PC11_CS – CMOS input or Summit trigger input selection register of Pad PC_11

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.32 PC_12 pad control register

Address offset : 0x0B0

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC12_CS	PC12_IE	res	res	PC12_DS	PC12_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC12_PUPD – Pull-up, Pull-down selection register of Pad PC_12

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC12_DS – Driving strength selection register of Pad PC_12

0 : Low driving strength

1 : High driving strength

[5] PC12_IE : Input buffer enable selection register of Pad PC_12

0 : Input buffer disable

1 : Input buffer enable

[6] PC12_CS – CMOS input or Summit trigger input selection register of Pad PC_12

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.33 PC_13 pad control register

Address offset : 0x0B4

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC13_CS	PC13_IE	res	res	PC13_DS	PC13_PUPD	

									R/W	R/W			R/W	R/W

[1:0] PC13_PUPD – Pull-up, Pull-down selection register of Pad PC_13

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC13_DS – Driving strength selection register of Pad PC_13

0 : Low driving strength

1 : High driving strength

[5] PC13_IE : Input buffer enable selection register of Pad PC_13

0 : Input buffer disable

1 : Input buffer enable

[6] PC13_CS – CMOS input or Summit trigger input selection register of Pad PC_13

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.34 PC_14 pad control register

Address offset : 0x0B8

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC14_CS	PC14_IE	res	res	PC14_DS	PC14_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC14_PUPD – Pull-up, Pull-down selection register of Pad PC_14

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC14_DS – Driving strength selection register of Pad PC_14

0 : Low driving strength

1 : High driving strength

[5] PC14_IE : Input buffer enable selection register of Pad PC_14

0 : Input buffer disable

1 : Input buffer enable

[6] PC14_CS – CMOS input or Summit trigger input selection register of Pad PC_14

0 : CMOS input buffer

1 : Summit trigger input buffer

14.4.35 PC_15 pad control register

Address offset : 0x0BC

Reset value : 0x0000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	PC15_CS	PC15_IE	res	res	PC15_DS	PC15_PUPD	
									R/W	R/W			R/W	R/W	

[1:0] PC15_PUPD – Pull-up, Pull-down selection register of Pad PC_15

These bits are written by S/W.

00 : Neither

01 : pull-down

10 : pull-up

11 : Neither

[2] PC15_DS – Driving strength selection register of Pad PC_15

0 : Low driving strength

1 : High driving strength

[5] PC15_IE : Input buffer enable selection register of Pad PC_15

0 : Input buffer disable

1 : Input buffer enable

[6] PC15_CS – CMOS input or Summit trigger input selection register of Pad PC_15

0 : CMOS input buffer

1 : Summit trigger input buffer

14.5 Register map

The following Table 13 summarizes the PAD controller registers.

Table 13 PAD controller register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	PCR_PA00	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA00_CS	PA00_IE	res	res	PA00_DS	PA00_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x004	PCD_PA01	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA01_CS	PA01_IE	res	res	PA01_DS	PA01_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x008	PCD_PA02	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA02_CS	PA02_IE	res	res	PA02_DS	PA02_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x00C	PCR_PA03	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA03_CS	PA03_IE	res	res	PA03_DS	PA03_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x010	PCR_PA04	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA04_CS	PA04_IE	res	res	PA04_DS	PA04_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x014	PCR_PA05	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA05_CS	PA05_IE	res	res	PA05_DS	PA05_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x018	PCR_PA06	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA06_CS	PA06_IE	res	res	PA06_DS	PA06_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x01C	PCR_PA07	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA07_CS	PA07_IE	res	res	PA07_DS	PA07_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x020	PCR_PA08	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA08_CS	PA08_IE	res	res	PA08_DS	PA08_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x024	PCR_PA09	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA09_CS	PA09_IE	res	res	PA09_DS	PA09_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x028	PCR_PA10	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA10_CS	PA10_IE	res	res	PA10_DS	PA10_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x02C	PCR_PA11	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA11_CS	PA11_IE	res	res	PA11_DS	PA11_PUPD	
	reset value																									0	0	0	0	0	0	0	0
0x030	PCR_PA12	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA12_CS	PA12_IE	res	res	PA12_DS	PA12_PUPD	
	reset value																	0	0	0	0	0	0	0	0								

0x034	PCR_PA13	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA13_CS	PA13_IE	res	res	PA13_DS	PA13_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x038	PCR_PA14	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA14_CS	PA14_IE	res	res	PA14_DS	PA14_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x040	PCR_PB00	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB00_CS	PB00_IE	res	res	PB00_DS	PB00_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x044	PCR_PB01	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB01_CS	PB01_IE	res	res	PB01_DS	PB01_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x048	PCR_PB02	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB02_CS	PB02_IE	res	res	PB02_DS	PB02_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04C	PCR_PB03	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PB03_CS	PB03_IE	res	res	PB03_DS	PB03_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x058	PCR_PB06	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PA00_CS	PA00_IE	res	res	PA00_DS	PB06_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x080	PCR_PC00	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC00_CS	PC00_IE	res	res	PC00_DS	PC00_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x084	PCR_PC01	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC01_CS	PC01_IE	res	res	PC01_DS	PC01_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x088	PCR_PC02	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC02_CS	PC02_IE	res	res	PC02_DS	PC02_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08C	PCR_PC03	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC03_CS	PC03_IE	res	res	PC03_DS	PC03_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x090	PCR_PC04	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC04_CS	PC04_IE	res	res	PC04_DS	PC04_PUPD	
	reset value																									0	0	0	0	0	0	0	0
0x094	PCR_PC05	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC05_CS	PC05_IE	res	res	PC05_DS	PC05_PUPD	
	reset value																	0	0	0	0	0	0	0	0								
0x098	PCR_PC06	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC06_CS	PC06_IE	res	res	PC06_DS	PC06_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x0A0	PCR_PC08	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC08_CS	PC08_IE	res	res	PC08_DS	PC08_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0A4	PCR_PC09	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC09_CS	PC09_IE	res	res	PC09_DS	PC09_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0A8	PCR_PC10	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC10_CS	PC10_IE	res	res	PC10_DS	PC10_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0AC	PCR_PC11	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC11_CS	PC11_IE	res	res	PC11_DS	PC11_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0B0	PCR_PC12	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC12_CS	PC12_IE	res	res	PC12_DS	PC12_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0B4	PCR_PC13	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC13_CS	PC13_IE	res	res	PC13_DS	PC13_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0B8	PCR_PC14	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC14_CS	PC14_IE	res	res	PC14_DS	PC14_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xBC	PCR_PC15	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PC15_CS	PC15_IE	res	res	PC15_DS	PC15_PUPD	
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15 General-purpose I/Os(GPIO)

15.1 Introduction

The GPIO(General-Purpose I/O Port) is composed of three physical GPIO blocks, each corresponding to an individual GPIO port(PORT A, PORT B and PORT C). The GPIO supports up to 34 programmable input/output pins, depending on the peripherals being used.

15.2 Features

- The GPIO peripheral consists the following features.
  - GPIO_DATAOUT can SET/CLEAR by the SET register and CLEAR register. (1 for set and 0 for clear)
  - Mask registers allow treating sets of port bits as a group leaving other bits unchanged.
  - Up to 34 GPIOs depending on configuration
  - Programmable control for GPIO interrupts
    - Interrupt generation masking
    - Edge-triggered on rising, falling, or both

15.3 Functional description

Figure 16 shows the GPIO block diagram.

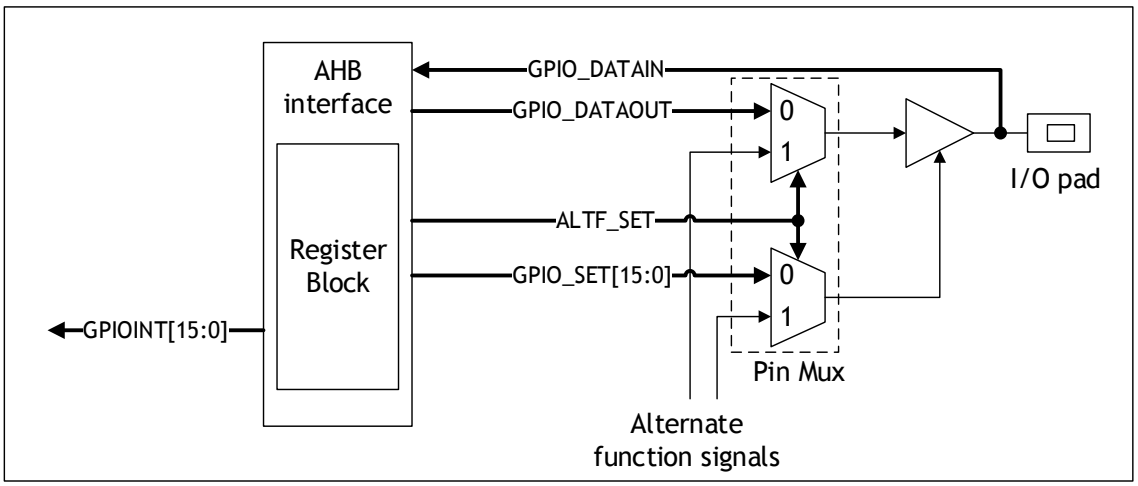


Figure 16. GPIO block diagram

Figure 17 shows the operation sequences available for the GPIO.

The pad alternate function is using the pad alternate function select register.

Refer to '12.Alternate Function Controller (AFC)' for more details about each register.

The pad control supports pull-down, pull-up, input buffer, and summit trigger input buffer. Refer to '14.Pad Controller (PADCON)' for more details about each register.

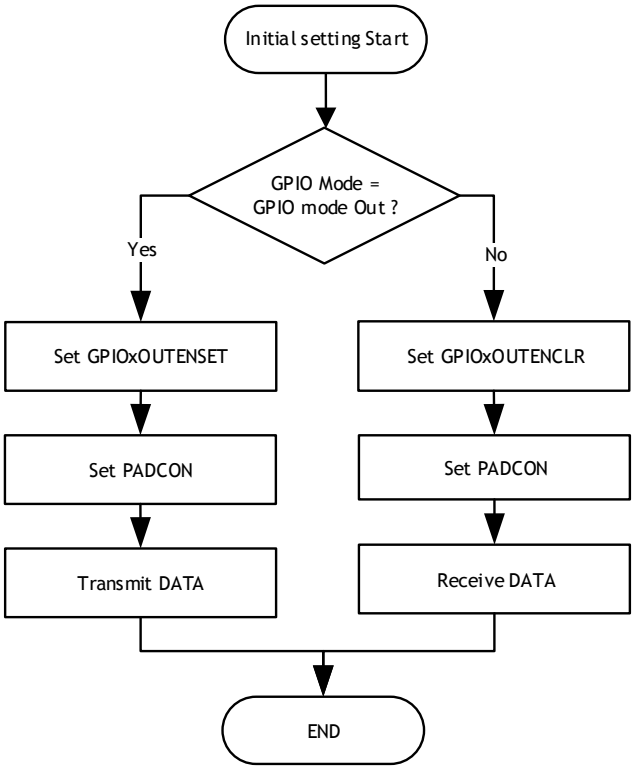


Figure 17. GPIO Flow chart

15.3.1 Masked access

The masked access feature permits individual bits or multiple bits to be read from or written to in a single transfer. This avoids software-based read-modify-write operations that are not thread safe. With the masked access operations, the 16-bit I/O is divided into two halves, lower byte and upper byte. The bit mask address spaces are defined as two arrays each containing 256 words.

For example, to set bits[1:0] to 1 and clear bits[7:6] in a single operation, users can carry out the write to the lower byte mask access address space. The required bit mask is 0xC3, and users can write the operation as MASKLOWBYTE[0xC3] = 0x03. Refer to Figure 18 below.

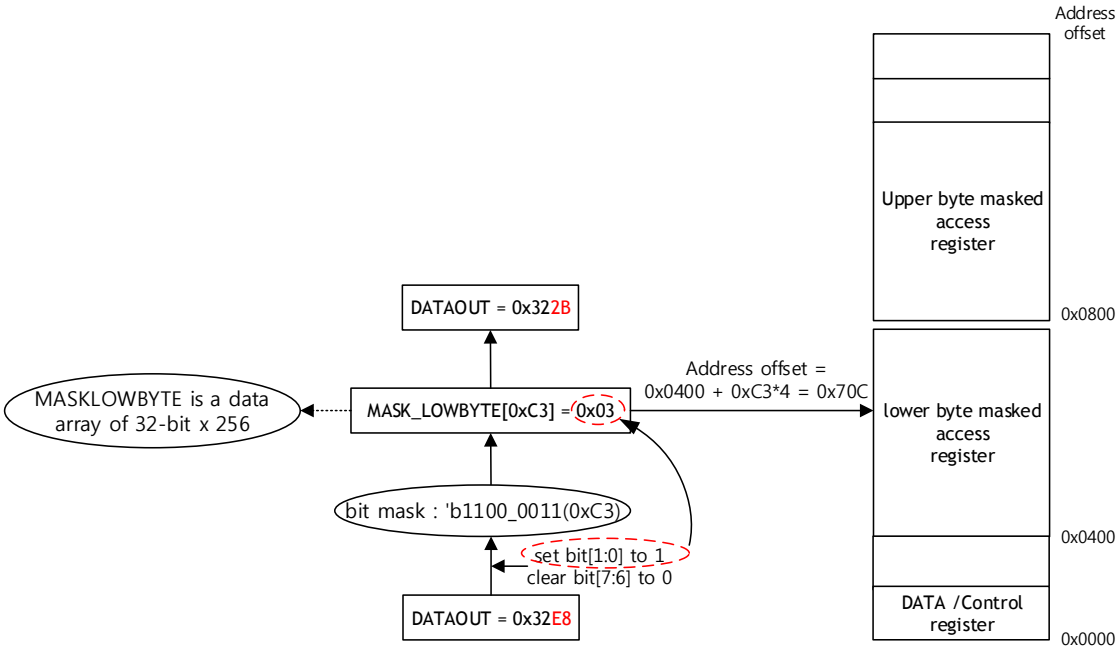


Figure 18. MASK LOWBYTE access

To update some of the bits in the upper eight bits of the GPIO port, users can use the MASKHIGHBYTE array as Figure 19 below.

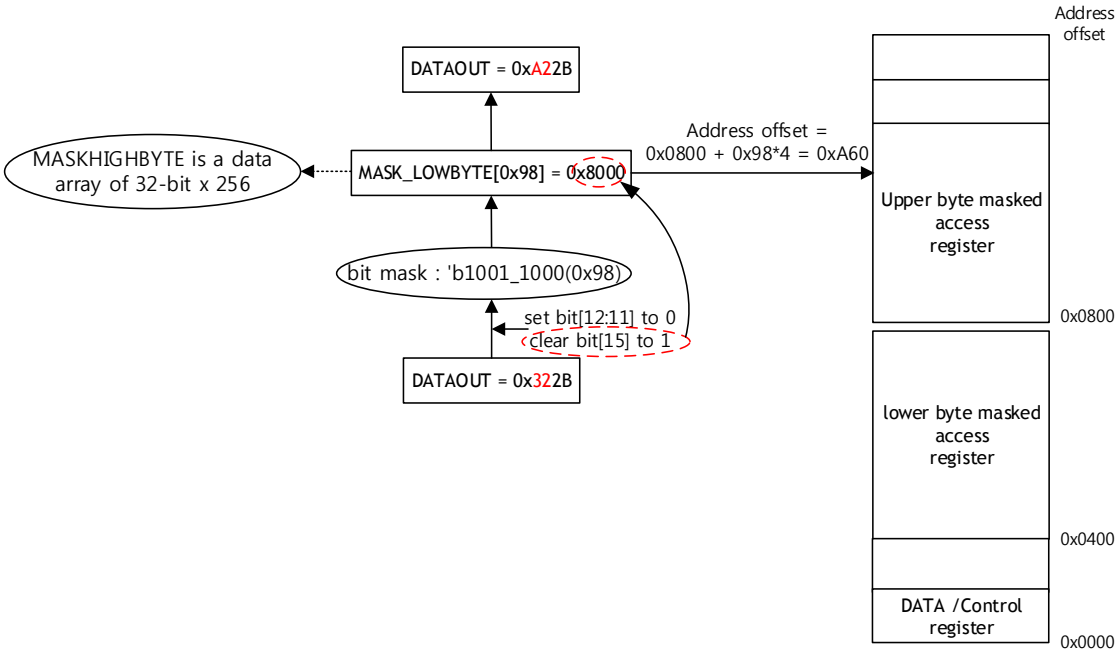


Figure 19 MASK HIGHBYTE access

15.4 GPIOA Registers(Address Base: 0x4200_0000)

15.4.1 GPIOA Data Register(GPIOA_DATA)

Address offset: 0x0000

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	DAT14	DAT13	DAT12	DAT11	DAT10	DAT9	DAT8	DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[14:0] DATy(y = 0..14)

READ as : Port input data bit

15.4.2 GPIOA Output Latch Register(GPIOA_DATAOUT)

Address offset: 0x0004

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	DAO14	DAO13	DAO12	DAO11	DAO10	DAO9	DAO8	DAO7	DAO6	DAO5	DAO4	DAO3	DAO2	DAO1	DAO0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] DAOy(y = 0..14)

READ as : Port out data bit

WRITE as : WRITE to GPIOA_DATAOUT register

15.4.3 GPIOA Enable Set Register(GPIOA_OUTENSET)

Address offset: 0x0010

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	ES14	ES13	ES12	ES11	ES10	ES9	ES8	ES7	ES6	ES5	ES4	ES3	ES2	ES1	ES0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] ESy(y = 0..14)

WRITE as :

'0' is no effect

'1' is sets the corresponding output enable bit

READ as :

'0' is indicates the signal direction as input

'1' is indicates the signal direction as output

15.4.4 GPIOA Enable Clear Register(GPIOA_OUTENCLR)

Address offset: 0x0014

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	EC14	EC13	EC12	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] ECy(y = 0..14)

WRITE as :

'0' is no effect

'1' is clears the output enable bit

READ as :

'0' is indicates the signal direction as input

'1' is indicates the signal direction as output

15.4.5 GPIOA Interrupt Enable Set Register(GPIOA_ INTENSET)

Address offset: 0x0020

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	IES14	IES13	IES12	IES11	IES10	IES9	IES8	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] IESy(y = 0..14)

WRITE as :

‘0’ is no effect

‘1’ is sets the interrupt enable bit

READ as :

‘0’ is indicates the interrupt disable

‘1’ is indicates the interrupt enable

15.4.6 GPIOA Interrupt Enable Clear Register(GPIOA_ INTENCLR)

Address offset: 0x0024

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] IECy(y = 0..14)

WRITE as :

‘0’ is no effect

‘1’ is clears the interrupt enable bit

READ as :

‘0’ is indicates the interrupt disable

‘1’ is indicates the interrupt enable

15.4.7 GPIOA Interrupt Type Set Register(GPIOA_ INTTYPESET)

Address offset: 0x0028

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	ITS14	ITS13	ITS12	ITS11	ITS10	ITS9	ITS8	ITS7	ITS6	ITS5	ITS4	ITS3	ITS2	ITS1	ITS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] ITSy(y = 0..14)

WRITE as :

'0' is no effect

'1' is sets the interrupt type bit

READ as :

'0' is indicates for LOW or HIGH level

'1' is indicates for falling edge or rising edge

15.4.8 GPIOA Interrupt Type Clear Register(GPIOA_ INTTYPECLR)

Address offset: 0x002c

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	ITC14	ITC13	ITC12	ITC11	ITC10	ITC9	ITC8	ITC7	ITC6	ITC5	ITC4	ITC3	ITC2	ITC1	ITC0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] ITCy(y = 0..14)

WRITE as :

'0' is no effect

'1' is clears the interrupt type bit

READ as :

'0' is indicates for LOW or HIGH level

'1' is indicates for falling edge or rising edge

15.4.9 GPIOA Interrupt Polarity Set Register(GPIOA_ INTPOLSET)

Address offset: 0x0030

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	IPS14	IPS13	IPS12	IPS11	IPS10	IPS9	IPS8	IPS7	IPS6	IPS5	IPS4	IPS3	IPS2	IPS1	IPS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] IPSy(y = 0..14)

WRITE as :

‘0’ is no effect

‘1’ is sets the interrupt polarity bit

READ as :

‘0’ is indicates for LOW level or falling edge

‘1’ is indicates for HIGH level or rising edge

15.4.10 GPIOA Interrupt Polarity Clear Register(GPIOA_ INTPOLCLR)

Address offset: 0x0034

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8	IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] IPCy(y = 0..14)

WRITE as :

‘0’ is no effect

‘1’ is clears the interrupt polarity bit

READ as :

‘0’ is indicates for LOW level or falling edge

‘1’ is indicates for HIGH level or rising edge

15.4.11 GPIOA Interrupt Status/Interrupt Clear Register(GPIOA_ INTSTATUS/ INTCLEAR)

Address offset: 0x0038

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	ISC14	ISC13	ISC12	ISC11	ISC10	ISC9	ISC8	ISC7	ISC6	ISC5	ISC4	ISC3	ISC2	ISC1	ISC0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[14:0] ISCy(y = 0..14)

WRITE as :

‘0’ is no effect

‘1’ is request to clear the interrupt

READ as : IRQ status Register

15.4.12 GPIOA Lower Byte Masked Access Register(GPIOA_ LB_MASKED)

Address offset: 0x0400 – 0x07FC

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	LBM							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Lower eight bits masked access

[15:8] Not used

[7:0] Data for lower byte access, with bits[9:2] of address value used as enable bit mask for each bit

15.4.13 GPIOA Upper Byte Masked Access Register(GPIOA_UB_MASKED)

Address offset: 0x0800-0x0FC

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HBM								res	res	res	res	res	res	res	res
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Higher eight bits masked access

[15:8] Data for higher byte access, with bits[9:2] of address value used as enable bit mask for each bit

[7:0] Not used

15.5 Register map

The following Table 14 summarizes the GPIOA registers.

Table 14 GPIOA register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	GPIOA DATA	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Data register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x04	GPIOA DATAOUT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DAO14	DAO13	DAO12	DAO11	DAO10	DAO9	DAO8	DAO7	DAO6	DAO5	DAO4	DAO3	DAO2	DAO1	DAO0	Dataout register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	GPIOA OUTENSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ES14	ES13	ES12	ES11	ES10	ES9	ES8	ES7	ES6	ES5	ES4	ES3	ES2	ES1	ES0	Output enable set register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x14	GPIOA OUTENCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	EC14	EC13	EC12	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Output enable clear register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x20	GPIOA INTENSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IES14	IES13	IES12	IES11	IES10	IES9	IES8	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0	Interrupt enable set register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x24	GPIOA INTENCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0	Interrupt enable clear register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x28	GPIOA INTTYPESET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ITS14	ITS13	ITS12	ITS11	ITS10	ITS9	ITS8	ITS7	ITS6	ITS5	ITS4	ITS3	ITS2	ITS1	ITS0	Interrupt type set register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x2C	GPIOA INTTYPECLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ITC14	ITC13	ITC12	ITC11	ITC10	ITC9	ITC8	ITC7	ITC6	ITC5	ITC4	ITC3	ITC2	ITC1	ITC0	Interrupt type clear register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x30	GPIOA INTPOLSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IPS14	IPS13	IPS12	IPS11	IPS10	IPS9	IPS8	IPS7	IPS6	IPS5	IPS4	IPS3	IPS2	IPS1	IPS0	Interrupt polarity set register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	GPIOA INTPOLCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8	IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0	Interrupt polarity clear register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x38	GPIOA INTSTATUS/ GPIOA INTCLEAR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ISC14	ISC13	ISC12	ISC11	ISC10	ISC9	ISC8	ISC7	ISC6	ISC5	ISC4	ISC3	ISC2	ISC1	ISC0	Interrupt status register/ Interrupt clear register
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x0400 - 0x07FC	GPIOA LB_MASKED	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	LBM								Lower byte masked access register
	reset value																									0	0	0	0	0	0	0	0	
0x0800 - 0x0BFC	GPIOA UB_MASKED	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	HBM								res	res	res	res	res	res	res	res	Upper byte maked access register
	reset value																	0	0	0	0	0	0	0	0									

15.6 GPIOB Registers(Address Base: 0x4300_0000)

15.6.1 GPIOB Data Register(GPIOB_DATA)

Address offset: 0x0000

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	DAT3	DAT2	DAT1	DAT0
												R	R	R	R

[3:0] DATy(y = 0..3)

READ as : Port input data bit

15.6.2 GPIOB Output Latch Register(GPIOB_DATAOUT)

Address offset: 0x0004

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	DAO3	DAO2	DAO1	DAO0
												R/W	R/W	R/W	R/W

[3:0] DAOy(y = 0..3)

READ as : Port out data bit

WRITE as : WRITE to GPIOB_DATAOUT register

15.6.3 GPIOB Enable Set Register(GPIOB_OUTENSET)

Address offset: 0x0010

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	Res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	ES3	ES2	ES1	ES0
												R/W	R/W	R/W	R/W

[3:0] ESy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is sets the corresponding output enable bit

READ as :

‘0’ is indicates the signal direction as input

‘1’ is indicates the signal direction as output

15.6.4 GPIOB Enable Clear Register(GPIOB_OUTENCLR)

Address offset: 0x0014

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	EC3	EC2	EC1	EC0
												R/W	R/W	R/W	R/W

[3:0] ECy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is clears the output enable bit

READ as :

‘0’ is indicates the signal direction as input

‘1’ is indicates the signal direction as output

15.6.5 GPIOB Interrupt Enable Set Register(GPIOB_ INTENSET)

Address offset: 0x0020

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	IES3	IES2	IES1	IES0
												R/W	R/W	R/W	R/W

[3:0] IESy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is sets the interrupt enable bit

READ as :

‘0’ is indicates the interrupt disable

‘1’ is indicates the interrupt enable

15.6.6 GPIOB Interrupt Enable Clear Register(GPIOB_ INTENCLR)

Address offset: 0x0024

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	IEC3	IEC2	IEC1	IEC0
												R/W	R/W	R/W	R/W

[3:0] IECy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is clears the interrupt enable bit

READ as :

‘0’ is indicates the interrupt disable

‘1’ is indicates the interrupt enable

15.6.7 GPIOB Interrupt Type Set Register(GPIOB_ INTTYPESET)

Address offset: 0x0028

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	ITS3	ITS2	ITS1	ITS0
												R/W	R/W	R/W	R/W

[3:0] ITSy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is sets the interrupt type bit

READ as :

‘0’ is indicates for LOW or HIGH level

‘1’ is indicates for falling edge or rising edge

15.6.8 GPIOB Interrupt Type Clear Register(GPIOB_ INTTYPECLR)

Address offset: 0x002c

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	ITC3	ITC2	ITC1	ITC0
												R/W	R/W	R/W	R/W

[3:0] ITCy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is clears the interrupt type bit

READ as :

‘0’ is indicates for LOW or HIGH level

‘1’ is indicates for falling edge or rising edge

15.6.9 GPIOB Interrupt Polarity Set Register(GPIOB_ INTPOLSET)

Address offset: 0x0030

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	IPS3	IPS2	IPS1	IPS0
												R/W	R/W	R/W	R/W

[3:0] IPSy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is sets the interrupt polarity bit

READ as :

‘0’ is indicates for LOW level or falling edge

‘1’ is indicates for HIGH level or rising edge

15.6.10 GPIOB Interrupt Polarity Clear Register(GPIOB_INTPOLCLR)

Address offset: 0x0034

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	IPC3	IPC2	IPC1	IPC0
												R/W	R/W	R/W	R/W

[3:0] IPCy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is clears the interrupt polarity bit

READ as :

‘0’ is indicates for LOW level or falling edge

‘1’ is indicates for HIGH level or rising edge

15.6.11 GPIOB Interrupt Status/Interrupt Clear Register(GPIOB_ INTSTATUS/ INTCLEAR)

Address offset: 0x0038

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	ISC3	ISC2	ISC1	ISC0
												R/W	R/W	R/W	R/W

[3:0] ISCy(y = 0..3)

WRITE as :

‘0’ is no effect

‘1’ is request to clear the interrupt

READ as : IRQ status Register

15.6.12 GPIOB Lower Byte Masked Access Register (GPIOB_LB_MASKED)

Address offset: 0x0400 – 0x07FC

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	LBM							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Lower eight bits masked access

[15:8] Not used

[7:0] Data for lower byte access, with bits[9:2] of address value used as enable bit mask for each bit

15.6.13 GPIOB Upper Byte Masked Access Register(GPIOB_UB_MASKED)

Address offset: 0x0800-0x0FC

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HBM								res	res	res	res	res	res	res	res
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Higher eight bits masked access

[15:8] Data for higher byte access, with bits[9:2] of address value used as enable bit mask for each bit

[7:0] Not used

15.7 Register map

The following Table 15 summarizes the GPIOB registers.

Table 15 GPIOB register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	GPIOB DATA	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DATA3	DATA2	DATA1	DATA0	Data register
	reset value																													0	0	0	0	
0x04	GPIOB DATAOUT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DAO3	DAO2	DAO1	DAO0	Dataout register
	reset value																													0	0	0	0	
0x10	GPIOB OUTENSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ES3	ES2	ES1	ES0	Output enable set register
	reset value																													0	0	0	0	
0x14	GPIOB OUTENCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	EC3	EC2	EC1	EC0	Output enable clear register
	reset value																													0	0	0	0	
0x20	GPIOB INTENSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IES3	IES2	IES1	IES0	Interrupt enable set register
	reset value																													0	0	0	0	
0x24	GPIOB INTENCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IEC3	IEC2	IEC1	IEC0	Interrupt enable clear register
	reset value																													0	0	0	0	
0x28	GPIOB INTTYPESET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ITS3	ITS2	ITS1	ITS0	Interrupt type set register
	reset value																													0	0	0	0	
0x2C	GPIOB INTTYPECLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ITC3	ITC2	ITC1	ITC0	Interrupt type clear register
	reset value																													0	0	0	0	
0x30	GPIOB INTPOLSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IPS3	IPS2	IPS1	IPS0	Interrupt polarity set register
	reset value																													0	0	0	0	
0x34	GPIOB INTPOLCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IPC3	IPC2	IPC1	IPC0	Interrupt polarity clear register
	reset value																													0	0	0	0	
0x38	GPIOB INTSTATUS/ GPIOB INTCLEAR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ISC3	ISC2	ISC1	ISC0	Interrupt status register/ Interrupt clear register
	reset value																													0	0	0	0	
0x0400 - 0x07FC	GPIOB LB_MASKED	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	LBM								Lower byte masked access register
	reset value																									0	0	0	0	0	0	0	0	
0x0800 - 0xBFC	GPIOB UB_MASKED	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	HBM								res	res	res	res	res	res	res	res	Upper byte maked access register
	reset value																	0	0	0	0	0	0	0	0									

15.8 GPIOC Registers(Address Base: 0x4400_0000)

15.8.1 GPIOC Data Register(GPIOC_DATA)

Address offset: 0x0000

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT15	DAT14	DAT13	DAT12	DAT11	DAT10	DAT9	DAT8	res	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0
R	R	R	R	R	R	R	R		R	R	R	R	R	R	R

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

READ as : Port input data bit

15.8.2 GPIOC Output Latch Register(GPIOC_DATAOUT)

Address offset: 0x0004

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAO15	DAO14	DAO13	DAO12	DAO11	DAO10	DAO9	DAO8	res	DAO6	DAO5	DAO4	DAO3	DAO2	DAO1	DAO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

READ as : Port out data bit

WRITE as : WRITE to GPIOC_DATAOUT register

15.8.3 GPIOC Enable Set Register(GPIOC_OUTENSET)

Address offset: 0x0010

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ES15	ES14	ES13	ES12	ES11	ES10	ES9	ES8	res	ES6	ES5	ES4	ES3	ES2	ES1	ES0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

‘0’ is no effect

‘1’ is sets the corresponding output enable bit

READ as :

‘0’ is indicates the signal direction as input

‘1’ is indicates the signal direction as output

15.8.4 GPIOC Enable Clear Register(GPIOC_OUTENCLR)

Address offset: 0x0014

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	res	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

‘0’ is no effect

‘1’ is clears the output enable bit

READ as :

‘0’ is indicates the signal direction as input

'1' is indicates the signal direction as output

15.8.5 GPIOC Interrupt Enable Set Register(GPIOC_ INTENSET)

Address offset: 0x0020

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IES15	IES14	IES13	IES12	IES11	IES10	IES9	IES8	res	IES6	IES5	IES4	IES3	IES2	IES1	IES0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

'0' is no effect

'1' is sets the interrupt enable bit

READ as :

'0' is indicates the interrupt disable

'1' is indicates the interrupt enable

15.8.6 GPIOC Interrupt Enable Clear Register(GPIOC_ INTENCLR)

Address offset: 0x0024

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8	res	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

'0' is no effect

'1' is clears the interrupt enable bit

READ as :

'0' is indicates the interrupt disable

'1' is indicates the interrupt enable

15.8.7 GPIOC Interrupt Type Set Register(GPIOC_ INTTYPESET)

Address offset: 0x0028

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ITS15	ITS14	ITS13	ITS12	ITS11	ITS10	ITS9	ITS8	res	ITS6	ITS5	ITS4	ITS3	ITS2	ITS1	ITS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

'0' is no effect

'1' is sets the interrupt type bit

READ as :

'0' is indicates for LOW or HIGH level

'1' is indicates for falling edge or rising edge

15.8.8 GPIOC Interrupt Type Clear Register(GPIOC_ INTTYPECLR)

Address offset: 0x002c

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ITC15	ITC14	ITC13	ITC12	ITC11	ITC10	ITC9	ITC8	res	ITC6	ITC5	ITC4	ITC3	ITC2	ITC1	ITC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

'0' is no effect

'1' is clears the interrupt type bit

READ as :

'0' is indicates for LOW or HIGH level

'1' is indicates for falling edge or rising edge

15.8.9 GPIOC Interrupt Polarity Set Register(GPIOC_ INTPOLSET)

Address offset: 0x0030

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPS15	IPS14	IPS13	IPS12	IPS11	IPS10	IPS9	IPS8	res	IPS6	IPS5	IPS4	IPS3	IPS2	IPS1	IPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

'0' is no effect

'1' is sets the interrupt polarity bit

READ as :

'0' is indicates for LOW level or falling edge

'1' is indicates for HIGH level or rising edge

15.8.10 GPIOC Interrupt Polarity Clear Register(GPIOC_ INTPOLCLR)

Address offset: 0x0034

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8	res	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

‘0’ is no effect

‘1’ is clears the interrupt polarity bit

READ as :

‘0’ is indicates for LOW level or falling edge

‘1’ is indicates for HIGH level or rising edge

15.8.11 GPIOC Interrupt Status/Interrupt Clear Register(GPIOC_ INTSTATUS/ INTCLEAR)

Address offset: 0x0038

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISC15	ISC14	ISC13	ISC12	ISC11	ISC10	ISC9	ISC8	res	ISC6	ISC5	ISC4	ISC3	ISC2	ISC1	ISC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

[15:8] DATy(y = 8..15)

[7] Reserved

[6:0] DATy(y = 0..6)

WRITE as :

‘0’ is no effect

‘1’ is request to clear the interrupt

READ as : IRQ status Register

15.8.12 GPIOC Lower Byte Masked Access Register(GPIOC_LB_MASKED)

Address offset: 0x0400 – 0x07FC

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	LBM							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Lower eight bits masked access

[15:8] Not used

[7:0] Data for lower byte access, with bits[9:2] of address value used as enable bit mask for each bit

15.8.13 GPIOC Upper Byte Masked Access Register(GPIOC_UB_MASKED)

Address offset: 0x0800-0x0FC

Reset value: 0x----

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HBM								res	res	res	res	res	res	res	res
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Higher eight bits masked access

[15:8] Data for higher byte access, with bits[9:2] of address value used as enable bit mask for each bit

[7:0] Not used

15.9 Register map

The following Table 16 summarizes the GPIOC registers.

Table 16 GPIOC register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	GPIOC DATA	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8	res	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Data register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x04	GPIOC DATAOUT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DAO15	DAO14	DAO13	DAO12	DAO11	DAO10	DAO9	DAO8	res	DAO6	DAO5	DAO4	DAO3	DAO2	DAO1	DAO0	Dataout register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x10	GPIOC OUTENSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ES15	ES14	ES13	ES12	ES11	ES10	ES9	ES8	res	ES6	ES5	ES4	ES3	ES2	ES1	ES0	Output enable set register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x14	GPIOC OUTENCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	res	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Output enable clear register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x20	GPIOC INTENSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IES15	IES14	IES13	IES12	IES11	IES10	IES9	IES8	res	IES6	IES5	IES4	IES3	IES2	IES1	IES0	Interrupt enable set register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x24	GPIOC INTENCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8	res	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0	Interrupt enable clear register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x28	GPIOC INTTYPESET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ITS15	ITS14	ITS13	ITS12	ITS11	ITS10	ITS9	ITS8	res	ITS6	ITS5	ITS4	ITS3	ITS2	ITS1	ITS0	Interrupt type set register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x2C	GPIOC INTTYPECLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ITC15	ITC14	ITC13	ITC12	ITC11	ITC10	ITC9	ITC8	res	ITC6	ITC5	ITC4	ITC3	ITC2	ITC1	ITC0	Interrupt type clear register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x30	GPIOC INTPOLSET	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IPS15	IPS14	IPS13	IPS12	IPS11	IPS10	IPS9	IPS8	res	IPS6	IPS5	IPS4	IPS3	IPS2	IPS1	IPS0	Interrupt polarity set register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x34	GPIOC INTPOLCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IPC15	IPC14	IPC13	IPC12	IPC11	IPC10	IPC9	IPC8	res	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0	Interrupt polarity clear register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x38	GPIOC INTSTATUS/ GPIOC INTCLEAR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IS C15	IS C14	IS C13	IS C12	IS C11	IS C10	IS C9	IS C8	res	IS C6	IS C5	IS C4	IS C3	IS C2	IS C1	IS C0	Interrupt status register/ Interrupt clear register
	reset value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
0x0400 - 0x07FC	GPIOC LB_MASKED	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	LBM								Lower byte masked access register
	reset value																									0	0	0	0	0	0	0	0	
0x0800 - 0x0BFC	GPIOC UB_MASKED	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	HBM								res	res	res	res	res	res	res	res	Upper byte maked access register
	reset value																	0	0	0	0	0	0	0	0									

16 Direct memory access controller (DMA)

16.1 Introduction

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The DMA controller has up to 6 channels in total, each dedicated to managing memory access requests from one or more peripherals. It has an arbiter for handling the priority between DMA requests. For more details, refer to “PrimeCell® µDMA Controller (PL230)” from the Technical Reference Manual

16.2 Features

- 6 channels
- Each channel is connected to dedicated hardware DMA requests and software trigger is also supported on each channel.
- Priorities between requests from the DMA channels are software programmable (2 levels consisting of high, default)
- Memory-to-memory transfer (software request only)
- TCP/IP-to-memory transfer (software request only)
- SPI/UART-to-memory transfer (hardware request and software request)
- Access to Flash, SRAM, APB and AHB peripherals as source and destination

16.3 Functional description

Figure 20 shows the DMA block diagram.

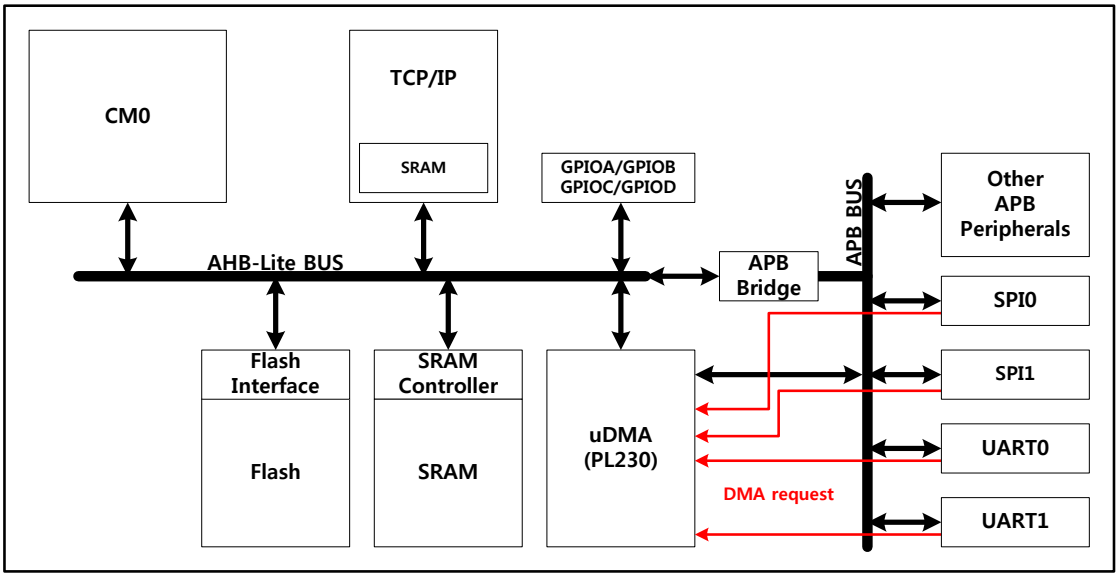


Figure 20. DMA Block diagram

16.3.1 DMA request mapping

The hardware requests from the peripherals (UART0, UART1, SSP0, SSP1) are simply connected to the DMA. Refer to Table 1 which lists the DMA requests for each channel.

Table 17 Summary of the DMA requests for each channel

	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6
Hardware Request	SSP0_TX SSP0_RX	SSP1_TX SSP1_RX	UART0_TX UART0_RX	UART1_TX UART1_RX	NONE	NONE
Software Request(1)	Support	Support	Support	Support	Support	Support

1. Software request is the only way to use DMA for memory-to-memory or TCP/IP-to-memory.

16.3.2 DMA arbitration

The controller can be configured to perform arbitration during a DMA cycle before and after a programmable number of transfers. This reduces the latency for servicing a higher priority channel.

The controller uses four bits in the channel control data structure that configures how many AHB bus transfers occur before the controller re-arbitrates. These bits are known as the R_power bits because the value R is raised to the power of two and this determines the arbitration rate. For example, if R = 4, then the arbitration rate is 2^4, which means the controller arbitrates every 16 DMA transfers.

Remark: Do not assign a low-priority channel with a large R_power value because this prevents the controller from servicing high-priority requests until it re-arbitrates.

When N > 2^R and is not an integer multiple of 2^R, then the controller always performs sequences of 2^Rtransfers until N < 2^R remain to be transferred. The controller performs the remaining N transfers at the end of the DMA cycle.

16.3.3 DMA cycle types

The cycle_ctrl bits in the channel control data structure controls how the DMA controller performs a cycle.

The controller uses four cycle types described in this manual:

- Invalid
- Basic
- Auto-request

- Ping-pong

See ARM micro DMA (PL230) documentation for additional cycle types.

For all cycle types, the controller arbitrates after 2^R DMA transfers. If a low-priority channel is set to a large 2^R value then it prevents all other channels from performing a DMA transfer until the low-priority DMA transfer completes. Therefore, the user must take care when setting the R_power bit in the channel_cfg data structure, that the latency for high-priority channels is not significantly increased.

16.3.3.1 Invalid cycle

After the controller completes a DMA cycle, it sets the cycle type to invalid to prevent it from repeating the same DMA cycle.

16.3.3.2 Basic cycle

In this mode, the controller can be configured to use either the primary or the alternate channel control data structure. After the channel is enabled and the controller receives a request for this channel, the flow for basic cycle is as below:

1. The controller performs 2^R transfers.
   If the number of transfers remaining is zero the flow continues at step 3.
2. The controller arbitrates:
   - If a higher-priority channel is requesting service, then the controller services that channel.
   - If the peripheral or software signals a request to the controller, then it continues at step 1.
3. The controller sets dma_done[c] signal for this channel HIGH for one system clock cycle. This indicates to the host processor that the DMA cycle is complete.

16.3.3.3 Auto-request cycle

When the controller operates in this mode, it is only necessary to receive a single request to enable the controller to complete the entire DMA cycle. This enables a large data transfer to occur, without significantly increasing the latency for servicing higher priority requests or requiring multiple requests from the processor or peripheral.

The auto-request cycle is typically used for memory-to-memory requests. In this case, software generates the starting request for the 2^R transfers after setting up the DMA control data structure.

In this mode, the controller can be configured to use either the primary or the alternate channel control data structure. After the channel is enabled and the controller receives a request for this channel, the flow for the auto-request cycle is as below:

1. The controller performs 2^R transfers. If the number of transfers remaining is zero the flow continues at step 3.
2. The controller arbitrates if there are any transfers remaining after 2^R transfers. If the current channel c has the highest priority, the cycle continues at step 1.

The controller sets dma_done[c] signal for this channel HIGH for one system clock cycle. This indicates to the host processor that the DMA cycle is complete.

16.3.3.4 Ping-pong cycle

In this mode, the controller performs a DMA cycle using one of the data structures and then performs a DMA cycle using the other data structure. The controller continues to switch between primary and alternate structures until it reads a data structure that is invalid, until the user reprograms the cycle_type to basic, or until the host processor disables the channel.

In ping-pong mode, the user can program or reprogram one of the two channel data structures (primary or alternate) while using the other channel data structure for the active transfer. When a transfer is done, the next transfer can be started immediately using the prepared channel data structure – provided that a higher priority channel does not require servicing. If the user does not reprogram the channel control data structure not in use for a transfer, the cycle type remains invalid (which is the value at the end of the last transfer using that structure), and the ping-pong cycle completes.

The ping-pong cycle can be used for transfers to or from peripherals or for memory- to-memory transfers.

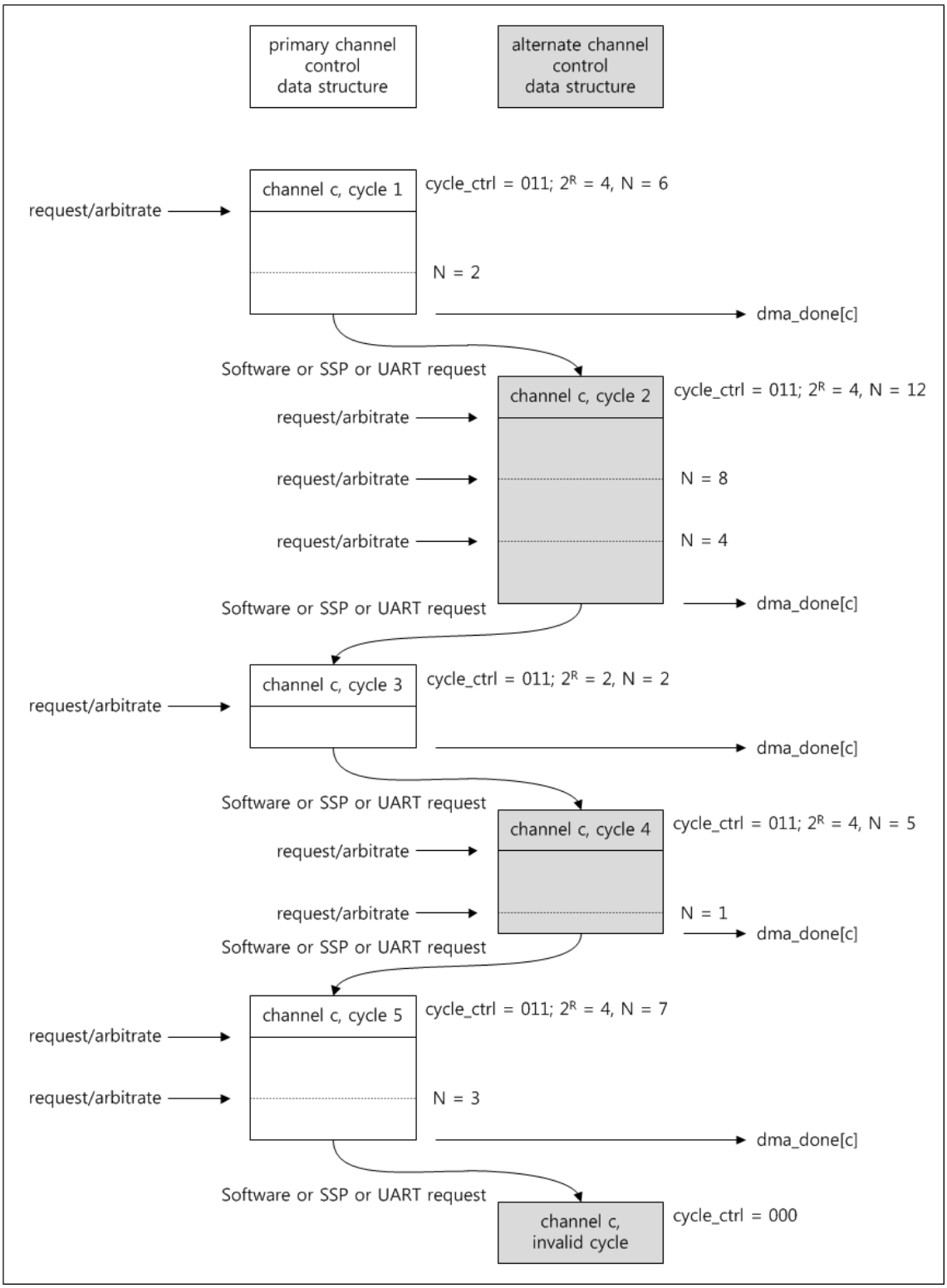


Figure 21. DMA ping pong cycle

16.4 Registers (Base address : 0x4100_4000)

16.4.1 DMA status register (DMA_STATUS)

Address offset : 0x000

Reset value : 0x0005_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	STATE				res	res	res	ENABLE
								RO							RO

[0] ENABLE – Enable status of the controller

This bit is read only register to check enable status of DMA controller

0 : controller is disabled

1 : controller is enabled

[7:4] STATE – Current state of the control state machine.

These bits are read only register to check current state of controller. State can be one of the following

0000 : idle

0001 : reading channel controller data

0010 : reading source data end pointer

0011 : reading destination data end pointer

0100 : reading source data

0101 : writing destination data

0110 : waiting channel controller data

1000 : stalled

1001 : done

1010 : peripheral scatter-gather transition

1011 – 1111 : undefined.

16.4.2 DMA configuration register (DMA_CFG)

Address offset : 0x004

Reset value : -

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	PROT_CTRL			res	res	res	res	ENABLE
								WO							WO

[0] ENABLE – Enable for the controller

This bit is write only register to enable of DMA controller

0 : disable the controller

1 : enable the controller

[7:5] PROT_CTRL – Set the AHB-Lite protection by controlling the HPROT[3:1] signal levels

These bits are write only register to set HPROT[3:1] signal as follows

[7] : controls HPROT[3] to indicate if a cacheable access is occurring.

[6] : controls HPROT[2] to indicate if a bufferable access is occurring.

[5] : controls HPROT[1] to indicate if a privileged access is occurring.

16.4.3 DMA control data base pointer register (DMA_CTRL_BASE_PTR)

Address offset : 0x008

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTRL_BASE_PTR[31:16]															
R/W															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRL_BASE_PTR[15:8]								res	res	res	res	res	res	res	res
R/W															

[31:8] CTRL_BASE_PTR – Pointer to the base address of the primary data structure

These bits are read/write register. User must configure this register so that the base pointer points to a location in system memory.

16.4.4 DMA channel alternate control data base pointer register (DMA_ALT_CTRL_BASE_PTR)

Address offset : 0x00c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALT_CTRL_BASE_PTR[31:16]															
RO															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALT_CTRL_BASE_PTR[15:0]															
RO															

[31:0] ALT_CTRL_BASE_PTR : Base address of the alternate data structure

This read only register returns the base address of the alternate data structure.

16.4.5 DMA channel wait on request status register (DMA_WAITONREQ_STATUS)

Address offset : 0x010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	DMA_WAITONREQ[5:0]					
										RO					

[Channel-1] DMA_WAITONREQ – Channel wait on request status

This read-only register returns the status of dma_waitonreq[Channel-1].

0 : dma_waitonreq is low

1 : dma_waitonreq is high

16.4.6 DMA channel software request register (DMA_CHNL_SW_REQUEST)

Address offset : 0x014

Reset value : -

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_SW_REQUEST[5:0]					
										WO					

[Channel-1] CHNL_SW_REQUEST – Set the appropriate bit to generate a software DMA request on the corresponding DMA channel

This read-only register enables to generate a software DMA request.

0 : dose not create a DMA request for [Channel-1]

1 : creates a DMA request for [Channel -1]

16.4.7 DMA channel useburst set register (DMA_CHNL_USEBURST_SET)

Address offset : 0x018

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_USEBURST_SET[5:0]					
										RW					

[Channel-1] CHNL_USEBURST_SET – Returns the useburst status, or disable dma_sreq[Channel-1] form generating DMA requests.

This read/write register disables the single request dma_sreq[Channel-1] input from generating requests, and therefore only the request, dma_req[Channel-1],generates requests. Reading the register returns the useburst status.

Read as :

0 : DMA [Channel-1] responds to requests that it receives on dma_req[Channel-1] or dma_sreq[Channel-1]

1 : DMA [Channel-1] does not responds to requests that it receives on dma_sreq[Channel-1]. The controller only responds to dma_req[Channel-1] requests

Write as :

0 : No effect. Use the CHNL_USEBURST_CLR register to set bit [Channel-1] to 0

1 : Disables dma_sreq[Channel-1] form generating DMA requests.

16.4.8 DMA channel useburst clear register (DMA_CHNL_USEBURST_CLR)

Address offset : 0x01c

Reset value : -

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_USEBURST_CLR[5:0]					
										WO					

[Channel-1] CHNL_USEBURST_CLR - Set the appropriate bit to enable dma_sreq[Channel-1] to generate requests.

This Write register enables dma_sreq[Channel-1] to generate requests.

0 – No effect. User the CHNL_USEBURST_SET register to disable dma_sreq[Channel-1] from generating requests.

1 – Enable dma_sreq[Channel-1] to generate DMA requests.

16.4.9 DMA channel request mask set register (DMA_CHNL_REQ_MASK_SET)

Address offset : 0x020

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_REQ_MASK_SET[5:0]					
										R/W					

[Channel-1] CHNL_REQ_MASK_SET - Returns the request mask status of dma_req[Channel-1] and dma_sreq[Channel-1], or disables the corresponding channel from generating DMA requests.

This read/write register disables a HIGH on dma_req[Channel-1], for dma_sreq[Channel-1], from generating a request. Reading the register returns the request mask status for dma_req[Channel-1] and dma_sreq[Channel-1].

Read as :

0 – External requests are enabled for channel [Channel-1]

1 – External requests are disabled for channel [Channel-1]

Write as :

0 – No effect. Use the CHNL_REQ_MASK_CLR register to enable DMA requests.

1 – Disables dma_req[Channel-1] and dma_sreq[Channel-1] from generating DMA requests.

16.4.10 DMA channel request mask clear register (DMA_CHNL_REQ_MASK_CLR)

Address offset : 0x024

Reset value : -

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_REQ_MASK_CLR[5:0]					
										WO					

[Channel-1] CHNL_REQ_MASK_CLR – Set the appropriate bit to enable DMA requests for the channel corresponding to dma_req[Channel-1] and dma_sreq[Channel-1]

This write only register enables a HIGH on dma_req[Channel-1], or dma_sreq[Channel-1].

0 : No effect. Use the CHNL_REQ_MASK_SET register to disable dma_req[Channel-1] and dma_sreq[Channel-1] from generating requests.

1 : Enables dma_req[Channel-1] or dma_sreq[Channel] to generate DMA requests.

16.4.11 DMA channel enable set register (DMA_CHNL_ENABLE_SET)

Address offset : 0x028

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_ENABLE_SET[5:0]					
										R/W					

[Channel-1] CHNL_ENABLE_SET - Returns the enable status of channels or enables the corresponding channels.

This read/write register enables a DMA channel. Reading the register returns the enable status of the channels.

Read as :

0 – Channel [Channel-1] is disabled

1 – Channel [Channel-1] is enabled

Write as :

0 – No effect. Use the CHNL_ENABLE_CLR register to disable a channel.

1 – Enables channels [Channel-1]

16.4.12 DMA channel enable clear register (DMA_CHNL_ENABLE_CLR)

Address offset : 0x02c

Reset value : -

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_ENABLE_CLR[5:0]					
										WO					

[Channel-1] CHNL_ENABLE_CLR – Set the appropriate bit to disable the corresponding DMA channel.

This write only register disable a DMA channel.

0 : No effect. Use the CHNL_ENABLE_SET register to enable DMA channel.

1 : Disable channel [Channel-1]

16.4.13 DMA channel primary-alternate set register (DMA_CHNL_PRI_ALT_SET)

Address offset : 0x030

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_PRI_ALT_SET[5:0]					
										R/W					

[Channel-1] CHNL_PRI_ALT_SET - Returns the channel control data structure status, or selects the alternate data structure for the corresponding DMA channels.

This read/write register configure a DMA channel to use the alternate data structure. Reading the register returns the status of which data structure is in use for the corresponding DMA channel.

Read as :

0 – DMA Channel [Channel-1] is using the primary data structure.

1 – DMA Channel [Channel-1] is using the alternate data structure.

Write as :

0 – No effect. Use the CHNL_PRI_ALT _CLR register to set bit [Channel-1] to 0

1 – Selects the alternate data structure for channel [Channel-1]

16.4.14 DMA channel primary-alternate clear register (DMA_CHNL_PRI_ALT _CLR)

Address offset : 0x034

Reset value : -

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_PRI_ALT_CLR[5:0]					
										WO					

[Channel-1] CHNL_PRI_ALT_CLR – Set the appropriate bit to select the primary data structure for the corresponding DMA channel.

This write only register configures a DMA channels to use the primary data structure.

0 : No effect. Use the CHNL_PRI_ALT _SET register to select the alternate data structure.

1 : Selects the primary data structure for channel [Channel-1]

16.4.15 DMA channel priority set register (DMA_CHNL_PRIORITY_SET)

Address offset : 0x038

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_PRIORITY_SET [5:0]					
										R/W					

[Channel-1] CHNL_PRIORITY_SET - Returns the channel priority mask status, or set the channel priority to high.

This read/write register configure a DMA channel to use the high priority level. Reading the register returns the status of channel priority mask

Read as :

0 – DMA Channel [Channel-1] is using the default priority level.

1 – DMA Channel [Channel-1] is using a high priority level.

Write as :

0 – No effect. Use the CHNL_PRIORITY_CLR register to set bit [Channel-1] to default priority level

1 – Channel [Channel-1] uses the high priority level.

16.4.16 DMA channel priority clear register (DMA_CHNL_PRIORITY_CLR)

Address offset : 0x03C

Reset value : -

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	CHNL_PRIORITY_CLR[5:0]					
										WO					

[Channel-1] CHNL_PRIORITY_CLR – Set the appropriate bit to select the default priority level for the specified DMA channel.

This write only register configures a DMA channels to use the default priority level.

0 : No effect. Use the CHNL_PRIORITY_SET register to set channel [Channel-1] to the high priority level.

1 : channel [Channel-1] uses the default priority level.

16.4.17 DMA bus error clear register (DMA_ERR_CLR)

Address offset : 0x04C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ERR_CLR
															R/W

[0] ERR_CLR – Returns the status of DMA_ERR, or set the signal LOW.

This read/write register returns the status of DMA_ERR, and enables set DMA_ERR LOW.

Read as :

0 : DMA_ERR is LOW

1 : DMA_ERR is HIGH

Write as :

0 : No effect, status of DMA_ERR is unchanged.

1 : Sets DMA_ERR LOW.

16.5 Register map

The following Table 18 summarizes the DMA registers.

Table 18 DMA register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	DMA_STATUS	res																								STATE				res			ENABLE
	reset value																									0	0	0	0				0
0x004	DMA_CFG	res																								PROT_CTRL				res			ENABLE
	reset value																																
0x008	DMA_CTRL_BASE_PTR	CTRL_BASE_PTR																								res							
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
0x00C	DMA_ALT_CTRL_BASE_PTR	ALT_CTRL_BASE_PTR																															
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x010	DMA_WAITONREQ_STATUS	res																								res	res	DMA_WAITONREQ					
	reset value																											0	0	0	0	0	0
0x014	DMA_CHNL_SW_REQUEST	res																								res	res	CHNL_SW_REQUEST					
	reset value																																
0x018	DMA_CHNL_USEBURST_SET	res																								res	res	CHNL_USEBURST_SET					
	reset value																											0	0	0	0	0	0
0x01C	DMA_CHNL_USEBURST_CLR	res																								res	res	CHNL_USEBURST_CLR					
	reset value																																
0x020	DMA_CHNL_REQ_MASK_SET	res																								res	res	CHNL_REQ_MASK_SET					
	reset value																											0	0	0	0	0	0
0x024	DMA_CHNL_REQ_MASK_CLR	res																								res	res	CHNL_REQ_MASK_CLR					
	reset value																																
0x028	DMA_CHNL_ENABLE_SET	res																								res	res	CHNL_ENABLE_SET					
	reset value																											0	0	0	0	0	0
0x02C	DMA_CHNL_ENABLE_CLR	res																								res	res	CHNL_ENABLE_CLR					
	reset value																																
0x030	DMA_CHNL_PRI_ALT_SET	res																								res	res	CHNL_PRI_ALT_SET					
	reset value																											0	0	0	0	0	0
0x034	DMA_CHNL_PRI_ALT_CLR	res																								res	res	CHNL_PRI_ALT_CLR					
	reset value																																
0x038	DMA_CHNL_PRIORITY_SET	res																								res	res	CHNL_PRIORITY_SET					
	reset value																											0	0	0	0	0	0
0x03C	DMA_CHNL_PRIORITY_CLR	res																								res	res	CHNL_PRIORITY_CLR					
	reset value																																
0x04C	DMA_ERR_CLR	res																								res	res	res					ERR_CLR
	reset value																																0

17 Analog-to-digital converter (ADC)

17.1 Introduction

ADC is a 12bit analog-to-digital converter. It has up to 9 multiplexed channels allowing it to measure signals from 8 externals and 1 internal source.

ADC of various channels can be performed in single mode. The result of the ADC is stored in 12 bit register.

17.2 Features

- 12bit configuration resolution
- Conversion time : Max 10MHz (Sampling time can be programmable)

  8 channel for external analog inputs
  - CH0 : PC_15
  - CH1 : PC_14
  - CH2 : PC_13
  - CH3 : PC_12
  - CH4 : PC_11
  - CH5 : PC_10
  - CH6 : PC_09
  - CH7 : PC_08

  1 channel for internal LDO(1.5v) voltage.
  - CH15 : Internal voltage
- Start of conversion can be initiated by software.
- Convert selected inputs once per trigger.
- Interrupt generation at the end of conversion.

17.3 Functional description

Figure 22 shows the ADC block diagram.

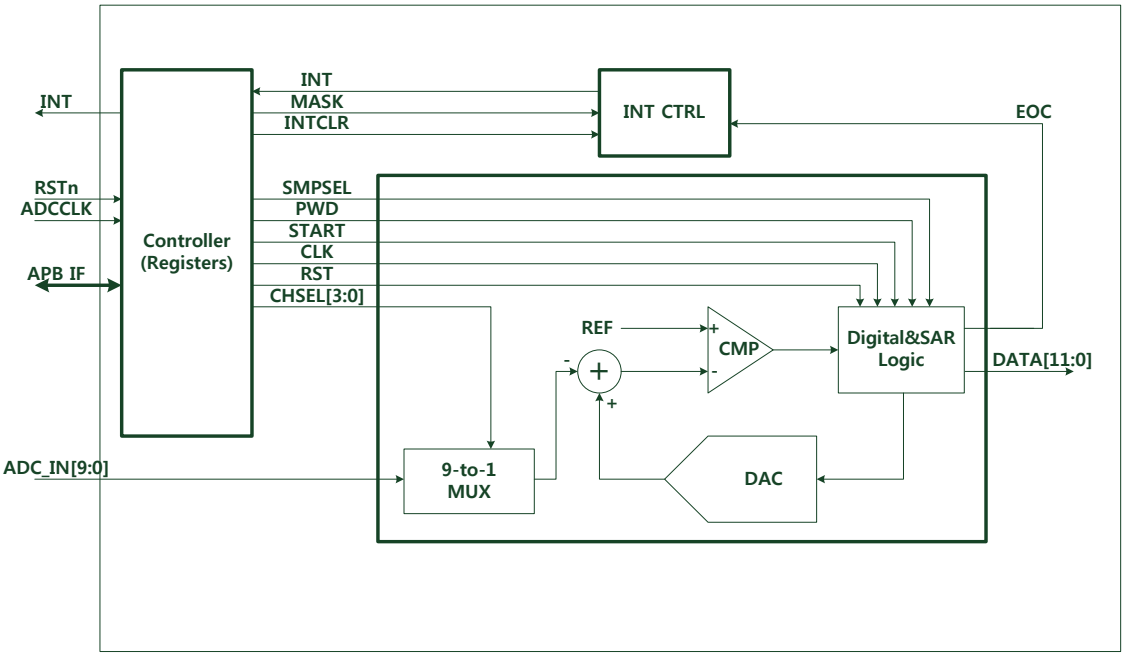


Figure 22. ADC block diagram

17.3.1 Operation ADC with non-interrupt

Figure 23 shows the flowchart of ADC operation with non-interrupt.

ADC can be used as below:

1. ADC needs to be initialized before operation.
   To initialize the ADC, clear the PWD bit first.
2. Select the ADC channel from 0 to 7 and 15 (initial core voltage).
3. Run start ADC conversion by set ADC_SRT bit.
4. Check INT bit to know finish of conversion.
5. If INT bit is high (1), read ADC conversion data.
6. Finally, ADC operation is finished by setting the PWD bit.

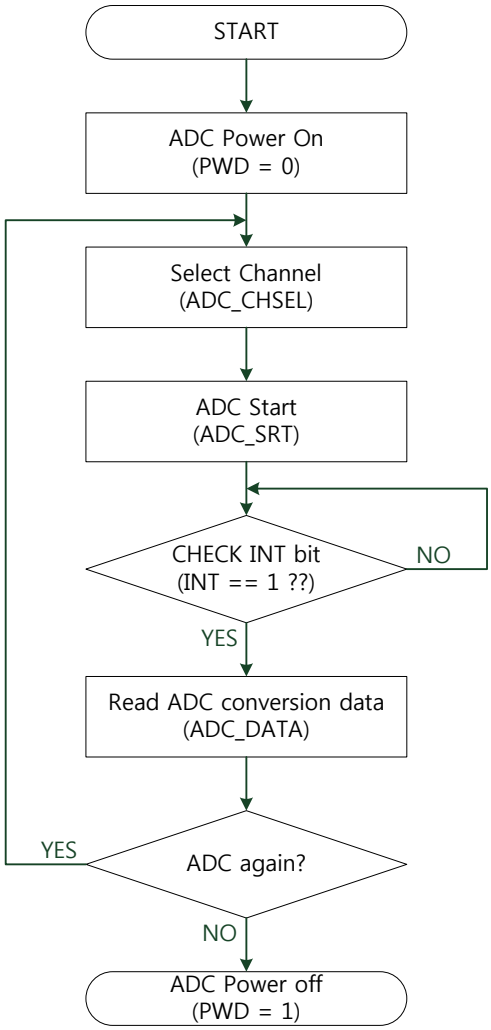


Figure 23. The ADC operation flowchart with non-interrupt

17.3.2 Operation ADC with interrupt

Figure 24 shows the flowchart of ADC operation with interrupt.

Operation is almost the same as the non-interrupt mode except checking INT register bit to know when enabling interrupt mask bit and conversion is completed.

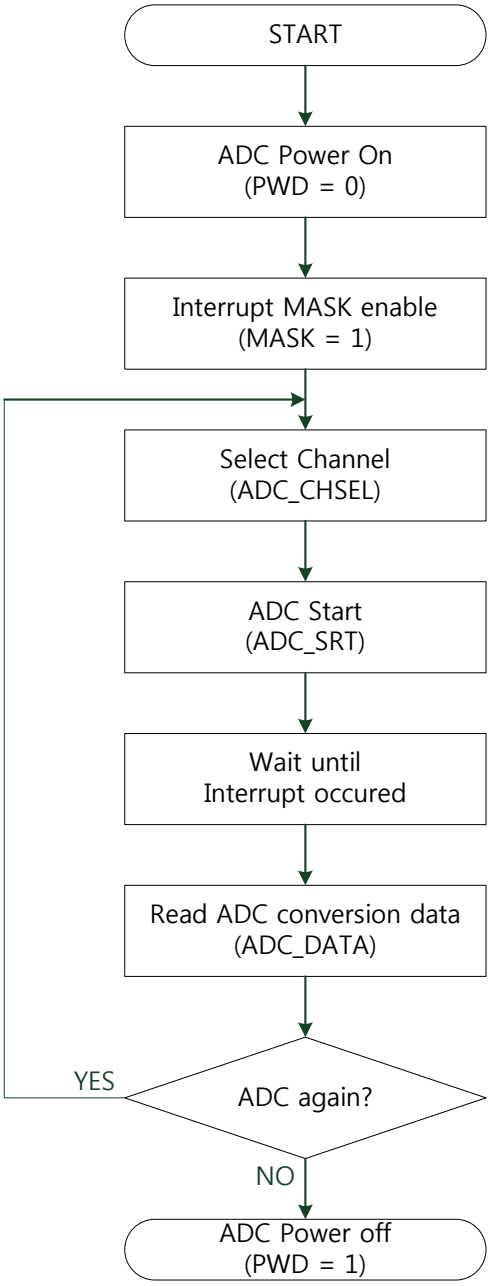


Figure 24. The ADC operation flowchart with interrupt

17.4 Registers (Base address : 0x4100_0000)

17.4.1 ADC control register (ADC_CTR)

Address offset : 0x000

Reset value : 0x0000_0003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PWD	SMPSEL
														R/W	R/W

[0] SMPSEL – Sampling mode select

This bit written by S/W to select sampling mode

0 : Abnormal mode

1 : Normal mode

[1] PWD – Power down

This bit set and cleared by S/W to enable/disable power down mode

O : Active

1 : Power down

17.4.2 ADC channel select register (ADC_CHSEL)

Address offset : 0x004

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	CHSEL			
												R/W			

[3:0] CHSEL – ADC Channel Select

These bits are written by S/W to define which channel is selected to be converted.

0000 : Channel 0 select

0001 : Channel 1 select

0010 : Channel 2 select

0011 : Channel 3 select

0100 : Channel 4 select

0101 : Channel 5 select

0110 : Channel 6 select

0111 : Channel 7 select

1000 ~ 1000 : no select

1111 : LDO output(1.5V) select

17.4.3 ADC start register (ADC_START)

Address offset : 0x008

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ADC_SRT
															W

[0] ADC_SRT – ADC Start bit

This bit set by S/W to start ADC for conversion. This bit is write-only.

0 : ready to start

1 : start ADC for conversion (This bit clear automatically after conversion)

17.4.4 ADC conversion data register (ADC_DATA)

Address offset : 0x00C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	ADC_DATA											
				R											

[11:0] ADC_DATA – ADC conversion result data

It contains ADC conversion result data of last converted channel. These bits are read-only.

17.4.5 ADC Interrupt register (ADC_INT)

Address offset : 0x010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	MASK	INT
														R/W	R

[0] DONE – Interrupt bit

This bit indicates that conversion is done or not. This bit is set after conversion is done and this bit is cleared by set of Interrupt clear bit. This bit is read-only.

[1] MASK – Interrupt mask signal.

This bit is interrupt mask bit of ADC. This bit can be set and cleared by S/W to enable/disable interrupt mask.

0 : Interrupt disable

1 : Interrupt enable

17.4.6 ADC Interrupt Clear register (ADC_INTCLR)

Address offset : 0x01c

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	INTCLR
															W

[0] INTCLR – Interrupt Clear bit.

This bit set by S/W to clear interrupt signal to CM0. This bit is write-only.

0 – nothing

1 – Clear interrupt signal (This bit clear automatically after clear interrupt)

17.5 Register map

The following Table 19 summarizes the ADC registers.

Table 19 ADC register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	ADC_CTR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PWD	SMPSEL
	reset value																															1	1
0x004	ADC_CHSEL	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CHSEL			
	reset value																													0	0	0	0
0x008	ADC_START	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	START
	reset value																																0
0x00C	ADC_DATA	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DATA											
	reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x010	ADC_INT	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MASK	INT
	reset value																															0	0
0x01C	ADC_INTCLR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	INTCLR
	reset value																																0

18 Pulse-Width Modulation (PWM)

18.1 Introduction

The PWM consists a 8-channel 32-bit Timer/Counter driven by a programmable prescaler. The function of the PWM is based on the basic Timer. Each timer and counter runs independently.

The PWM can be used to control the width of the pulse, formally the pulse duration, to generate output waveform or to count the counter triggered by external input.

18.2 Features

- Counter or Timer operation can use the peripheral clock, external clock source, or one of the capture inputs as the clock source.
- Eight independent 32-bit Timer/Counter driven by a programmable 6 bits prescaler runs as the PWM or standard timer if the PWM mode is not enabled.
- Eight PWM output waveforms.
- Each of Timer/Counter can have different or same clock source.
- Counter or timer operation.
- Eight capture registers that can take the timer value when an external input signal. A capture event can generate an interrupt signal optionally.
- 32-bit match register and limit register.

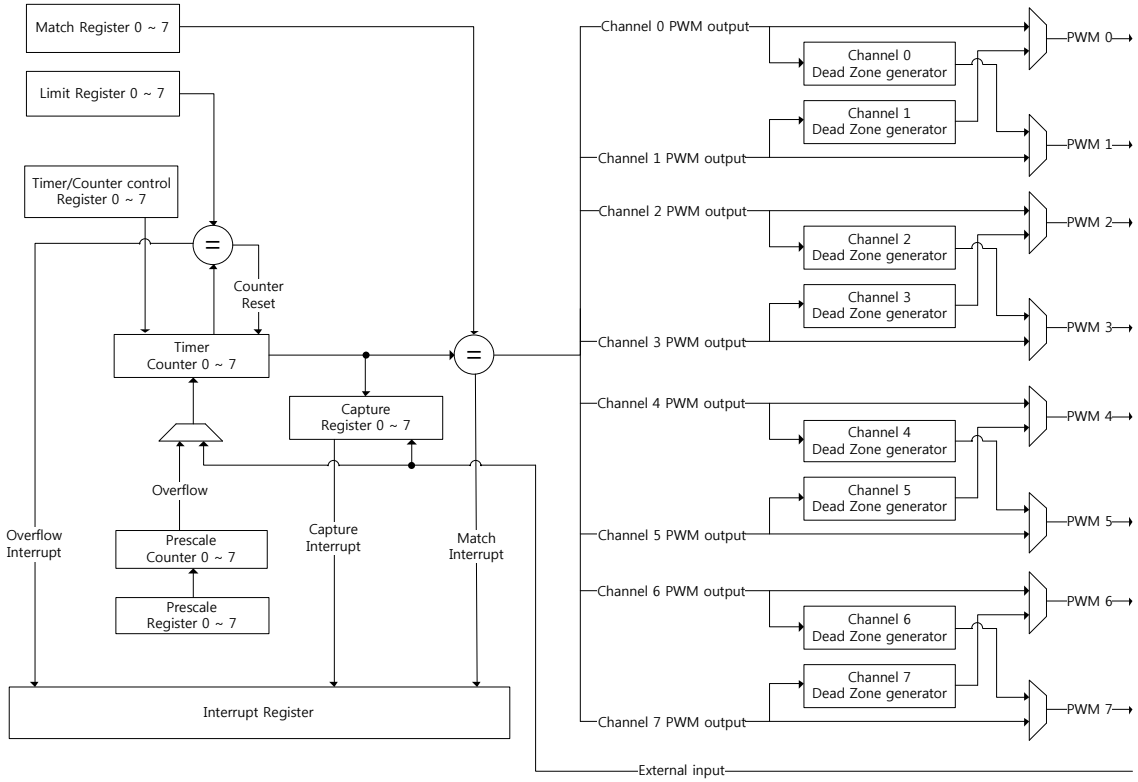


Figure 25 PWM block diagram

18.3 Functional description

18.3.1 Timer/Counter control

The PWM has Start/Stop register. It controls start or stop of the Timer/Counter. If you set this register, the Timer/Counter starts to run. If you reset this register, the Timer/Counter stops immediately. Also there is a pause register. The pause register is used to stop temporarily after one period. Although you set this register while the Timer/Counter is running, the Timer/Counter will stop when the period ends.

The registers of PWM can be updated when it stops or pauses. Users cannot update the registers while PWM is running.

18.3.2 Timer/Counter

The PWM has 8 Timer/Counter clocks, which can be divided by a prescaler. Each Timer/Counter runs independently. The Timer/Counter is designed to count cycles of the clocks or external input signal and generate interrupts when specified timer values are occurred based on match register and limit register. The Timer/Counter can count up or down.

The PWM has match registers and limit registers. The match registers control the duty cycle of PWM output waveform. The limit registers control the period of the PWM output waveform. The Timer/Counter becomes 0 when it reaches value of the limit register. If PDMR(Periodic Mode Register) is set, the Timer/Counter counts repeatedly and if PDMR is reset, the Timer/Counter stops counting.
Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

Repetition mode

The Timer/Counter has two repetition mode: periodic and one-shot mode. In periodic mode, the Timer/Counter recycles and then restarts when the Timer/Counter reaches the value of limit register. Figure 26 shows periodic mode timing diagram.

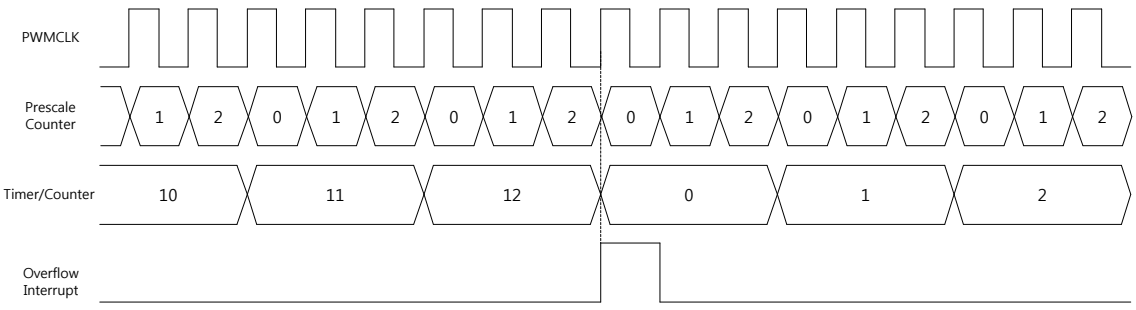


Figure 26 Periodic mode

In one-shot mode, the Timer /Counter reset to the initial value and then stops when the Timer/Counter reaches the value of limit register. Figure 27 shows one-shot mode timing diagram.

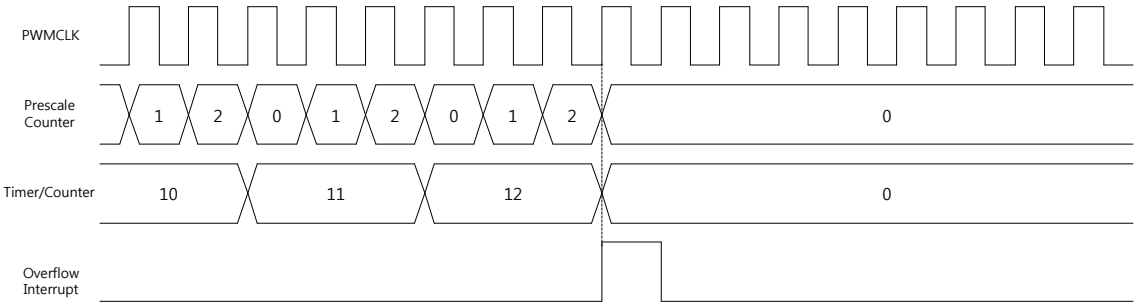


Figure 27 one-shot mode

Counting mode

The Timer/Counter has two counting mode: Up-count and Down-count mode. In up-count mode, the Timer/Counter counts up from 0 to the limit register value, then recycles. If repetition mode is periodic, the Timer/Counter restarts, if repetition mode is one-shot mode, the Timer/Counter stops. Figure 28 shows up-count mode timing diagram.

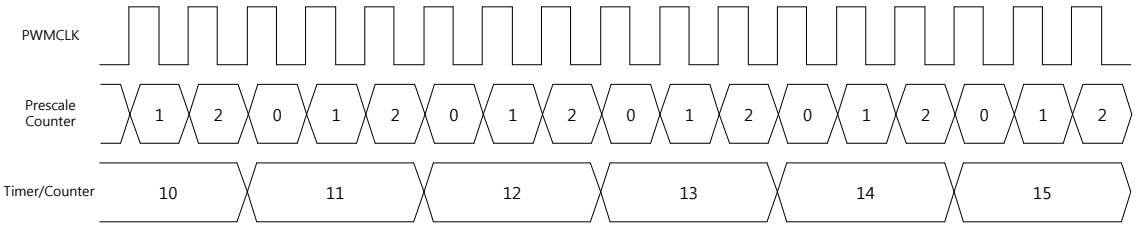


Figure 28 Up-count mode

In Down-count mode, the Timer/Counter counts from 0xFFFF_FFFF, then recycles. If repetition mode is periodic, the Timer/Counter restarts, if repetition mode is one-shot mode, the Timer/Counter stops. Figure 29 shows down-count mode timing diagram.

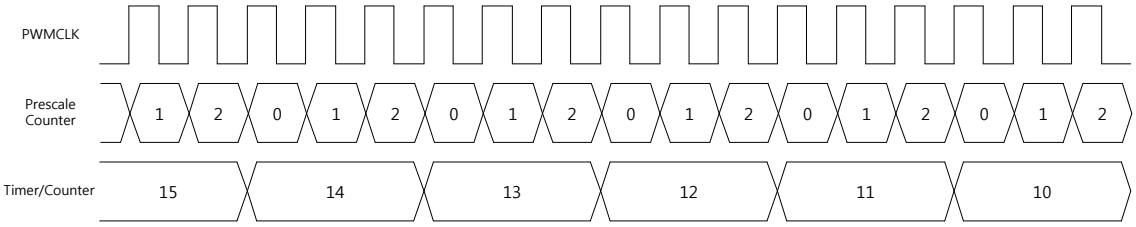


Figure 29 Down-count mode

Timer and Counter mode

The Timer/Counter can run in timer mode or counter mode. In timer mode, the Timer/Counter is counted by PWMCLK after Prescale counter is overflowed. If prescale is set by 0, the Timer/Counter counts every PWMCLK period. In counter mode, the Timer/Counter is counted by external input signal. There are three counting method: rising edge, falling edge, and both edge. The counter mode has up-count or down-count mode and also has periodic or one-shot mode. The external input pin and PWM output pin are the same, so PWM output is disabled in counter mode.

Figure 30 is counter mode example with rising edge mode,
Figure 31 is with falling edge mode and
Figure 32 is with both rising and falling edge mode.

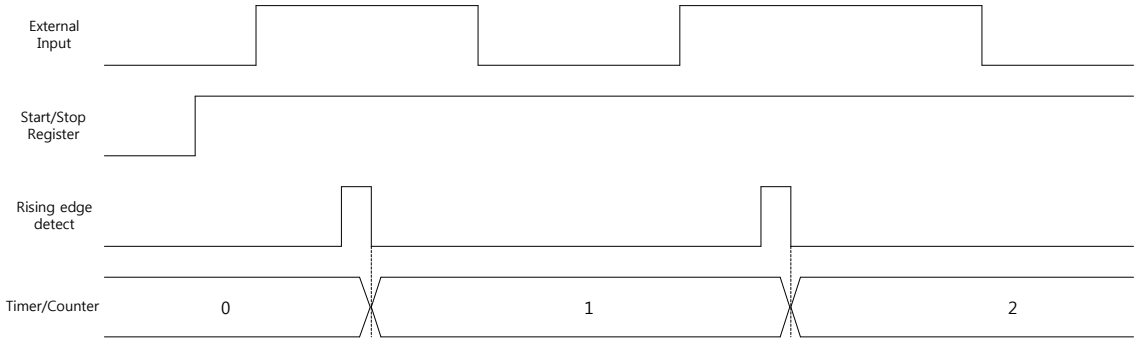


Figure 30 Counter mode with rising edge

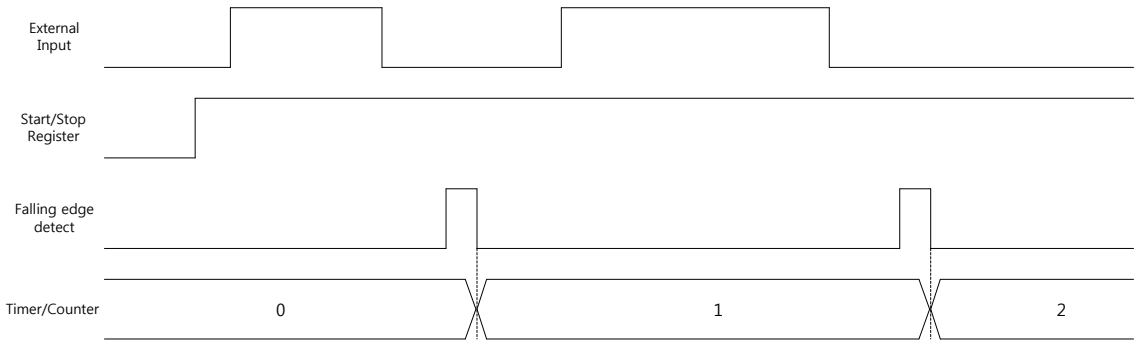


Figure 31 Counter mode with falling edge

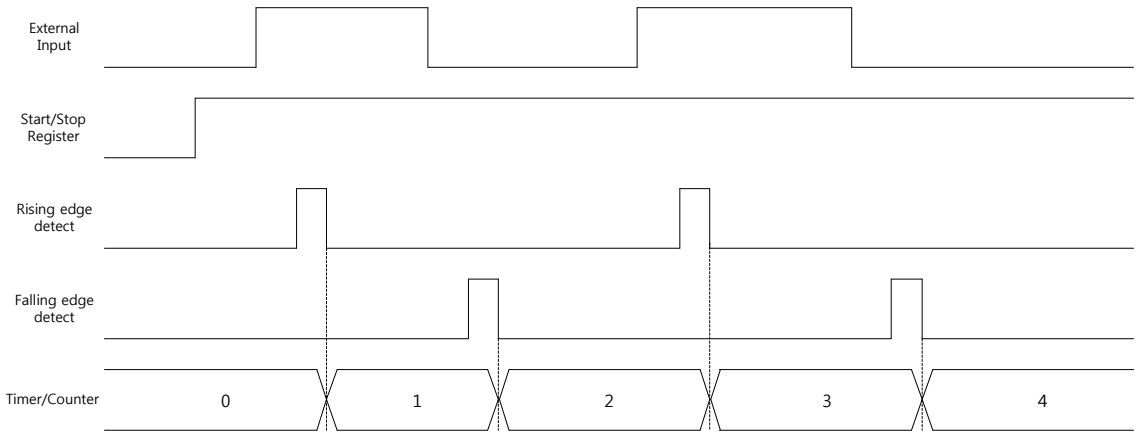


Figure 32 Counter mode with rising and falling edge

Prescaler description

The PWM has 6-bit prescale counter(PC) and the prescaler can divide the Timer/Counter clock frequency. Users can control it by Prescale Register(PR).

Figure 33 and Figure 34 shows some examples of the Timer/Counter timing with prescale register is 2, match register is 2, limit register is 12, timer mode, periodic mode, up-count mode, and no interrupt clear.

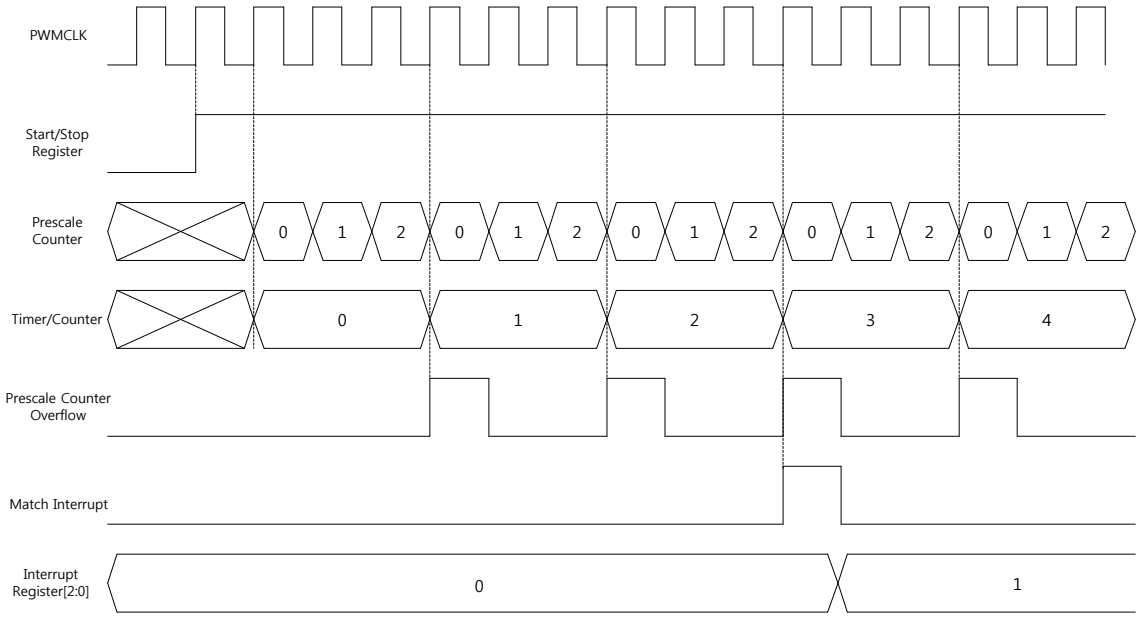


Figure 33 Timer/Counter timing diagram with match interrupt

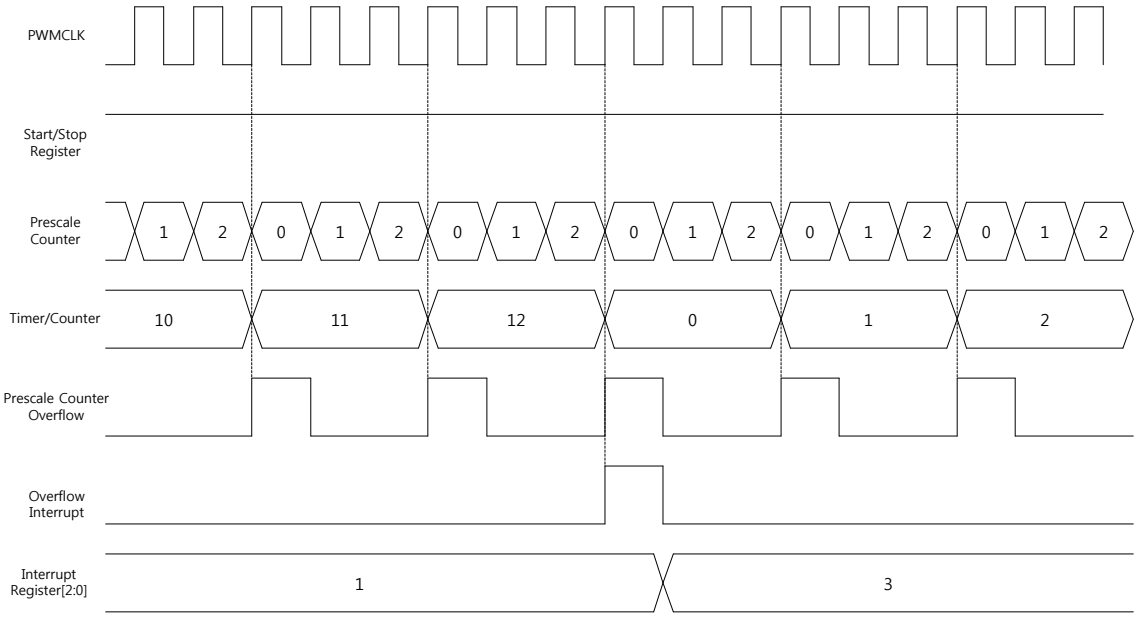


Figure 34 Timer/Counter timing diagram with overflow interrupt

18.3.3 PWM mode

Pulse Width Modulation mode generates a waveform with a period determined by the value of limit register and a duty cycle determined by the value of the match register.

The PWM output becomes always 1 when the Timer/Counter starts to count. Then the PWM output becomes 0 when the Timer/Counter reaches the value of match register. If the Timer/Counter is in periodic mode, the PWM output becomes 1 again when the Timer/Counter reaches the value of limit register. In one-shot mode, the PWM output does not change to 1 but stays 0 and the Timer/Counter stops.

The PWM mode can be selected independently on each channel(0~7) by PWM output enable and external input enable register. The external input pin and PWM output pin are the same, so external input is disabled in PWM mode.

Figure 35 is an example of the PWM output waveform when the Timer/Counter is reached to the value of match register.
Figure 36 is example of the PWM output waveform when to the Timer/Counter is reached to the value of limit register.

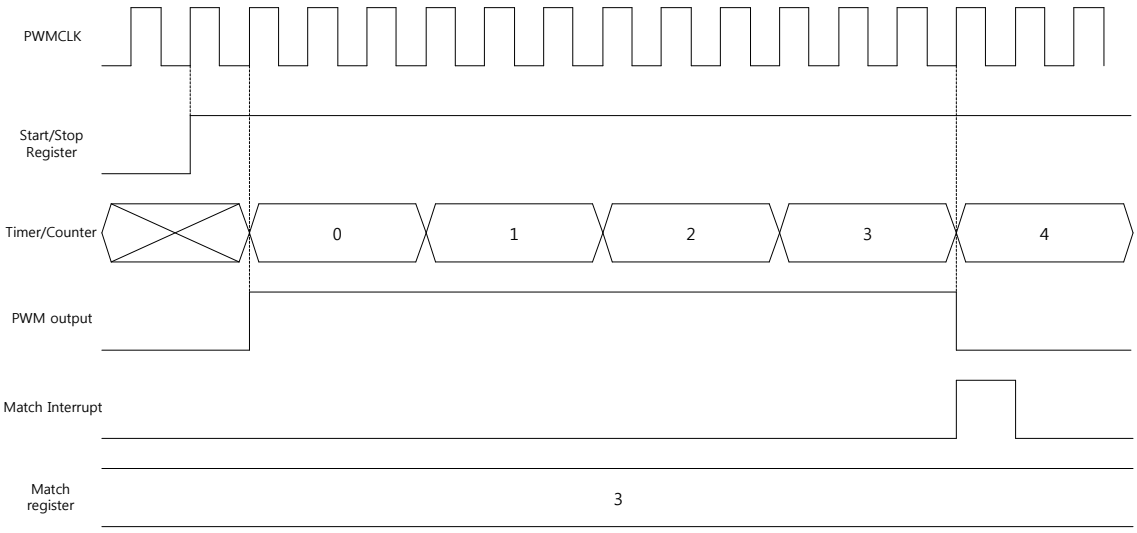


Figure 35 The PWM output up to match register

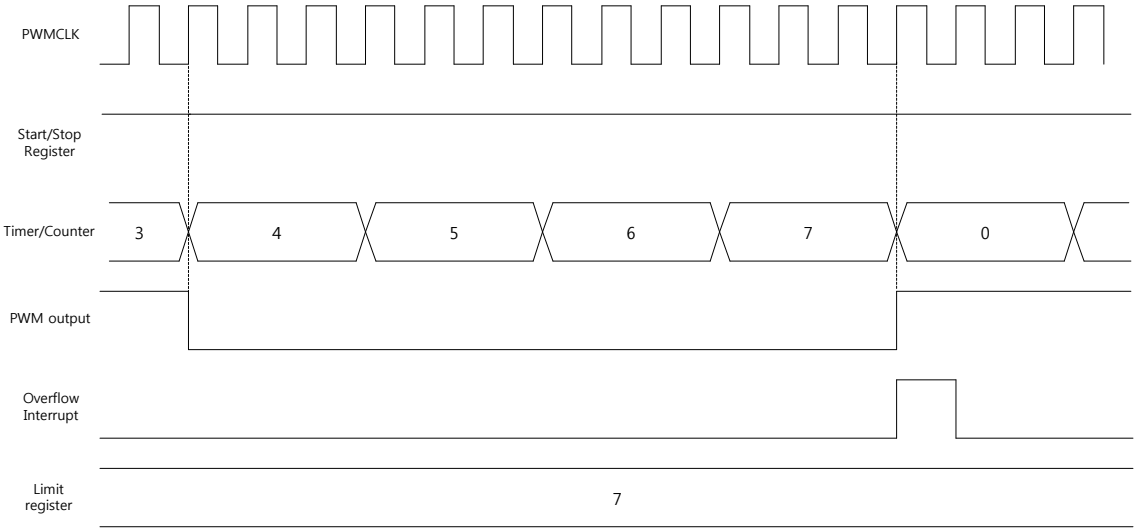


Figure 36 The PWM output up to limit register

If match register is set as 0, the PWM output will be 1 while the Timer/Counter is 0.

If the match register is bigger than the limit register, the PWM output is always 1.

18.3.4 Interrupt

The PWM has 8-bit interrupt enable register(IER) and each bit of IER corresponds to each interrupt of channel. Each PWM channel has Channel-n Interrupt Enable register(CHn_IER). The CHn_IER includes three types of interrupt: match, overflow, and capture. The match interrupt occurs when the Timer/Counter is reached to value of match register. The overflow interrupt occurs when the Timer/Counter is reached to value of limit register. The capture interrupt occurs when external input is entered for capture.

If interrupt occurs, corresponded bit of Channel-x interrupt register(CHn_IR) bit is set and PWM channel-n interrupt signal is generated. All CHn_IR is cleared by channel-n interrupt clear register(CHn_ICR) and then PWM channel-n interrupt signal is cleared.

18.3.5 Dead zone generation

Each PWM channel can output two complementary signals with dead zone time and it can be enabled by Channel-n Dead Zone Enable Register(CHn_DZER). Only 4 channels can be enabled because there are 8 PWM output pins. Channel 0 and 1 are a pair, channel 2 and 3 are a pair, channel 4 and 5 are a pair, and channel 6 and 7 are a pair. If users want to use channel-0 dead zone generation, channel-1 should be disabled. If channel 0 and 1 dead zone generation are enabled both, all outputs are 0. In that case, users should choose 1 channel.

Dead zone time are generated by the value of Channel-n Dead Zone Counter Register(DZCR). The dead zone counter counts up to value of DZCR. During the dead zone time, both complementary signals are both 0. Users have to adjust the signal depending on the devices that are connected to the outputs and their characteristics. If DZCR is bigger than the limit register, main output signal is toggled 0 to1 and then 1 to 0 while 1 PWMCLK and inverted output signal is always 0.

Figure 37 shows two complementary PWM outputs with dead zone time. During dead zone time, both outputs are 0. Figure 38 shows a more detailed timing with dead zone counter. The dead zone counter and the Timer/Counter starts to count together and PWM output is 0 until dead zone counter is reached to value of dead zone counter register. The PWM output becomes 1 and 0 when the Timer/Counter is reached to value of match register. The inverted PWM output is also 0 until dead zone counter is reached to value of dead zone counter register. Then inverted PWM output becomes 1 after dead zone counter is reached to the value of dead zone counter register.

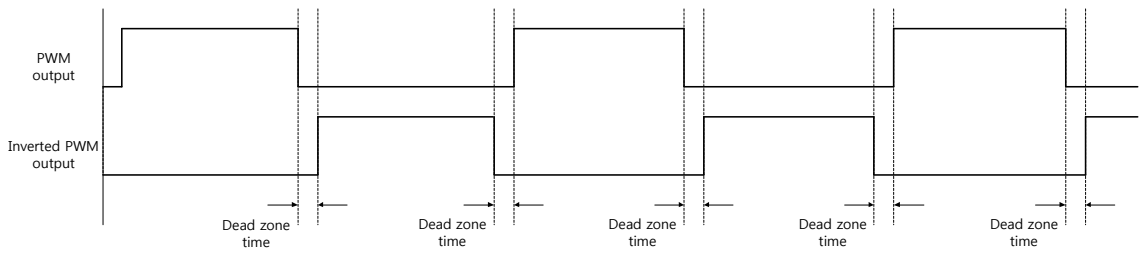


Figure 37 PWM waveform with dead zone time

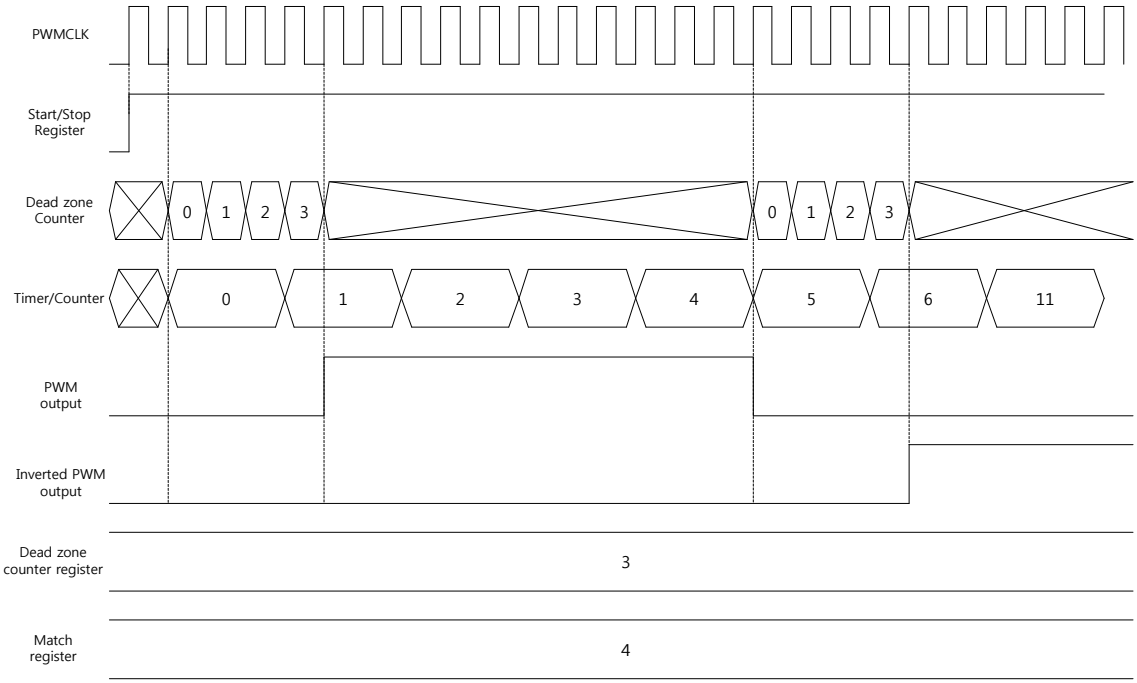


Figure 38 PWM waveform with dead zone counter

18.3.6 Capture event

Each PWM channel can capture its Timer/Counter value when an external input signal changes. Any channel could use any method of rising or falling edges. If capture interrupt is enabled, capture interrupt occurs when the external input signal is toggled. The Timer/Counter value is saved in Channel-n Capture Register(CHn_CR) and the capture register is not overwritten until capture interrupt is cleared. Figure 39 shows the capture event timing diagram. There is no interrupt clear, so second capture does not save during second rising edge detection.

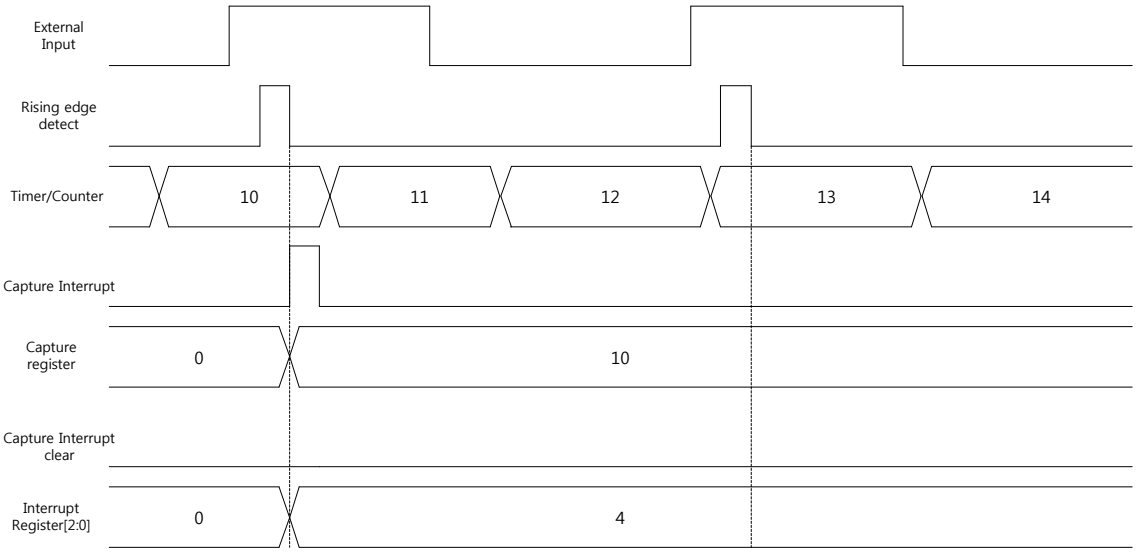


Figure 39 Capture event with no interrupt clear

Figure 40 shows, also, capture event timing diagram with interrupt clear. The second capture is saved at the second rising edge detection because there is interrupt clear.

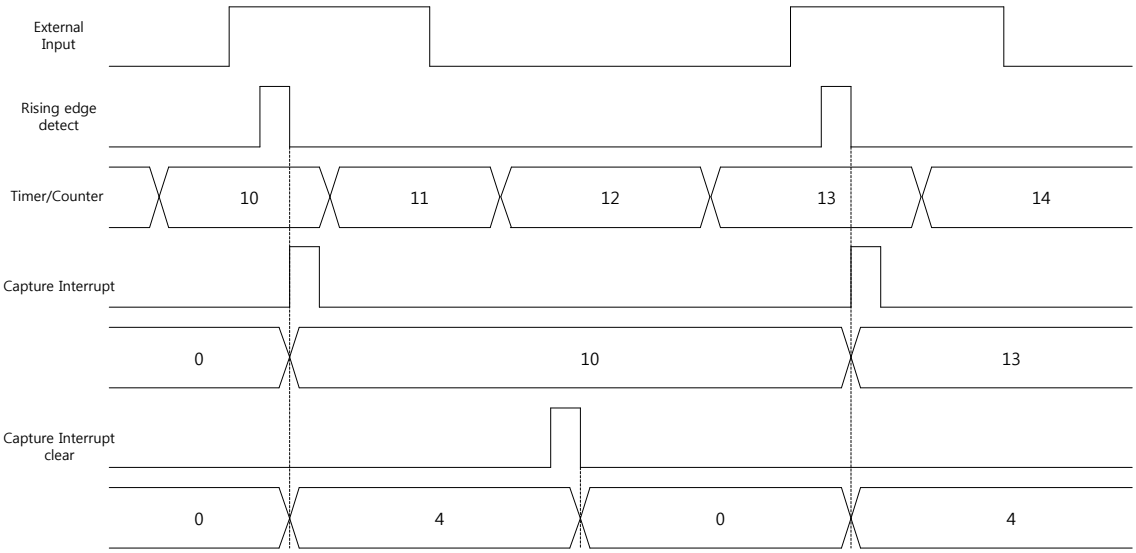


Figure 40 Capture event with interrupt clear

18.3.7 How to set the PWM

Figure 41 shows the PWM setting flow step by step.

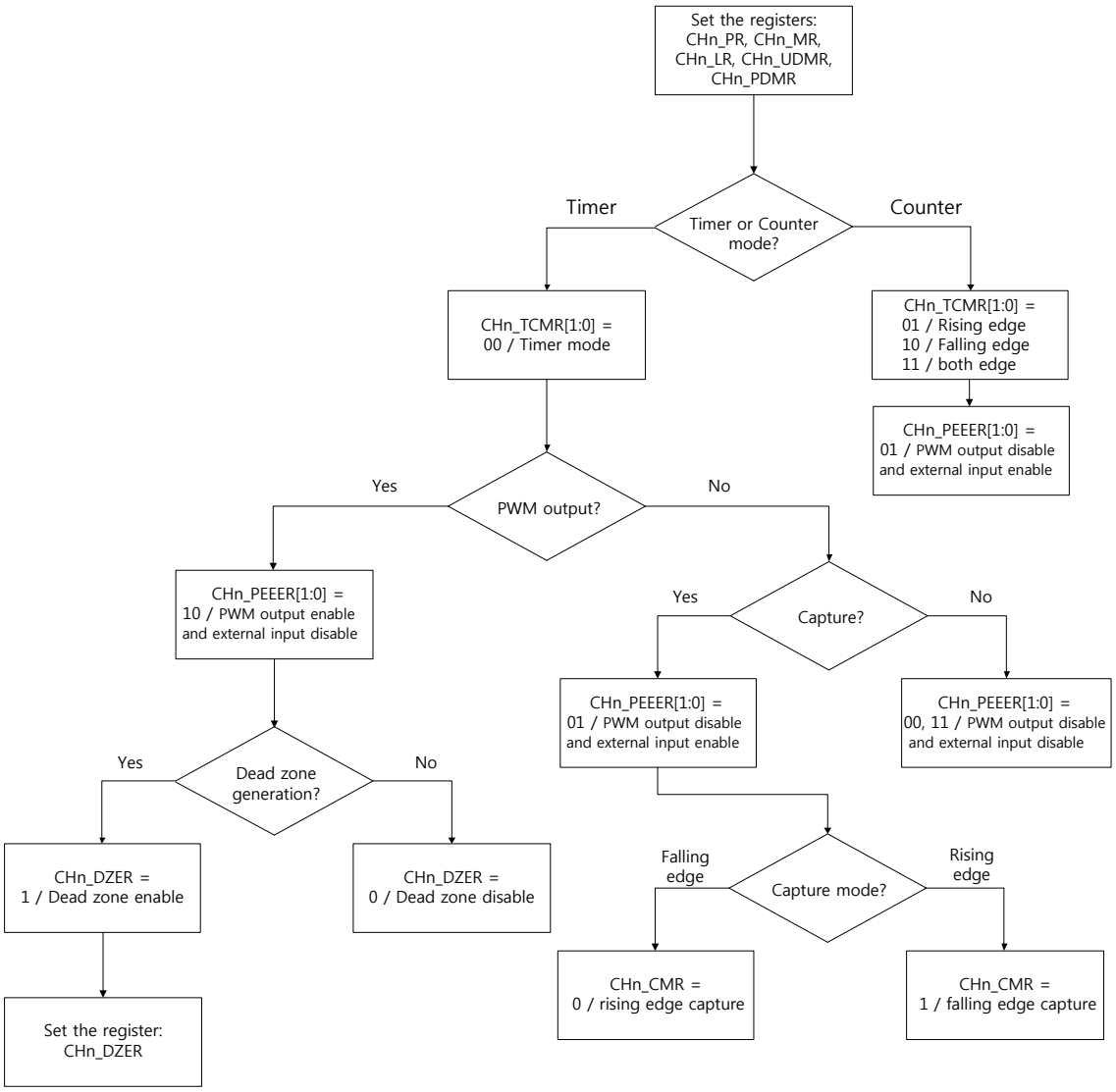


Figure 41 The PWM setting flow

18.4 PWM Channel-0 Registers (Base address : 0x4000_5000)

18.4.1 Channel-0 interrupt register(PWMCH0IR)

Base address : 0x4000_5000

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI
													R	R	R

[0] MI – Match Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Match interrupt does not occur.

1 : Match interrupt occurs.

[1] OI – Overflow Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Overflow interrupt does not occur.

1 : Overflow interrupt occurs.

[2] CI – Capture Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Capture interrupt does not occur.

1 : Capture interrupt occurs.

18.4.2 Channel-0 interrupt enable register(PWMCH0IER)

Base address : 0x4000_5000

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE
													R/W	R/W	R/W

[0] MIE – Match Interrupt Enabled.

0 : Match interrupt is not enabled.

1 : Match interrupt is enabled.

[1] OIE – Overflow Interrupt Enable.

0 : Overflow interrupt is not enabled.

1 : Overflow interrupt is enabled.

[2] CIE – Capture Interrupt Enable.

0 : Capture interrupt is not enabled.

1 : Capture interrupt is enabled.

18.4.3 Channel-0 interrupt clear register(PWMCH0ICR)

Base address : 0x4000_5000

Address offset : 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC
													W	W	W

This bit is set by software, cleared by hardware when a capture interrupt becomes 0.

[0] MIC – Match Interrupt

0 : No action.

1 : Match interrupt is cleared.

[1] OIC – Overflow Interrupt

0 : No action.

1 : Overflow Interrupt is cleared.

[2] CIC – Capture Interrupt Clear.

0 : No action.

1 : Capture Interrupt is cleared.

18.4.4 Channel-0 Timer/Counter Register (PWMCH0TCR)

Base address : 0x4000_5000

Address offset : 0x0C

Reset value : 0x0000_0000

31	0
TCR	
R	

[31:0] TCR – Timer/Counter register

Timer/Counter register. These register hold the current values of the Timer/Counter(TC). The TC is incremented every PR cycles. When the TC is reached to value of match register, the match interrupt is occurred and PWM output waveform becomes 0. When the TC is reached to the value of limit register, the overflow interrupt is occurred, the TC is reset as 0.

18.4.5 Channel-0 Prescale Counter Register (PWMCH0PCR)

Base address : 0x4000_5000

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PCR					
										R					

[5:0] PC – Prescale Counter register

Prescale Counter register. These registers hold the current values of prescale counter(PC). The PC is incremented to the value stored in PR. When the PC is reached to PR, the TC is incremented and the PC is reset as 0.

18.4.6 Channel-0 Prescale Register (PWMCH0PR)

Base address : 0x4000_5000

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PR					
										R/W					

[5 - 0] PR – Prescale Register

Prescale register. The PC is incremented when the PC is reached to the PR.

18.4.7 Channel-0 Match Register (PWMCH0MR)

Base address : 0x4000_5000

Address offset : 0x18

Reset value : 0x0000_0000

31	0
MR	
R/W	

[31:0] MR – Match Register

Match register. The MR can generate a match interrupt and PWM output waveform becomes 0 when the TC is reached to the MR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.4.8 Channel-0 Limit Register (PWMCH0LR)

Base address : 0x4000_5000

Address offset : 0x1C

Reset value : 0x0000_0000

31	0
LR	
R/W	

[31:0] LR – Limit Register

Limit Register. The LR can generate an overflow interrupt and PWM output waveform becomes 1 when the TC is reached to the LR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.4.9 Channel-0 Up-Down Mode Register (PWMCH0UDMR)

Base address : 0x4000_5000

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM
															R/W

[0] UDM – Up-Down mode

0 : TC runs up count.

1 : TC runs down count.

18.4.10 Channel-0 Timer/Counter Mode Register (PWMCH0TCMR)

Base address : 0x4000_5000

Address offset : 0x24

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM	
														R/W	

[1:0] TCM – Timer/Counter mode

00 : Timer mode.

01 : Counter mode with counting driven by rising edge external input .

10 : Counter mode with counting driven by falling edge external input.

11 : Counter mode with counting driven by rising and falling edge external input.

18.4.11 Channel-0 PWM output Enable and External input Enable Register (PWMCH0PEEER)

Base address : 0x4000_5000

Address offset : 0x28

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE	
														R/W	

[1:0] PEEE – PWM output Enable and External input Enable

00 : PWM output is disable and external input is disable.

01 : PWM output is disable and external input is enable.

10 : PWM output is enable and external input is disable.

18.4.12 Channel-0 Capture Mode Register (PWMCH0CMR)

Base address : 0x4000_5000

Address offset : 0x2C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM
															R/W

[0] CM – Capture mode

0 : Timer/Counter is captured when external input signal is rising edge.

1 : Timer/Counter is captured when external input signal is falling edge.

18.4.13 Channel-0 Capture Register (PWMCH0CR)

Base address : 0x4000_5000

Address offset : 0x30

Reset value : 0x0000_0000

31	0
CR	
R	

[31:0] CR – Capture Register

Capture register. The CR is loaded with the value of the TC when external input signal is triggered.

18.4.14 Channel-0 Periodic Mode Register (PWMCH0PDMR)

Base address : 0x4000_5000

Address offset : 0x34

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM

															R/W

[0] PDM – Periodic Mode

0 : Periodic mode. When the TC is reached to the LR, the TC returns to 0 and then continues counting periodically.

1 : One-shot mode. When the TC is reached to the LR, the TC returns to 0 and then stops counting.

18.4.15 Channel-0 Dead Zone Enable Register (PWMCH0DZER)

Base address : 0x4000_5000

Address offset : 0x38

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE
															R/W

[0] DZE – Dead Zone Enable

0 : Dead zone generation is disabled.

1 : Dead zone generation is enabled.

18.4.16 Channel-0 Dead Zone Counter Register (PWMCH0DZCR)

Base address : 0x4000_5000

Address offset : 0x3C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	DZC									
						R/W									

[9:0] DZC – Dead Zone Counter value

Dead zone generation counter value register. If the DZE bit in DZER is 1, dead zone counter counts to this value and during this time, the two PWM output waveforms are all 0.

18.5 Register map

The following Table 20 summarizes the PWM Channel-0 registers.

Table 20 PWM channel 0 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	PWMCH0IR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI	Channel-0 interrupt register
	reset value																														0	0	0	
0x04	PWMCH0IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE	Channel-0 interrupt enable register
	reset value																														0	0	0	
0x08	PWMCH0ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC	Channel-0 interrupt clear register
	reset value																																	Write only register
0x0C	PWMCH0TCR	TCR																																Channel-0 Timer/Counter Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	PWMCH0PCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PCR						Channel-0 Prescale Counter Register
	reset value																										0	0	0	0	0	0	0	
0x14	PWMCH0PR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PR						Channel-0 Prescale Register
	reset value																										0	0	0	0	0	0	0	
0x18	PWMCH0MR	MR																																Channel-0 Match Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x1C	PWMCH0LR	LR																																Channel-0 Limit Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x20	PWMCH0UDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM	Channel-0 Up-Down Mode Register
	reset value																																0	
0x24	PWMCH0TCMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM		Channel-0 Timer/Counter Mode Register
	reset value																															0	0	
0x28	PWMCH0PEEER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE		Channel-0 PWM output Enable and External input Enable Register
	reset value																															0	0	
0x2C	PWMCH0CMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM	Channel-0 Capture Mode Register
	reset value																																0	
0x30	PWMCH0CR	CR																																Channel-0 Capture Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	PWMCH0PDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM	Channel-0 Periodic Mode Register
	reset value																																0	
0x38	PWMCH0DZER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE	Channel-0 Dead Zone Enable Register
	reset value																																0	
0x3C	PWMCH0DZCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZC										Channel-0 Dead Zone Counter Register
	reset value																							0	0	0	0	0	0	0	0	0	0	

18.6 PWM Channel-1 Registers (Base address : 0x4000_5100)

18.6.1 Channel-1 interrupt register(PWMCH1IR)

Base address : 0x4000_5100

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI
													R	R	R

[0] MI – Match Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Match interrupt does not occur.

1 : Match interrupt occurs.

[1] OI – Overflow Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Overflow interrupt does not occur.

1 : Overflow interrupt occurs.

[2] CI – Capture Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Capture interrupt does not occur.

1 : Capture interrupt occurs.

18.6.2 Channel-1 interrupt enable register(PWMCH1IER)

Base address : 0x4000_5100

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE
													R/W	R/W	R/W

[0] MIE – Match Interrupt Enabled.

0 : Match interrupt is not enabled.

1 : Match interrupt is enabled.

[1] OIE – Overflow Interrupt Enable.

0 : Overflow interrupt is not enabled.

1 : Overflow interrupt is enabled.

[2] CIE – Capture Interrupt Enable.

0 : Capture interrupt is not enabled.

1 : Capture interrupt is enabled.

18.6.3 Channel-1 interrupt clear register(PWMCH1ICR)

Base address : 0x4000_5100

Address offset : 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC
													W	W	W

This bit is set by software, cleared by hardware when a capture interrupt becomes 0.

[0] MIC – Match Interrupt

0 : No action.

1 : Match interrupt is cleared.

[1] OIC – Overflow Interrupt

0 : No action.

1 : Overflow Interrupt is cleared.

[2] CIC – Capture Interrupt Clear.

0 : No action.

1 : Capture Interrupt is cleared.

18.6.4 Channel-1 Timer/Counter Register (PWMCH1TCR)

Base address : 0x4000_5100

Address offset : 0x0C

Reset value : 0x0000_0000

31	0
TCR	
R	

[31:0] TCR – Timer/Counter register

Timer/Counter register. These register hold the current values of the Timer/Counter(TC). The TC is incremented every PR cycles. When the TC is reached to value of match register, the match interrupt is occurred and PWM output waveform becomes 0. When the TC is reached to the value of limit register, the overflow interrupt is occurred, the TC is reset as 0.

18.6.5 Channel-1 Prescale Counter Register (PWMCH1PCR)

Base address : 0x4000_5100

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PCR					
										R					

[5:0] PC – Prescale Counter register

Prescale Counter register. These registers hold the current values of prescale counter(PC). The PC is incremented to the value stored in PR. When the PC is reached to PR, the TC is incremented and the PC is reset as 0.

18.6.6 Channel-1 Prescale Register (PWMCH1PR)

Base address : 0x4000_5100

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PR					
										R/W					

[5: 0] PR – Prescale Register

Prescale register. The PC is incremented when the PC is reached to the PR.

18.6.7 Channel-1 Match Register (PWMCH1MR)

Base address : 0x4000_5100

Address offset : 0x18

Reset value : 0x0000_0000

31	0
MR	
R/W	

[31:0] MR – Match Register

Match register. The MR can generate a match interrupt and PWM output waveform becomes 0 when the TC is reached to the MR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.6.8 Channel-1 Limit Register (PWMCH1LR)

Base address : 0x4000_5100

Address offset : 0x1C

Reset value : 0x0000_0000

31	0
LR	
R/W	

[31:0] LR – Limit Register

Limit Register. The LR can generate an overflow interrupt and PWM output waveform becomes 1 when the TC is reached to the LR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.6.9 Channel-1 Up-Down Mode Register (PWMCH1UDMR)

Base address : 0x4000_5100

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM
															R/W

[0] UDM – Up-Down mode

0 : TC runs up count.

1 : TC runs down count.

18.6.10 Channel-1 Timer/Counter Mode Register (PWMCH1TCMR)

Base address : 0x4000_5100

Address offset : 0x24

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM	
														R/W	

[1:0] TCM – Timer/Counter mode

00 : Timer mode.

01 : Counter mode with counting driven by rising edge external input .

10 : Counter mode with counting driven by falling edge external input.

11 : Counter mode with counting driven by rising and falling edge external input.

18.6.11 Channel-1 PWM output Enable and External input Enable Register (PWMCH1PEEER)

Base address : 0x4000_5100

Address offset : 0x28

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE	
														R/W	

[1:0] PEEE – PWM output Enable and External input Enable

00 : PWM output is disable and external input is disable.

01 : PWM output is disable and external input is enable.

10 : PWM output is enable and external input is disable.

18.6.12 Channel-1 Capture Mode Register (PWMCH1CMR)

Base address : 0x4000_5100

Address offset : 0x2C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM
															R/W

[0] CM – Capture mode

0 : Timer/Counter is captured when external input signal is rising edge.

1 : Timer/Counter is captured when external input signal is falling edge.

18.6.13 Channel-1 Capture Register (PWMCH1CR)

Base address : 0x4000_5100

Address offset : 0x30

Reset value : 0x0000_0000

31	0
CR	
R	

[31:0] CR – Capture Register

Capture register. The CR is loaded with the value of the TC when external input signal is triggered.

18.6.14 Channel-1 Periodic Mode Register (PWMCH1PDMR)

Base address : 0x4000_5100

Address offset : 0x34

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM

															R/W

[0] PDM – Periodic Mode

0 : Periodic mode. When the TC is reached to the LR, the TC returns to 0 and then continues counting periodically.

1 : One-shot mode. When the TC is reached to the LR, the TC returns to 0 and then stops counting.

18.6.15 Channel-1 Dead Zone Enable Register (PWMCH1DZER)

Base address : 0x4000_5100

Address offset : 0x38

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE
															R/W

[0] DZE – Dead Zone Enable

0 : Dead zone generation is disabled.

1 : Dead zone generation is enabled.

18.6.16 Channel-1 Dead Zone Counter Register (PWMCH1DZCR)

Base address : 0x4000_5100

Address offset : 0x3C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	DZC									
						R/W									

[9:0] DZC – Dead Zone Counter value

Dead zone generation counter value register. If the DZE bit in DZER is 1, dead zone counter counts to this value and during this time, the two PWM output waveforms are all 0.

18.7 Register map

The following Table 21 summarizes the PWM Channel-1 registers.

Table 21 PWM channel 1 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	PWMCH1IR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CI1	OI1	MI	Channel-1 interrupt register
	reset value																														0	0	0	
0x04	PWMCH1IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE	Channel-1 interrupt enable register
	reset value																														0	0	0	
0x08	PWMCH1ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC	Channel-1 interrupt clear register
	reset value																																	Write only register
0x0C	PWMCH1TCR	TCR																																Channel-1 Timer/Counter Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	PWMCH1PCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PCR						Channel-1 Prescale Counter Register
	reset value																										0	0	0	0	0	0		
0x14	PWMCH1PR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PR						Channel-1 Prescale Register
	reset value																										0	0	0	0	0	0		
0x18	PWMCH1MR	MR																																Channel-1 Match Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x1C	PWMCH1LR	LR																																Channel-1 Limit Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x20	PWMCH1UDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM	Channel-1 Up-Down Mode Register
	reset value																																0	
0x24	PWMCH1TCMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM		Channel-1 Timer/Counter Mode Register
	reset value																															0	0	
0x28	PWMCH1PEEER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE		Channel-1 PWM output Enable and External input Enable Register
	reset value																															0	0	
0x2C	PWMCH1CMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM	Channel-1 Capture Mode Register
	reset value																																0	
0x30	PWMCH1CR	CR																																Channel-1 Capture Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	PWMCH1PDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM	Channel-1 Periodic Mode Register
	reset value																																0	
0x38	PWMCH1DZER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE	Channel-1 Dead Zone Enable Register
	reset value																																0	
0x3C	PWMCH1DZCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZC										Channel-1 Dead Zone Counter Register
	reset value																							0	0	0	0	0	0	0	0	0	0	

18.8 PWM Channel-2 Registers (Base address : 0x4000_5200)

18.8.1 Channel-2 interrupt register(PWMCH2IR)

Base address : 0x4000_5200

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI
													R	R	R

[0] MI – Match Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Match interrupt does not occur.

1 : Match interrupt occurs.

[1] OI – Overflow Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Overflow interrupt does not occur.

1 : Overflow interrupt occurs.

[2] CI – Capture Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Capture interrupt does not occur.

1 : Capture interrupt occurs.

18.8.2 Channel-2 interrupt enable register(PWMCH2IER)

Base address : 0x4000_5200

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE
													R/W	R/W	R/W

[0] MIE – Match Interrupt Enabled.

0 : Match interrupt is not enabled.

1 : Match interrupt is enabled.

[1] OIE – Overflow Interrupt Enable.

0 : Overflow interrupt is not enabled.

1 : Overflow interrupt is enabled.

[2] CIE – Capture Interrupt Enable.

0 : Capture interrupt is not enabled.

1 : Capture interrupt is enabled.

18.8.3 Channel-2 interrupt clear register(PWMCH2ICR)

Base address : 0x4000_5200

Address offset : 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC
													W	W	W

This bit is set by software, cleared by hardware when a capture interrupt becomes 0.

[0] MIC – Match Interrupt

0 : No action.

1 : Match interrupt is cleared.

[1] OIC – Overflow Interrupt

0 : No action.

1 : Overflow Interrupt is cleared.

[2] CIC – Capture Interrupt Clear.

0 : No action.

1 : Capture Interrupt is cleared.

18.8.4 Channel-2 Timer/Counter Register (PWMCH2TCR)

Base address : 0x4000_5200

Address offset : 0x0C

Reset value : 0x0000_0000

31	0
TCR	
R	

[31:0] TCR – Timer/Counter register

Timer/Counter register. These register hold the current values of the Timer/Counter(TC). The TC is incremented every PR cycles. When the TC is reached to value of match register, the match interrupt is occurred and PWM output waveform becomes 0. When the TC is reached to the value of limit register, the overflow interrupt is occurred, the TC is reset as 0.

18.8.5 Channel-2 Prescale Counter Register (PWMCH2PCR)

Base address : 0x4000_5200

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PCR					
										R					

[5:0] PC – Prescale Counter register

Prescale Counter register. These registers hold the current values of prescale counter(PC). The PC is incremented to the value stored in PR. When the PC is reached to PR, the TC is incremented and the PC is reset as 0.

18.8.6 Channel-2 Prescale Register (PWMCH2PR)

Base address : 0x4000_5200

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PR					
										R/W					

[5: 0] PR – Prescale Register

Prescale register. The PC is incremented when the PC is reached to the PR.

18.8.7 Channel-2 Match Register (PWMCH2MR)

Base address : 0x4000_5200

Address offset : 0x18

Reset value : 0x0000_0000

31	0
MR	
R/W	

[31:0] MR – Match Register

Match register. The MR can generate a match interrupt and PWM output waveform becomes 0 when the TC is reached to the MR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.8.8 Channel-2 Limit Register (PWMCH2LR)

Base address : 0x4000_5200

Address offset : 0x1C

Reset value : 0x0000_0000

31	0
LR	
R/W	

[31:0] LR – Limit Register

Limit Register. The LR can generate an overflow interrupt and PWM output waveform becomes 1 when the TC is reached to the LR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.8.9 Channel-2 Up-Down Mode Register (PWMCH2UDMR)

Base address : 0x4000_5200

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM
															R/W

[0] UDM – Up-Down mode

0 : TC runs up count.

1 : TC runs down count.

18.8.10 Channel-2 Timer/Counter Mode Register (PWMCH2TCMR)

Base address : 0x4000_5200

Address offset : 0x24

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM	
														R/W	

[1:0] TCM – Timer/Counter mode

00 : Timer mode.

01 : Counter mode with counting driven by rising edge external input .

10 : Counter mode with counting driven by falling edge external input.

11 : Counter mode with counting driven by rising and falling edge external input.

18.8.11 Channel-2 PWM output Enable and External input Enable Register (PWMCH2PEEER)

Base address : 0x4000_5200

Address offset : 0x28

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE	
														R/W	

[1:0] PEEE – PWM output Enable and External input Enable

00 : PWM output is disable and external input is disable.

01 : PWM output is disable and external input is enable.

10 : PWM output is enable and external input is disable.

18.8.12 Channel-2 Capture Mode Register (PWMCH2CMR)

Base address : 0x4000_5200

Address offset : 0x2C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM
															R/W

[0] CM – Capture mode

0 : Timer/Counter is captured when external input signal is rising edge.

1 : Timer/Counter is captured when external input signal is falling edge.

18.8.13 Channel-2 Capture Register (PWMCH2CR)

Base address : 0x4000_5200

Address offset : 0x30

Reset value : 0x0000_0000

31	0
CR	
R	

[31:0] CR – Capture Register

Capture register. The CR is loaded with the value of the TC when external input signal is triggered.

18.8.14 Channel-2 Periodic Mode Register (PWMCH2PDMR)

Base address : 0x4000_5200

Address offset : 0x34

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM

															R/W

[0] PDM – Periodic Mode

0 : Periodic mode. When the TC is reached to the LR, the TC returns to 0 and then continues counting periodically.

1 : One-shot mode. When the TC is reached to the LR, the TC returns to 0 and then stops counting.

18.8.15 Channel-2 Dead Zone Enable Register (PWMCH2DZER)

Base address : 0x4000_5200

Address offset : 0x38

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE
															R/W

[0] DZE – Dead Zone Enable

0 : Dead zone generation is disabled.

1 : Dead zone generation is enabled.

18.8.16 Channel-2 Dead Zone Counter Register (PWMCH2DZCR)

Base address : 0x4000_5200

Address offset : 0x3C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	DZC									
						R/W									

[9:0] DZC – Dead Zone Counter value

Dead zone generation counter value register. If the DZE bit in DZER is 1, dead zone counter counts to this value and during this time, the two PWM output waveforms are all 0.

18.9 Register map

The following Table 22 summarizes the PWM Channel-2 registers.

Table 22 PWM channel 2 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	특징
0x00	PWMCH2IR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI	Channel-2 interrupt register
	reset value																														0	0	0	
0x04	PWMCH2IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE	Channel-2 interrupt enable register
	reset value																														0	0	0	
0x08	PWMCH2ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC	Channel-2 interrupt clear register
	reset value																																	Write only register
0x0C	PWMCH2TCR	TCR																																Channel-2 Timer/Counter Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	PWMCH2PCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PCR						Channel-2 Prescale Counter Register
	reset value																										0	0	0	0	0	0	0	
0x14	PWMCH2PR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PR						Channel-2 Prescale Register
	reset value																										0	0	0	0	0	0	0	
0x18	PWMCH2MR	MR																																Channel-2 Match Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x1C	PWMCH2LR	LR																																Channel-2 Limit Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x20	PWMCH2UDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM	Channel-2 Up-Down Mode Register
	reset value																																0	
0x24	PWMCH2TCMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM		Channel-2 Timer/Counter Mode Register
	reset value																															0	0	
0x28	PWMCH2PEEER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE		Channel-2 PWM output Enable and External input Enable Register
	reset value																															0	0	
0x2C	PWMCH2CMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM	Channel-2 Capture Mode Register
	reset value																																0	
0x30	PWMCH2CR	CR																																Channel-2 Capture Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	PWMCH2PDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM	Channel-2 Periodic Mode Register
	reset value																																0	
0x38	PWMCH2DZER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE	Channel-2 Dead Zone Enable Register
	reset value																																0	
0x3C	PWMCH2DZCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZC										Channel-2 Dead Zone Counter Register
	reset value																							0	0	0	0	0	0	0	0	0	0	

18.10 PWM Channel-3 Registers (Base address : 0x4000_5300)

18.10.1 Channel-3 interrupt register(PWMCH3IR)

Base address : 0x4000_5300

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI
													R	R	R

[0] MI – Match Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Match interrupt does not occur.

1 : Match interrupt occurs.

[1] OI – Overflow Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Overflow interrupt does not occur.

1 : Overflow interrupt occurs.

[2] CI – Capture Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Capture interrupt does not occur.

1 : Capture interrupt occurs.

18.10.2 Channel-3 interrupt enable register(PWMCH3IER)

Base address : 0x4000_5300

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE
													R/W	R/W	R/W

[0] MIE – Match Interrupt Enabled.

0 : Match interrupt is not enabled.

1 : Match interrupt is enabled.

[1] OIE – Overflow Interrupt Enable.

0 : Overflow interrupt is not enabled.

1 : Overflow interrupt is enabled.

[2] CIE – Capture Interrupt Enable.

0 : Capture interrupt is not enabled.

1 : Capture interrupt is enabled.

18.10.3 Channel-3 interrupt clear register(PWMCH3ICR)

Base address : 0x4000_5300

Address offset : 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC
													W	W	W

This bit is set by software, cleared by hardware when a capture interrupt becomes 0.

[0] MIC – Match Interrupt

0 : No action.

1 : Match interrupt is cleared.

[1] OIC – Overflow Interrupt

0 : No action.

1 : Overflow Interrupt is cleared.

[2] CIC – Capture Interrupt Clear.

0 : No action.

1 : Capture Interrupt is cleared.

18.10.4 Channel-3 Timer/Counter Register (PWMCH3TCR)

Base address : 0x4000_5300

Address offset : 0x0C

Reset value : 0x0000_0000

31	0
TCR	
R	

[31:0] TCR – Timer/Counter register

Timer/Counter register. These register hold the current values of the Timer/Counter(TC). The TC is incremented every PR cycles. When the TC is reached to value of match register, the match interrupt is occurred and PWM output waveform becomes 0. When the TC is reached to the value of limit register, the overflow interrupt is occurred, the TC is reset as 0.

18.10.5 Channel-3 Prescale Counter Register (PWMCH3PCR)

Base address : 0x4000_5300

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PCR					
										R					

[5:0] PC – Prescale Counter register

Prescale Counter register. These registers hold the current values of prescale counter(PC). The PC is incremented to the value stored in PR. When the PC is reached to PR, the TC is incremented and the PC is reset as 0.

18.10.6 Channel-3 Prescale Register (PWMCH3PR)

Base address : 0x4000_5300

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PR					
										R/W					

[5: 0] PR – Prescale Register

Prescale register. The PC is incremented when the PC is reached to the PR.

18.10.7 Channel-3 Match Register (PWMCH3MR)

Base address : 0x4000_5300

Address offset : 0x18

Reset value : 0x0000_0000

31	0
MR	
R/W	

[31:0] MR – Match Register

Match register. The MR can generate a match interrupt and PWM output waveform becomes 0 when the TC is reached to the MR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.10.8 Channel-3 Limit Register (PWMCH3LR)

Base address : 0x4000_5300

Address offset : 0x1C

Reset value : 0x0000_0000

31	0
LR	
R/W	

[31:0] LR – Limit Register

Limit Register. The LR can generate an overflow interrupt and PWM output waveform becomes 1 when the TC is reached to the LR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.10.9 Channel-3 Up-Down Mode Register (PWMCH3UDMR)

Base address : 0x4000_5300

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM

															R/W

[0] UDM – Up-Down mode

0 : TC runs up count.

1 : TC runs down count.

18.10.10 Channel-3 Timer/Counter Mode Register (PWMCH3TCMR)

Base address : 0x4000_5300

Address offset : 0x24

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM	
														R/W	

[1:0] TCM – Timer/Counter mode

00 : Timer mode.

01 : Counter mode with counting driven by rising edge external input .

10 : Counter mode with counting driven by falling edge external input.

11 : Counter mode with counting driven by rising and falling edge external input.

18.10.11 Channel-3 PWM output Enable and External input Enable Register (PWMCH3PEEER)

Base address : 0x4000_5300

Address offset : 0x28

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE	
														R/W	

[1:0] PEEE – PWM output Enable and External input Enable

00 : PWM output is disable and external input is disable.

01 : PWM output is disable and external input is enable.

10 : PWM output is enable and external input is disable.

18.10.12 Channel-3 Capture Mode Register (PWMCH3CMR)

Base address : 0x4000_5300

Address offset : 0x2C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM
															R/W

[0] CM – Capture mode

0 : Timer/Counter is captured when external input signal is rising edge.

1 : Timer/Counter is captured when external input signal is falling edge.

18.10.13 Channel-3 Capture Register (PWMCH3CR)

Base address : 0x4000_5300

Address offset : 0x30

Reset value : 0x0000_0000

31	0
CR	
R	

[31:0] CR – Capture Register

Capture register. The CR is loaded with the value of the TC when external input signal is triggered.

18.10.14 Channel-3 Periodic Mode Register (PWMCH3PDMR)

Base address : 0x4000_5300

Address offset : 0x34

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM
															R/W

[0] PDM – Periodic Mode

0 : Periodic mode. When the TC is reached to the LR, the TC returns to 0 and then continues counting periodically.

1 : One-shot mode. When the TC is reached to the LR, the TC returns to 0 and then stops counting.

18.10.15 Channel-3 Dead Zone Enable Register (PWMCH3DZER)

Base address : 0x4000_5300

Address offset : 0x38

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE
															R/W

[0] DZE – Dead Zone Enable

0 : Dead zone generation is disabled.

1 : Dead zone generation is enabled.

18.10.16 Channel-3 Dead Zone Counter Register (PWMCH3DZCR)

Base address : 0x4000_5300

Address offset : 0x3C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	DZC									
						R/W									

[9:0] DZC – Dead Zone Counter value

Dead zone generation counter value register. If the DZE bit in DZER is 1, dead zone counter counts to this value and during this time, the two PWM output waveforms are all 0.

18.11 Register map

The following Table 23 summarizes the PWM Channel-3 registers.

Table 23 PWM channel 3 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	PWMCH3IR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI	Channel-3 interrupt register
	reset value																														0	0	0	
0x04	PWMCH3IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE	Channel-3 interrupt enable register
	reset value																														0	0	0	
0x08	PWMCH3ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC	Channel-3 interrupt clear register
	reset value																																	Write only register
0x0C	PWMCH3TCR	TCR																																Channel-3 Timer/Counter Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	PWMCH3PCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PCR						Channel-3 Prescale Counter Register
	reset value																											0	0	0	0	0	0	
0x14	PWMCH3PR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PR						Channel-3 Prescale Register
	reset value																											0	0	0	0	0	0	
0x18	PWMCH3MR	MR																																Channel-3 Match Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x1C	PWMCH3LR	LR																																Channel-3 Limit Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x20	PWMCH3UDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM	Channel-3 Up-Down Mode Register
	reset value																																0	
0x24	PWMCH3TCMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM		Channel-3 Timer/Counter Mode Register
	reset value																															0	0	
0x28	PWMCH3PEEER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE		Channel-3 PWM output Enable and External input Enable Register
	reset value																															0	0	
0x2C	PWMCH3CMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM	Channel-3 Capture Mode Register
	reset value																																0	
0x30	PWMCH3CR	CR																																Channel-3 Capture Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	PWMCH3PDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM	Channel-3 Periodic Mode Register
	reset value																																0	
0x38	PWMCH3DZER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE	Channel-3 Dead Zone Enable Register
	reset value																																0	
0x3C	PWMCH3DZCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZC										Channel-3 Dead Zone Counter Register
	reset value																							0	0	0	0	0	0	0	0	0	0	

18.12 PWM Channel-4 Registers (Base address : 0x4000_5400)

18.12.1 Channel-4 interrupt register(PWMCH4IR)

Base address : 0x4000_5400

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI
													R	R	R

[0] MI – Match Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Match interrupt does not occur.

1 : Match interrupt occurs.

[1] OI – Overflow Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Overflow interrupt does not occur.

1 : Overflow interrupt occurs.

[2] CI – Capture Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Capture interrupt does not occur.

1 : Capture interrupt occurs.

18.12.2 Channel-4 interrupt enable register(PWMCH4IER)

Base address : 0x4000_5400

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE
													R/W	R/W	R/W

[0] MIE – Match Interrupt Enabled.

0 : Match interrupt is not enabled.

1 : Match interrupt is enabled.

[1] OIE – Overflow Interrupt Enable.

0 : Overflow interrupt is not enabled.

1 : Overflow interrupt is enabled.

[2] CIE – Capture Interrupt Enable.

0 : Capture interrupt is not enabled.

1 : Capture interrupt is enabled.

18.12.3 Channel-4 interrupt clear register(PWMCH4ICR)

Base address : 0x4000_5400

Address offset : 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC
													W	W	W

This bit is set by software, cleared by hardware when a capture interrupt becomes 0.

[0] MIC – Match Interrupt

0 : No action.

1 : Match interrupt is cleared.

[1] OIC – Overflow Interrupt

0 : No action.

1 : Overflow Interrupt is cleared.

[2] CIC – Capture Interrupt Clear.

0 : No action.

1 : Capture Interrupt is cleared.

18.12.4 Channel-4 Timer/Counter Register (PWMCH4TCR)

Base address : 0x4000_5400

Address offset : 0x0C

Reset value : 0x0000_0000

31	0
TCR	
R	

[31:0] TCR – Timer/Counter register

Timer/Counter register. These register hold the current values of the Timer/Counter(TC). The TC is incremented every PR cycles. When the TC is reached to value of match register, the match interrupt is occurred and PWM output waveform becomes 0. When the TC is reached to the value of limit register, the overflow interrupt is occurred, the TC is reset as 0.

18.12.5 Channel-4 Prescale Counter Register (PWMCH4PCR)

Base address : 0x4000_5400

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PCR					
										R					

[5:0] PC – Prescale Counter register

Prescale Counter register. These registers hold the current values of prescale counter(PC). The PC is incremented to the value stored in PR. When the PC is reached to PR, the TC is incremented and the PC is reset as 0.

18.12.6 Channel-4 Prescale Register (PWMCH4PR)

Base address : 0x4000_5400

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PR					
										R/W					

[5: 0] PR – Prescale Register

Prescale register. The PC is incremented when the PC is reached to the PR.

18.12.7 Channel-4 Match Register (PWMCH4MR)

Base address : 0x4000_5400

Address offset : 0x18

Reset value : 0x0000_0000

31	0
MR	
R/W	

[31:0] MR – Match Register

Match register. The MR can generate a match interrupt and PWM output waveform becomes 0 when the TC is reached to the MR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.12.8 Channel-4 Limit Register (PWMCH4LR)

Base address : 0x4000_5400

Address offset : 0x1C

Reset value : 0x0000_0000

31	0
LR	
R/W	

[31:0] LR – Limit Register

Limit Register. The LR can generate an overflow interrupt and PWM output waveform becomes 1 when the TC is reached to the LR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.12.9 Channel-4 Up-Down Mode Register (PWMCH4UDMR)

Base address : 0x4000_5400

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM
															R/W

[0] UDM – Up-Down mode

0 : TC runs up count.

1 : TC runs down count.

18.12.10 Channel-4 Timer/Counter Mode Register (PWMCH4TCMR)

Base address : 0x4000_5400

Address offset : 0x24

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM	
														R/W	

[1:0] TCM – Timer/Counter mode

00 : Timer mode.

01 : Counter mode with counting driven by rising edge external input .

10 : Counter mode with counting driven by falling edge external input.

11 : Counter mode with counting driven by rising and falling edge external input.

18.12.11 Channel-4 PWM output Enable and External input Enable Register (PWMCH4PEEER)

Base address : 0x4000_5400

Address offset : 0x28

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE	
														R/W	

[1:0] PEEE – PWM output Enable and External input Enable

00 : PWM output is disable and external input is disable.

01 : PWM output is disable and external input is enable.

10 : PWM output is enable and external input is disable.

18.12.12 Channel-4 Capture Mode Register (PWMCH4CMR)

Base address : 0x4000_5400

Address offset : 0x2C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM
															R/W

[0] CM – Capture mode

0 : Timer/Counter is captured when external input signal is rising edge.

1 : Timer/Counter is captured when external input signal is falling edge.

18.12.13 Channel-4 Capture Register (PWMCH4CR)

Base address : 0x4000_5400

Address offset : 0x30

Reset value : 0x0000_0000

31	0
CR	
R	

[31:0] CR – Capture Register

Capture register. The CR is loaded with the value of the TC when external input signal is triggered.

18.12.14 Channel-4 Periodic Mode Register (PWMCH4PDMR)

Base address : 0x4000_5400

Address offset : 0x34

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM
															R/W

[0] PDM – Periodic Mode

0 : Periodic mode. When the TC is reached to the LR, the TC returns to 0 and then continues counting periodically.

1 : One-shot mode. When the TC is reached to the LR, the TC returns to 0 and then stops counting.

18.12.15 Channel-4 Dead Zone Enable Register (PWMCH4DZER)

Base address : 0x4000_5400

Address offset : 0x38

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE
															R/W

[0] DZE – Dead Zone Enable

0 : Dead zone generation is disabled.

1 : Dead zone generation is enabled.

18.12.16 Channel-4 Dead Zone Counter Register (PWMCH4DZCR)

Base address : 0x4000_5400

Address offset : 0x3C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	DZC									
						R/W									

[9:0] DZC – Dead Zone Counter value

Dead zone generation counter value register. If the DZE bit in DZER is 1, dead zone counter counts to this value and during this time, the two PWM output waveforms are all 0.

18.13 Register map

The following Table 24 summarizes the PWM Channel-4 registers.

Table 24 PWM channel 4 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	PWMCH4IR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI	Channel-4 interrupt register
	reset value																														0	0	0	
0x04	PWMCH4IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE	Channel-4 interrupt enable register
	reset value																														0	0	0	
0x08	PWMCH4ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC	Channel-4 interrupt clear register
	reset value																																	Write only register
0x0C	PWMCH4TCR	TCR																																Channel-4 Timer/Counter Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	PWMCH4PCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PCR						Channel-4 Prescale Counter Register
	reset value																											0	0	0	0	0	0	
0x14	PWMCH4PR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PR						Channel-4 Prescale Register
	reset value																											0	0	0	0	0	0	
0x18	PWMCH4MR	MR																																Channel-4 Match Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x1C	PWMCH4LR	LR																																Channel-4 Limit Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x20	PWMCH4UDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM	Channel-4 Up-Down Mode Register
	reset value																																0	
0x24	PWMCH4TCMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM		Channel-4 Timer/Counter Mode Register
	reset value																															0	0	
0x28	PWMCH4PEEER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE		Channel-4 PWM output Enable and External input Enable Register
	reset value																															0	0	
0x2C	PWMCH4CMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM	Channel-4 Capture Mode Register
	reset value																																0	
0x30	PWMCH4CR	CR																																Channel-4 Capture Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	PWMCH4PDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM	Channel-4 Periodic Mode Register
	reset value																																0	
0x38	PWMCH4DZER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE	Channel-4 Dead Zone Enable Register
	reset value																																0	
0x3C	PWMCH4DZCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZC										Channel-4 Dead Zone Counter Register
	reset value																							0	0	0	0	0	0	0	0	0	0	

18.14 PWM Channel-5 Registers (Base address : 0x4000_5500)

18.14.1 Channel-5 interrupt register(PWMCH5IR)

Base address : 0x4000_5500

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI
													R	R	R

[0] MI – Match Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Match interrupt does not occur.

1 : Match interrupt occurs.

[1] OI – Overflow Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Overflow interrupt does not occur.

1 : Overflow interrupt occurs.

[2] CI – Capture Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Capture interrupt does not occur.

1 : Capture interrupt occurs.

18.14.2 Channel-5 interrupt enable register(PWMCH5IER)

Base address : 0x4000_5500

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE
													R/W	R/W	R/W

[0] MIE – Match Interrupt Enabled.

0 : Match interrupt is not enabled.

1 : Match interrupt is enabled.

[1] OIE – Overflow Interrupt Enable.

0 : Overflow interrupt is not enabled.

1 : Overflow interrupt is enabled.

[2] CIE – Capture Interrupt Enable.

0 : Capture interrupt is not enabled.

1 : Capture interrupt is enabled.

18.14.3 Channel-5 interrupt clear register(PWMCH5ICR)

Base address : 0x4000_5500

Address offset : 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC
													W	W	W

This bit is set by software, cleared by hardware when a capture interrupt becomes 0.

[0] MIC – Match Interrupt

0 : No action.

1 : Match interrupt is cleared.

[1] OIC – Overflow Interrupt

0 : No action.

1 : Overflow Interrupt is cleared.

[2] CIC – Capture Interrupt Clear.

0 : No action.

1 : Capture Interrupt is cleared.

18.14.4 Channel-5 Timer/Counter Register (PWMCH5TCR)

Base address : 0x4000_5500

Address offset : 0x0C

Reset value : 0x0000_0000

31	0
TCR	
R	

[31:0] TCR – Timer/Counter register

Timer/Counter register. These register hold the current values of the Timer/Counter(TC). The TC is incremented every PR cycles. When the TC is reached to value of match register, the match interrupt is occurred and PWM output waveform becomes 0. When the TC is reached to the value of limit register, the overflow interrupt is occurred, the TC is reset as 0.

18.14.5 Channel-5 Prescale Counter Register (PWMCH5PCR)

Base address : 0x4000_5500

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PCR					
										R					

[5:0] PC – Prescale Counter register

Prescale Counter register. These registers hold the current values of prescale counter(PC). The PC is incremented to the value stored in PR. When the PC is reached to PR, the TC is incremented and the PC is reset as 0.

18.14.6 Channel-5 Prescale Register (PWMCH5PR)

Base address : 0x4000_5500

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PR					
										R/W					

[5: 0] PR – Prescale Register

Prescale register. The PC is incremented when the PC is reached to the PR.

18.14.7 Channel-5 Match Register (PWMCH5MR)

Base address : 0x4000_5500

Address offset : 0x18

Reset value : 0x0000_0000

31	0
MR	
R/W	

[31:0] MR – Match Register

Match register. The MR can generate a match interrupt and PWM output waveform becomes 0 when the TC is reached to the MR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.14.8 Channel-5 Limit Register (PWMCH5LR)

Base address : 0x4000_5500

Address offset : 0x1C

Reset value : 0x0000_0000

31	0
LR	
R/W	

[31:0] LR – Limit Register

Limit Register. The LR can generate an overflow interrupt and PWM output waveform becomes 1 when the TC is reached to the LR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.14.9 Channel-5 Up-Down Mode Register (PWMCH5UDMR)

Base address : 0x4000_5500

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM
															R/W

[0] UDM – Up-Down mode

0 : TC runs up count.

1 : TC runs down count.

18.14.10 Channel-5 Timer/Counter Mode Register (PWMCH5TCMR)

Base address : 0x4000_5500

Address offset : 0x24

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM	
														R/W	

[1:0] TCM – Timer/Counter mode

00 : Timer mode.

01 : Counter mode with counting driven by rising edge external input .

10 : Counter mode with counting driven by falling edge external input.

11 : Counter mode with counting driven by rising and falling edge external input.

18.14.11 Channel-5 PWM output Enable and External input Enable Register (PWMCH5PEEER)

Base address : 0x4000_5500

Address offset : 0x28

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE	
														R/W	

[1:0] PEEE – PWM output Enable and External input Enable

00 : PWM output is disable and external input is disable.

01 : PWM output is disable and external input is enable.

10 : PWM output is enable and external input is disable.

18.14.12 Channel-5 Capture Mode Register (PWMCH5CMR)

Base address : 0x4000_5500

Address offset : 0x2C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM
															R/W

[0] CM – Capture mode

0 : Timer/Counter is captured when external input signal is rising edge.

1 : Timer/Counter is captured when external input signal is falling edge.

18.14.13 Channel-5 Capture Register (PWMCH5CR)

Base address : 0x4000_5500

Address offset : 0x30

Reset value : 0x0000_0000

31	0
CR	
R	

[31:0] CR – Capture Register

Capture register. The CR is loaded with the value of the TC when external input signal is triggered.

18.14.14 Channel-5 Periodic Mode Register (PWMCH5PDMR)

Base address : 0x4000_5500

Address offset : 0x34

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM
															R/W

[0] PDM – Periodic Mode

0 : Periodic mode. When the TC is reached to the LR, the TC returns to 0 and then continues counting periodically.

1 : One-shot mode. When the TC is reached to the LR, the TC returns to 0 and then stops counting.

18.14.15 Channel-5 Dead Zone Enable Register (PWMCH5DZER)

Base address : 0x4000_5500

Address offset : 0x38

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE
															R/W

[0] DZE – Dead Zone Enable

0 : Dead zone generation is disabled.

1 : Dead zone generation is enabled.

18.14.16 Channel-5 Dead Zone Counter Register (PWMCH5DZCR)

Base address : 0x4000_5500

Address offset : 0x3C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	DZC									
						R/W									

[9:0] DZC – Dead Zone Counter value

Dead zone generation counter value register. If the DZE bit in DZER is 1, dead zone counter counts to this value and during this time, the two PWM output waveforms are all 0.

18.15 Register map

The following Table 25 summarizes the PWM Channel-5 registers.

Table 25 PWM channel 5 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	PWMCH5IR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI	Channel-5 interrupt register
	reset value																														0	0	0	
0x04	PWMCH5IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE	Channel-5 interrupt enable register
	reset value																														0	0	0	
0x08	PWMCH5ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC	Channel-5 interrupt clear register
	reset value																																	Write only register
0x0C	PWMCH5TCR	TCR																																Channel-5 Timer/Counter Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	PWMCH5PCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PCR						Channel-5 Prescale Counter Register
	reset value																											0	0	0	0	0	0	
0x14	PWMCH5PR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PR						Channel-5 Prescale Register
	reset value																											0	0	0	0	0	0	
0x18	PWMCH5MR	MR																																Channel-5 Match Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x1C	PWMCH5LR	LR																																Channel-5 Limit Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x20	PWMCH5UDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM	Channel-5 Up-Down Mode Register
	reset value																																0	
0x24	PWMCH5TCMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM		Channel-5 Timer/Counter Mode Register
	reset value																															0	0	
0x28	PWMCH5PEEER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE		Channel-5 PWM output Enable and External input Enable Register
	reset value																															0	0	
0x2C	PWMCH5CMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM	Channel-5 Capture Mode Register
	reset value																																0	
0x30	PWMCH5CR	CR																																Channel-5 Capture Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	PWMCH5PDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM	Channel-5 Periodic Mode Register
	reset value																																0	
0x38	PWMCH5DZER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE	Channel-5 Dead Zone Enable Register
	reset value																																0	
0x3C	PWMCH5DZCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZC										Channel-5 Dead Zone Counter Register
	reset value																							0	0	0	0	0	0	0	0	0	0	

18.16 PWM Channel-6 Registers (Base address : 0x4000_5600)

18.16.1 Channel-6 interrupt register(PWMCH6IR)

Base address : 0x4000_5600

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI
													R	R	R

[0] MI – Match Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Match interrupt does not occur.

1 : Match interrupt occurs.

[1] OI – Overflow Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Overflow interrupt does not occur.

1 : Overflow interrupt occurs.

[2] CI – Capture Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Capture interrupt does not occur.

1 : Capture interrupt occurs.

18.16.2 Channel-6 interrupt enable register(PWMCH6IER)

Base address : 0x4000_5600

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE
													R/W	R/W	R/W

[0] MIE – Match Interrupt Enabled.

0 : Match interrupt is not enabled.

1 : Match interrupt is enabled.

[1] OIE – Overflow Interrupt Enable.

0 : Overflow interrupt is not enabled.

1 : Overflow interrupt is enabled.

[2] CIE – Capture Interrupt Enable.

0 : Capture interrupt is not enabled.

1 : Capture interrupt is enabled.

18.16.3 Channel-6 interrupt clear register(PWMCH6ICR)

Base address : 0x4000_5600

Address offset : 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC
													W	W	W

This bit is set by software, cleared by hardware when a capture interrupt becomes 0.

[0] MIC – Match Interrupt

0 : No action.

1 : Match interrupt is cleared.

[1] OIC – Overflow Interrupt

0 : No action.

1 : Overflow Interrupt is cleared.

[2] CIC – Capture Interrupt Clear.

0 : No action.

1 : Capture Interrupt is cleared.

18.16.4 Channel-6 Timer/Counter Register (PWMCH6TCR)

Base address : 0x4000_5600

Address offset : 0x0C

Reset value : 0x0000_0000

31	0
TCR	
R	

[31:0] TCR – Timer/Counter register

Timer/Counter register. These register hold the current values of the Timer/Counter(TC). The TC is incremented every PR cycles. When the TC is reached to value of match register, the match interrupt is occurred and PWM output waveform becomes 0. When the TC is reached to the value of limit register, the overflow interrupt is occurred, the TC is reset as 0.

18.16.5 Channel-6 Prescale Counter Register (PWMCH6PCR)

Base address : 0x4000_5600

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PCR					
										R					

[5:0] PC – Prescale Counter register

Prescale Counter register. These registers hold the current values of prescale counter(PC). The PC is incremented to the value stored in PR. When the PC is reached to PR, the TC is incremented and the PC is reset as 0.

18.16.6 Channel-6 Prescale Register (PWMCH6PR)

Base address : 0x4000_5600

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PR					
										R/W					

[5:0] PR – Prescale Register

Prescale register. The PC is incremented when the PC is reached to the PR.

18.16.7 Channel-6 Match Register (PWMCH6MR)

Base address : 0x4000_5600

Address offset : 0x18

Reset value : 0x0000_0000

31	0
MR	
R/W	

[31:0] MR – Match Register

Match register. The MR can generate a match interrupt and PWM output waveform becomes 0 when the TC is reached to the MR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.16.8 Channel-6 Limit Register (PWMCH6LR)

Base address : 0x4000_5600

Address offset : 0x1C

Reset value : 0x0000_0000

31	0
LR	
R/W	

[31:0] LR – Limit Register

Limit Register. The LR can generate an overflow interrupt and PWM output waveform becomes 1 when the TC is reached to the LR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.16.9 Channel-6 Up-Down Mode Register (PWMCH6UDMR)

Base address : 0x4000_5600

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM
															R/W

[0] UDM – Up-Down mode

0 : TC runs up count.

1 : TC runs down count.

18.16.10 Channel-6 Timer/Counter Mode Register (PWMCH6TCMR)

Base address : 0x4000_5600

Address offset : 0x24

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM	
														R/W	

[1:0] TCM – Timer/Counter mode

00 : Timer mode.

01 : Counter mode with counting driven by rising edge external input .

10 : Counter mode with counting driven by falling edge external input.

11 : Counter mode with counting driven by rising and falling edge external input.

18.16.11 Channel-6 PWM output Enable and External input Enable Register (PWMCH6PEEER)

Base address : 0x4000_5600

Address offset : 0x28

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE	
														R/W	

[1:0] PEEE – PWM output Enable and External input Enable

00 : PWM output is disable and external input is disable.

01 : PWM output is disable and external input is enable.

10 : PWM output is enable and external input is disable.

18.16.12 Channel-6 Capture Mode Register (PWMCH6CMR)

Base address : 0x4000_5600

Address offset : 0x2C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM
															R/W

[0] CM – Capture mode

0 : Timer/Counter is captured when external input signal is rising edge.

1 : Timer/Counter is captured when external input signal is falling edge.

18.16.13 Channel-6 Capture Register (PWMCH6CR)

Base address : 0x4000_5600

Address offset : 0x30

Reset value : 0x0000_0000

31	0
CR	
R	

[31:0] CR – Capture Register

Capture register. The CR is loaded with the value of the TC when external input signal is triggered.

18.16.14 Channel-6 Periodic Mode Register (PWMCH6PDMR)

Base address : 0x4000_5600

Address offset : 0x34

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM
															R/W

[0] PDM – Periodic Mode

0 : Periodic mode. When the TC is reached to the LR, the TC returns to 0 and then continues counting periodically.

1 : One-shot mode. When the TC is reached to the LR, the TC returns to 0 and then stops counting.

18.16.15 Channel-6 Dead Zone Enable Register (PWMCH6DZER)

Base address : 0x4000_5600

Address offset : 0x38

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE
															R/W

[0] DZE – Dead Zone Enable

0 : Dead zone generation is disabled.

1 : Dead zone generation is enabled.

18.16.16 Channel-6 Dead Zone Counter Register (PWMCH6DZCR)

Base address : 0x4000_5600

Address offset : 0x3C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	DZC									
						R/W									

[9:0] DZC – Dead Zone Counter value

Dead zone generation counter value register. If the DZE bit in DZER is 1, dead zone counter counts to this value and during this time, the two PWM output waveforms are all 0.

18.17 Register map

The following Table 26 summarizes the PWM Channel-5 registers.

Table 26 PWM channel 6 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	PWMCH6IR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI	Channel-6 interrupt register
	reset value																														0	0	0	
0x04	PWMCH6IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE	Channel-6 interrupt enable register
	reset value																														0	0	0	
0x08	PWMCH6ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC	Channel-6 interrupt clear register
	reset value																																	Write only register
0x0C	PWMCH6TCR	TCR																																Channel-6 Timer/Counter Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	PWMCH6PCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PCR						Channel-6 Prescale Counter Register
	reset value																											0	0	0	0	0	0	
0x14	PWMCH6PR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PR						Channel-6 Prescale Register
	reset value																											0	0	0	0	0	0	
0x18	PWMCH6MR	MR																																Channel-6 Match Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x1C	PWMCH6LR	LR																																Channel-6 Limit Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x20	PWMCH6UDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM	Channel-6 Up-Down Mode Register
	reset value																																0	
0x24	PWMCH6TCMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM		Channel-6 Timer/Counter Mode Register
	reset value																															0	0	
0x28	PWMCH6PEEER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE		Channel-6 PWM output Enable and External input Enable Register
	reset value																															0	0	
0x2C	PWMCH6CMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM	Channel-6 Capture Mode Register
	reset value																																0	
0x30	PWMCH6CR	CR																																Channel-6 Capture Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	PWMCH6PDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM	Channel-6 Periodic Mode Register
	reset value																																0	
0x38	PWMCH6DZER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE	Channel-6 Dead Zone Enable Register
	reset value																																0	
0x3C	PWMCH6DZCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZC										Channel-6 Dead Zone Counter Register
	reset value																							0	0	0	0	0	0	0	0	0	0	

18.18 PWM Channel-7 Registers (Base address : 0x4000_5700)

18.18.1 Channel-7 interrupt register(PWMCH7IR)

Base address : 0x4000_5700

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI
													R	R	R

[0] MI – Match Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Match interrupt does not occur.

1 : Match interrupt occurs.

[1] OI – Overflow Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Overflow interrupt does not occur.

1 : Overflow interrupt occurs.

[2] CI – Capture Interrupt

This bit is set by hardware and cleared by interrupt clear register.

0 : Capture interrupt does not occur.

1 : Capture interrupt occurs.

18.18.2 Channel-7 interrupt enable register(PWMCH7IER)

Base address : 0x4000_5700

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE
													R/W	R/W	R/W

[0] MIE – Match Interrupt Enabled.

0 : Match interrupt is not enabled.

1 : Match interrupt is enabled.

[1] OIE – Overflow Interrupt Enable.

0 : Overflow interrupt is not enabled.

1 : Overflow interrupt is enabled.

[2] CIE – Capture Interrupt Enable.

0 : Capture interrupt is not enabled.

1 : Capture interrupt is enabled.

18.18.3 Channel-7 interrupt clear register(PWMCH7ICR)

Base address : 0x4000_5700

Address offset : 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC
													W	W	W

This bit is set by software, cleared by hardware when a capture interrupt becomes 0.

[0] MIC – Match Interrupt

0 : No action.

1 : Match interrupt is cleared.

[1] OIC – Overflow Interrupt

0 : No action.

1 : Overflow Interrupt is cleared.

[2] CIC – Capture Interrupt Clear.

0 : No action.

1 : Capture Interrupt is cleared.

18.18.4 Channel-7 Timer/Counter Register (PWMCH7TCR)

Base address : 0x4000_5700

Address offset : 0x0C

Reset value : 0x0000_0000

31	0
TCR	
R	

[31:0] TCR – Timer/Counter register

Timer/Counter register. These register hold the current values of the Timer/Counter(TC). The TC is incremented every PR cycles. When the TC is reached to value of match register, the match interrupt is occurred and PWM output waveform becomes 0. When the TC is reached to the value of limit register, the overflow interrupt is occurred, the TC is reset as 0.

18.18.5 Channel-7 Prescale Counter Register (PWMCH7PCR)

Base address : 0x4000_5700

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PCR					
										R					

[5:0] PC – Prescale Counter register

Prescale Counter register. These registers hold the current values of prescale counter(PC). The PC is incremented to the value stored in PR. When the PC is reached to PR, the TC is incremented and the PC is reset as 0.

18.18.6 Channel-7 Prescale Register (PWMCH7PR)

Base address : 0x4000_5700

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	PR					
										R/W					

[5:0] PR – Prescale Register

Prescale register. The PC is incremented when the PC is reached to the PR.

18.18.7 Channel-7 Match Register (PWMCH7MR)

Base address : 0x4000_5700

Address offset : 0x18

Reset value : 0x0000_0000

31	0
MR	
R/W	

[31:0] MR – Match Register

Match register. The MR can generate a match interrupt and PWM output waveform becomes 0 when the TC is reached to the MR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.18.8 Channel-7 Limit Register (PWMCH7LR)

Base address : 0x4000_5700

Address offset : 0x1C

Reset value : 0x0000_0000

31	0
LR	
R/W	

[31:0] LR – Limit Register

Limit Register. The LR can generate an overflow interrupt and PWM output waveform becomes 1 when the TC is reached to the LR. Match register should be smaller than limit register(LR). If not, match interrupt is not occurred and PWM output waveform is always 1.

18.18.9 Channel-7 Up-Down Mode Register (PWMCH7UDMR)

Base address : 0x4000_5700

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM

															R/W

[0] UDM – Up-Down mode

0 : TC runs up count.

1 : TC runs down count.

18.18.10 Channel-7 Timer/Counter Mode Register (PWMCH7TCMR)

Base address : 0x4000_5700

Address offset : 0x24

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM	
														R/W	

[1:0] TCM – Timer/Counter mode

00 : Timer mode.

01 : Counter mode with counting driven by rising edge external input .

10 : Counter mode with counting driven by falling edge external input.

11 : Counter mode with counting driven by rising and falling edge external input.

18.18.11 Channel-7 PWM output Enable and External input Enable Register (PWMCH7PEEER)

Base address : 0x4000_5700

Address offset : 0x28

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE	
														R/W	

[1:0] PEEE – PWM output Enable and External input Enable

00 : PWM output is disable and external input is disable.

01 : PWM output is disable and external input is enable.

10 : PWM output is enable and external input is disable.

18.18.12 Channel-7 Capture Mode Register (PWMCH7CMR)

Base address : 0x4000_5700

Address offset : 0x2C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM
															R/W

[0] CM – Capture mode

0 : Timer/Counter is captured when external input signal is rising edge.

1 : Timer/Counter is captured when external input signal is falling edge.

18.18.13 Channel-7 Capture Register (PWMCH7CR)

Base address : 0x4000_5700

Address offset : 0x30

Reset value : 0x0000_0000

31	0
CR	
R	

[31:0] CR – Capture Register

Capture register. The CR is loaded with the value of the TC when external input signal is triggered.

18.18.14 Channel-7 Periodic Mode Register (PWMCH7PDMR)

Base address : 0x4000_5700

Address offset : 0x34

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM
															R/W

[0] PDM – Periodic Mode

0 : Periodic mode. When the TC is reached to the LR, the TC returns to 0 and then continues counting periodically.

1 : One-shot mode. When the TC is reached to the LR, the TC returns to 0 and then stops counting.

18.18.15 Channel-7 Dead Zone Enable Register (PWMCH7DZER)

Base address : 0x4000_5700

Address offset : 0x38

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE
															R/W

[0] DZE – Dead Zone Enable

0 : Dead zone generation is disabled.

1 : Dead zone generation is enabled.

18.18.16 Channel-7 Dead Zone Counter Register (PWMCH7DZCR)

Base address : 0x4000_5700

Address offset : 0x3C

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	DZC									
						R/W									

[9:0] DZC – Dead Zone Counter value

Dead zone generation counter value register. If the DZE bit in DZER is 1, dead zone counter counts to this value and during this time, the two PWM output waveforms are all 0.

18.19 Register map

The following Table 27 summarizes the PWM Channel-5 registers.

Table 27 PWM channel 7 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	PWMCH7IR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CI	OI	MI	Channel-7 interrupt register
	reset value																														0	0	0	
0x04	PWMCH7IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIE	OIE	MIE	Channel-7 interrupt enable register
	reset value																														0	0	0	
0x08	PWMCH7ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CIC	OIC	MIC	Channel-7 interrupt clear register
	reset value																																	Write only register
0x0C	PWMCH7TCR	TCR																																Channel-7 Timer/Counter Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x10	PWMCH7PCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PCR						Channel-7 Prescale Counter Register
	reset value																											0	0	0	0	0	0	
0x14	PWMCH7PR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PR						Channel-7 Prescale Register
	reset value																											0	0	0	0	0	0	
0x18	PWMCH7MR	MR																																Channel-7 Match Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x1C	PWMCH7LR	LR																																Channel-7 Limit Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x20	PWMCH7UDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	UDM	Channel-7 Up-Down Mode Register
	reset value																																0	
0x24	PWMCH7TCMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TCM		Channel-7 Timer/Counter Mode Register
	reset value																															0	0	
0x28	PWMCH7PEEER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PEEE		Channel-7 PWM output Enable and External input Enable Register
	reset value																															0	0	
0x2C	PWMCH7CMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CM	Channel-7 Capture Mode Register
	reset value																																0	
0x30	PWMCH7CR	CR																																Channel-7 Capture Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x34	PWMCH7PDMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PDM	Channel-7 Periodic Mode Register
	reset value																																0	
0x38	PWMCH7DZER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZE	Channel-7 Dead Zone Enable Register
	reset value																																0	
0x3C	PWMCH7DZCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	DZC										Channel-7 Dead Zone Counter Register
	reset value																							0	0	0	0	0	0	0	0	0	0	

18.20 PWM Common Registers (Base address : 0x4000_5800)

18.20.1 Interrupt Enable Register (IER)

Base address : 0x4000_5800

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[0] IE0 – Channel 0 Interrupt Enable

0 : Channel 0 interrupt is disabled.

1 : Channel 0 interrupt is enabled.

[1] IE1 – Channel 1 Interrupt Enable

0 : Channel 1 interrupt is disabled.

1 : Channel 1 interrupt is enabled.

[2] IE2 – Channel 2 Interrupt Enable

0 : Channel 2 interrupt is disabled.

1 : Channel 2 interrupt is enabled.

[3] IE3 – Channel 3 Interrupt Enable

0 : Channel 3 interrupt is disabled.

1 : Channel 3 interrupt is enabled.

[4] IE4 – Channel 4 Interrupt Enable

0 : Channel 4 interrupt is disabled.

1 : Channel 4 interrupt is enabled.

[5] IE5 – Channel 5 Interrupt Enable

0 : Channel 5 interrupt is disabled.

1 : Channel 5 interrupt is enabled.

[6] IE6 – Channel 6 Interrupt Enable

0 : Channel 6 interrupt is disabled.

1 : Channel 6 interrupt is enabled.

[7] IE7 – Channel 7 Interrupt Enable

0 : Channel 7 interrupt is disabled.

1 : Channel 7 interrupt is enabled.

18.20.2 Start/Stop Register (SSR)

Base address : 0x4000_5800

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[0] SS0 – Channel 0 Timer/Counter Start or Stop.

0 : Timer/Counter stop.

1 : Timer/Counter start.

[1] SS1 – Channel 1 Timer/Counter Start or Stop.

0 : Timer/Counter stop.

1 : Timer/Counter start.

[2] SS2 – Channel 2 Timer/Counter Start or Stop.

0 : Timer/Counter stop.

1 : Timer/Counter start.

[3] SS3 – Channel 3 Timer/Counter Start or Stop.

0 : Timer/Counter stop.

1 : Timer/Counter start.

[4] SS4 – Channel 4 Timer/Counter Start or Stop.

0 : Timer/Counter stop.

1 : Timer/Counter start.

[5] SS5 – Channel 5 Timer/Counter Start or Stop.

0 : Timer/Counter stop.

1 : Timer/Counter start.

[6] SS6 – Channel 6 Timer/Counter Start or Stop.

0 : Timer/Counter stop.

1 : Timer/Counter start.

[7] SS7 – Channel 7 Timer/Counter Start or Stop.

0 : Timer/Counter stop.

1 : Timer/Counter start.

18.20.3 Pause Register (PSR)

Base address : 0x4000_5800

Address offset : 0x04

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The Timer/Counter is paused after TC is reached to value of limit register.

[0] PS0 – Channel 0 Timer/Counter Pause.

0 : Timer/Counter is not paused.

1 : Timer/Counter is paused.

[1] PS1 – Channel 1 Timer/Counter Pause.

0 : Timer/Counter is not paused.

1 : Timer/Counter is paused.

[2] PS2 – Channel 2 Timer/Counter Pause.

0 : Timer/Counter is not paused.

1 : Timer/Counter is paused.

[3] PS3 – Channel 3 Timer/Counter Pause.

0 : Timer/Counter is not paused.

1 : Timer/Counter is paused.

[4] PS0 – Channel 4 Timer/Counter Pause.

0 : Timer/Counter is not paused.

1 : Timer/Counter is paused.

[5] PS0 – Channel 5 Timer/Counter Pause.

0 : Timer/Counter is not paused.

1 : Timer/Counter is paused.

[6] PS0 – Channel 6 Timer/Counter Pause.

0 : Timer/Counter is not paused.

1 : Timer/Counter is paused.

[7] PS0 – Channel 7 Timer/Counter Pause.

0 : Timer/Counter is not paused.

1 : Timer/Counter is paused.

18.21 Register map

The following Table 28 summarizes the PWM Common registers.

Table 28 PWM common register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	IER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0	Interrupt enable register
	reset value																									0	0	0	0	0	0	0	0	
0x04	SSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0	Start/Stop register
	reset value																									0	0	0	0	0	0	0	0	
0x08	PSR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Pause register
	reset value																									0	0	0	0	0	0	0	0	

19 Dual timers

19.1 Introduction

The dual timer consists two programmable 32-bit or 16-bit Free-running counters(FRCs) that can generate interrupts when they reach 0. There are two dual timers and 4 FRCs. One dual timers has one interrupt handler, resulting in two interrupts of timers. Also one dual timer has one clock but two clock enable signals. Users can select one repetition modes one-shot or wrapping mode, and wrapping mode consists free-running and periodic mode. Two FRCs are one set so two FRCs has one clock, reset, and interrupt but each FRC has an individual clock enable.

19.2 Features

- One dual timer has two Free-Running Counters(FRCs).
- One dual timer has one interrupt handler and one clock.
- One dual timer has two clock enable signals.
- There are 2 dual timers.
- A 32-bit or a 16-bit down counter.
- One of the following repetition modes: one-shot and wrapping mode.
- One of the following wrapping modes: Free-running and periodic mode.
- There is a prescaler that can divide down the clock rate by 1, 16, or 256.

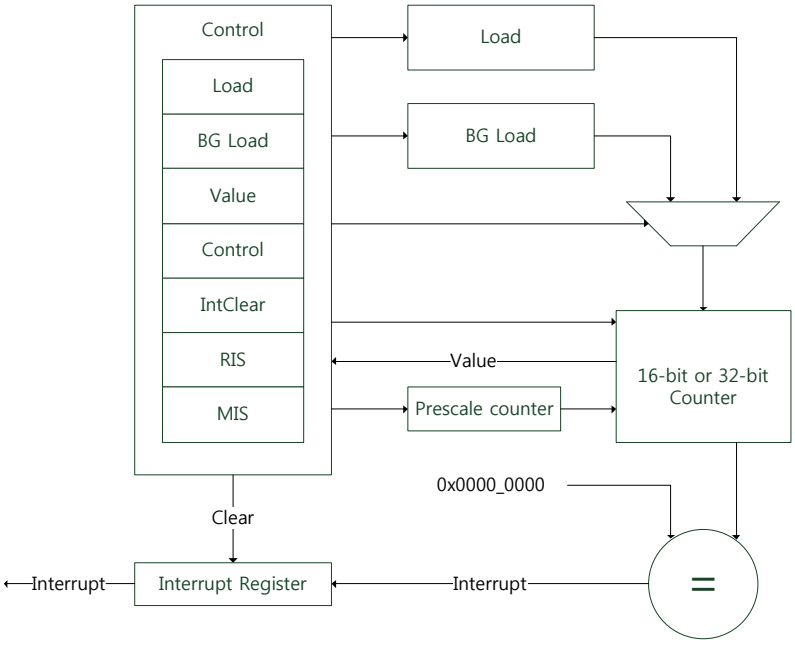


Figure 42 Block diagram of Dualtimer

19.3 Functional description

19.3.1 Clock and clock enable

The dual timers contain PCLK and TIMERCLK clock inputs. PCLK is the main APB system clock and is used by the register interface. TIMERCLK is the input to the prescale units and the decrementing counters. PCLK and TIMERCLK are synchronous.

The dual timers consist two programmable 32-bit Free-Running Counters(FRC) which operate independently. The two timers operate from one TIMERCLK but Each FRC is controlled independently by individual clock enable.

19.3.2 Timer size

Users can select FRC as 16-bit or 32-bit using the control register.

19.3.3 Prescaler

The timer has a prescaler that can divide down the enabled clock rate by 1, 16 or 256.

19.3.4 Repetition mode

There are two repetition mode: one-shot and wrapping mode. Wrapping mode has two modes: free-running and periodic mode.

One-shot mode

The counter generates an interrupt once. When the counter reaches 0, it halts until users reprogram it. Users can do this as below:

- Clear the one-shot count bit in the control register, in which case the count proceeds according to the selection of wrapping mode(free-running or periodic mode).
- Write a new value to the Load Value register.

Wrapping mode

Free-running mode

The counter wraps after reaching its zero value, and continues to count down from the maximum value. This is the default mode.

Periodic mode

The counter generates an interrupt at a constant interval, reloading the original value after wrapping past zero.

19.3.5 Interrupt

An interrupt is generated when the counter reaches 0 and is only cleared when the interrupt clear register is accessed.
The register holds the value until the interrupt is cleared.

Users can mask interrupts by writing 0 to the Interrupt Enable bit in the control register. Users can read the following from status registers:

- Raw interrupt status before masking.
- Final interrupt status after masking.

The interrupts from the individual timers after masking are logically ORed into a combined interrupt.

19.3.6 Operation

The operation of each timer is identical. The timer is loaded by writing to the load register and counts down to 0 if enabled. When a counter is already running, writing to the load register causes the counter to immediately restart at the new value. Writing to the background load value has no effect on the current count. In periodic mode, the counter continues to decrease to 0 and restart from the new load value.

An interrupt is generated when 0 is reached. Users can clear the interrupt by writing to the clear register. If users select one-shot mode, the counter halts when it reaches 0 until users deselect one-shot mode or write a new load value.

Otherwise, after reaching a zero count, if the timer is operating in free-running mode, it continues to decrease from its maximum value. If users select periodic mode, the timer reloads the count value from the load register and continues to decrease. In this mode, the counter effectively generates a periodic interrupt.

19.3.7 How to set the dual timers

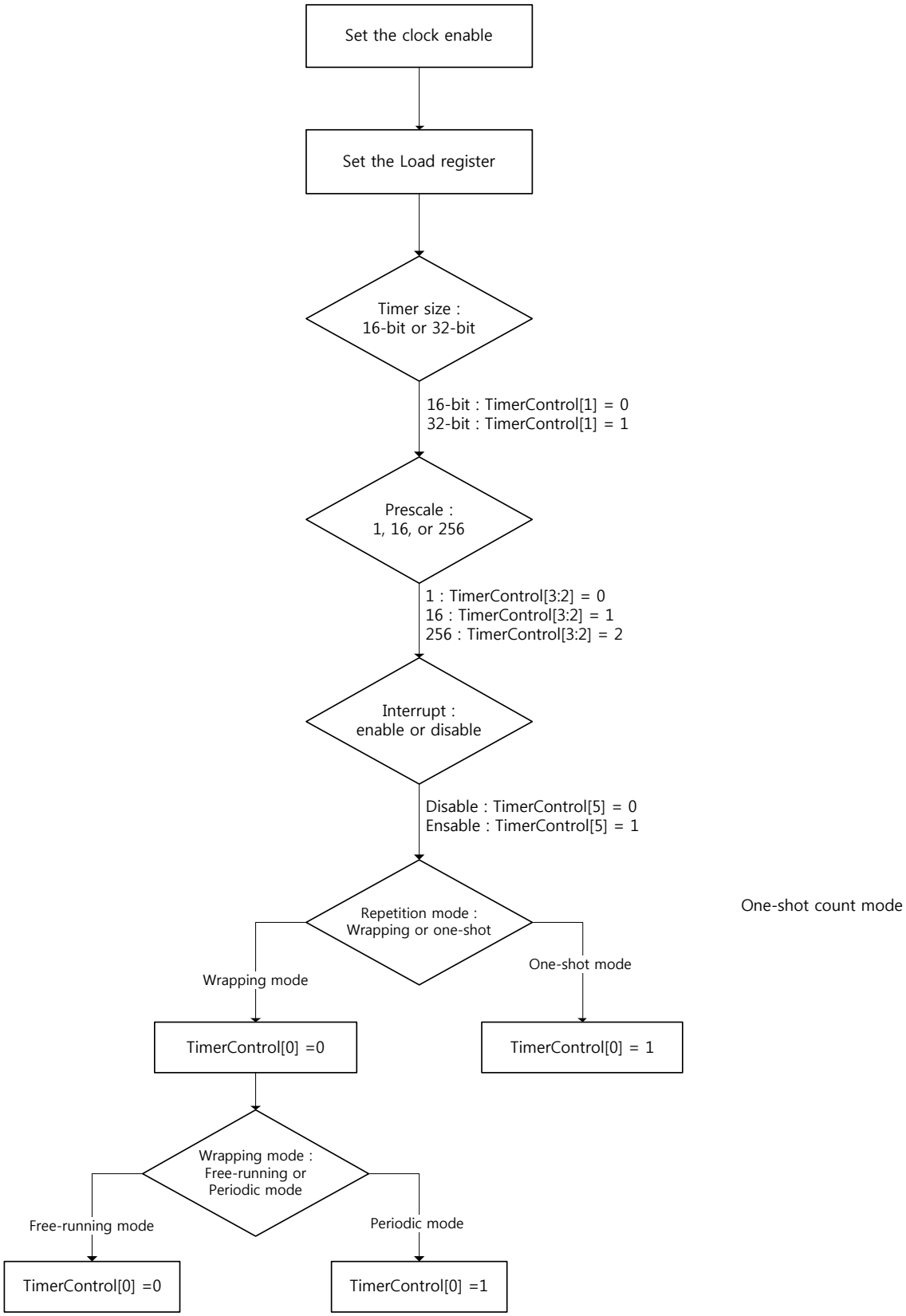


Figure 43 The Dual timer setting flow

19.4 Dual timer0_0 Registers (Base address : 0x4000_1000)

19.4.1 Timer0_0 Load Register(DUALTIMER0_0TimerLoad)

Base address : 0x4000_1000

Address offset : 0x00

Reset value : 0x0000_0000

31	0
TLR	
R/W	

[31:0] TLR – Timer Load Register

This register contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches 0.

19.4.2 Timer0_0 Value Register(DUALTIMER0_0TimerValue)

Base address : 0x4000_1000

Address offset : 0x04

Reset value : 0xFFFF_FFFF

31	0
TVR	
R	

[31:0] TVR – Timer Value Register

This register provides the current value of the decrementing counter.

19.4.3 Timer0_0 Control Register(DUALTIMER0_0TimerControl)

Base address : 0x4000_1000

Address offset : 0x08

Reset value : 0x0000_0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	TE	TM	IE	res	TP		TS	OC
								R/W	R/W	R/W		R/W		R/W	R/W

[0] OC – One-shot Count

0 : Wrapping mode, default.

1 : One-shot mode.

[1] TS – Timer Size

0 : 16-bit counter, default.

1 : 32-bit counter.

[3:2] TP – Timer Prescale.

00 : 0 stages of prescale, clock is divided by 1, default.

01 : 4 stages of prescale, clock is divided by 16.

10 : 8 stages of prescale, clock is divided by 256.

11 : Undefined, do not use.

[5] IE – Interrupt Enable.

0 : Timer Interrupt disable.

1 : Timer Interrupt enabled, default.

[6] TM – Timer Mode.

0 : Timer is in free-running mode, default.

1 : Timer is in periodic mode.

[7] TE – Timer Enable.

0 : Timer disabled, default.

1 : Timer enabled.

19.4.4 Timer0_0 Interrupt Clear Register (DUALTIMER0_0TimerIntClr)

Base address : 0x4000_1000

Address offset : 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TIC
															W

[0] TIC – Interrupt Clear

Set to this register clears the interrupt output from the counter.

19.4.5 Timer0_0 Raw Interrupt Status Register (DUALTIMER0_0TimerRIS)

Base address : 0x4000_1000

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS
															R

[0] RIS – Raw Interrupt Status Register

This register indicates the raw interrupt status from the counter. This value is ANDed with the timer interrupt enable bit from the Timer Control Register to create the masked interrupt, that is passed to the interrupt output pin.

19.4.6 Timer0_0 Masked Interrupt Status Register (DUALTIMER0_0TimerMIS)

Base address : 0x4000_1000

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS
															R

[0] MIS – Masked Interrupt Status Register

This register indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the Timer Control Register, and is the same value that is passed to the interrupt output pin.

19.4.7 Timer0_0 Background Load Register (DUALTIMER0_0TimerBGLoad)

Base address : 0x4000_1000

Address offset : 0x18

Reset value : 0x0000_0000

31	0
BGL	
R/W	

[31:0] BGL – Background Load Register

This register contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches 0.

This register provides an alternative method of accessing the TimerLoad Register. The difference is that writes to TimerBGLoad Register do not cause the counter to immediately restart from the new value.

Reading from this register returns the same value returned from TimerLoad Register.

19.5 Register map

The following Table 29 summarizes the Dual timer 0_0 registers.

Table 29 Dual timer 0_0 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	DUALTIMER0_0TimerLoad	TLR																																Timer0_0 Load Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x04	DUALTIMER0_0TimerValue	TVR																																Timer0_0 Value Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x08	DUALTIMER0_0TimerControl	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TE	TM	IE	res	TP		TS	OC	Timer0_0 Control Register
	reset value																									0	0	1		0	0	0	0	
0x0C	DUALTIMER0_0TimerIntClr	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TIC	Timer0_0 Interrupt Clear Register
	reset value																																	Write only register
0x10	DUALTIMER0_0TimerRIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS	Timer0_0 Raw Interrupt Status Register
	reset value																																0	
0x14	DUALTIMER0_0TimerMIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS	Timer0_0 Masked Interrupt Status Register
	reset value																																0	
0x18	DUALTIMER0_0TimerBGLoad	BGL																																Timer0_0 Background Load Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

19.6 Dual timer0_1 Registers (Base address : 0x4000_1020)

19.6.1 Timer0_1 Load Register(DUALTIMER0_1TimerLoad)

Base address : 0x4000_1020

Address offset : 0x00

Reset value : 0x0000_0000

31	0
TLR	
R/W	

[31:0] TLR – Timer Load Register

This register contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches 0.

19.6.2 Timer0_1 Value Register(DUALTIMER0_1TimerValue)

Base address : 0x4000_1020

Address offset : 0x04

Reset value : 0xFFFF_FFFF

31	0
TVR	
R	

[31:0] TVR – Timer Value Register

This register provides the current value of the decrementing counter.

19.6.3 Timer0_1 Control Register(DUALTIMER0_1TimerControl)

Base address : 0x4000_1020

Address offset : 0x08

Reset value : 0x0000_0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	TE	TM	IE	res	TP		TS	OC
								R/W	R/W	R/W		R/W		R/W	R/W

[0] OC – One-shot Count

0 : Wrapping mode, default.

1 : One-shot mode.

[1] TS – Timer Size

0 : 16-bit counter, default.

1 : 32-bit counter.

[3:2] TP – Timer Prescale.

00 : 0 stages of prescale, clock is divided by 1, default.

01 : 4 stages of prescale, clock is divided by 16.

10 : 8 stages of prescale, clock is divided by 256.

11 : Undefined, do not use.

[5] IE – Interrupt Enable.

0 : Timer Interrupt disable.

1 : Timer Interrupt enabled, default.

[6] TM – Timer Mode.

0 : Timer is in free-running mode, default.

1 : Timer is in periodic mode.

[7] TE – Timer Enable.

0 : Timer disabled, default.

1 : Timer enabled.

19.6.4 Timer0_1 Interrupt Clear Register (DUALTIMER0_1TimerIntClr)

Base address : 0x4000_1020

Address offset : 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IC
															W

[0] IC – Interrupt Clear

Set to the this register clears the interrupt output from the counter.

19.6.5 Timer0_1 Raw Interrupt Status Register (DUALTIMER0_1TimerRIS)

Base address : 0x4000_1020

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS
															R

[0] RIS – Raw Interrupt Status Register

This register indicates the raw interrupt status from the counter. This value is ANDed with the timer interrupt enable bit from the Timer Control Register to create the masked interrupt, that is passed to the interrupt output pin.

19.6.6 Timer0_1 Masked Interrupt Status Register (DUALTIMER0_1TimerMIS)

Base address : 0x4000_1020

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS
															R

[0] MIS – Masked Interrupt Status Register

This register indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the Timer Control Register, and is the same value that is passed to the interrupt output pin.

19.6.7 Timer0_1 Background Load Register (DUALTIMER0_1TimerBGLoad)

Base address : 0x4000_1020

Address offset : 0x18

Reset value : 0x0000_0000

31	0
BGL	
R/W	

[31:0] BGL – Background Load Register

This register contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches 0.

This register provides an alternative method of accessing the TimerLoad Register. The difference is that writes to TimerBGLoad Register do not cause the counter to immediately restart from the new value.

Reading from this register returns the same value returned from TimerLoad Register.

19.7 Register map

The following Table 30 summarizes the Dual timer 0_1 registers.

Table 30 Dual timer 0_1 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	DUALTIMER0_1TimerLoad	TLR																																Timer0_1 Load Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x04	DUALTIMER0_1TimerValue	TVR																																Timer0_1 Value Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x08	DUALTIMER0_1TimerControl	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TE	TM	IE	res	TP		TS	OC	Timer0_1 Control Register
	reset value																									0	0	1		0	0	0	0	
0x0C	DUALTIMER0_1TimerIntClr	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TIC	Timer0_1 Interrupt Clear Register
	reset value																																	Write only register
0x10	DUALTIMER0_1TimerRIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS	Timer0_1 Raw Interrupt Status Register
	reset value																																0	
0x14	DUALTIMER0_1TimerMIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS	Timer0_1 Masked Interrupt Status Register
	reset value																																0	
0x18	DUALTIMER0_1TimerBGLoad	BGL																																Timer0_1 Background Load Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

19.8 Dual Timer 0 Clock Enable Register (Base address : 0x4000_1080)

19.8.1 Timer0_0 Clock Enable Register (TIMCLKEN0_0)

Base address : 0x4000_1080

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE
															R/W

[0] CE – Clock Enable Register

0 : Clock disable

1 : Clock enable

19.8.2 Timer0_1 Clock Enable Register (TIMCLKEN0_1)

Base address : 0x4000_1080

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE
															R/W

[0] CE – Clock Enable Register

0 : Clock disable

1 : Clock enable

19.9 Register map

The following Table 31 summarizes the Dual timer 0 registers.

Table 31 Dual timer 0 clock enable register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	TIMCLKEN0_0	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE	Timer0_0 Clock Enable Register
	reset value																																0	
0x04	TIMCLKEN0_1	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE	Timer0_1 Clock Enable Register
	reset value																																0	

19.10 Dual timer1_0 Registers (Base address : 0x4000_2000)

19.10.1 Timer1_0 Load Register(DUALTIMER1_0TimerLoad)

Base address : 0x4000_2000

Address offset : 0x00

Reset value : 0x0000_0000

31	0
TLR	
R/W	

[31:0] TLR – Timer Load Register

This register contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches 0.

19.10.2 Timer1_0 Value Register(DUALTIMER1_0TimerValue)

Base address : 0x4000_2000

Address offset : 0x04

Reset value : 0xFFFF_FFFF

31	0
TVR	
R	

[31:0] TVR – Timer Value Register

This register provides the current value of the decrementing counter.

19.10.3 Timer1_0 Control Register(DUALTIMER1_0TimerControl)

Base address : 0x4000_2000

Address offset : 0x08

Reset value : 0x0000_0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	TE	TM	IE	res	TP		TS	OC
								R/W	R/W	R/W		R/W		R/W	R/W

[0] OC – One-shot Count

0 : Wrapping mode, default.

1 : One-shot mode.

[1] TS – Timer Size

0 : 16-bit counter, default.

1 : 32-bit counter.

[3:2] TP – Timer Prescale.

00 : 0 stages of prescale, clock is divided by 1, default.

01 : 4 stages of prescale, clock is divided by 16.

10 : 8 stages of prescale, clock is divided by 256.

11 : Undefined, do not use.

[5] IE – Interrupt Enable.

0 : Timer Interrupt disable.

1 : Timer Interrupt enabled, default.

[6] TM – Timer Mode.

0 : Timer is in free-running mode, default.

1 : Timer is in periodic mode.

[7] TE – Timer Enable.

0 : Timer disabled, default.

1 : Timer enabled.

19.10.4 Timer1_0 Interrupt Clear Register (DUALTIMER1_0TimerIntClr)

Base address : 0x4000_2000

Address offset : 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IC
															W

[0] IC – Interrupt Clear

Set to the this register clears the interrupt output from the counter.

19.10.5 Timer1_0 Raw Interrupt Status Register (DUALTIMER1_0TimerRIS)

Base address : 0x4000_2000

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS
															R

[0] RIS – Raw Interrupt Status Register

This register indicates the raw interrupt status from the counter. This value is ANDed with the timer interrupt enable bit from the Timer Control Register to create the masked interrupt, that is passed to the interrupt output pin.

19.10.6 Timer1_0 Masked Interrupt Status Register (DUALTIMER1_0TimerMIS)

Base address : 0x4000_2000

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS
															R

[0] MIS – Masked Interrupt Status Register

This register indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the Timer Control Register, and is the same value that is passed to the interrupt output pin.

19.10.7 Timer1_0 Background Load Register (DUALTIMER1_0TimerBGLoad)

Base address : 0x4000_2000

Address offset : 0x18

Reset value : 0x0000_0000

31	0
BGL	
R/W	

[31:0] BGL – Background Load Register

This register contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches 0.

This register provides an alternative method of accessing the TimerLoad Register. The difference is that writes to TimerBGLoad Register do not cause the counter to immediately restart from the new value.

Reading from this register returns the same value returned from TimerLoad Register.

19.11 Register map

The following Table 32 summarizes the Dual timer 1_0 registers.

Table 32 Dual timer 1_0 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	DUALTIMER1_0TimerLoad	TLR																																Timer1_0 Load Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x04	DUALTIMER1_0TimerValue	TVR																																Timer1_0 Value Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x08	DUALTIMER1_0TimerControl	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TE	TM	IE	res	TP		TS	OC	Timer1_0 Control Register
	reset value																									0	0	1		0	0	0	0	
0x0C	DUALTIMER1_0TimerIntClr	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TIC	Timer1_0 Interrupt Clear Register
	reset value																																	Write only register
0x10	DUALTIMER1_0TimerRIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS	Timer1_0 Raw Interrupt Status Register
	reset value																																0	
0x14	DUALTIMER1_0TimerMIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS	Timer1_0 Masked Interrupt Status Register
	reset value																																0	
0x18	DUALTIMER1_0TimerBGLoad	BGL																																Timer1_0 Background Load Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

19.12 Dual timer1_1 Registers (Base address : 0x4000_2020)

19.12.1 Timer1_1 Load Register(DUALTIMER1_1TimerLoad)

Base address : 0x4000_2020

Address offset : 0x00

Reset value : 0x0000_0000

31	0
TLR	
R/W	

[31:0] TLR – Timer Load Register

This register contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches 0.

19.12.2 Timer1_1 Value Register(DUALTIMER1_1TimerValue)

Base address : 0x4000_2020

Address offset : 0x04

Reset value : 0xFFFF_FFFF

31	0
TVR	
R	

[31:0] TVR – Timer Value Register

This register provides the current value of the decrementing counter.

19.12.3 Timer1_1 Control Register(DUALTIMER1_1TimerControl)

Base address : 0x4000_2020

Address offset : 0x08

Reset value : 0x0000_0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	TE	TM	IE	res	TP		TS	OC
								R/W	R/W	R/W		R/W		R/W	R/W

[0] OC – One-shot Count

0 : Wrapping mode, default.

1 : One-shot mode.

[1] TS – Timer Size

0 : 16-bit counter, default.

1 : 32-bit counter.

[3:2] TP – Timer Prescale.

00 : 0 stages of prescale, clock is divided by 1, default.

01 : 4 stages of prescale, clock is divided by 16.

10 : 8 stages of prescale, clock is divided by 256.

11 : Undefined, do not use.

[5] IE – Interrupt Enable.

0 : Timer Interrupt disable.

1 : Timer Interrupt enabled, default.

[6] TM – Timer Mode.

0 : Timer is in free-running mode, default.

1 : Timer is in periodic mode.

[7] TE – Timer Enable.

0 : Timer disabled, default.

1 : Timer enabled.

19.12.4 Timer1_1 Interrupt Clear Register (DUALTIMER1_1TimerIntClr)

Base address : 0x4000_2020

Address offset : 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	IC
															W

[0] IC – Interrupt Clear

Set to the this register clears the interrupt output from the counter.

19.12.5 Timer1_1 Raw Interrupt Status Register (DUALTIMER1_1TimerRIS)

Base address : 0x4000_2020

Address offset : 0x10

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS
															R

[0] RIS – Raw Interrupt Status Register

This register indicates the raw interrupt status from the counter. This value is ANDed with the timer interrupt enable bit from the Timer Control Register to create the masked interrupt, that is passed to the interrupt output pin.

19.12.6 Timer1_1 Masked Interrupt Status Register (DUALTIMER1_1TimerMIS)

Base address : 0x4000_2020

Address offset : 0x14

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS
															R

[0] MIS – Masked Interrupt Status Register

This register indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the Timer Control Register, and is the same value that is passed to the interrupt output pin.

19.12.7 Timer1_1 Background Load Register (DUALTIMER1_1TimerBGLoad)

Base address : 0x4000_2020

Address offset : 0x18

Reset value : 0x0000_0000

31	0
BGL	
R/W	

[31:0] BGL – Background Load Register

This register contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches 0.

This register provides an alternative method of accessing the TimerLoad Register. The difference is that writes to TimerBGLoad Register do not cause the counter to immediately restart from the new value.

Reading from this register returns the same value returned from TimerLoad Register.

19.13 Register map

The following Table 33 summarizes the Dual timer 1_1 registers.

Table 33 Dual timer 1_1 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	DUALTIMER1_1TimerLoad	TLR																																Timer1_1 Load Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x04	DUALTIMER1_1TimerValue	TVR																																Timer1_1 Value Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x08	DUALTIMER1_1TimerControl	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TE	TM	IE	res	TP		TS	OC	Timer1_1 Control Register
	reset value																									0	0	1		0	0	0	0	
0x0C	DUALTIMER1_1TimerIntClr	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	TIC	Timer1_1 Interrupt Clear Register
	reset value																																	Write only register
0x10	DUALTIMER1_1TimerRIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS	Timer1_1 Raw Interrupt Status Register
	reset value																																0	
0x14	DUALTIMER1_1TimerMIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS	Timer1_1 Masked Interrupt Status Register
	reset value																																0	
0x18	DUALTIMER1_1TimerBGLoad	BGL																																Timer1_1 Background Load Register
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

19.14 Dual Timer 1 Clock Enable Register (Base address : 0x4000_2080)

19.14.1 Timer1_0 Clock Enable Register (TIMCLKEN1_0)

Base address : 0x4000_2080

Address offset : 0x00

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE
															R/W

[0] CE – Clock Enable Register

0 : Clock disable

1 : Clock enable

19.14.2 Timer1_1 Clock Enable Register (TIMCLKEN1_1)

Base address : 0x4000_2080

Address offset : 0x20

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE
															R/W

[0] CE – Clock Enable Register

0 : Clock disable

1 : Clock enable

19.15 Register map

The following Table 34 summarizes the Dual timer 1 registers.

Table 34 Dual timer 1 clock enable register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	TIMCLKEN1_0	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE	Timer1_0 Clock Enable Register
	reset value																																0	
0x04	TIMCLKEN1_1	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE	Timer1_1 Clock Enable Register
	reset value																																0	

20 Watchdog timer

20.1 Introduction

The watchdog is based on a 32-bit down-counter that is initialized from the Reload Register, WDTLoad. The watchdog generates a regular interrupt depending on a programmed value. The counter decreases by one on each positive clock edge of watchdog clock.

The watchdog monitors the interrupt and asserts a reset request signal when the counter reaches 0 and the counter is stopped. On the next enabled watchdog clock edge, the counter is reloaded from the WDTLoad Register and the countdown sequence continues. The watchdog reasserts the reset signal if the interrupt is not cleared by the time the counter next reaches 0.

The watchdog applies a reset to a system in the event of a software failure to provide a way to recover from software crashes. Users can enable or disable the watchdog unit as required.

20.2 Features

- 32-bit down counter.
- Internally resets chip if not periodically reloaded.
- The watchdog timer has lock register to prevent rogue software from disabling the watchdog timer functionality.
- The watchdog timer clock(WDTCLK) and system clock(PCLK) are synchronous.

20.3 Functional description

20.3.1 Clock

The watchdog timer contains PCLK and WDTCLK clock inputs.
PCLK is the main APB system clock and is used by the register interface.

20.3.2 Interrupt and reset request

An interrupt is generated when the counter reaches 0 and is only cleared when the interrupt clear register is accessed.
The register holds the value until the interrupt is cleared.

Reset request is asserted when the counter reaches 0 repeatedly and is not reprogrammed.

Users can mask interrupts by writing 0 to the Interrupt Enable bit in the control register.

Users can read the following from status registers:

- Raw interrupt status, before masking.
- Final interrupt status, after masking.

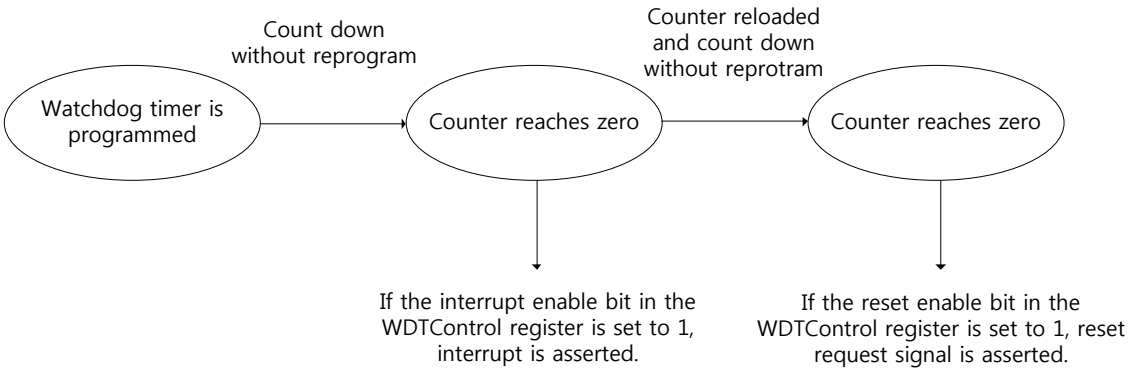


Figure 44 Watchdog timer operation flow diagram

20.4 Watchdog timer Registers (Base address : 0x4000_0000)

20.4.1 Watchdog timer Load Register(WDTLoad)

Address offset : 0x000

Reset value : 0xFFFF_FFFF

31	0
WLR	
R/W	

[31:0] WLR – Watchdog timer Load Register.

This register contains the value from which the counter is to decrement. When this register is written to, the count is immediately restarted from the new value. The minimum valid value for WDTLoad is 1.

20.4.2 Watchdog timer Value Register(WDTValue)

Address offset : 0x004

Reset value : 0xFFFF_FFFF

31	0
WVR	
R	

[31:0] WVR – Watchdog timer Value Register.

This register gives the current value of the decrementing counter.

20.4.3 Watchdog timer Control Register(WDTControl)

Address offset : 0x008

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	REN	IEN
														R/W	R/W

[0] IEN – Interrupt Enable.

0 : Disable the counter and the interrupt.

1 : Enable the counter and the interrupt. Reloads the counter from the value in WDTLoad, after previously being disabled.

[1] REN – Reset Request Enable.

0 : Disable watchdog reset output.

1 : Enable watchdog reset output.

20.4.4 Watchdog timer Interrupt Clear Register (WDTIntClr)

Address offset : 0x00C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	WIC
															W

[0] WIC – Watchdog timer Interrupt Clear

A write of 1 to this register clears the watchdog interrupt, and reloads the counter from the value in WDTLoad.

20.4.5 Watchdog timer Raw Interrupt Status Register (WDTRIS)

Address offset : 0x010

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS
															R

[0] RIS – Watchdog timer Raw Interrupt Status.

This register indicates the raw interrupt status from the counter. This value is ANDed with the interrupt enable bit from the control register to create the masked interrupt, that is passed to the interrupt output pin.

20.4.6 Watchdog timer Masked Interrupt Status Register (WDTMIS)

Address offset : 0x014

Reset value : 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS
															R

[0] MIS – Watchdog timer Masked Interrupt Status.

This register indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the interrupt enable(IEN) bit from the control register, and is the same value that is passed to the interrupt output pin.

20.4.7 Watchdog timer Lock Register(WDTLock)

Address offset : 0xC00

Reset value : 0x0000_0000

31	1	0
ERW		WES
W		R

This register disables write accesses to all other registers. This is to prevent rogue software from disabling the watchdog functionality. Writing a value of 0x1ACCE551

enables write access to all other registers. Writing any other value disables write accesses. A read from this register returns only the bottom bit.

[0] WES – Register Write Enable status.

0 : Indicates that write access is enabled, not locked. Default.

1 : Indicates that write access is disabled, locked.

[31:1] ERW – Enable Register Writes

Enable write access to all other registers by writing 0x1ACCE551. Disable write access by writing any other value.

20.5 Register map

The following Table 35 summarizes the Watchdog timer registers.

Table 35 Watchdog Timer register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x000	WDTLoad	WLR																																Watchdog timer Load Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x004	WDTValue	WVR																																Watchdog timer Value Register
	reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x008	WDTControl	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	REN	IEN	Watchdog timer Control Register
	reset value																															0	0	
0x00C	WDTIntClr	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	WIC	Watchdog timer Interrupt Clear Register
	reset value																																	Write only register
0x010	WDTRIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RIS	Watchdog timer Raw Interrupt Status Register
	reset value																																0	
0x014	WDTMIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	MIS	Watchdog timer Raw Interrupt Status Register
	reset value																																0	
0xC00	WDTLock	ERW																															WES	Watchdog timer Lock Register
	reset value	W																															R	

21 Inter-integrated circuit interface (I2C)

21.1 Introduction

The I^2C (inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It supports standard speed mode(100Kbps).

21.2 Features

- Use APB interface
- Supports Slave and Master Mode
- Standard mode (up to 100 KHz)
- Supports 7 bit Slave address mode
- Start/Stop/Repeated Start detection
- Start/Stop/Repeated Start/Acknowledge generation
- Control the Read/Write operation
- General Call enable or disable
- Slave busy detection
- Repeated START

21.3 Functional description

I^2C is comprised of both master and slave functions. For proper operation, the SDA and SCL pins must be configured as open-drain signals. A I^2C bus configuration is shown in Figure 45.

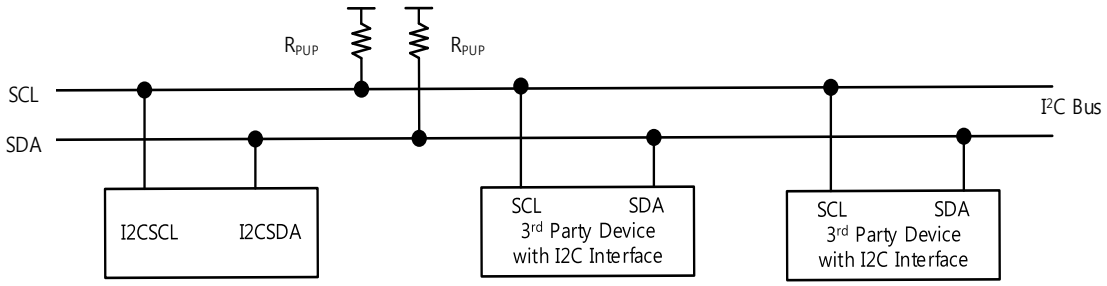


Figure 45. I2C Bus Configuration

Figure 46 shows the I2C block diagram.

In addition to receiving and transmitting data, this interface converts it from serial to parallel format and vice versa. The interrupt is enabled or disabled by software. The interface is connected to the I^2C bus by a data pin (SDA) and by a Clock pin (SCL). It can be connected with a standard (up to 100 KHz) I^2C bus.

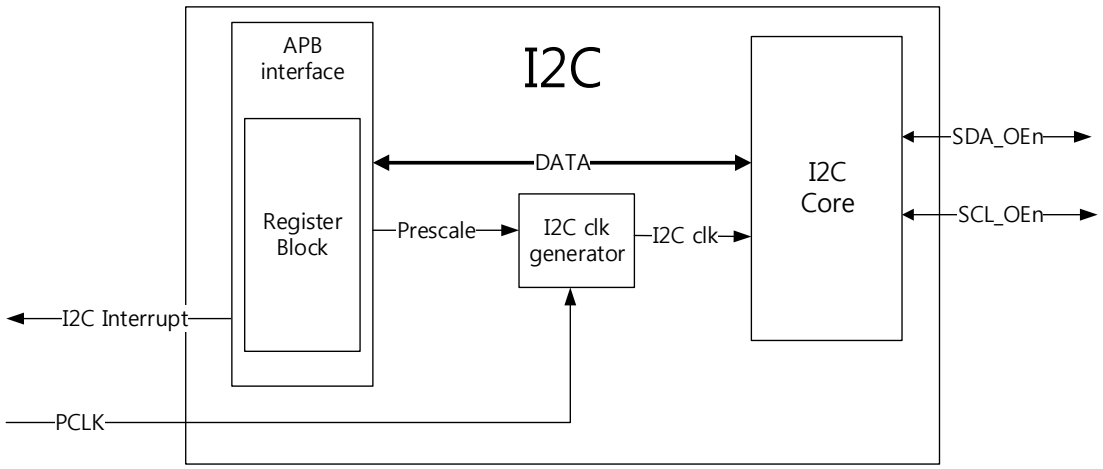


Figure 46. I2C block diagram

SDA is the bi- directions serial data line and SCL is the bi-directions serial clock line. The bus is considered idle when both lines are high. Every transaction on the I^2C bus is nine bits long, consisting of eight data bits and a single acknowledge bit and data must be transferred MSB first.

21.3.1 Data validity

The data on the SDA line must be stable during the HIGH period of the SCL. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 47). One clock pulse is generated for each data bit transferred.

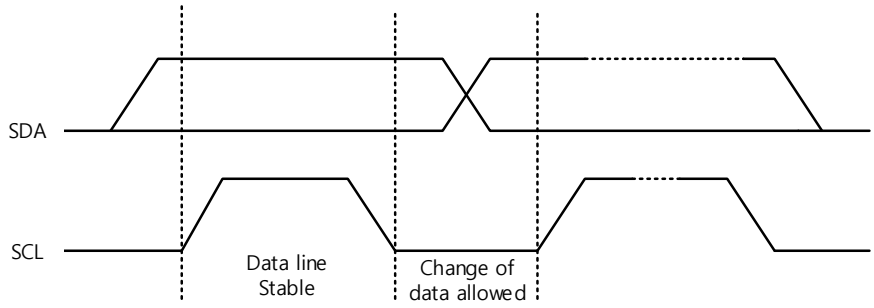


Figure 47. Data Validity

21.3.2 Acknowledge

All bus transactions have a required acknowledge clock cycle that is generated by the master. During the acknowledge cycle, the transmitter cannot operate the next operation.

21.3.3 Bit Command Controller

The Bit command Controller handles the actual transmission of data and the generation of the specific levels for START, STOP and Repeated START signals by controlling the SCL and SDA lines. The Byte Command controller tells the Bit command Controller which operation has to be performed. For a single byte read, the Bit command Controller receives 8 separate read command. Each bit-operation is divided into 5 pieces (idle and A,B,C,and D) except for a STOP operation which is divided into 4 pieces(idle and A, B,C)

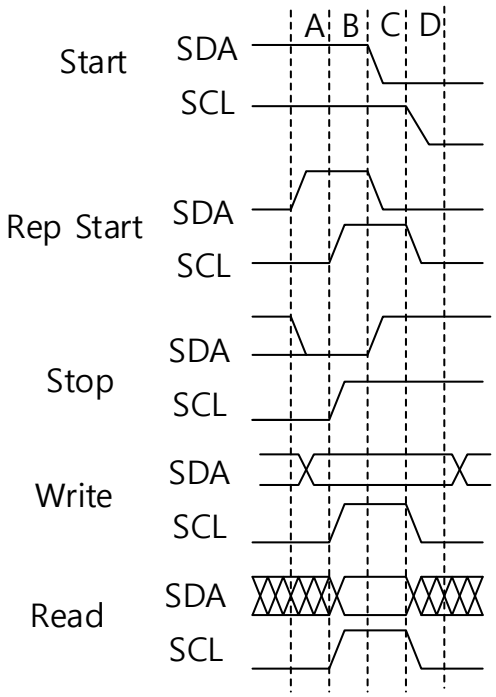


Figure 48. Bit Conditions

21.3.3.1 START and STOP Conditions

The protocol of the I^2C bus defines two states to START and STOP conditions.

A High to Low transition on the SDA line while SCL is High is one unique case and indicates a START condition. A Low to High transition on the SDA line while SCL is high defines a STOP condition.

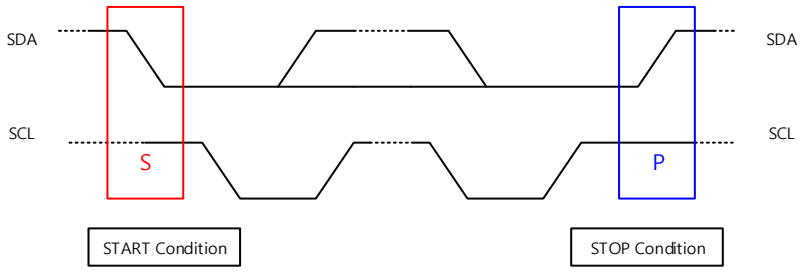


Figure 49. START and STOP Conditions

START and STOP conditions are always generated by the master.

This bus is considered to be again a certain time after the STOP condition. The bus stays busy if a Repeated START is generated instead of a STOP condition.

21.3.3.2 RESTART Condition

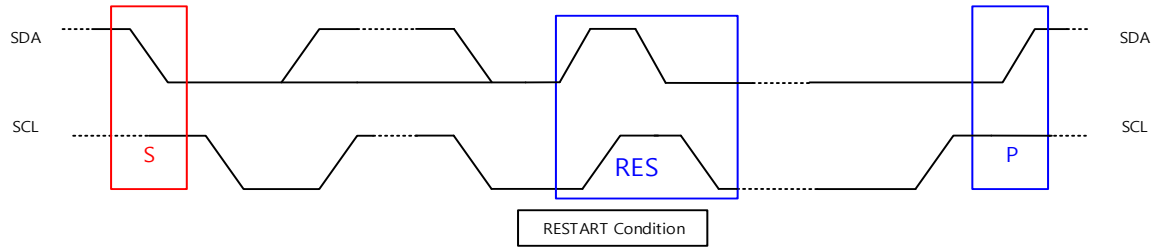


Figure 50. RESTART Condition

21.3.4 Slave address

The SDA line must be eight bits long.

Each byte must be followed by an Acknowledge bit.



Figure 51. 7-bit Slave address

21.3.5 Read/Write bit

This address is seven bits followed by an eight bit which is a data direction bit(R/$\overline{W}$) :

'0' indicates a WRITE, '1' indicates a READ

There are two methods of setting data direction bit by I2Cx_CTR.

The 32-bits I2Cx_CTR is reconfigured with COREEN, INTEREN, MODE, ADDR10, CTRRWN, CTREN.

CTREN bit select the R/W – a 'Zero' indicates the slave address bit 0, a 'one' indicates a CTRRWN bit.

21.3.6 Acknowledge(ACK) and Not Acknowledge(NACK)

The acknowledge bit takes place after every bytes. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent.

The master generates all clock pulses, including acknowledge ninth clock.

21.3.7 Data transfer

The data transfer is managed through the shift, transmit data, and receive data registers. Data transfers follow the format shown in Figure 52. After START condition, a Slave address is transmitted. If CTREN bit in the I2Cx_CTR register is enable, LSB of Slave address (bit 0) is superseded by value of CTRRWN bit in the I2Cx_CTR register.

If CTREN bit in the I2Cx_CTR register is disable, LSB of slave address is used for Read/Write operation.

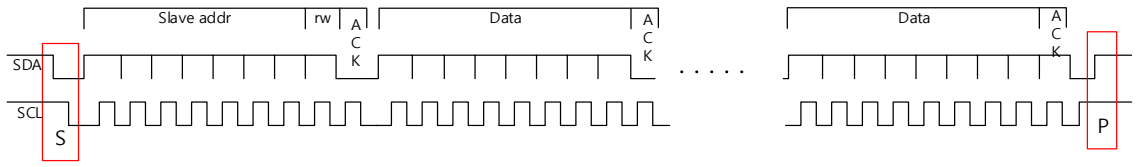


Figure 52. Complete Data Transfer with a 7-bit slave address

21.3.8 Operating Modes

The interface can operate in one of four following:

- Master Transmitter Mode
- Master Receiver Mode
- Slave Transmitter Mode
- Slave Receiver Mode

By default, it operates in slave mode. The interface switches from slave to master when it generates the mode bit in the I2Cx_CTR. And COREEN bit in the I2Cx_CTR must be switched from 1 to 0.

In Master mode

Master Transmitter Mode:

In this mode, data is transmitted from master to slave before the master transmitter mode can be entered and I2Cx_CTR must be initialized

Master Receiver Mode:

In this mode, data is received from slave to master before the master receive mode can be entered and I2Cx_CTR must be initialized

In Slave mode

Slave Transmitter Mode:

In this mode, data is transmitted from slave to master and setting of I2Cx_SADDR must be done.

Slave Receiver Mode:

In this mode, data is received from master to slave before the master transmitter mode can be entered and setting of I2Cx_SADDR must be done.

21.3.9 Interrupts

The I^2C can generate interrupt when the following conditions are observed:

- Start conditions on bus detected
- Stop conditions on bus detected
- Timeout error
- Master transaction completed
- Slave transaction received

I^2C bus have separate interrupt signals.

21.3.10 Master mode

21.3.10.1 Initialization

Figure 53 shows the command sequences available for the I^2C master.

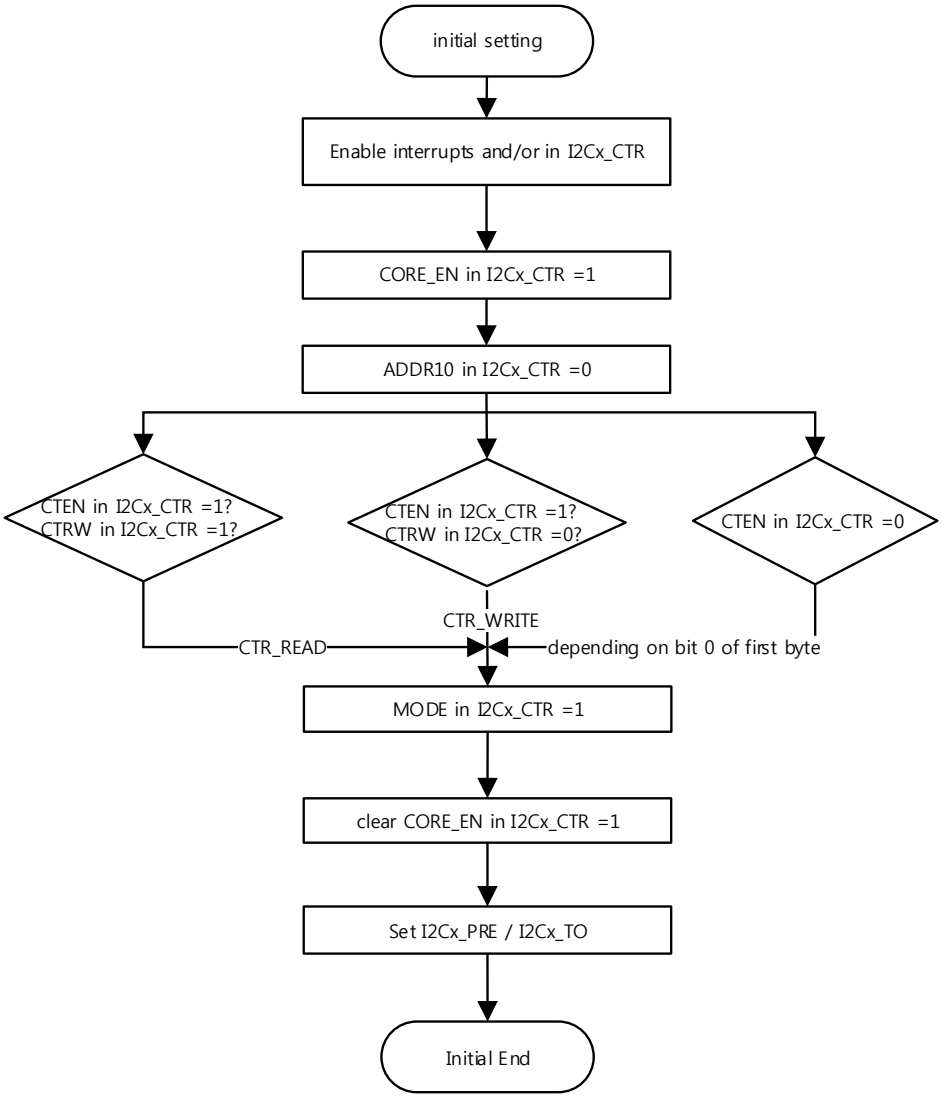


Figure 53. I2C initial setting

Figure 54 shows the master operation using a 7-bit slave address.

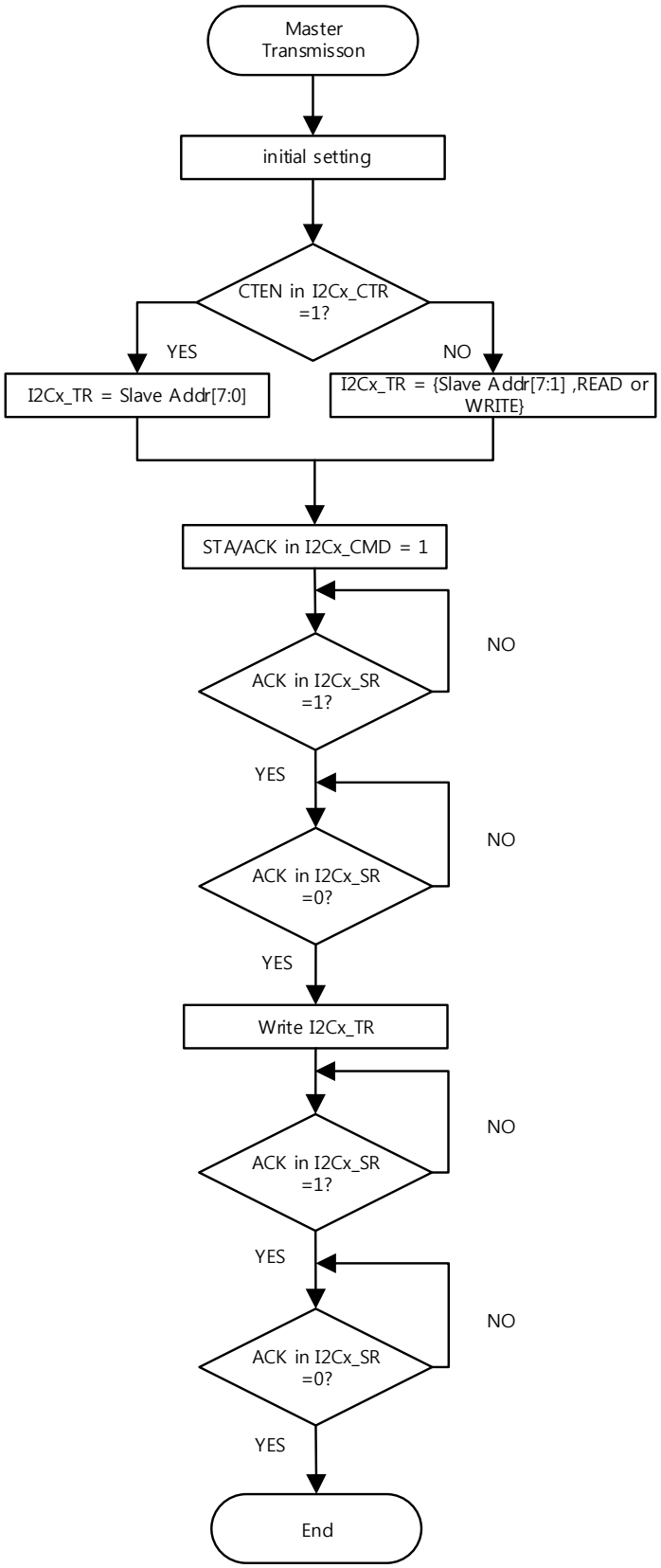


Figure 54. Master TRANSMIT with ADDR10=0 in the I2Cx_CTR

Figure 55 shows the operation of repeated START.

The repeated START operates for data read operation execution.

The operation sequences are Slave address, send data, repeated START, and send data.

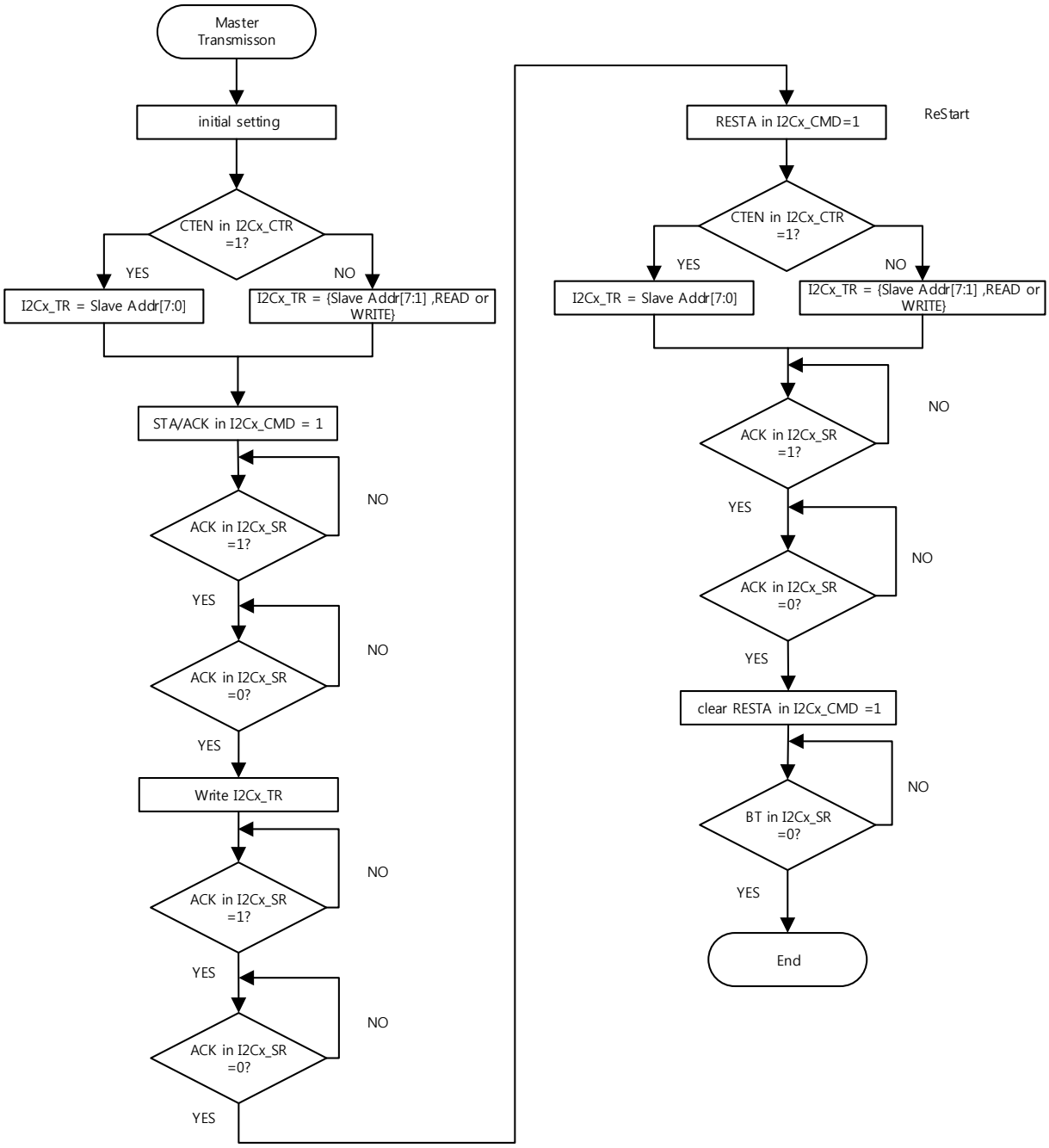


Figure 55. Master Transmit with Repeated START

21.3.11 Slave mode

Figure 56 shows the command sequences available for the I^2C slave.

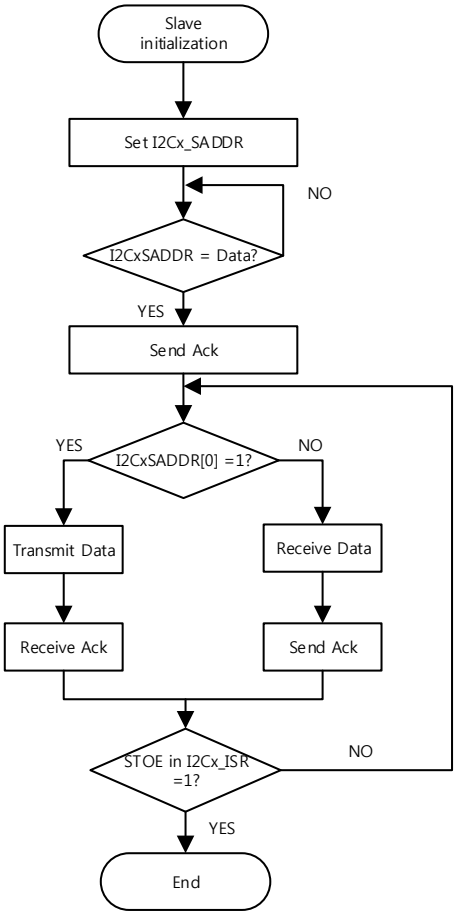


Figure 56. Slave Command Sequence

21.4 I2C0 Registers(Base address: 0x4000_8000)

21.4.1 I2C0 Prescaler Register(I2C0[1]_PRER)

Software must set value for register I2C0_PRER to select the appropriate data rate. The frequency is determined by the following formula:

Address offset: 0x00

Reset value: 0x0000_0014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	PRER							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[7:0] PRER – Prescaler Register

This field is used to prescaler F_{clk} in order to generate the clock period SCL use for data counters

$$\mathrm{SCL} = \frac{F_{clk}}{PRER * 2 + 6}$$

Where f_{clk} is the frequency of pclk. The value should be greater than or equal to 4.

PRER	Bit Freq(KHz) at F_{clk}(MHz)		
	8	20	48
37	**100**	X	X
57	67	X	X
97	40	**100**	X
237	17	42	**100**

[31:8] Reserved, must be kept at reset value

21.4.2 I2C0 Control Register(I2C0_CTR)

Address offset: 0x04

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

[1] The number of I2C, It means the 0,1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	COREEN	INTEREN	MODE	ADDR10	CTRRWN	CTREN	res	res
								R/W	R/W	R/W	R/W	R/W	R/W		

[1:0] Reserved, must be kept at reset value

[2] CTREN – Control enable

0: Disable Control mode

By eight bit of slave address

1: Enable Control mode

[3] CTRRWN – Write/Read mode control

0: Write mode

1: Read mode

When CTREN is '1', this bit is valid

[4] ADDR10 - Slave address 7bit Select

0: Slave address 7bit select

[5] MODE - Master / Slave Select

0: Slave mode

1: Master mode

[6] INTEREN - Interrupt Enable

0: interrupt disable

1: interrupt enable

[7] COREEN – Core Enable

0: core reset disable

1: core reset enable

[31:8] Reserved, must be kept at reset value

21.4.3 I2C0 Command Register(I2C0_CMDR)

Address offset: 0x08

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	STA	STO	ACK	RESTA	res	res	res	res
								R/W	R/W	R/W	R/W				

[3:0] Reserved, must be kept at reset value

[4] RESTA – Repeat start condition (master mode)

0: disable Repeat start

1: enable Repeat start

[5] ACK – Acknowledgement condition (master mode)

0: NACK condition

1: ACK condition

[6] STO – Stop Condition (master mode)

0: disable condition

1: enable condition

[7] STA – Start Condition (master mode)

0: disable Start condition

1: enable Start condition

[31:8] Reserved, must be kept at reset value

21.4.4 I2C0 Status Register(I2C0_SR)

Address offset: 0x0C

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	TX	RX	ACKT	BT	SA	SB	res	TO	SRW	ACKR
						R	R	R	R	R	R		R	R	R

[0] ACKR – Acknowledge Receive

[1] SRW – Slave Read/Write

This bit set by hardware when receive status.

[2] TO – Time Out

This bit set by hardware when the timeout occur by I2C0_TSR register setting value

[3] Reserved, must be kept at reset value

[4] SB – Slave Busy (Slave mode)

This bit set by hardware when the slave address and R/W bit have been transmitted and an acknowledgment bit has been received (waiting for data).

[5] SA – Slave Address Transmit (master mode)

This bit set by hardware when the Slave address have been transmitted.

[6] BT – Byte Transmit

This bit set by hardware when the 1byte data was transmitted except ack signal.

[7] ACKT – Acknowledge Transmit

This bit set by hardware when the ack signal was transmitted.

[8] RX – Receive status

[9] TX – Transmit status

This bit set by hardware when the data is transmitting and the data to be transmitted must be written in the I2C0_TXDR register.

[31:10] Reserved, must be kept at reset value

21.4.5 I2C0 Timeout Set Register(I2C0_TSR)

Address offset: 0x10

Reset value: 0x0000_FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSR															
R/W															

[15:0] TSR - Time Set

This register configures the retransmission timeout period. The default value is '0xFFFF'.

[31:16] Reserved, must be kept at reset value

21.4.6 I2C0 Slave Address Register(I2C0_SADDR)

Address offset: 0x14

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	res	res	res	res	res	res	SADDR							
								R/W							

[0] SADDR – Slave address bit 0

7-bit addressing mode(ADDR10=0)

CTREN = 0 : It indicates a R/W bit

CTREN = 1 : This bit are don't care

[7:1] SADDR[7:1] – Slave address bit 7:1

7-bit addressing mode (ADDR10=0)

These bits should be written with the 7-bit slave address to be sent.

[31:8] Reserved, must be kept at reset value

21.4.7 I2C0 Transmit Register(I2C0_TXR)

Address offset: 0x18

Reset value: 0x0000_00FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	TXD							
								R/W							

[7:0] TXD – 8-bit transmit data

Data byte to be transmitted to the I^2C bus.

[31:8] Reserved, must be kept at reset value

21.4.8 I2C0 Receive Register(I2C0_RXR)

Address offset: 0x1C

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	RXD							
								R							

[7:0] RXD – 8-bit receive data

Data byte received from the I^2C bus.

[31:8] Reserved, must be kept at reset value

21.4.9 I2C0 Interrupt Status Register(I2C0_ISR)

Address offset: 0x20

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	STAE	STOE	TOE	ACK_RXE	ACK_TXE
											R	R	R	R	R

[0]ACK_TXE – Acknowledge Transmit status

[1]ACK_RXE – Acknowledge Receive status

[2]TOE - Timeout detection flag

[3]STOE– STOP detection flag (master mode)

This flag is set by hardware when a STOP condition is detected on the bus and the peripheral is involved in this transfer: – either as a master, provided that the STOP

condition is generated by the peripheral. – or as a slave, provided that the peripheral has been addressed previously during this transfer.

[4] STAE – START detection flag (master mode)
This flag is set by hardware when a START condition is detected on the bus and the peripheral is involved in this transfer: – either as a master, provided that the START condition is generated by the peripheral. – or as a slave, provided that the peripheral has been addressed previously during this transfer.

[31:5] Reserved, must be kept at reset value

21.4.10 I2C0 Interrupt Status Clear Register(I2C0_ISCR)

Address offset: 0x24

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RST
															R/W

[0]RST – interrupt reset

All interrupt is clear.

(TXE,RXE,TSR,BT)

[31:1] Reserved, must be kept at reset value

21.4.11 I2C0 Interrupt Status Mask Register(I2C0_ISMR)

Address offset: 0x28

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	STAEM	STOEM	TOEM	ACK_	ACK_

														RXEM	TXEM
											R/CW1	R/CW1	R/CW1	R/CW1	R/CW1

[0]ACK_TXEM – Acknowledge Transmit status clear

Writing a 1 to this bit clears the ACK_TRANS bit in the I2C0_ISR register

Writing 0 has no effect

[1]ACK_RXEM – Acknowledge Receive status clear

Writing a 1 to this bit clears the ACK_RECV bit in the I2C0_ISR register

Writing 0 has no effect

[2]TOEM - Timeout interrupt clear

Writing a 1 to this bit clears the TO bit in the I2C0_ISR register

Writing 0 has no effect

[3]STOEM – STOP detection flag clear (master mode)

Writing a 1 to this bit clears the STOP bit in the I2C0_ISR register

Writing 0 has no effect

[4] STAEM – START detection flag clear (master mode)

Writing a 1 to this bit clears the STA bit in the I2C0_ISR register

Writing 0 has no effect

[31:5] Reserved, must be kept at reset value

21.5 Register map

The following Table 36 summarizes the I2C0 registers.

Table 36 I2C0 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	I2C0PRER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	COUNT																SCL/SCH Register
	reset value																	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	
0x04	I2C0CTR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	Core_en	Inter_en	mode	addr10	ctr_rw	ctr_en	res	res	Control Register
	reset value																									0	0	0	0	0	0			
0x08	I2C0CMD	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	STA	STO	ACK	rep_s	res	res	res	res	Command Register
	reset value																									0	0	0	0					
0x0C	I2C0SR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	txe	rxe	ack_trans	byte_trans	s_addr	bb	arb_lost	to	s_rw	ack_rec	Status Register
	reset value																							0	0	0	0	0	0	0	0	0	0	
0x10	I2C0TO	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	COUNT																Timeout Register
	reset value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x14	I2C0ADDR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ADDR								Slave address Register
	reset value																									0	0	0	0	0	0	0	0	
0x18	I2C0TXR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	Transmit Data								Transmit Register
	reset value																									1	1	1	1	1	1	1	1	
0x1C	I2C0RXR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	Receive Data								Receive Register
	reset value																									0	0	0	0	0	0	0	0	
0x20	I2C0ISR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	sta_e	sto-e	to	ack_rec_o	ack_tra_o	Interrupt Status Register
	reset value																												0	0	0	0	0	
0x24	I2C0ISCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	inter_rst	Interrupt Status Clear Register
	reset value																																0	
0x28	I2C0ISMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	sta_e	sto-e	to	ack_rec_o	ack_tra_o	Interrupt Status Mask Register
	reset value																												0	0	0	0	0	

21.6 I2C1 Registers(Base address : 0x4000_9000)

21.6.1 I2C1 Prescaler Register(I2C1[2]_PRER)

Software must set value for register I2C1_PRER to select the appropriate data rate. The frequency is determined by the following formula:

Address offset: 0x00

Reset value: 0x0000_0014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	PRER							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[7:0] PRER – Prescaler Register

This field is used to prescaler F_{clk} in order to generate the clock period SCL use for data counters

$$\mathrm{SCL} = \frac{F_{clk}}{PRER * 2 + 6}$$

Where F_{clk} is the frequency of pclk. The value should be greater than or equal to 4.

PRER	Bit Freq(KHz) at F_{clk}(MHz)		
	8	20	48
37	**100**	X	X
57	67	X	X
97	40	**100**	X
237	17	42	**100**

[31:8] Reserved, must be kept at reset value

21.6.2 I2C1 Control Register(I2C1_CTR)

Address offset: 0x04

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

[2] The number of I2C. It means the 0,1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	COREEN	INTEREN	MODE	ADDR10	CTRRWN	CTREN	res	res
								R/W	R/W	R/W	R/W	R/W	R/W		

[1:0] Reserved, must be kept at reset value

[2] CTREN – Control enable

0: Disable Control mode

By eight bit of slave address

1: Enable Control mode

[3] CTRRWN – Write/Read mode control

0: Write mode

1: Read mode

When CTREN is '1', this bit is valid

[4] ADDR10 - Slave address 7bit Select

0: Slave address 7bit select

[5] MODE - Master / Slave Select

0: Slave mode

1: Master mode

[6] INTEREN - Interrupt Enable

0: interrupt disable

1: interrupt enable

[7] COREEN – Core Enable

0: core reset disable

1: core reset enable

[31:8] Reserved, must be kept at reset value

21.6.3 I2C1 Command Register(I2C1_CMDR)

Address offset: 0x08

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	STA	STO	ACK	RESTA	res	res	res	res
								R/W	R/W	R/W	R/W				

[3:0] Reserved, must be kept at reset value

[4] RESTA – Repeat start condition (master mode)

0: disable Repeat start

1: enable Repeat start

[5] ACK – Acknowledgement condition (master mode)

0: NACK condition

1: ACK condition

[6] STO – Stop Condition (master mode)

0: disable condition

1: enable condition

[7] STA – Start Condition (master mode)

0: disable Start condition

1: enable Start condition

[31:8] Reserved, must be kept at reset value

21.6.4 I2C1 Status Register(I2C1_SR)

Address offset: 0x0C

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	TX	RX	ACKT	BT	SA	SB	res	TO	SRW	ACKR
						R	R	R	R	R	R		R	R	R

[0] ACKR – Acknowledge Receive

[1] SRW – Slave Read/Write

This bit set by hardware when receive status.

[2] TO – Time Out

This bit set by hardware when the timeout occur by I2C1_TSR register setting value

[3] Reserved, must be kept at reset value

[4] SB – Slave Busy (Slave mode)

This bit set by hardware when the slave address and R/W bit have been transmitted and an acknowledgment bit has been received (waiting for data).

[5] SA – Slave Address Transmit (master mode)

This bit set by hardware when the Slave address have been transmitted.

[6] BT – Byte Transmit

This bit set by hardware when the 1byte data was transmitted except ack signal.

[7] ACKT – Acknowledge Transmit

This bit set by hardware when the ack signal was transmitted.

[8] RX – Receive status

[9] TX – Transmit status

This bit set by hardware when the data is transmitting and the data to be transmitted must be written in the I2C1_TXDR register.

[31:10] Reserved, must be kept at reset value

21.6.5 I2C1 Timeout Set Register(I2C1_TSR)

Address offset: 0x10

Reset value: 0x0000_FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSR															
R/W															

[15:0] TSR - Time Set

This register configures the retransmission timeout period. The default value is '0xFFFF'.

[31:16] Reserved, must be kept at reset value

21.6.6 I2C1 Slave Address Register(I2C1_SADDR)

Address offset: 0x14

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	res	res	res	res	res	res	SADDR							
								R/W							

[0] SADDR – Slave address bit 0

7-bit addressing mode(ADDR10=0)

CTREN = 0 : It indicates a R/W bit

CTREN = 1 : This bit are don't care

[7:1] SADDR[7:1] – Slave address bit 7:1

7-bit addressing mode (ADDR10=0)

These bits should be written with the 7-bit slave address to be sent.

[31:8] Reserved, must be kept at reset value

21.6.7 I2C1 Transmit Register(I2C1_TXR)

Address offset: 0x18

Reset value: 0x0000_00FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	TXD							

								R/W

[7:0] TXD – 8-bit transmit data

Data byte to be transmitted to the I^2C bus.

[31:8] Reserved, must be kept at reset value

21.6.8 I2C1 Receive Register(I2C1_RXR)

Address offset: 0x1C

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	RXD							
								R							

[7:0] RXD – 8-bit receive data

Data byte received from the I^2C bus.

[31:8] Reserved, must be kept at reset value

21.6.9 I2C1 Interrupt Status Register(I2C1_ISR)

Address offset: 0x20

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	STAE	STOE	TOE	ACK_RXE	ACK_TXE
											R	R	R	R	R

[0]ACK_TXE – Acknowledge Transmit status

[1]ACK_RXE – Acknowledge Receive status

[2]TOE - Timeout detection flag

[3]STOE- STOP detection flag (master mode)

This flag is set by hardware when a STOP condition is detected on the bus and the peripheral is involved in this transfer: - either as a master, provided that the STOP condition is generated by the peripheral. - or as a slave, provided that the peripheral has been addressed previously during this transfer.

[4] STAE - START detection flag (master mode)

This flag is set by hardware when a START condition is detected on the bus and the peripheral is involved in this transfer: - either as a master, provided that the START condition is generated by the peripheral. - or as a slave, provided that the peripheral has been addressed previously during this transfer.

[31:5] Reserved, must be kept at reset value

21.6.10 I2C1 Interrupt Status Clear Register(I2C1_ISCR)

Address offset: 0x24

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RST
															R/W

[0]RST - interrupt reset

All interrupt is clear.

(TXE,RXE,TSR,BT)

[31:1] Reserved, must be kept at reset value

21.6.11 I2C1 Interrupt Status Mask Register(I2C1_ISMR)

Address offset: 0x28

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	STAEM	STOEM	TOEM	ACK_ RXEM	ACK_ TXEM
											R/CW1	R/CW1	R/CW1	R/CW1	R/CW1

[0]ACK_TXEM – Acknowledge Transmit status clear

Writing a 1 to this bit clears the ACK_TRANS bit in the I2C1_ISR register

Writing 0 has no effect

[1]ACK_RXEM – Acknowledge Receive status clear

Writing a 1 to this bit clears the ACK_RECV bit in the I2C1_ISR register

Writing 0 has no effect

[2]TOEM - Timeout interrupt clear

Writing a 1 to this bit clears the TO bit in the I2C1_ISR register

Writing 0 has no effect

[3]STOEM – STOP detection flag clear (master mode)

Writing a 1 to this bit clears the STOP bit in the I2C1_ISR register

Writing 0 has no effect

[4] STAEM – START detection flag clear (master mode)

Writing a 1 to this bit clears the STA bit in the I2C1_ISR register

Writing 0 has no effect

[31:5] Reserved, must be kept at reset value

21.7 Register map

The following Table 37 summarizes the I2C1 registers.

Table 37 I2C1 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	I2C1PRER	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	COUNT																SCL/SCH Register
	reset value																	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	
0x04	I2C1CTR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	Core_en	Inter_en	mode	addr10	ctr_rw	ctr_en	res	res	Control Register
	reset value																									0	0	0	0	0	0			
0x08	I2C1CMD	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	STA	STO	ACK	rep_s	res	res	res	res	Command Register
	reset value																									0	0	0	0					
0x0C	I2C1SR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	txe	rxe	ack_trans	byte_trans	s_addr	bb	arb_lost	to	s_rw	ack_rec	Status Register
	reset value																							0	0	0	0	0	0	0	0	0	0	
0x10	I2C1TO	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	COUNT																Timeout Register
	reset value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x14	I2C1ADDR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ADDR								Slave address Register
	reset value																									0	0	0	0	0	0	0	0	
0x18	I2C1TXR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	Transmit Data								Transmit Register
	reset value																									1	1	1	1	1	1	1	1	
0x1C	I2C1RXR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	Receive Data								Receive Register
	reset value																									0	0	0	0	0	0	0	0	
0x20	I2C1ISR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	sta_e	sto-e	to	ack_rec_o	ack_tra_o	Interrupt Status Register
	reset value																												0	0	0	0	0	
0x24	I2C1ISCR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	inter_rst	Interrupt Status Clear Register
	reset value																																0	
0x28	I2C1ISMR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	sta_e	sto-e	to	ack_rec_o	ack_tra_o	Interrupt Status Mask Register
	reset value																												0	0	0	0	0	

22 UART(Universal Asynchronous Receive Transmit)

22.1 Introduction

The UART supports synchronous one-way communication, half-duplex single wire communication, and multiprocessor communications(CTS/RTS).

22.2 Features

- Serial-to-parallel conversion on data received from a peripheral device
- Parallel-to-serial conversion on data transmitted to the peripheral device
- Data size of 5,6,7 and 8 its
- One or two stop bits
- Even, odd, stick, or no-parity bit generation and detection
- Support of hardware flow control
- Programmable FIFO disabling for 1-byte depth.
- Programmable use of UART or IrDA SIR input/output
- False start bit detection

22.3 Functional description

UART bidirectional communication requires a minimum of two pins: RX, TX

The frame are comprised of:

- An Idle Line prior to transmission or reception
- A start bit
- A data word (8 or 9 bits) least significant bit first
- 1, 1.5, 2 Stop bits indicating that the frame is complete
- The USART interface uses a baud rate generator
- A status register (UART1_RISR)
- data registers (UART1DR)
- A baud rate register (UART1_IBRD,UART1_FBRD)

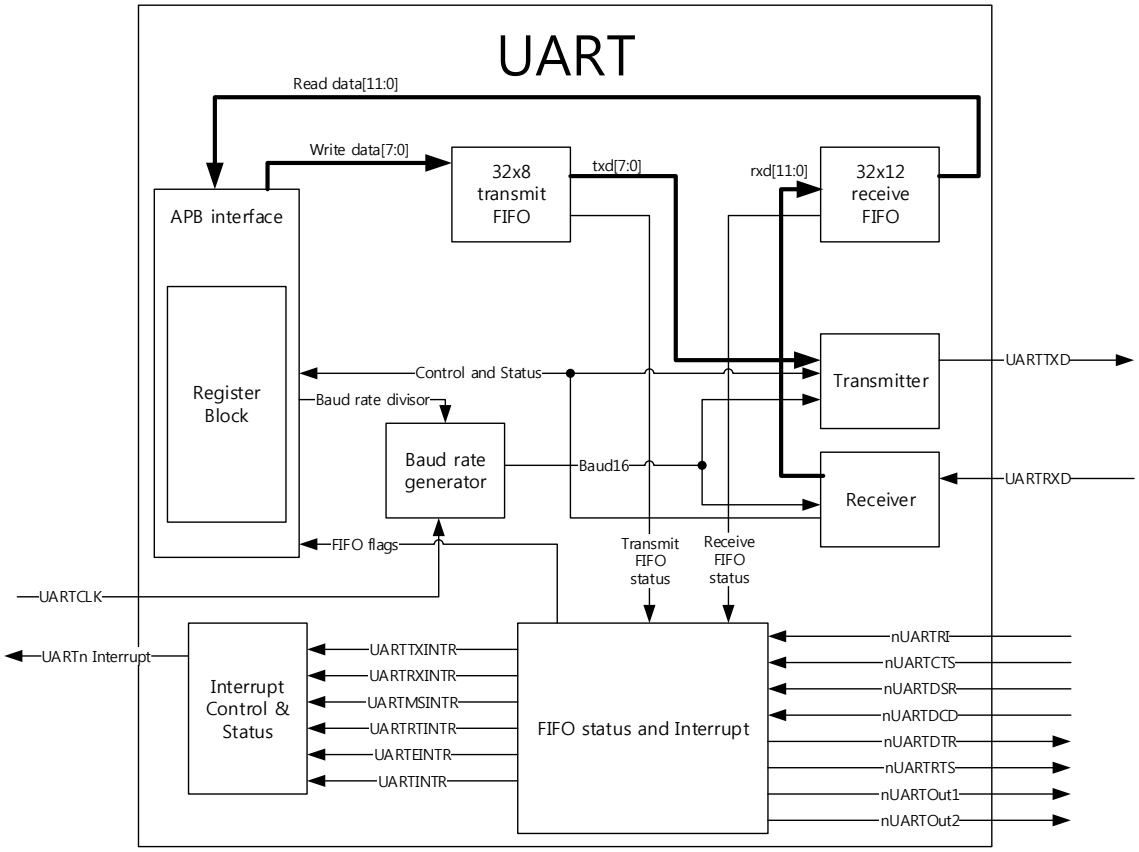


Figure 57. UART0,1 Block diagram

Figure 58 shows the UART character frame

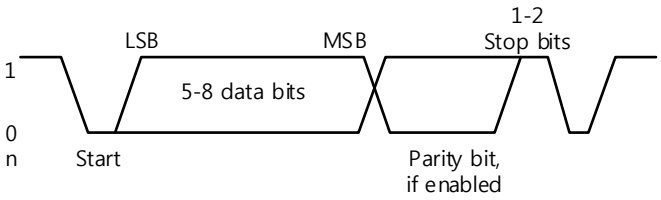


Figure 58. UART character frame

22.3.1 Baud rate calculation

UARTx can operate with or without using the Fractional Divider. The baud rate divisor is a 22-bit number consisting the UARTxIBRD(16-bit integer) and the UARTxFBRD(6-bit fractional). This is used by the baud rate generator to determine the bit period.

- Baud Rate Divisor $= \frac{\text{UARTCLK}}{(16 * baud\ rate)} = BRD_I + BRD_F$

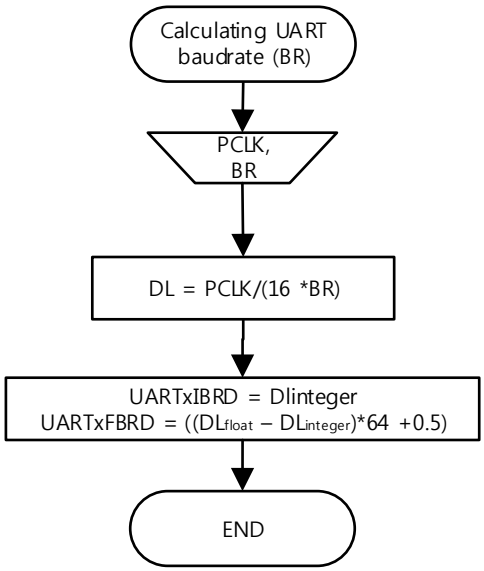


Figure 59. UART divider flow chart

Figure 60 show how to set the UART Initial value.

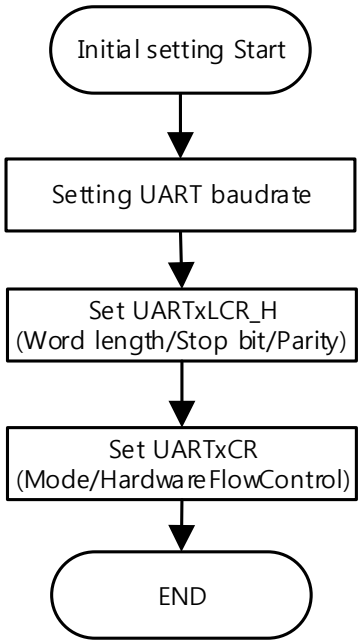


Figure 60. UART Initial setting flow chart

22.3.2 Data transmission

Data transmitted is stored in a 32-byte FIFOs. Transmit data is written into the transmit FIFO for transmission. If UART is enabled, it causes a data frame to start transmitting with parameters indicated in the UARTxLCR_H.

Data continues to transmit until there is no data left in the transmit FIFO. The BUSY bit of UARTxFR is '1' as soon as data is written to the transmit FIFO, which means the FIFO is not empty, and remains as '1' while data is being transmitted.

22.3.3 Data receive

Received data is stored in the 32-byte FIFOs. When a start bit has been received, it begins running and data is sampled on the eighth cycle of that counter in UART mode. A valid stop bit is confirmed if UARTRXD is '1'. When a full word is received, the data is stored in the receive FIFO. Error bit is stored in bit[10:8] of UARTxCR and overrun is stored in bit[11] of UARTxCR.

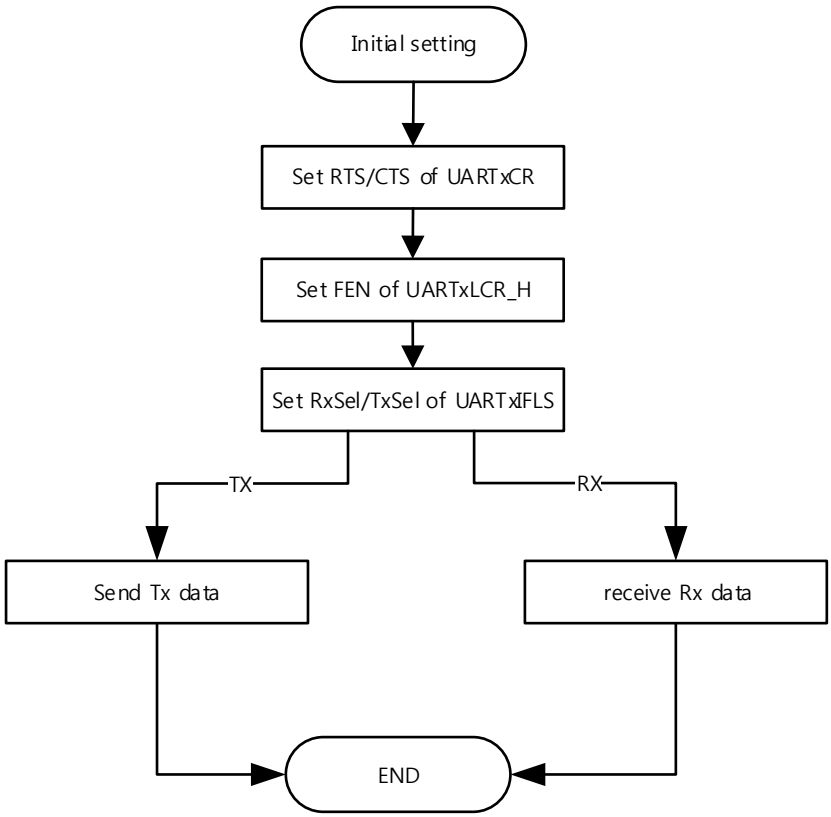


Figure 61. Transmit and Receive data flow chart

22.3.4 Hardware flow control

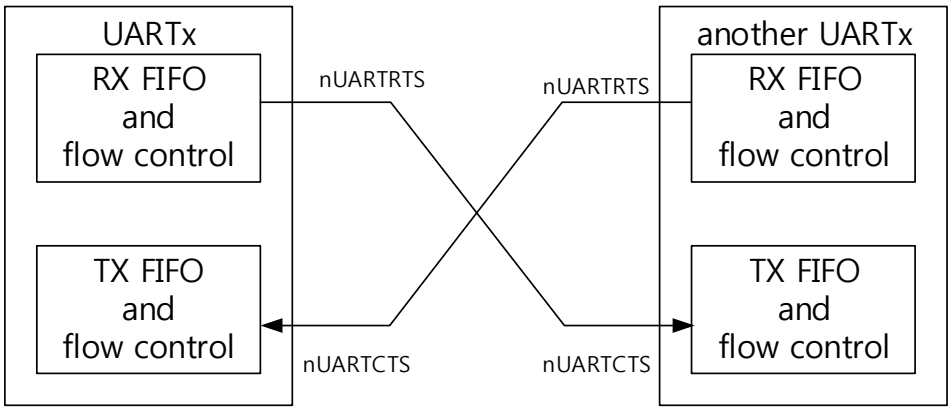


Figure 62. Hardware flow control description

The RTS flow control is enabled by setting the RTSen of UARTxCR. If RTS is enabled, the data flow is controlled as follows.

When the receiver FIFO level reaches the programmed trigger level, nUARTRTS(pin) is asserted(to a low value). nUARTRTS is reasserted(to a low level) once the receiver FIFO has reached the previous trigger level. The reasserted of nUARTRTS signals to the sending UART to continue transmitting data.

The CTS flow control is enabled, the transmitter can only transmit data when nUARTCTS is asserted. When nUARTCTR is re-asserted(to a low) the transmitter sends the next byte. To stop the transmitter from sending the following byte, nUARTCTS must be released before the middle of the last stop bit that is currently being sent.

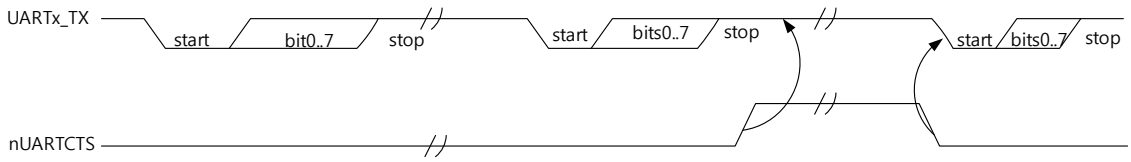


Figure 63. CTS Functional Timing

Figure 64 shows how software should use the RTS/CTR.

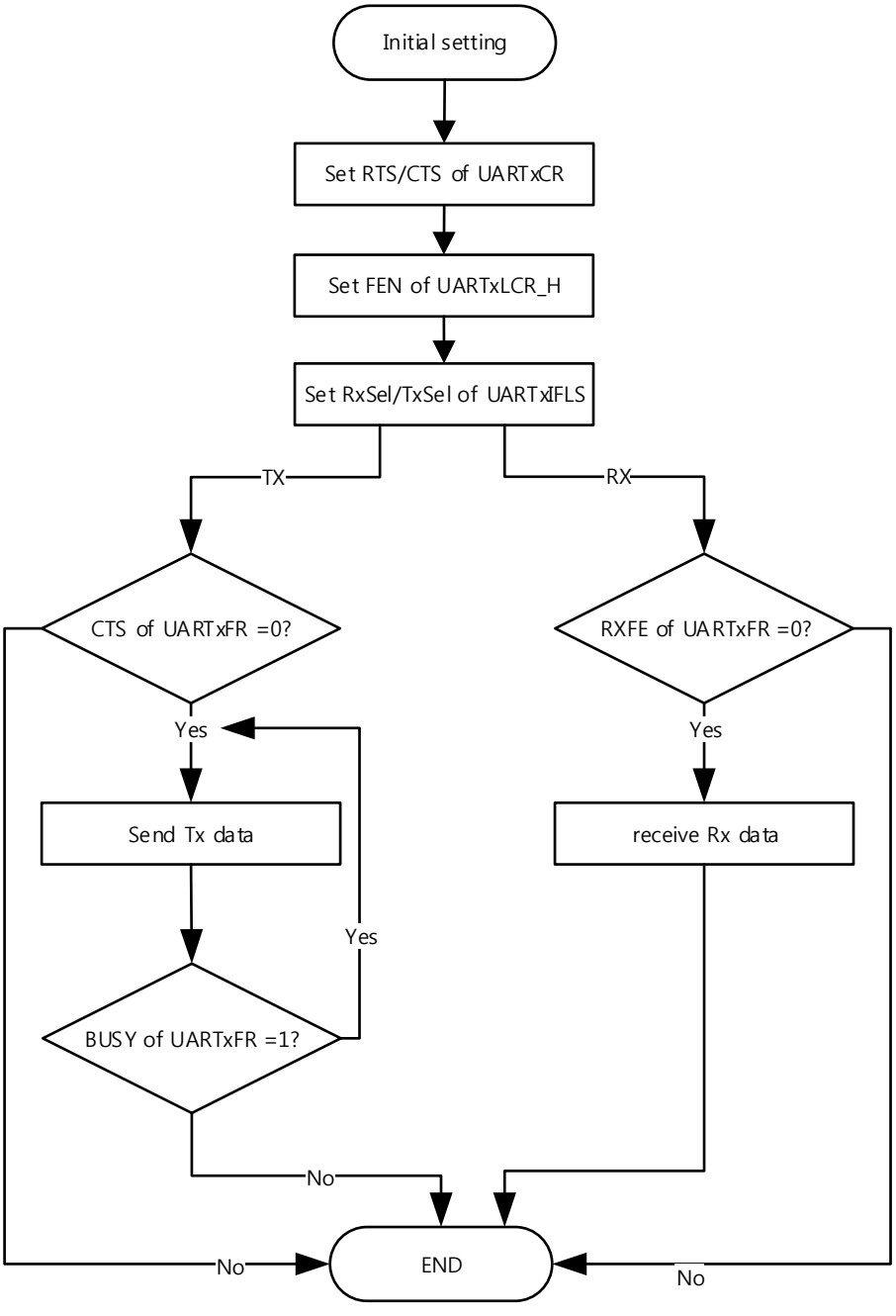


Figure 64. Algorithm for setting CTS/RTS flowchart

22.4 UART0 Registers(Base address: 0x4000_C000)

22.4.1 UART0DR (UART0 Data Register)

Address offset: 0x000

Reset value: 0x0000_0000

The UART0DR is the data register.

The write operation initiates transmission from the UART. The data is prefixed with a start bit, appended with the appropriate parity bit(if parity is enabled), and a stop bit. The resultant word is then transmitted.

The received data byte is read by performing reads from the UARTDR register along with the corresponding status information.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	OE	BE	PE	FE	DATA							
				R	R	R	R	R/W							

[11] OE – Overrun error

0: data is empty

1: data is received and the receive FIFO is already full.

[10] BE – Break error

1: if a break condition was detected, indicating that the received data input was held LOW of longer than a full-word transmission time(defined as start, data, parity and stop bits)

[9] PE – Parity error

1: it indicates that the parity of the received, it indicates that the parity of the received data character does not match the parity that the EPS and SPS bits in the line control register, UARTLCR_H

[8] FE – Framing error

1: it indicates that the received

[7:0] DATA – Receive (READ)/Transmit (WRITE) data

22.4.2 UART0RSR/ECR (UART0 Receive Status Register/Error Clear Register)

Address offset: 0x004

Reset value: 0x0000_0000

The UART0RSR/ECR is the receive status register/error clear register.

Receive status can also be read from the UART0RSR register.

A write to the UART0ECR register clears the framing, parity, break, and overrun errors.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	OE	BE	PE	FE

[3] OE – Overrun error

This bit is set to 1 if data is received and the FIFO is already full.

This bit is cleared to 0 by a write to UART0ECR

[2] BE – Break error

This bit is cleared to 0 by a write to UART0ECR

[1] PE – Parity error

When set to 1, it indicates that the parity of the received data character does not match

the parity that the EPS and SPS bits in the line control register, UARTLCR_H select

This bit is cleared to 0 by a write to UART0ECR

[0] FE – Framing error

When set to 1, in indicates that the received character didn't have a valid stop bit

This bit is cleared to 0 by a write to UART0ECR

22.4.3 UART0FR (UART0 Flag Register)

Address offset: 0x0018

Reset value: 0bx11000xxx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	RI	TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS
							R	R	R	R	R	R	R	R	R

[8] RI – Ring indicator

This bit is the complement of the UART ring indicator, UART0RI.

1: When nUART0RI is LOW

[7] TXFE – Transmit FIFO empty

This bit depends on the state of the FEN bit in the line control register, UARTLCR_H.

0: The bit is set when transmit holding register is empty.

1: The bit is set when transmit FIFO is empty

[6] RXFF – Receive FIFO full

This bit depends on the state of the FEN bit in the line control register, UARTLCR_H.

0: The bit is set when the receive holding register is full

1: The bit is set when the receive FIFO is full

[5] TXFF – Transmit FIFO full

This bit depends on the state of the FEN bit in the line control register, UARTLCR_H.

0: The bit is set when transmit holding register is full.

1: The bit is set when transmit FIFO is full.

[4] RXFE – Receive FIFO empty

This bit depends on the state of the FEN bit in the line control register, UARTLCR_H.

0: The bit is set when the receive holding register is empty.

1: The bit is set when the receive FIFO is empty.

[3] BUSY – UART busy

1: the UART is busy transmitting data

[2] DCD – Data carrier detect

This bit is the complement of the UART data carrier detect, UART0DCD, status input

1: The bit is the complement of the UART data carrier detect

[1] DSR – Data set ready

This bit is the complement of the UART data set ready, UART0DSR, status input

1: The bit is the complement of the UART data set ready

[0] CTS – Clear to send

This bit is the complement of the UART clear to send, UART0CTS, status input

1: The bit is the complement of the UART clear to send

22.4.4 UART0ILPR (UART0 IrDA Low-Power Counter Register)

Address offset: 0x0020

Reset value: 0x00

The UARTILPR Register is the IrDA low-power counter register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	ILPDVSR							
								R/W							

[7:0] ILPDVSR – 8-bit low-power divisor value

These bits are cleared to 0 at reset

$$\text{ILPDVSR} = (F_{UARTCLK}/F_{IrLPBaud16})$$

Where, $F_{IrLPBaud16}$ is nominally 1.8432MHz

The divisor is 1.42MHz < $F_{IrLPBaud16}$ < 2.12MHz, results in a low-power pulse duration of 1.41 – 2.11us.

22.4.5 UART0IBRD (UART0 Integer Baud Rate Register)

Address offset: 0x0024

Reset value: 0x00

The UART0IBRD Register is the integer part of the baud rate divisor value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAUD DIVINT															
w															

[15:0] BAUD DIVINT – The integer baud rate divisor.

These bits are cleared to 0 on reset

22.4.6 UART0FBRD (UART0 Fractional Baud Rate Register)

Address offset: 0x0028

Reset value: 0x00

The UART0FBRD register is the fractional part of the baud rate divisor value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	BAUD DIVFRAC					
										w					

[5:0] BAUD DIVFRAC – The fractional baud rate divisor.

These bits are cleared to 0 on reset

The baud rate divisor is calculated as follows:

Baud rate divisor BAUDDIV = $(F_{UARTCLK}/(16 \times Baud\ rate))$

Where, $F_{UARTCLK}$ is the UART reference clock frequency.

The BAUDDIV is comprised of the integer value (BAUD DIVINT) and the fractional value (BAUD DIVFRAC).

Example 1

If the required baud rate is 115200 and UARTCLK = 8MHz then:

Baud rate divisor = $(8 \times 10^6)/(16 \times 115200) = 4.340278$

This means BRD_I = 4 and BRD_F = 0.340278

(Therefore, UART0IBRD = 4)

Therefore, UART0FBRD = $\text{inerger}[(0.340278 \times 64) + 0.5] = 22$

Generated baud rate divider = $\text{UART0IBRD} + (\text{UART0FBRD}/64) = 4.34375$

Generated baud rate = $(8 \times 10^6)/(16 \times 4.34375) = 115107.914$

Error = $(115108 - 115200)/(115200) \times 100 = -0.07861\%$

When UartCLK = 8MHz

Integer divisor	Fractional divisor	Required bit rate(bps)	Generated bit rate(bps)	Error%
0x2	0x0B	230400	2.171875	-0.07994
0x4	0x16	115200	4.34375	-0.07994
0x6	0x21	76800	6.515625	-0.07994
0x8	0x2C	57600	8.6875	-0.07994
0x22	0x2E	14400	34.71875	0.010001

22.4.7 UART0LCR_H (UART0 Line Control Register)

Address offset: 0x002C

Reset value: 0x00

The UART0LCR_H register is the line control register. This register accesses bits 29 to 22 of the UART line control register, UART0LCR.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	SPS	WLEN		FEN	STP2	EPS	PEN	BRK
								R/W							

[7] SPS – Stick parity select

0: stick parity is disable

1: either:

The parity bit is transmitted and checked as a 1 when EPS bit set '0'

The parity bit is transmitted and checked as a 0 when EPS bit set '1'

[6:5] WLEN - Word length

00	01	10	11
5 bits	6 bits	7 bits	8 bits

[4] FEN – Enable FIFO

0: The FIFO become 1-byte-deep holding register.

1: The transmit and receive FIFO buffers are enable (FIFO mode)

[3] STP2 – Two stop bit select

1: Two stop bits are transmitted at the end of the frame

[2] EPS – Even parity select

0: odd parity.

1: even parity

[1] PEN – Parity enable

0: parity is disabled and no parity bit added to the data frame

1: parity checking and generations is enabled

[0] BRK – Send break

0: For normal use, the bit must be cleared to 0

1: The low-level is continually output on the UARTTXD output

PEN	EPS	SPS	Parity bit(Transmitted or checked)
0	X	X	Not transmitted or checked
1	1	0	Even parity
1	0	0	Odd parity
1	0	1	1
1	1	1	0

22.4.8 UART0CR (UART0 Control register)

Address offset: 0x0030

Reset value: 0x0300

The UART0CR register is the control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTSEn	RTSEn	Out2	Out1	RTS	DTR	RXE	TXE	res					SIRLP	SIREN	UARTEN

[15] CTSEn – CTS hardware flow control enable.

1: CTS hardware flow control is enable. Data is only transmitted when the UART0CTS signal is asserted.

[14] RTSEn – RTS hardware flow control enable

1: RTS hardware flow control is enable. Data is only requested when there is space in the receive FIFO for it to be received.

[13] Out2

This bit is the complement of the UART Out2 (nUARTOut2) modem status output.

That is, when the bit is programmed to 1, the output is 0.

For DTE this can be used as “Ring Indicator” (RI).

[12] Out1

This bit is the complement of the UART Out1 (nUARTOut1) modem status output.

That is, when the bit is programmed to 1 the output is 0.

For DTE this can be used as “Data Carrier Detect”(DCD).

[11] RTS – Request to send

This bit is the complement of the UART request to send, UART0RTS, modem status output.

That is, when the bit is programmed to 1 then UART0RTS is LOW.

[10] DTS – Data transmit ready

This bit is the complement of the UART data transmit ready, UART0DTR, modem status output.

That is, when the bit is programmed to 1 then UART0DTR is LOW.

[9] RXE – Receive enable

If this bit is set to 1, the receive section of the UART is enabled.

Data reception occurs for either UART signals or SIR signals depending on the setting of the SIREN bit. When the UART is disabled in the middle of reception, it completes the current character before stopping.

[8] TXE – Transmit enable

1: The transmit section of the UART is enabled,

[7:3] Reserved

[2] SIRLP – SIR low-power IrDA mode

0: low-level bits are transmitted as an active high pulse with a width of 3/16th of the bit period.

1: low-level bits are transmitted with a pulse width that is 3 times the period of the IrLPBaud16 input signal, regardless of the selected bit rate.

[1] SIREN – SIR enable

0: IrDA SIR ENDEC is disable

1: IrDA SIR ENDEC is enable

[0] UARTEN – Loopback enable

0: UART is disabled

1: UART is enabled

Program the control registers as follows:

1. Disable the UART.
2. Wait for the end of transmission or reception of the current character.
3. Flush the transmit FIFO by setting the FEN bit to 0 in the Line Control Register, UARTLCR_H.
4. Reprogram the UARTCR Register.
5. Enable the UART.

22.4.9 UART0IFLS (UART0 Interrupt FIFO Level Select Register)

Address offset: 0x0034

Reset value: 0x12

The UARTIFLS register is the interrupt FIFO level select register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	RXIFLSEL			TXIFLSEL		
										W			W		

[5:3] RXIFLSEL – Receive interrupt FIFO level select

7	6	5	4	3	2	1	0
Reserved			7/8 full	3/4 full	1/2 full	1/4 full	1/8 full

[2:0] TXIFLSEL – Transmit interrupt FIFO level select

7	6	5	4	3	2	1	0
Reserved			7/8 full	3/4 full	1/2 full	1/4 full	1/8 full

22.4.10 UART0IMSC (UART0 Interrupt Mask Set/Clear Register)

Address offset: 0x0038

Reset value: 0x00

The UART0IMSC register is the interrupt mask set/clear interrupts. When a bit of UART0IMSC is '1' and the corresponding bit of interrupt register is '1', an interrupt will be issued.

In other words, if a bit of UART0IMSC is '0', an interrupt will not be issued even if the corresponding bit of interrupt register is '1'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	res	res	res	OEIM	BEIM	PEIM	FEIM	RTIM	TXIM	RXIM	DSR MIM	DCD MIM	CTS MIM	RIMI M
					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[10] OEIM – Overrun error interrupt mask

0: Disable UART0OEINTR

1: Enable UART0OEINTR

[9] BEIM – Break error interrupt mask

0: Disable UART0BEINTR

1: Enable UART0BEINTR

[8] PEIM – Parity error interrupt mask

0: Disable UART0EINTR

1: Enable UART0EINTR

[7] FEIM – Framing error interrupt mask

0: Disable UART0FEINTR

1: Enable UART0FEINTR

[6] RTIM – Receive timeout interrupt mask

0: Disable UART0RTINTR

1: Enable UART0RTINTR

[5] TXIM – Transmit interrupt mask

0: Disable UART0TXINTR

1: Enable UART0TXINTR

[4] RXIM – Receive interrupt mask

0: Disable UART0RXINTR

1: Enable UART0RXINTR

[3] DSRMIM – nUART0DSR modem interrupt mask

0: Disable UART0DSRINTR

1: Enable UART0DSRINTR

[2] DCDMIM – nUART0DCD modem interrupt mask

0: Disable UART0DCDINTR

1: Enable UART0DCDINTR

[1] CTSMIM – nUART0CTS modem interrupt mask

0: Disable UART0CRSINTR

1: Enable UART0CRSINTR

[0] RIMIM – nUART0RI modem interrupt mask

0: Disable UART0RIINTR

1: Enable UART0RIINTR

22.4.11 UART0RIS (UART0 Raw Interrupt Status Register)

Address offset: 0x003C

Reset value: 0x00-

The UART0RIS register indicates the raw interrupt status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	OE RIS	BE RIS	PE RIS	FE RIS	RT RIS	TX RIS	RX RIS	DRR RMIS	DCD RMIS	CTSR MIS	RI RMIS
					R	R	R	R	R	R	R	R	R	R	R

[10] OERIS – Overrun error interrupt status

It indicates state of the UART0OEINTR interrupt.

[9] BERIS – Break error interrupt status

It indicates state of the UART0BEINTR interrupt.

[8] PERIS – Parity error interrupt status

It indicates state of the UART0PEINTR interrupt.

[7] FERIS – Framing error interrupt status

It indicates state of the UART0FEINTR interrupt.

[6] RTRIS – Receive timeout interrupt status

It indicates state of the UART0RTINTR interrupt.

[5] TXRIS – Transmit interrupt status

It indicates state of the UART0TXINTR interrupt.

[4] RXRIS – Receive interrupt status

It indicates state of the UART0RXINTR interrupt.

[3] DSRRMIS – nUART0DSR modem interrupt status

It indicates state of the UART0DSRINTR interrupt.

[2] DCDRMIS – nUART0DCD modem interrupt status

It indicates state of the UART0DCDINTR interrupt.

[1] CTSRMIS – nUART0CTS modem interrupt status

It indicates state of the UART0CTSINTR interrupt.

[0] RIRMIS – nUART0RI modem interrupt status

It indicates state of the UART0RIINTR interrupt.

22.4.12 UART0MIS (UART0 Masked Interrupt Status Register)

Address offset: 0x0040

Reset value: 0x00-

The UART0MIS register is the masked interrupt status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	OEMIS	BEMIS	PEMIS	FEMIS	RTMIS	TXMIS	RXMIS	DRRMMIS	DCDMMIS	CTSMMIS	RIMMIS
					R	R	R	R	R	R	R	R	R	R	R

[10] OEMIS – Overrun error masked interrupt status

It indicates state of the UART0OEINTR interrupt.

[9] BEMIS – Break error masked interrupt status

It indicates state of the UART0BEINTR interrupt.

[8] PEMIS – Parity error masked interrupt status

It indicates state of the UART0PEINTR interrupt.

[7] FEMIS – Framing error masked interrupt status

It indicates state of the UART0FEINTR interrupt.

[6] RTMIS – Receive timeout masked interrupt status

It indicates state of the UART0RTINTR interrupt.

[5] TXMIS – Transmit masked interrupt status

It indicates state of the UART0TXINTR interrupt.

[4] RXMIS – Receive masked interrupt status

It indicates state of the UART0RXINTR interrupt.

[3] DSRMMIS – nUART0DSR modem masked interrupt status

It indicates state of the UART0DSRINTR interrupt.

[2] DCDMMIS – nUART0DCD modem masked interrupt status

It indicates state of the UART0DCDINTR interrupt.

[1] CTSMMIS – nUART0CTS modem masked interrupt status

It indicates state of the UART0CTSINTR interrupt.

[0] RIMMIS – nUART0RI modem masked interrupt status

It indicates state of the UART0RIINTR interrupt.

22.4.13 UART0ICR (UART0 Interrupt Clear Register)

Address offset: 0x0044

Reset value: -

The UART0ICR register is the interrupt clear register and is write-only.

31	30	29	28	27	26	25	24	23		22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res		res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7		6	5	4	3	2	1	0
res	res	res	res	res	OEIC	BEIC	PEIC	FEIC		RTIC	TXIC	RXIC	DSR MIC	DCD MIC	CTS MIC	RI MIC
					R	R	R	R		R	R	R	R	R	R	R

[10] OEIC – Overrun error interrupt clear

Clear the UART0OEINTR interrupt.

[9] BEIC – Break error interrupt clear

Clear the UART0BEINTR interrupt.

[8] PEIC – Parity error interrupt clear

Clear the UART0PEINTR interrupt.

[7] FEIC – Framing error interrupt clear

Clear the UART0FEINTR interrupt.

[6] RTIC – Receive timeout interrupt clear

Clear the UART0RTINTR interrupt.

[5] TXIC – Transmit interrupt clear

Clear the UART0TXINTR interrupt.

[4] RXIC – Receive interrupt clear

Clear the UART0RXINTR interrupt.

[3] DSRMIC – nUART0DSR modem interrupt clear

Clear the UART0DSRINTR interrupt.

[2] DCDMIC – nUART0DCD modem interrupt clear

Clear the UART0DCDINTR interrupt.

[1] CTSMIC – nUART0CTS modem interrupt clear

Clear the UART0CTSINTR interrupt.

[0] RIMIC – nUART0RI modem interrupt clear

Clear the UART0RIINTR interrupt.

22.5 Register map

The following Table 38 summarizes the UART0 registers.

Table 38 UART0 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x000	UART0DR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OE	BE	PE	FE	DATA								Data Register
	reset value																					0	0	0	0	0	0	0	0	0	0	0	0	
0x004	UART0RSR/ UART0ECR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CE	BE	PE	FE	Receive Status/Error Clear Register
	reset value																													0	0	0	0	
0x018	UART0FR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RI	TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS	Flage Register
	reset value																								X	1	1	0	0	0	X	X	X	
0x020	UART0ILPR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ILPDVSR								IrDA Low-Power Counter Register
	reset value																									0	0	0	0	0	0	0	0	
0x024	UART0IBRD	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	BAUD DIVINT																Integer Baud Rate Register
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x028	UART0FBRD	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	BAUD DIVFRAC							Fractional Baud Rate Register
	reset value																										0	0	0	0	0	0	0	
0x02C	UART0LCR_H	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	SPS	WLEN			FEN	STP2	EPS	PEN	BRK	Line Control. Register
	reset value																									1	1	1	1	1	1	1	1	
0x030	UART0CR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CTSEn	RTSEn	Out2	out1	RTS	DTR	RXE	TXE	res	res	res	res	res	SIRLP	SIREN	UARTO	Control Register
	reset value																	0	0	1	1	0	0	0	0						0	0	0	
0x034	UART0IFLS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RXIFLSEL			TXIFLSEL			Interrupt FIFO Level Select Register
	reset value																											0	1	0	0	1	0	
0x038	UART0IMSC	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OEIM	BEIM	PEIM	FEIM	RTIM	TXIM	RXIM	DSRMIM	DCDMIM	CTSMIM	RIMIM	Interrupt Mask Set/Clear Register
	reset value																						0	0	0	0	0	0	0	0	0	0	0	
0x03C	UART0RIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OERIS	BERIS	PERIS	FERIS	RTRIS	TXRIS	RXRIS	DRRMIS	DCDRMIS	CTSRMIS	RIRMIS	Raw Interrupt Status Register
	reset value																						0	0	0	0	0	0	0	0	0	0	0	
0x040	UART0MIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OEMIS	BEMIS	PEMIS	FEMIS	RTMIS	TXMIS	RXMIS	DRRMMIS	DCDMMIS	CTSMMIS	RIMMIS	Masked Interrupt StatusRegister
	reset value																						0	0	0	0	0	0	0	0	0	0	0	
0x044	UART0ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OEIC	BEIC	PEIC	FEIC	RTIC	TXIC	RXIC	DSRMIC	DCDMIC	CTSMIC	RIMMIC	Interrupt Clear Register
	reset value																						0	0	0	0	0	0	0	0	0	0	0	

22.6 UART1 Registers(Base address: 0x4000_D000)

22.6.1 UART1DR (UART1 Data Register)

Address offset: 0x000

Reset value: 0x0000_0000

The UART1DR is the data register.

The write operation initiates transmission from the UART. The data is prefixed with a start bit, appended with the appropriate parity bit(if parity is enabled), and a stop bit. The resultant word is then transmitted.

The received data byte is read by performing reads from the UARTDR register along with the corresponding status information.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	OE	BE	PE	FE	DATA							
				R	R	R	R	R/W							

[11] OE – Overrun error

0: data is empty

1: data is received and the receive FIFO is already full.

[10] BE – Break error

1: if a break condition was detected, indicating that the received data input was held LOW of longer than a full-word transmission time(defined as start, data, parity and stop bits)

[9] PE – Parity error

1: it indicates that the parity of the received, it indicates that the parity of the received data character does not match the parity that the EPS and SPS bits in the line control register, UARTLCR_H

[8] FE – Framing error

1: it indicates that the received

[7:0] DATA – Receive (READ)/Transmit (WRITE) data

22.6.2 UART1RSR/ECR (UART1 Receive Status Register/Error Clear Register)

Address offset: 0x004

Reset value: 0x0000_0000

The UART1RSR/ECR is the receive status register/error clear register.

Receive status can also be read from the UART1RSR register.

A write to the UART1ECR register clears the framing, parity, break, and overrun errors.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	OE	BE	PE	FE

[3] OE – Overrun error

This bit is set to 1 if data is received and the FIFO is already full.

This bit is cleared to 0 by a write to UART1ECR

[2] BE – Break error

This bit is cleared to 0 by a write to UART1ECR

[1] PE – Parity error

When set to 1, it indicates that the parity of the received data character does not match

the parity that the EPS and SPS bits in the line control register, UARTLCR_H select

This bit is cleared to 0 by a write to UART1ECR

[0] FE – Framing error

When set to 1, in indicates that the received character didn't have a valid stop bit

This bit is cleared to 0 by a write to UART1ECR

22.6.3 UART1FR (UART1 Flag Register)

Address offset: 0x0018

Reset value: 0bx11000xxx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	RI	TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS
							R	R	R	R	R	R	R	R	R

[8] RI – Ring indicator

This bit is the complement of the UART ring indicator, UART1RI.

1: When nUART1RI is LOW

[7] TXFE – Transmit FIFO empty

This bit depends on the state of the FEN bit in the line control register, UARTLCR_H.

0: The bit is set when transmit holding register is empty.

1: The bit is set when transmit FIFO is empty

[6] RXFF – Receive FIFO full

This bit depends on the state of the FEN bit in the line control register, UARTLCR_H.

0: The bit is set when the receive holding register is full

1: The bit is set when the receive FIFO is full

[5] TXFF – Transmit FIFO full

This bit depends on the state of the FEN bit in the line control register, UARTLCR_H.

0: The bit is set when transmit holding register is full.

1: The bit is set when transmit FIFO is full.

[4] RXFE – Receive FIFO empty

This bit depends on the state of the FEN bit in the line control register, UARTLCR_H.

0: The bit is set when the receive holding register is empty.

1: The bit is set when the receive FIFO is empty.

[3] BUSY – UART busy

1: the UART is busy transmitting data

[2] DCD – Data carrier detect

This bit is the complement of the UART data carrier detect, UART1DCD, status input

1: The bit is the complement of the UART data carrier detect

[1] DSR – Data set ready

This bit is the complement of the UART data set ready, UART1DSR, status input

1: The bit is the complement of the UART data set ready

[0] CTS – Clear to send

This bit is the complement of the UART clear to send, UART1CTS, status input

1: The bit is the complement of the UART clear to send

22.6.4 UART1ILPR (UART1 IrDA Low-Power Counter Register)

Address offset: 0x0020

Reset value: 0x00

The UARTILPR Register is the IrDA low-power counter register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	ILPDVSR							
								R/W							

[7:0] ILPDVSR – 8-bit low-power divisor value

These bits are cleared to 0 at reset

$$\text{ILPDVSR} = (F_{UARTCLK}/F_{IrLPBaud16})$$

Where, $F_{IrLPBaud16}$ is nominally 1.8432MHz

The divisor is 1.42MHz < $F_{IrLPBaud16}$ < 2.12MHz, results in a low-power pulse duration of 1.41 – 2.11us.

22.6.5 UART1IBRD (UART1 Integer Baud Rate Register)

Address offset: 0x0024

Reset value: 0x00

The UART1IBRD Register is the integer part of the baud rate divisor value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAUD DIVINT															
w															

[15:0] BAUD DIVINT – The integer baud rate divisor.

These bits are cleared to 0 on reset

22.6.6 UART1FBRD (UART1 Fractional Baud Rate Register)

Address offset: 0x0028

Reset value: 0x00

The UART1FBRD register is the fractional part of the baud rate divisor value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	BAUD DIVFRAC					
										w					

[5:0] BAUD DIVFRAC – The fractional baud rate divisor.

These bits are cleared to 0 on reset

The baud rate divisor is calculated as follows:

Baud rate divisor BAUDDIV = $(F_{UARTCLK}/(16 \times Baud\ rate))$

Where, $F_{UARTCLK}$ is the UART reference clock frequency.

The BAUDDIV is comprised of the integer value (BAUD DIVINT) and the fractional value (BAUD DIVFRAC).

Example 1

If the required baud rate is 115200 and UARTCLK = 8MHz then:

Baud rate divisor = $(8 \times 10^6)/(16 \times 115200) = 4.340278$

This means BRD_I = 4 and BRD_F = 0.340278

(Therefore, UART1IBRD = 4)

Therefore, UART1FBRD = $\text{inerger}[(0.340278 \times 64) + 0.5] = 22$

Generated baud rate divider = $\text{UART1IBRD} + (\text{UART1FBRD}/64) = 4.34375$

Generated baud rate = $(8 \times 10^6)/(16 \times 4.34375) = 115107.914$

Error = $(115108 - 115200)/(115200) \times 100 = -0.07861\%$

When UartCLK = 8MHz

Integer divisor	Fractional divisor	Required bit rate(bps)	Generated bit rate(bps)	Error%
0x2	0x0B	230400	2.171875	-0.07994
0x4	0x16	115200	4.34375	-0.07994
0x6	0x21	76800	6.515625	-0.07994
0x8	0x2C	57600	8.6875	-0.07994
0x22	0x2E	14400	34.71875	0.010001

22.6.7 UART1LCR_H (UART1 Line Control Register)

Address offset: 0x002C

Reset value: 0x00

The UART1LCR_H register is the line control register. This register accesses bits 29 to 22 of the UART line control register, UART1LCR.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	SPS	WLEN		FEN	STP2	EPS	PEN	BRK
								R/W							

[7] SPS – Stick parity select

0: stick parity is disable

1: either:

The parity bit is transmitted and checked as a 1 when EPS bit set ‘0’

The parity bit is transmitted and checked as a 0 when EPS bit set ‘1’

[6:5] WLEN – Word length

00	01	10	11
5 bits	6 bits	7 bits	8 bits

[4] FEN – Enable FIFO

0: The FIFO become 1-byte-deep holding register.

1: The transmit and receive FIFO buffers are enable (FIFO mode)

[3] STP2 – Two stop bit select

1: Two stop bits are transmitted at the end of the frame

[2] EPS – Even parity select

0: odd parity.

1: even parity

[1] PEN – Parity enable

0: parity is disabled and no parity bit added to the data frame

1: parity checking and generations is enabled

[0] BRK – Send break

0: For normal use, the bit must be cleared to 0

1: The low-level is continually output on the UARTTXD output

PEN	EPS	SPS	Parity bit(Transmitted or checked)
0	X	X	Not transmitted or checked
1	1	0	Even parity
1	0	0	Odd parity
1	0	1	1
1	1	1	0

22.6.8 UART1CR (UART1 Control register)

Address offset: 0x0030

Reset value: 0x0300

The UART1CR register is the control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTSEn	RTSEn	Out2	Out1	RTS	DTR	RXE	TXE	res					SIRLP	SIREN	UARTEN

[15] CTSEn – CTS hardware flow control enable.

1: CTS hardware flow control is enable. Data is only transmitted when the UART1CTS signal is asserted.

[14] RTSEn – RTS hardware flow control enable

1: RTS hardware flow control is enable. Data is only requested when there is space in the receive FIFO for it to be received.

[13] Out2

This bit is the complement of the UART Out2 (nUARTOut2) modem status output.

That is, when the bit is programmed to 1, the output is 0.

For DTE this can be used as “Ring Indicator” (RI).

[12] Out1

This bit is the complement of the UART Out1 (nUARTOut1) modem status output.

That is, when the bit is programmed to 1 the output is 0.

For DTE this can be used as “Data Carrier Detect”(DCD).

[11] RTS – Request to send

This bit is the complement of the UART request to send, UART1RTS, modem status output.

That is, when the bit is programmed to 1 then UART1RTS is LOW.

[10] DTS – Data transmit ready

This bit is the complement of the UART data transmit ready, UART1DTR, modem status output.

That is, when the bit is programmed to 1 then UART1DTR is LOW.

[9] RXE – Receive enable

If this bit is set to 1, the receive section of the UART is enabled.

Data reception occurs for either UART signals or SIR signals depending on the setting of the SIREN bit. When the UART is disabled in the middle of reception, it completes the current character before stopping.

[8] TXE – Transmit enable

1: The transmit section of the UART is enabled,

[7:3] Reserved

[2] SIRLP – SIR low-power IrDA mode

0: low-level bits are transmitted as an active high pulse with a width of 3/16th of the bit period.

1: low-level bits are transmitted with a pulse width that is 3 times the period of the IrLPBaud16 input signal, regardless of the selected bit rate.

[1] SIREN – SIR enable

0: IrDA SIR ENDEC is disable

1: IrDA SIR ENDEC is enable

[0] UARTEN – Loopback enable

0: UART is disabled

1: UART is enabled

Program the control registers as follows:

1. Disable the UART.
2. Wait for the end of transmission or reception of the current character.

3. Flush the transmit FIFO by setting the FEN bit to 0 in the Line Control Register, UARTLCR_H on page 3-12.
4. Reprogram the UARTCR Register.
5. Enable the UART.

22.6.9 UART1IFLS (UART1 Interrupt FIFO Level Select Register)

Address offset: 0x0034

Reset value: 0x12

The UARTIFLS register is the interrupt FIFO level select register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	RXIFLSEL			TXIFLSEL		
										W			W		

[5:3] RXIFLSEL – Receive interrupt FIFO level select

7	6	5	4	3	2	1	0
Reserved			7/8 full	3/4 full	1/2 full	1/4 full	1/8 full

[2:0] TXIFLSEL – Transmit interrupt FIFO level select

7	6	5	4	3	2	1	0
Reserved			7/8 full	3/4 full	1/2 full	1/4 full	1/8 full

22.6.10 UART1IMSC (UART1 Interrupt Mask Set/Clear Register)

Address offset: 0x0038

Reset value: 0x00

The UART1IMSC register is the interrupt mask set/clear interrupts. When a bit of UART1IMSC is '1' and the corresponding bit of interrupt register is '1', an interrupt will be issued.

In other words, if a bit of UART1IMSC is '0', an interrupt will not be issued even if the corresponding bit of interrupt register is '1'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	Res	res	res	res	OEIM	BEIM	PEIM	FEIM	RTIM	TXIM	RXIM	DSR MIM	DCD MIM	CTS MIM	RIMI M

					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[10] OEIM – Overrun error interrupt mask

0: Disable UART1OEINTR

1: Enable UART1OEINTR

[9] BEIM – Break error interrupt mask

0: Disable UART1BEINTR

1: Enable UART1BEINTR

[8] PEIM – Parity error interrupt mask

0: Disable UART1EINTR

1: Enable UART1EINTR

[7] FEIM – Framing error interrupt mask

0: Disable UART1FEINTR

1: Enable UART1FEINTR

[6] RTIM – Receive timeout interrupt mask

0: Disable UART1RTINTR

1: Enable UART1RTINTR

[5] TXIM – Transmit interrupt mask

0: Disable UART1TXINTR

1: Enable UART1TXINTR

[4] RXIM – Receive interrupt mask

0: Disable UART1RXINTR

1: Enable UART1RXINTR

[3] DSRMIM – nUART1DSR modem interrupt mask

0: Disable UART1DSRINTR

1: Enable UART1DSRINTR

[2] DCDMIM – nUART1DCD modem interrupt mask

0: Disable UART1DCDINTR

1: Enable UART1DCDINTR

[1] CTSMIM – nUART1CTS modem interrupt mask

0: Disable UART1CRSINTR

1: Enable UART1CRSINTR

[0] RIMIM – nUART1RI modem interrupt mask

0: Disable UART1RIINTR

1: Enable UART1RIINTR

22.6.11 UART1RIS (UART1 Raw Interrupt Status Register)

Address offset: 0x003C

Reset value: 0x00-

The UART1RIS register indicates the raw interrupt status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	OERIS	BERIS	PERIS	FERIS	RTRIS	TXRIS	RXRIS	DRRRMIS	DCDRMIS	CTSRMIS	RIRMIS
					R	R	R	R	R	R	R	R	R	R	R

[10] OERIS – Overrun error interrupt status

It indicates state of the UART1OEINTR interrupt.

[9] BERIS – Break error interrupt status

It indicates state of the UART1BEINTR interrupt.

[8] PERIS – Parity error interrupt status

It indicates state of the UART1PEINTR interrupt.

[7] FERIS – Framing error interrupt status

It indicates state of the UART1FEINTR interrupt.

[6] RTRIS – Receive timeout interrupt status

It indicates state of the UART1RTINTR interrupt.

[5] TXRIS – Transmit interrupt status

It indicates state of the UART1TXINTR interrupt.

[4] RXRIS – Receive interrupt status

It indicates state of the UART1RXINTR interrupt.

[3] DSRRMIS – nUART1DSR modem interrupt status

It indicates state of the UART1DSRINTR interrupt.

[2] DCDRMIS – nUART1DCD modem interrupt status

It indicates state of the UART1DCDINTR interrupt.

[1] CTSRMIS – nUART1CTS modem interrupt status

It indicates state of the UART1CTSINTR interrupt.

[0] RIRMIS – nUART1RI modem interrupt status

It indicates state of the UART1RIINTR interrupt.

22.6.12 UART1MIS (UART1 Masked Interrupt Status Register)

Address offset: 0x0040

Reset value: 0x00-

The UART1MIS register is the masked interrupt status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	OE MIS	BE MIS	PE MIS	FE MIS	RT MIS	TX MIS	RX MIS	DRR MMIS	DCD MMIS	CTS MMIS	RI MMIS
					R	R	R	R	R	R	R	R	R	R	R

[10] OEMIS – Overrun error masked interrupt status

It indicates state of the UART1OEINTR interrupt.

[9] BEMIS – Break error masked interrupt status

It indicates state of the UART1BEINTR interrupt.

[8] PEMIS – Parity error masked interrupt status

It indicates state of the UART1PEINTR interrupt.

[7] FEMIS – Framing error masked interrupt status

It indicates state of the UART1FEINTR interrupt.

[6] RTMIS – Receive timeout masked interrupt status

It indicates state of the UART1RTINTR interrupt.

[5] TXMIS – Transmit masked interrupt status

It indicates state of the UART1TXINTR interrupt.

[4] RXMIS – Receive masked interrupt status

It indicates state of the UART1RXINTR interrupt.

[3] DSRMMIS – nUART1DSR modem masked interrupt status

It indicates state of the UART1DSRINTR interrupt.

[2] DCDMMIS – nUART1DCD modem masked interrupt status

It indicates state of the UART1DCDINTR interrupt.

[1] CTSMMIS – nUART1CTS modem masked interrupt status

It indicates state of the UART1CTSINTR interrupt.

[0] RIMMIS – nUART1RI modem masked interrupt status

It indicates state of the UART1RIINTR interrupt.

22.6.13 UART1ICR (UART1 Interrupt Clear Register)

Address offset: 0x0044

Reset value: -

The UART1ICR register is the interrupt clear register and is write-only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	OEIC	BEIC	PEIC	FEIC	RTIC	TXIC	RXIC	DSRM IC	DCDM IC	CTSM IC	RI MIC

					R	R	R	R	R	R	R	R	R	R	R

[10] OEIC – Overrun error interrupt clear

Clear the UART1OEINTR interrupt.

[9] BEIC – Break error interrupt clear

Clear the UART1BEINTR interrupt.

[8] PEIC – Parity error interrupt clear

Clear the UART1PEINTR interrupt.

[7] FEIC – Framing error interrupt clear

Clear the UART1FEINTR interrupt.

[6] RTIC – Receive timeout interrupt clear

Clear the UART1RTINTR interrupt.

[5] TXIC – Transmit interrupt clear

Clear the UART1TXINTR interrupt.

[4] RXIC – Receive interrupt clear

Clear the UART1RXINTR interrupt.

[3] DSRMIC – nUART1DSR modem interrupt clear

Clear the UART1DSRINTR interrupt.

[2] DCDMIC – nUART1DCD modem interrupt clear

Clear the UART1DCDINTR interrupt.

[1] CTSMIC – nUART1CTS modem interrupt clear

Clear the UART1CTSINTR interrupt.

[0] RIMIC – nUART1RI modem interrupt clear

Clear the UART1RIINTR interrupt.

22.7 Register map

The following Table 39 summarizes the UART1 registers.

Table 39 UART1 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x000	UART1DR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OE	BE	PE	FE	DATA								Data Register
	reset value																					0	0	0	0	0	0	0	0	0	0	0	0	
0x004	UART1RSR/ UART1ECR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OE	BE	PE	FE	Receive Status/Error Clear Register
	reset value																													0	0	0	0	
0x018	UART1FR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RI	TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS	Flage Register
	reset value																								X	1	1	0	0	0	X	X	X	
0x020	UART1ILPR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	ILPDVSR								IrDA Low-Power Counter Register
	reset value																									0	0	0	0	0	0	0	0	
0x024	UART1IBRD	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	BAUD DIVINT																Integer Baud Rate Register
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x028	UART1FBRD	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	BAUD DIVFRAC						Fractional Baud Rate Register
	reset value																											0	0	0	0	0	0	
0x02C	UART1LCR_H	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	SPS	WLEN			FEN	STP2	EPS	PEN	BRK	Line Control. Register
	reset value																								1	1	1	1	1	1	1	1	1	
0x030	UART1CR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	CTSEn	RTSEn	Out2	out1	RTS	DTR	RXE	TXE	res	res	res	res	SIRLP		SIREN	UART1	Control Register
	reset value																	0	0	1	1	0	0	0	0					0		0	0	
0x034	UART1IFLS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	RXIFLSEL			TXIFLSEL			Interrupt FIFO Level Select Register
	reset value																											0	1	0	0	1	0	
0x038	UART1IMSC	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OEIM	BEIM	PEIM	FEIM	RTIM	TXIM	RXIM	DSRMIM	DCDMIM	CTSMIM	RIMIM		Interrupt Mask Set/Clear Register
	reset value																					0	0	0	0	0	0	0	0	0	0	0	0	
0x03C	UART1RIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OERIS	BERIS	PERIS	FERIS	RTRIS	TXRIS	RXRIS	DRRMIS	DCDRMIS	CTSRMIS	RIRMIS		Raw Interrupt Status Register
	reset value																					0	0	0	0	0	0	0	0	0	0	0	0	
0x040	UART1MIS	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OEMIS	BEMIS	PEMIS	FEMIS	RTMIS	TXMIS	RXMIS	DRRMMIS	DCDMMIS	CTSMMIS	RIMMIS		Masked Interrupt StatusRegister
	reset value																					0	0	0	0	0	0	0	0	0	0	0	0	
0x044	UART1ICR	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	OEIC	BEIC	PEIC	FEIC	RTIC	TXIC	RXIC	DSRMIC	DCDMIC	CTSMIC	RIMMIC		Interrupt Clear Register
	reset value																					0	0	0	0	0	0	0	0	0	0	0	0	

23 Synchronous Serial Port (SSP)

23.1 Introduction

The SSP block is an IP provided by ARM (PL022 “PrimeCell® Synchronous Serial Port”). Additional details about its functional blocks may be found in “ARM PrimeCell® Synchronous Serial Port (PL022) Technical Reference Manual”.

23.2 Features

- The SSP is a master or slave interface that enables synchronous serial communication with slave or master peripherals having one of the following:
  - A MOTOROLA SPI-compatible interface
  - A TEXAS INSTRUMENTS synchronous serial interface
  - A National Semiconductor MICROWIRE® interface.

- The SPI interface operates as a master or slave interface. It supports bit rates up to 20 MHz in both master and slave configurations. The SPI has the following features:
  - Parallel-to-serial conversion on data written to an internal 16-bit wide, 8-location deep transmit FIFO
  - Serial-to-parallel conversion on received data, buffering it in a 16-bit wide, 8-location deep receive FIFO
  - Programmable data frame size from 4 to 16 bits
  - Programmable clock bit rate and prescaler. The input clock may be divided by a factor of 2 to 254 in steps of two to provide the serial output clock
  - Programmable clock phase and polarity.

23.3 Functional description

Figure 65 shows the SSP block diagram.

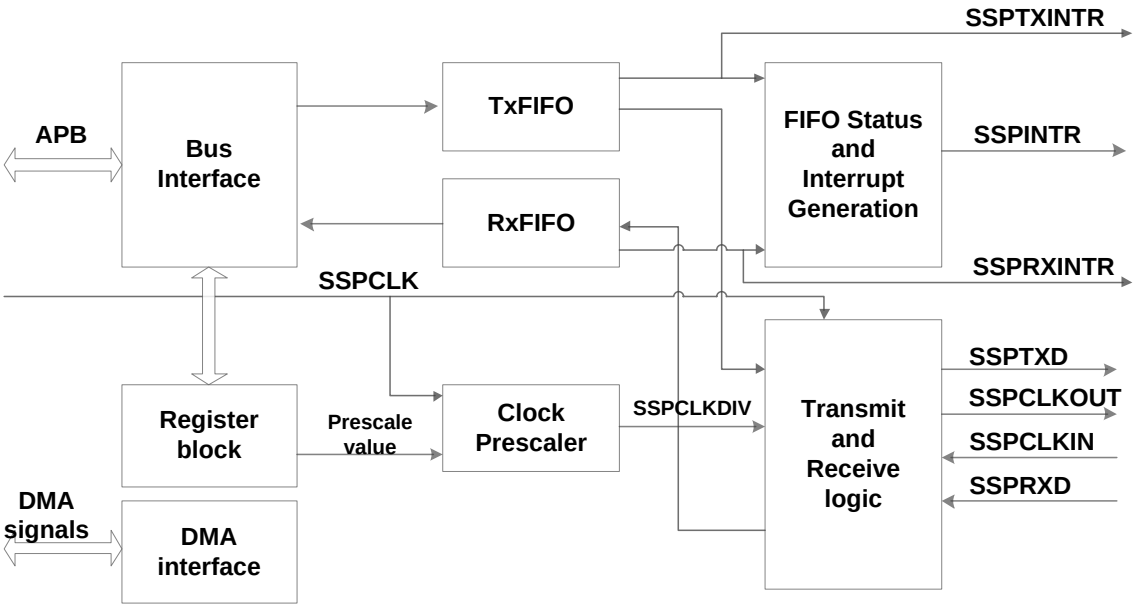


Figure 65. SSP block diagram

23.3.1 Clock prescaler

When configured as a master, an internal prescaler is used to provide the serial output clock. The prescaler may be programmed through the SSPCPSR register to divide the SSPCLK by a factor of 2 to 254 in two steps. As the least significant bit of the SSPCPSR register is not used, division by an odd number is impossible and this ensures a symmetrical (equal mark space ratio) clock is generated.

The output of this prescaler is further divided by a factor 1 to 256 through the programming of the SSPCR0 control register, to give a final master output clock.

23.3.2 Transmit FIFO

The common transmit FIFO is a 16-bit wide, 8-locations deep, First-In, First-Out (FIFO) memory buffer. CPU data written across the AMBA APB interface are stored in the buffer until it is read out by the transmit logic.

When configured as a master or a slave, parallel data is written into the transmit FIFO prior to serial conversion and is transmitted to the attached slave or master through the SSPTXD pin.

23.3.3 Receive FIFO

The common receive FIFO is a 16-bit wide, 8-locations deep, first-in, first-out memory buffer. Received data from the serial interface are stored in the buffer until it is read out by the CPU across the AMBA APB interface.

When configured as a master or slave, serial data received through the SSPRXD pin is registered prior to parallel loading into the attached slave or master receive FIFO.

23.3.4 Interrupt generation logic

The PrimeCell SSP generates four individual maskable, active-HIGH interrupts. A combined interrupt output is also generated as an OR function of the individual interrupt requests.

Users can use the single combined interrupt with a system interrupt controller that provides another level of masking on a per-peripheral basis. This enables use of modular device drivers that always know where to find the interrupt source control register bits.

Users can also use the individual interrupt requests with a system interrupt controller that provides masking for the outputs of each peripheral. In this way, a global interrupt controller service routine can read the entire set of sources from one wide register in the system interrupt controller. This is attractive when the time to read from the peripheral registers is significant compared to the CPU clock speed in a real-time system.

The peripheral supports both methods above.

The transmit and receive dynamic data-flow interrupts, SSPTXINTR and SSPRXINTR, are separated from the status interrupts so that data can be read or written in response to the FIFO trigger levels.

23.3.5 DMA interface

The PrimeCell SSP provides an interface to connect to the DMA controller. The PrimeCell SSP DMA control register, SSPDMACR controls the DMA operation of the PrimeCell SSP.

Receive – The DMA interface includes the following signals for receive:

- SSPRXDMASREQ
  - Single-character DMA transfer request asserted by the SSP. This signal is asserted when the receive FIFO contains at least one character.
- SSPRXDMABREQ

- Burst DMA transfer request, asserted by the SSP. This signal is asserted when the receive FIFO contains four or more characters.

- SSPRXDMACLR
  - DMA request clear asserted by the DMA controller to clear the receive request signals. If DMA burst transfer is requested, the clear signal is asserted during the transfer of the last data in the burst.

Transmit – The DMA interface includes the following signals for transmit:

- SSPTXDMASREQ
  - Single-character DMA transfer request asserted by the SSP. This signal is asserted when there is at least one empty location in the transmit FIFO.
- SSPTXDMABREQ
  - Burst DMA transfer request asserted by the SSP. This signal is asserted when the transmit FIFO contains four characters or fewer.
- SSPTXDMACLR
  - DMA request clear asserted by the DMA controller to clear the transmit request signals. If a DMA burst transfer is requested, the clear signal is asserted during the transfer of the last data in the burst.

The burst transfer and single transfer request signals are not mutually exclusive. They can both be asserted at the same time. For example, when there is more data than the watermark level of four in the receive FIFO, the burst transfer request and the single transfer request are asserted.

When the amount of data left in the receive FIFO is less than the watermark level, the single request only is asserted. This is useful for situations when the number of characters left to be received in the stream is less than a burst.

For example, if 19 characters must be received, the DMA controller then transfers four bursts of four characters and three single transfers to complete the stream.

The PrimeCell SSP does not assert the burst request for the remaining three characters.

Each request signal remains asserted until the relevant DMA clear signal is asserted. After the request clear signal is de-asserted, a request signal can become active again depending on the conditions that previous sections describe. All request signals are de-asserted if the PrimeCell SSP is disabled or the DMA enable signal is cleared.

Table 40 shows the trigger points for DMABREQ of both the transmit and receive FIFOs.

Table 40 DMA trigger points for the transmit and receive FIFOs.

Burst length

Watermark level	Transmit, number of empty locations	Receive, number of filled locations
1/2	4	4

Figure 66 shows the timing diagram for both a single transfer request, and a burst transfer request, with the appropriate DMA clear signal. The signals are all synchronous to PCLK.

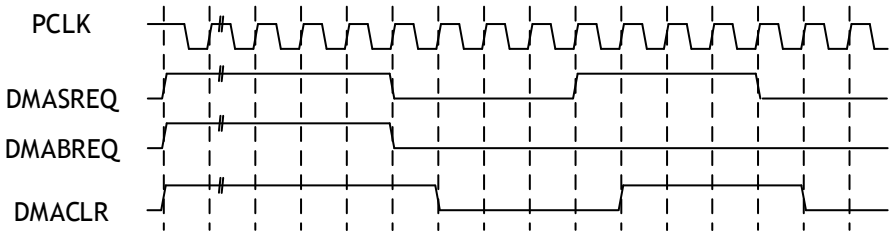


Figure 66. DMA transfer waveforms

23.3.6 Interface reset

The PrimeCell SSP is reset by the global reset signal, PRESETn, and a block-specific reset signal, nSSPRST. An external reset controller must use PRESETn to assert nSSPRST asynchronously and negate it synchronously to SSPCLK. PRESETn must be asserted LOW for a period long enough to reset the slowest block in the on-chip system, and then taken HIGH again. The PrimeCell SSP requires PRESETn to be asserted LOW for at least one period of PCLK.

23.3.7 Configuring the SSP

The Following reset, the PrimeCell SSP logic is disabled and must be configured when in this state.

It is necessary to program control registers SSPCR0 and SSPCR1 to configure the peripheral as a master or slave operating under one of the following protocols:

- Motorola SPI
- Texas Instruments SSI
- National Semiconductor.

The bit rate, derived from the external SSPCLK, requires the programming of the clock prescale register SSPCPSR.

23.3.8 Enable PrimeCell SSP operation

You can either prime the transmit FIFO, by writing up to eight 16-bit values when the PrimeCell SSP is disabled, or permit the transmit FIFO service request to interrupt the CPU. Once enabled, transmission or reception of data begins on the transmit, SSPTXD, and receive, SSPRXD, pins.

23.3.9 Clock ratios

There is a constraint on the ratio of the frequencies of PCLK to SSPCLK. The frequency of SSPCLK must be less or equal to that of PCLK. This ensures that control signals from the SSPCLK domain to the PCLK domain are guaranteed to get synchronized before one frame duration:
FSSPCLK <= FPCLK.

In the slave mode of operation, the SSPCLKIN signal from the external master is double-synchronized and then delayed to detect an edge. It takes three SSPCLKs to detect an edge on SSPCLKIN. SSPTXD has less setup time to the falling edge of SSPCLKIN on which the master is sampling the line.

The setup and hold times on SSPRXD, with reference to SSPCLKIN, must be more conservative to ensure that it is at the right value when the actual sampling occurs within the SSPMS. To ensure correct device operation, SSPCLK must be at least 12 times faster than the maximum expected frequency of SSPCLKIN.
The frequency selected for SSPCLK must accommodate the desired range of bit clock rates.
The ratio of minimum SSPCLK frequency to SSPCLKOUT maximum frequency in the case of the slave mode is 12, and for the master mode, it is two.

To generate a maximum bit rate of 1.8432Mbps in the master mode, the frequency of SSPCLK must be at least 3.6864MHz. With an SSPCLK frequency of 3.6864MHz, the SSPCPSR register must be programmed with a value of 2, and the SCR[7:0] field in the SSPCR0 register must be programmed with a value of 0.

To work with a maximum bit rate of 1.8432Mbps in the slave mode, the frequency of SSPCLK must be at least 22.12MHz. With an SSPCLK frequency of 22.12MHz, the SSPCPSR register can be programmed with a value of 12 and the SCR[7:0] field in the SSPCR0 register can be programmed with a value of 0. Similarly, the ratio of SSPCLK maximum frequency to SSPCLKOUT minimum frequency is 254 x 256.

The minimum frequency of SSPCLK is calculated by the following equations, both of which must be satisfied:

$F_{SSPCLK}(min) => 2 \times F_{SSPCLKOUT}(max)$, for master mode

FSSPCLK(min) => 12 x FSSPCLKIN(max), for slave mode.

The maximum frequency of SSPCLK is calculated by the following equations, both of which must be satisfied:

FSSPCLK(max) <= 254 x 256 x FSSPCLKOUT(min), for master mode

FSSPCLK(max) <= 254 x 256 x FSSPCLKIN(min), for slave mode.

23.3.10 Programming the SSPCR0 Control Register

The SSPCR0 register is used to:

- program the serial clock rate
- select one of the three protocols
- select the data word size, where applicable.

The Serial Clock Rate (SCR) value in conjunction with the SSPCPSR clock prescale divisor value, CPSDVSR, is used to derive the PrimeCell SSP transmit and receive bit rate from the external SSPCLK.

The frame format is programmed through the FRF bits and the data word size through the DSS bits.

Bit phase and polarity applicable to Motorola SPI format only are programmed through the SPH and SPO bits.

23.3.11 Programming the SSPCR1 Control Register

The SSPCR1 register is used to:

- select master or slave mode
- enable a loop back test feature
- enable the PrimeCell SSP peripheral.

To configure the PrimeCell SSP as a master, clear the SSPCR1 register master or slave selection bit, MS, to 0. This is the default value on reset.

Setting the SSPCR1 register MS bit to 1 configures the PrimeCell SSP as a slave. When configured as a slave, enabling or disabling of the PrimeCell SSP SSPTXD signal is provided through the SSPCR1 slave mode SSPTXD output disable bit, SOD. You can use this in some multi-slave environments where masters might parallel broadcast.

Set the Synchronous Serial Port Enable (SSE) bit to 1 to enable the operation of the PrimeCell SSP.

Bit rate generation

The serial bit rate is derived by dividing down the input clock SSPCLK. The clock is first divided by an even prescale value CPSDVSR in the range of 2-254, and is programmed in SSPCPSR. The clock is divided again by a value in the range of 1-256, that is 1 + SCR, where SCR is the value programmed in SSPCR0.

The following equation defines the frequency of the output signal bit clock, SSPCLKOUT:

$$F_{SSPCLKOUT} = \frac{F_{SSPCLK}}{CPSDVSR \times (1 + SCR)}$$

For example, if SSPCLK is 20MHz, and CPSDVSR = 2, then SSPCLKOUT has a frequency range of 39.06kHz~10MHz.

23.3.12 Frame format

Each data frame is between 4-16 bits long depending on the size of data programmed and is transmitted starting with the MSB. Users can select the following basic frame types:

- Texas Instruments synchronous serial
- Motorola SPI
- National Semiconductor Microwire.

For all formats, the serial clock SSPCLKOUT is held inactive while the PrimeCell SSP is idle and transitions at the programmed frequency only during active transmission or reception of data. The idle state of SSPCLKOUT is utilized to provide a receive timeout indication that occurs when the receive FIFO still contains data after a timeout period.

For Motorola SPI and National Semiconductor Microwire frame formats, the serial frame SSPFSSOUT pin is active-LOW and is asserted and pulled-down during the entire transmission of the frame.

For Texas Instruments synchronous serial frame format, the SSPFSSOUT pin is pulsed for one serial clock period starting at its rising edge prior to the transmission of each frame. For this frame format, both the PrimeCell SSP and the off-chip slave device drive their output data on the rising edge of SSPCLKOUT and latch data from the other device on the falling edge.

Unlike the full-duplex transmission of the other two frame formats, the National Semiconductor Microwire format uses a special master-slave messaging technique which operates at half-duplex. In this mode, an 8-bit control message is transmitted to the off-chip slave when a frame begins. During this transmit, the SSP receives no incoming data. After the message has been sent, the off-chip slave decodes it and responds with the requested data after waiting one serial clock after the last bit of the 8-bit control message has been sent. The returned data can be 4-16 bits in length making the total frame length in the range of 13-25 bits.

23.3.13 Texas Instruments synchronous serial frame format

Figure 67 shows the Texas Instruments synchronous serial frame format for a single transmitted frame.

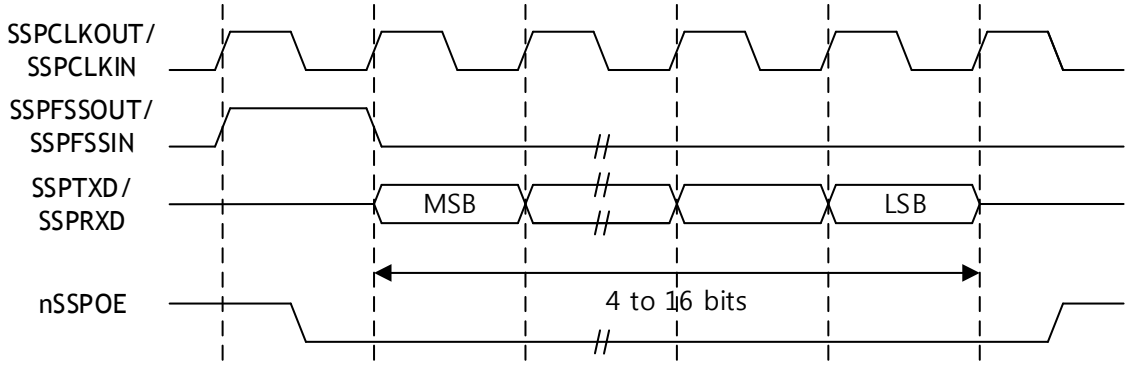


Figure 67. Texas Instruments synchronous serial frame format, single transfer

In this mode, SSPCLKOUT and SSPFSSOUT are forced LOW and the transmit data line SSPTXD is tristated whenever the PrimeCell SSP is idle. When the bottom entry of the transmit FIFO contains data, SSPFSSOUT is pulsed HIGH for one SSPCLKOUT period. The value to be transmitted is also transferred from the transmit FIFO to the serial shift register of the transmit logic. On the next rising edge of SSPCLKOUT, the MSB of the 4-bit to 16-bit data frame is shifted out on the SSPTXD pin. In a similar way, the MSB of the received data is shifted onto the SSPRXD pin by the off-chip serial slave device.

Both the PrimeCell SSP and the off-chip serial slave device then clock each data bit into their serial shifter on the falling edge of each SSPCLKOUT. The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of PCLK after the LSB has been latched.

Figure 68 shows the Texas Instruments synchronous serial frame format when back-to-back frames are transmitted.

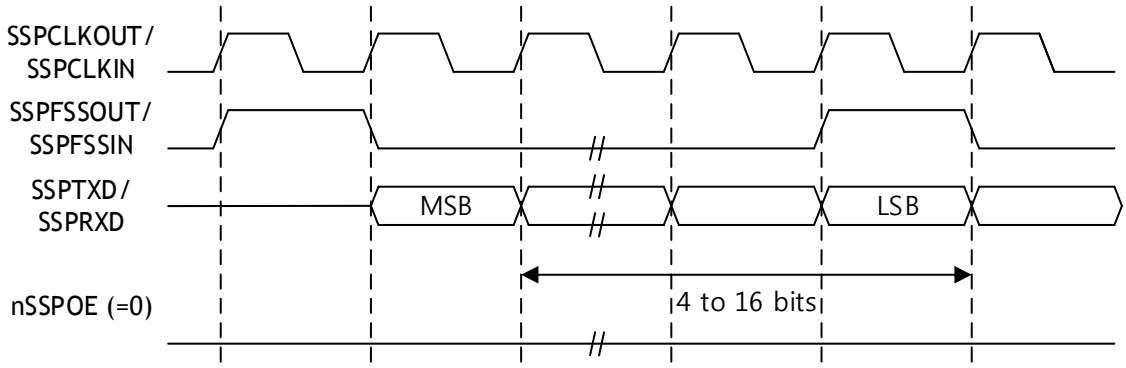


Figure 68. Texas Instruments synchronous serial frame format, continuous transfers

23.3.14 Motorola SPI frame format

The Motorola SPI interface is a four-wire interface where the SSPFSSOUT signal behaves as a slave select. The main feature of the Motorola SPI format is that you can program the inactive state and phase of the SSPCLKOUT signal using the SPO and SPH bits of the SSPSCR0 control register.

SPO, clock polarity

When the SPO clock polarity control bit is LOW, it produces a steady state LOW value on the SSPCLKOUT pin. If the SPO clock polarity control bit is HIGH, a steady state HIGH value is placed on the SSPCLKOUT pin when data is not being transferred.

SPH, clock phase

The SPH control bit selects the clock edge that captures data and enables it to change state. It has the most impact on the first bit transmitted by either permitting or not permitting a clock transition before the first data capture edge.

When the SPH phase control bit is LOW, data is captured on the first clock edge transition.

When the SPH clock phase control bit is HIGH, data is captured on the second clock edge transition.

Figure 69 and Figure 70 show single and continuous transmission signal sequences for Motorola SPI format with SPO=0, SPH=0.

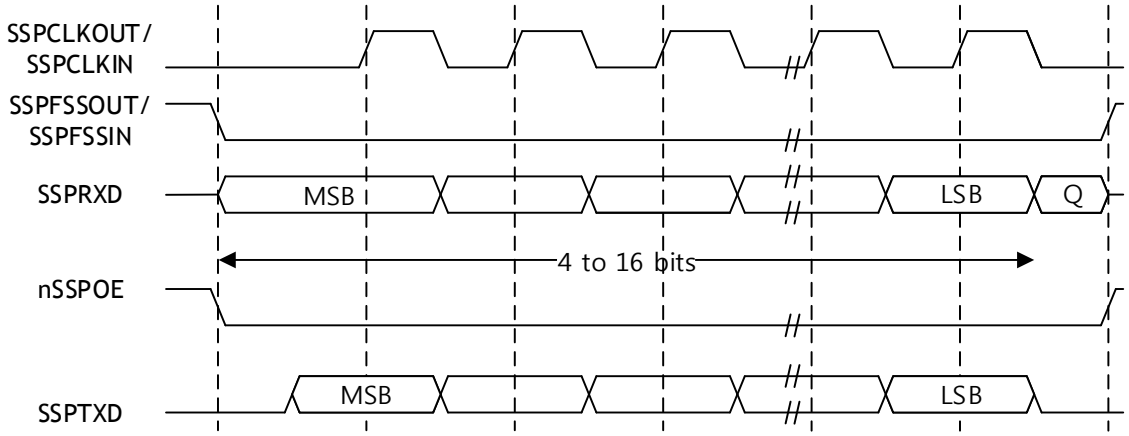


Figure 69 Motorola SPI frame format, single transfer, with SPO=0 and SPH=0

Figure 70 shows a continuous transmission signal sequence for Motorola SPI frame format with SPO=0, SPH=0.

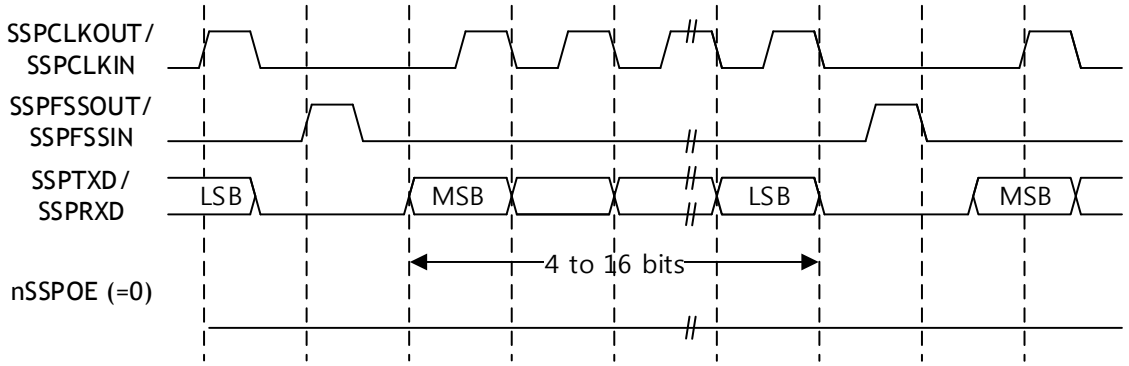


Figure 70 Motorola SPI frame format, continuous transfers, with SPO=0 and SPH=0

In this configuration, during idle periods:

- the SSPCLKOUT signal is forced LOW
- the SSPFSSOUT signal is forced HIGH
- the transmit data line SSPTXD is arbitrarily forced LOW
- the nSSPOE pad enable signal is forced HIGH, making the transmit pad high impedance
- when the PrimeCell SSP is configured as a master, the nSSPCTLOE line is driven LOW, enabling the SSPCLKOUT pad, active-LOW enable
- when the PrimeCell SSP is configured as a slave, the nSSPCTLOE line is driven HIGH, disabling the SSPCLKOUT pad, active-LOW enable.

If the PrimeCell SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSPFSSOUT master signal being driven LOW. This causes the slave data to be enabled onto the SSPRXD input line of the master. The nSSPOE line is driven LOW, enabling the master SSPTXD output pad.

One half SSPCLKOUT period later, valid master data is transferred to the SSPTXD pin. Now that both the master and slave data have been set, the SSPCLKOUT master clock pin goes HIGH after one additional half SSPCLKOUT period.

The data is now captured on the rising and propagated on the falling edges of the SSPCLKOUT signal.

In the case of a single word transmission after all bits of the data word have been transferred, the SSPFSSOUT line is returned to its idle HIGH state one SSPCLKOUT period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSPFSSOUT signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not permit it to be altered if the SPH bit is logic zero. Therefore, the master device must raise the SSPFSSIN pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSPFSSOUT pin is returned to its idle state one SSPCLKOUT period after the last bit has been captured.

Figure 71 shows the transfer signal sequence for Motorola SPI format with SPO=0, SPH=1, and it covers both single and continuous transfers.

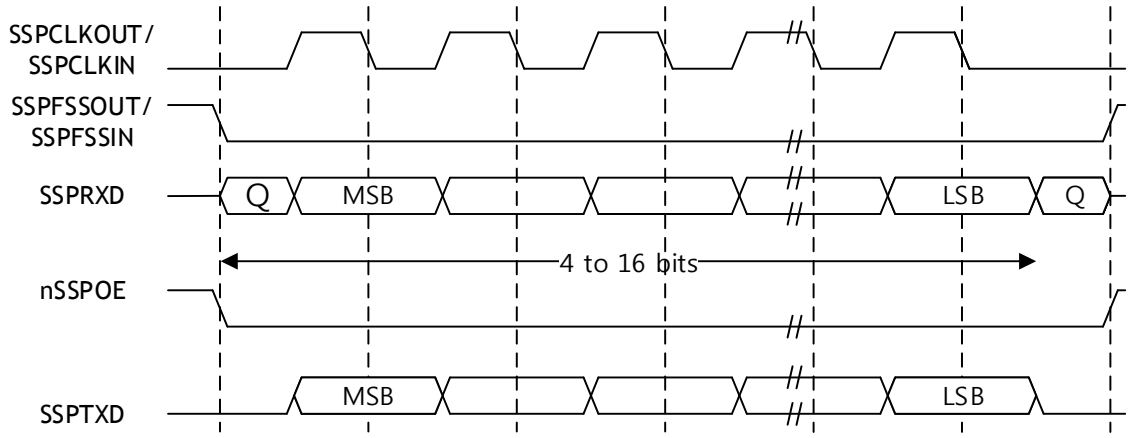


Figure 71 Motorola SPI frame format, single and continuous transfers, with SPO=0 and SPH=1

In this configuration, during idle periods:

- the SSPCLKOUT signal is forced LOW
- The SSPFSSOUT signal is forced HIGH
- the transmit data line SSPTXD is arbitrarily forced LOW

- the nSSPOE pad enable signal is forced HIGH, making the transmit pad high impedance
- when the PrimeCell SSP is configured as a master, the nSSPCTLOE line is driven LOW, enabling the SSPCLKOUT pad, active-LOW enable
- when the PrimeCell SSP is configured as a slave, the nSSPCTLOE line is driven HIGH, disabling the SSPCLKOUT pad, active-LOW enable.

If the PrimeCell SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSPFSSOUT master signal being driven LOW. The nSSPOE line is driven LOW, enabling the master SSPTXD output pad. After an additional one half SSPCLKOUT period, both master and slave valid data is enabled onto their respective transmission lines. At the same time, the SSPCLKOUT is enabled with a rising edge transition.

Data is then captured on the falling edges and propagated on the rising edges of the SSPCLKOUT signal.

In the case of a single word transfer after all bits have been transferred, the SSPFSSOUT line is returned to its idle HIGH state one SSPCLKOUT period after the last bit has been captured.

For continuous back-to-back transfers, the SSPFSSOUT pin is held LOW between successive data words and termination is the same as that of the single word transfer.

Figure 72 shows a single transmission signal sequence for Motorola SPI format with SPO=1, SPH=0.

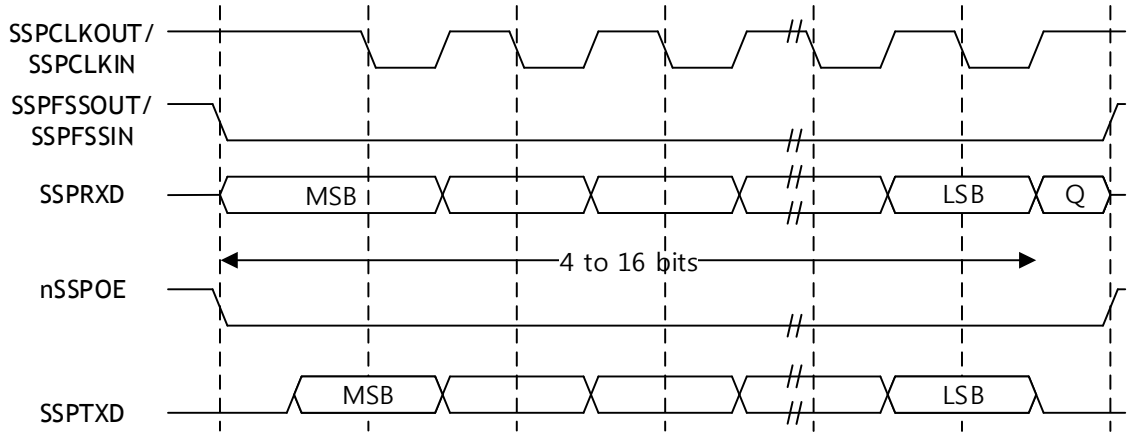


Figure 72 Motorola SPI frame format, single transfer, with SPO=1 and SPH=0

Figure 73 shows a continuous transmission signal sequence for Motorola SPI format with SPO=1, SPH=0. In Figure 9, Q is an undefined signal.

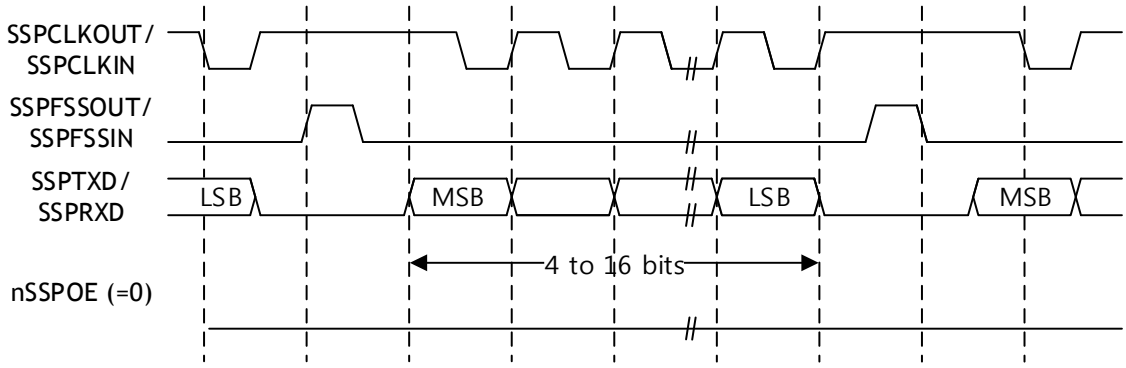


Figure 73. Motorola SPI frame format, continuous transfers, with SPO=1 and SPH=0

In this configuration, during idle periods:

- the SSPCLKOUT signal is forced HIGH
- the SSPFSSOUT signal is forced HIGH
- the transmit data line SSPTXD is arbitrarily forced LOW
- the nSSPOE pad enable signal is forced HIGH, making the transmit pad high impedance
- when the PrimeCell SSP is configured as a master, the nSSPCTLOE line is driven LOW, enabling the SSPCLKOUT pad, active-LOW enable
- when the PrimeCell SSP is configured as a slave, the nSSPCTLOE line is driven HIGH, disabling the SSPCLKOUT pad, active-LOW enable.

If the PrimeCell SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSPFSSOUT master signal being driven LOW, and this causes slave data to be immediately transferred onto the SSPRXD line of the master. The nSSPOE line is driven LOW, enabling the master SSPTXD output pad.

One half period later, valid master data is transferred to the SSPTXD line. Now that both the master and slave data have been set, the SSPCLKOUT master clock pin becomes LOW after one additional half SSPCLKOUT period. This means that data is captured on the falling edges and be propagated on the rising edges of the SSPCLKOUT signal.

In the case of a single word transmission after all bits of the data word are transferred, the SSPFSSOUT line is returned to its idle HIGH state one SSPCLKOUT period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSPFSSOUT signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not permit it to be altered if the SPH bit is logic zero. Therefore, the master device must raise the SSPFSSIN pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous

transfer, the SSPFSSOUT pin is returned to its idle state one SSPCLKOUT period after the last bit has been captured.

Figure 74 shows the transfer signal sequence for Motorola SPI format with SPO=1, SPH=1, and it covers both single and continuous transfers. In

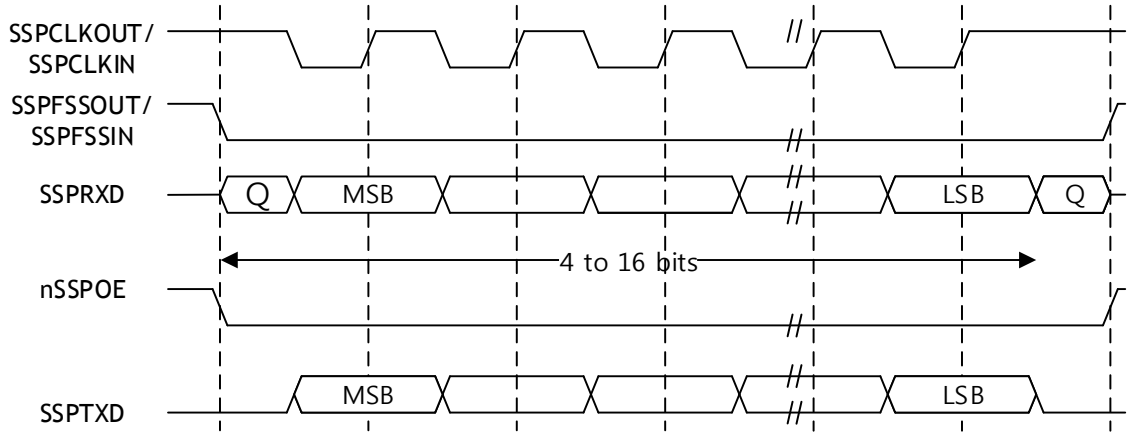


Figure 74. Motorola SPI frame format, single and continuous transfers, with SPO=1 and SPH=1, Q is an undefined signal.

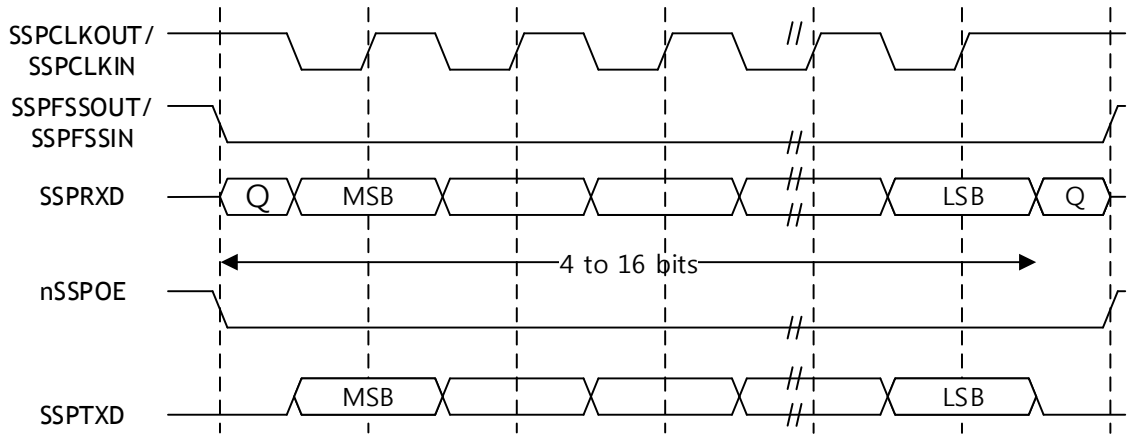


Figure 74. Motorola SPI frame format, single and continuous transfers, with SPO=1 and SPH=1

In this configuration, during idle periods:

- the SSPCLKOUT signal is forced HIGH
- the SSPFSSOUT signal is forced HIGH
- the transmit data line SSPTXD is arbitrarily forced LOW
- the nSSPOE pad enable signal is forced HIGH, making the transmit pad high impedance
- when the PrimeCell SSP is configured as a master, the nSSPCTLOE line is driven LOW, enabling the SSPCLKOUT pad, active-LOW enable
- when the PrimeCell SSP is configured as a slave, the nSSPCTLOE line is driven HIGH, disabling the SSPCLKOUT pad, active-LOW enable.

If the PrimeCell SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSPFSSOUT master signal being driven LOW. The nSSPOE line is driven LOW, enabling the master SSPTXD output pad. After an additional one half SSPCLKOUT period, both master and slave data are enabled onto their respective transmission lines. At the same time, the SSPCLKOUT is enabled with a falling edge transition. Data is then captured on the rising edges and propagated on the falling edges of the SSPCLKOUT signal.

After all bits have been transferred in the case of a single word transmission, the SSPFSSOUT line is returned to its idle HIGH state one SSPCLKOUT period after the last bit has been captured.

For continuous back-to-back transmissions, the SSPFSSOUT pin remains in its active-LOW state, until the final bit of the last word has been captured, and then returns to its idle state as the previous section describes.

For continuous back-to-back transfers, the SSPFSSOUT pin is held LOW between successive data words and termination is the same as that of the single word transfer.

23.3.15 National Semiconductor Microwire frame format

Figure 75 shows the National Semiconductor Microwire frame format for a single frame.

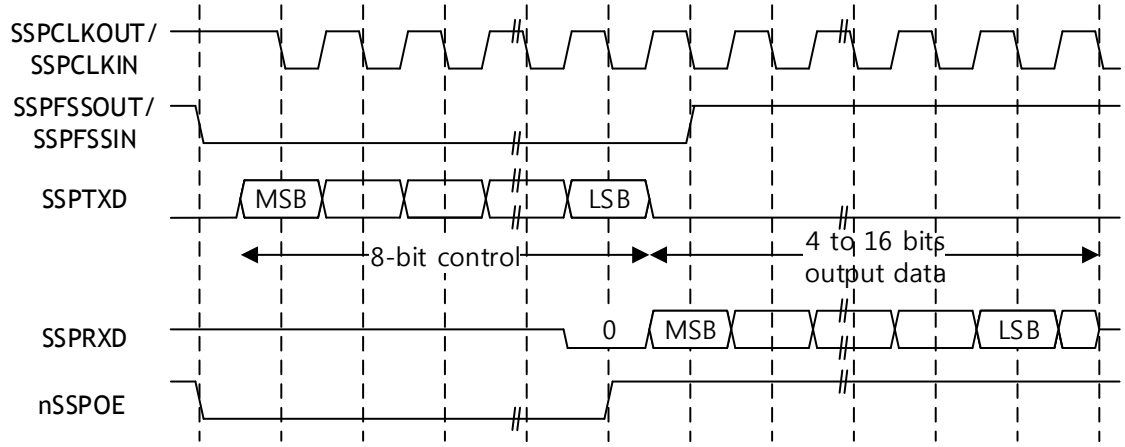


Figure 75. National Semiconductor Microwire frame format, single transfer

Microwire format is very similar to the SPI format except that transmission is half-duplex instead of full-duplex using a master-slave message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the PrimeCell SSP to the off-chip slave device. During this transmission, the PrimeCell SSP receives no incoming data. After the message has been sent, the off-chip slave decodes it and responds with the required data after waiting one serial clock after the last bit of the 8-bit control message has been sent. The

returned data is 4 to 16 bits in length, making the total frame length in the range of 13-25 bits.

In this configuration, during idle periods:

- SSPCLKOUT is forced LOW
- SSPFSSOUT is forced HIGH
- the transmit data line, SSPTXD, is arbitrarily forced LOW
- the nSSPOE pad enable signal is forced HIGH, making the transmit pad high impedance.

A transmission is triggered by writing a control byte to the transmit FIFO. The falling edge of SSPFSSOUT causes the value contained in the bottom entry of the transmit FIFO to be transferred to the serial shift register of the transmit logic and the MSB of the 8-bit control frame to be shifted out onto the SSPTXD pin. SSPFSSOUT remains LOW for the duration of the frame transmission. The SSPRXD pin remains tristated during this transmission.

The off-chip serial slave device latches each control bit into its serial shifter on the rising edge of each SSPCLKOUT. After the last bit is latched by the slave device, the control byte is decoded during a one clock wait-state and the slave responds by transmitting data back to the PrimeCell SSP. Each bit is driven onto the SSPRXD line on the falling edge of SSPCLKOUT. The PrimeCell SSP in turn latches each bit on the rising edge of SSPCLKOUT. At the end of the frame for single transfers, the SSPFSSOUT signal is pulled HIGH one clock period after the last bit has been latched in the receive serial shifter, which causes the data to be transferred to the receive FIFO.

The off-chip slave device can tristate the receive line either on the falling edge of SSPCLKOUT after the LSB has been latched by the receive shifter or when the SSPFSSOUT pin goes HIGH.

For continuous transfers, data transmission begins and ends in the same manner as a single transfer. However, the SSPFSSOUT line is continuously asserted, held LOW, and transmission of data occurs back-to-back. The control byte of the next frame follows directly after the LSB of the received data from the current frame. Each of the received values is transferred from the receive shifter on the falling edge SSPCLKOUT, after the LSB of the frame has been latched into the PrimeCell SSP.

Figure 76 shows the National Semiconductor Microwire frame format when back-to-back frames are transmitted.

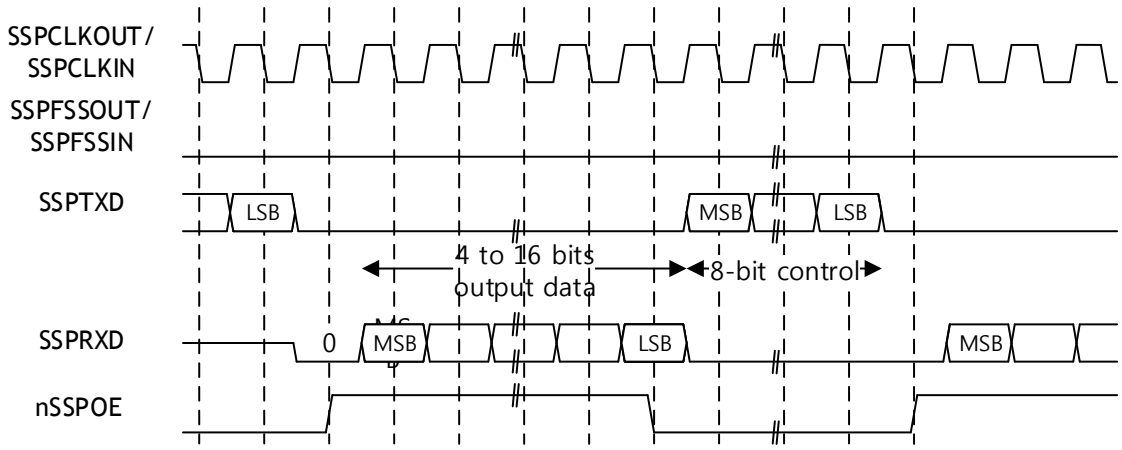


Figure 76. National Semiconductor Microwire frame format, continuous transfers

23.3.16 Master and Slave configurations

Figure 77 shows how a PrimeCell SSP (PL022) configured as master, interfaces to a Motorola SPI slave. The SPI Slave Select (SS) signal is permanently tied LOW and configures it as a slave. Similar to the above operation, the master can broadcast to the slave through the master PrimeCell SSP SSPTXD line. In response, the slave drives its SPI MISO port onto the SSPRXD line of the master.

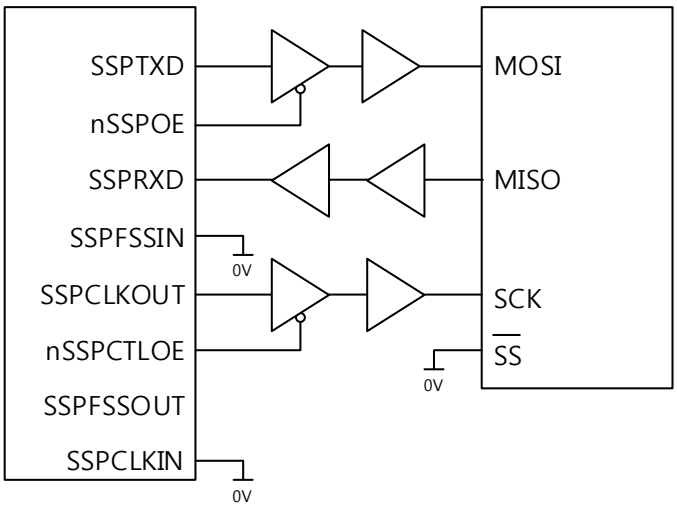


Figure 77. PrimeCell SSP master coupled to an SPI slave

Figure 78 shows a Motorola SPI configured as a master and interfaced to an instance of a PrimeCell SSP (PL022) configured as a slave. In this case, the slave Select Signal (SS) is permanently tied HIGH to configure it as a master. The master can broadcast to the slave through the master SPI MOSI line. In response, the slave drives its nSSPOE signal LOW.
This enables its SSPTXD data onto the MISO line of the master.

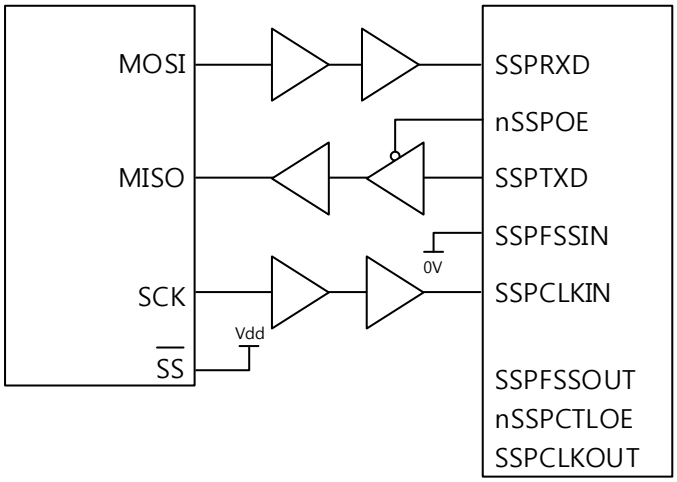


Figure 78. SPI master coupled to a PrimeCell SSP slave

23.3.17 SSP Flow chart

Figure 79 shows how to setting TI or Microwire mode.

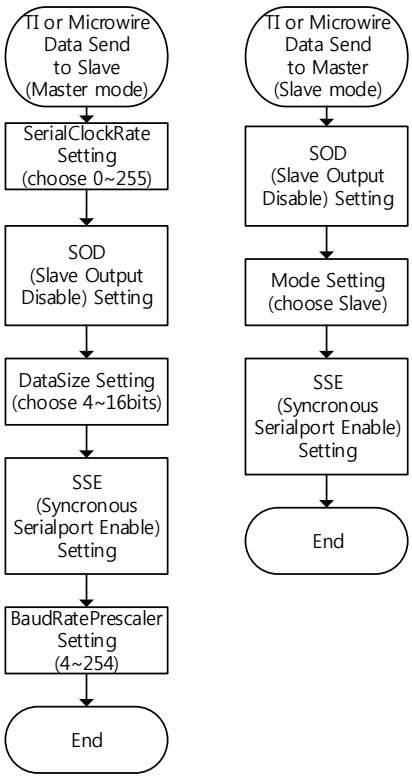


Figure 79. how to setting TI or Microwire mode flow chart

Figure 80 shows how to setting SPI mode.

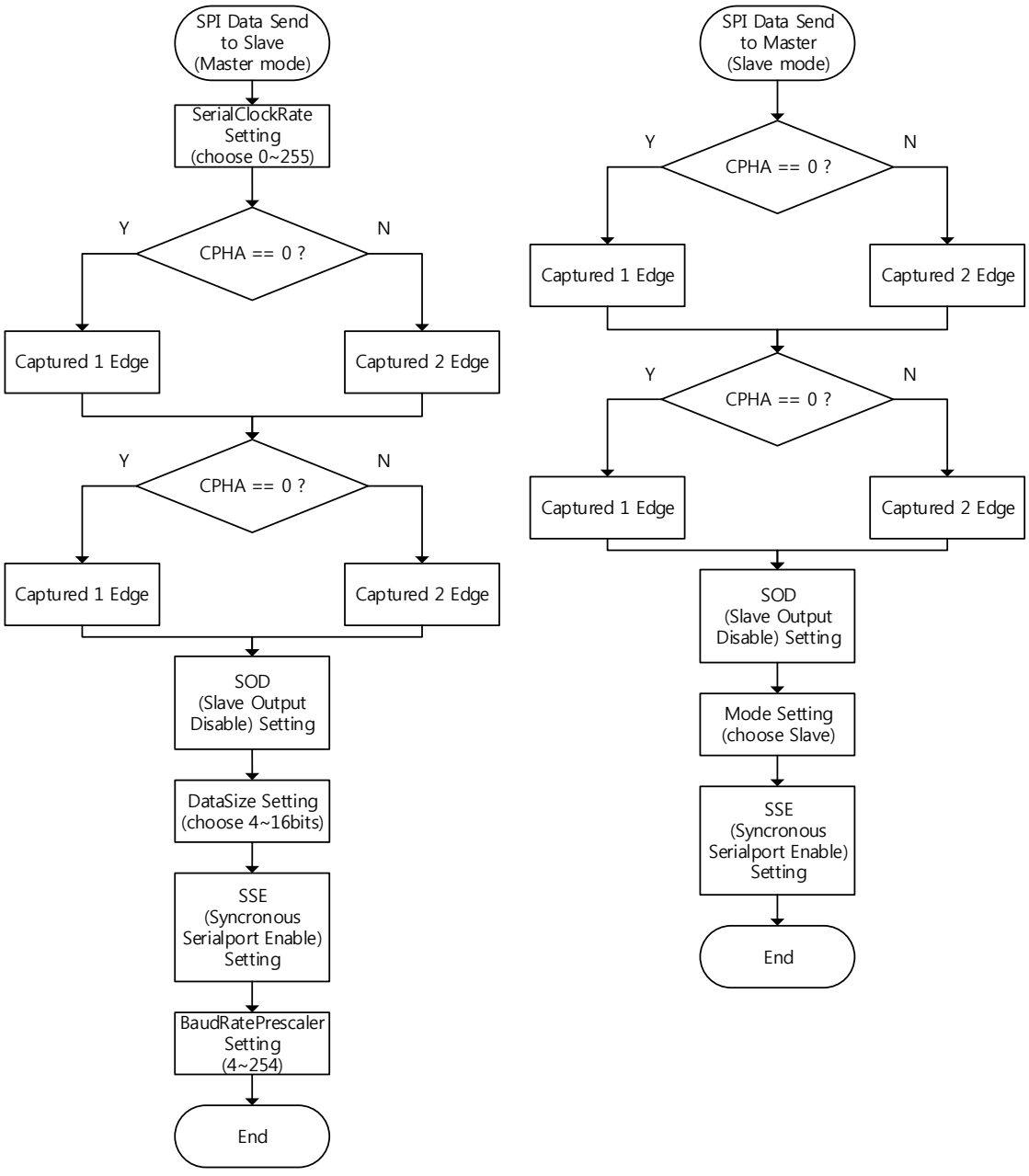


Figure 80. how to setting SPI mode flow chart

23.4 SSP0 Registers (Base Address : 0x4000_A000)

This section describes the SSP0 registers.

23.4.1 SSP0 Control register 0 (SSP0CR0)

Address offset: 0x0000

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR							SPH	SPO	FRF	DSS					
R/W							R/W	R/W	R/W	R/W					

[3:0] DSS – Data size select:

0000 : reserved, undefined operation

0001 : reserved, undefined operation

0010 : reserved, undefined operation

0011 : 4-bit data

[5:4] FRF – Frame Format

00 : Motorola SPI frame format

01 : TI synchronous serial frame format

10 : National Microwire frame format

11 : Reserved, undefined operation

[6] SPO – SSPCLKOUT polarity

This is applicable to Motorola SPI frame format only.

[7] SPH – SSPCLKOUT phase

This is applicable to Motorola SPI frame format only.

[15:8] SCR – Serial clock rate

The value SCR is used to generate the transmit and receive bit rate of the SSP. The bit rate is:

fSSPCLK / (CPSDVSR * (1 + SCR))

where

CPSDVSR is an even value from 2-254, programmed through the SSPCPSR register and SCR is a value from 0-255.

23.4.2 SSP0 Control register 1 (SSP0CR1)

Address offset: 0x0004

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	SOD	MS	SSE	LBM
												R/W	R/W	R/W	R/W

[0] LBM – Loop back mode:

0 : normal serial port operation enabled

1 : output of transmit serial shifter is connected to input of receive serial shifter internally

[1] SSE – Synchronous serial port enable:

0 : SSP0 operation disabled.

1 : SSP0 operation enabled.

[2] MS – Master or Slave mode select:

0 : device configured as master, default.

1 : device configured as slave.

[3] SOD – Slave-mode output disable.

This bit is relevant only in the slave mode, MS = 1. In multiple-slave systems, it is possible for a SSP0 master to broadcast a message to all slaves in the system while ensuring that only one slave drives data onto its serial output line. In such systems the RXD lines from multiple slaves could be tied together.

To operate in such systems, the SOD bit can be set if the SSP0 slave is not supposed to drive the SSPTXD line:

0 : SSP0 can drive the SSPTXD output in slave mode.

1 : SSP0 must not drive the SSPTXD output in slave mode.

23.4.3 SSP0 Data register (SSP0DR)

Address offset: 0x0008

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data															

R/W

15:0] DATA – Transmit/Receive FIFO:

Read: Read: receive FIFO.

Write: transmit FIFO.

You must right-justify data when the SSP0 is programmed for a data size that is less than 16 bits. Unused bits at the top are ignored by transmit logic. The receive logic automatically right-justifies.

23.4.4 SSP0 Status register (SSP0SR)

Address offset: 0x000C

Reset value: 0x0000_0003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	BSY	RFF	RNE	TNF	TFE
											R/W	R/W	R/W	R/W	R/W

[0] TFE – Transmit FIFO empty, RO

0 : Transmit FIFO is not empty.

1 : Transmit FIFO is empty.

[1] TNF – Transmit FIFO not full, RO:

0 : Transmit FIFO is full.

1 : Transmit FIFO is not full.

[2] RNE – Receive FIFO not empty, RO:

0 : Receive FIFO is empty.

1 : Receive FIFO is not empty.

[3] RFF – Receive FIFO full, RO:

0 : Receive FIFO is not full.

1 : Receive FIFO is full.

[4] BSY – SSP busy flag, RO:

0 : SSP is idle.No effect

1 : SSP is currently transmitting and/or receiving a frame or the transmit FIFO is not empty.

23.4.5 SSP0 Clock prescale register (SSP0CPSR)

Address offset: 0x0010

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	CPSDVSR							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[7:0] CPSDVSR – Clock prescale divisor

This must be an even number from 2-254, depending on the frequency of SSPCLK. The least significant bit always returns zero on reads.

23.4.6 SSP0 Interrupt mask set or clear register (SSP0IMSC)

Address offset: 0x0014

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	TXIM	RXIM	RTIM	RORIM
												R/W	R/W	R/W	R/W

[0] RORIM – Receive overrun interrupt mask:

0 : Receive FIFO written to while full condition interrupt is masked.

1 : Receive FIFO written to while full condition interrupt is not masked.

[1] RTIM – Receive timeout interrupt mask:

0 : Receive FIFO not empty and no read prior to timeout period interrupt is masked.

1 : Receive FIFO not empty and no read prior to timeout period interrupt is not masked.

[2] RXIM – Receive FIFO interrupt mask:

0 : Receive FIFO half full or less condition interrupt is masked.

1 : Receive FIFO half full or less condition interrupt is not masked.

[3] TXIM – Transmit FIFO interrupt mask:

0 : Transmit FIFO half empty or less condition interrupt is masked.

1 : Transmit FIFO half empty or less condition interrupt is not masked.

23.4.7 SSP0 Raw interrupt status register (SSP0RIS)

Address offset: 0x0018

Reset value: 0x0000_00004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	TXRIS	RXRIS	RTRIS	RORRIS
												R/W	R/W	R/W	R/W

[0] RORRIS – Gives the raw interrupt state, prior to masking, of the SSPRORINTR interrupt

[1] RTRIS – Gives the raw interrupt state, prior to masking, of the SSPRTINTR interrupt

[2] RXRIS – Gives the raw interrupt state, prior to masking, of the SSPRXINTR interrupt

[3] TXRIS – Gives the raw interrupt state, prior to masking, of the SSPTXINTR interrupt

23.4.8 SSP0 Masked interrupt status register, (SSP0MIS)

Address offset: 0x001C

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	TXMIS	RXMIS	RTMIS	RORMIS
												R/W	R/W	R/W	R/W

[0] RORMIS – Gives the receive over run masked interrupt status, after masking, of the SSPRORINTR interrupt

[1] RTMIS – Gives the receive timeout masked interrupt state, after masking, of the SSPRTINTR interrupt

[2] RXMIS – Gives the receive FIFO masked interrupt state, after masking, of the SSPRXINTR interrupt

[3] TXMIS – Gives the transmit FIFO masked interrupt state, after masking, of the SSPTXINTR interrupt

23.4.9 SSP0 Interrupt clear register (SSP0ICR)

Address offset: 0x0020

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	RTIC	RORIC
														R/W	R/W

[0] RORICS – Clears the SSPRORINTR interrupt

[1] RTIC – Clears the SSPRTINTR interrupt

23.4.10 SSP0 DMA control register, (SSP0DMACR)

Address offset: 0x0024

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TXDMAE	RXDMAE
														R/W	R/W

[0] RXDMAE – Receive DMA Enable:

0 : DMA for the receive FIFO is disabled.

1 : DMA for the receive FIFO is enabled.

[1] TXDMAE – Transmit DMA Enable:

0 : DMA for the transmit FIFO is disabled.

1 : DMA for the transmit FIFO is enabled.

23.5 Register map

The following Table 41 summarizes the SSP0 registers.

Table 41 SSP0 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	SSPCR0																	SCR								SPH	SPO			DSS				Control register 0
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x04	SSPCR1																													SOD	MS	SSE	LBM	Control register 1
	reset value																													0	0	0	0	
0x08	SSPDR																	Data																Data register
	reset value																	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0C	SSPSR																												BSY	RFF	RNE	TNF	TFE	Status register
	reset value																												0	0	0	1	1	
0x10	SSPCPSR																									CPSDVSR								Clock prescale register
	reset value																									0	0	0	0	0	0	0	0	
0x14	SSPIMSC																													TXIM	RXIM	RTIM	RORIM	Interrupt Mask set or clear register
	reset value																													0	0	0	0	
0x18	SSPRIS																													TXRIS	RXRIS	RTRIS	RORRIS	Raw interrupt status register
	reset value																													1	0	0	0	
0x1C	SSPMIS																													TXMIS	RXMIS	RTMIS	RORMIS	Masked interrupt status register
	reset value																													0	0	0	0	
0x20	SSPICR																															RTIC	RORIC	Interrupt clear register
	reset value																															0	0	
0x24	SSPDMACR																															TXDMAE	RXDMAE	DMA control regsiter
	reset value																															0	0	

23.6 SSP1 Registers (Base Address : 0x4000_B000)

This section describes the SSP0 registers.

23.6.1 SSP1 Control register 0 (SSP1CR0)

Address offset: 0x0000

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR							SPH	SPO	FRF	DSS					
R/W							R/W	R/W	R/W	R/W					

[3:0] DSS – Data size select:

0000 : reserved, undefined operation

0001 : reserved, undefined operation

0010 : reserved, undefined operation

0011 : 4-bit data

[5:4] FRF – Frame Format

00 : Motorola SPI frame format

01 : TI synchronous serial frame format

10 : National Microwire frame format

11 : Reserved, undefined operation

[6] SPO – SSPCLKOUT polarity

This is applicable to Motorola SPI frame format only.

[7] SPH – SSPCLKOUT phase

This is applicable to Motorola SPI frame format only.

[15:8] SCR – Serial clock rate

The value SCR is used to generate the transmit and receive bit rate of the SSP.

The bit rate is:

fSSPCLK / (CPSDVSR * (1 + SCR))

where

CPSDVSR is an even value from 2-254, programmed through the SSPCPSR register and SCR is a value from 0-255.

23.6.2 SSP1 Control register 1 (SSP1CR1)

Address offset: 0x0004

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	SOD	MS	SSE	LBM
												R/W	R/W	R/W	R/W

[0] LBM – Loop back mode:

0 : normal serial port operation enabled

1 : output of transmit serial shifter is connected to input of receive serial shifter internally

[1] SSE – Synchronous serial port enable:

0 : SSP1 operation disabled.

1 : SSP1 operation enabled.

[2] MS – Master or Slave mode select:

0 : device configured as master, default.

1 : device configured as slave.

[3] SOD – Slave-mode output disable.

This bit is relevant only in the slave mode, MS = 1. In multiple-slave systems, it is possible for a SSP1 master to broadcast a message to all slaves in the system while ensuring that only one slave drives data onto its serial output line. In such systems the RXD lines from multiple slaves could be tied together.

To operate in such systems, the SOD bit can be set if the SSP1 slave is not supposed to drive the SSPTXD line:

0 : SSP1 can drive the SSPTXD output in slave mode.

1 : SSP1 must not drive the SSPTXD output in slave mode.

23.6.3 SSP1 Data register (SSP1DR)

Address offset: 0x0008

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data															

R/W

[15:0] DATA – Transmit/Receive FIFO:

Read: Read: receive FIFO.

Write: transmit FIFO.

You must right-justify data when the SSP1 is programmed for a data size that is less than 16 bits. Unused bits at the top are ignored by transmit logic. The receive logic automatically right-justifies.

23.6.4 SSP1 Status register (SSP1SR)

Address offset: 0x000C

Reset value: 0x0000_0003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	BSY	RFF	RNE	TNF	TFE
											R/W	R/W	R/W	R/W	R/W

[0] TFE – Transmit FIFO empty, RO

0 : Transmit FIFO is not empty.

1 : Transmit FIFO is empty.

[1] TNF – Transmit FIFO not full, RO:

0 : Transmit FIFO is full.

1 : Transmit FIFO is not full.

[2] RNE – Receive FIFO not empty, RO:

0 : Receive FIFO is empty.

1 : Receive FIFO is not empty.

[3] RFF – Receive FIFO full, RO:

0 : Receive FIFO is not full.

1 : Receive FIFO is full.

[4] BSY – SSP busy flag, RO:

0 : SSP is idle.No effect

1 : SSP is currently transmitting and/or receiving a frame or the transmit FIFO is not empty.

23.6.5 SSP1 Clock prescale register (SSP1CPSR)

Address offset: 0x0010

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	CPSDVSR							
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[7:0] CPSDVSR – Clock prescale divisor

This must be an even number from 2-254, depending on the frequency of SSPCLK. The least significant bit always returns zero on reads.

23.6.6 SSP1 Interrupt mask set or clear register (SSP1IMSC)

Address offset: 0x0014

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	TXIM	RXIM	RTIM	RORIM
												R/W	R/W	R/W	R/W

[0] RORIM – Receive overrun interrupt mask:

0 : Receive FIFO written to while full condition interrupt is masked.

1 : Receive FIFO written to while full condition interrupt is not masked.

[1] RTIM – Receive timeout interrupt mask:

0 : Receive FIFO not empty and no read prior to timeout period interrupt is masked.

1 : Receive FIFO not empty and no read prior to timeout period interrupt is not masked.

[2] RXIM – Receive FIFO interrupt mask:

0 : Receive FIFO half full or less condition interrupt is masked.

1 : Receive FIFO half full or less condition interrupt is not masked.

[3] TXIM – Transmit FIFO interrupt mask:

0 : Transmit FIFO half empty or less condition interrupt is masked.

1 : Transmit FIFO half empty or less condition interrupt is not masked.

23.6.7 SSP1 Raw interrupt status register (SSP1RIS)

Address offset: 0x0018

Reset value: 0x0000_00004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	TXRIS	RXRIS	RTRIS	RORRIS
												R/W	R/W	R/W	R/W

[0] RORRIS – Gives the raw interrupt state, prior to masking, of the SSPRORINTR interrupt

[1] RTRIS – Gives the raw interrupt state, prior to masking, of the SSPRTINTR interrupt

[2] RXRIS – Gives the raw interrupt state, prior to masking, of the SSPRXINTR interrupt

[3] TXRIS – Gives the raw interrupt state, prior to masking, of the SSPTXINTR interrupt

23.6.8 SSP1 Masked interrupt status register, (SSP1MIS)

Address offset: 0x001C

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	TXMIS	RXMIS	RTMIS	RORMIS
												R/W	R/W	R/W	R/W

[0] RORMIS – Gives the receive over run masked interrupt status, after masking, of the SSPRORINTR interrupt

[1] RTMIS – Gives the receive timeout masked interrupt state, after masking, of the SSPRTINTR interrupt

[2] RXMIS – Gives the receive FIFO masked interrupt state, after masking, of the SSPRXINTR interrupt

[3] TXMIS – Gives the transmit FIFO masked interrupt state, after masking, of the SSPTXINTR interrupt

23.6.9 SSP1 Interrupt clear register (SSP1ICR)

Address offset: 0x0020

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	RTIC	RORIC
														R/W	R/W

[0] RORICS – Clears the SSPRORINTR interrupt

[1] RTIC – Clears the SSPRTINTR interrupt

23.6.10 SSP1 DMA control register, (SSP1DMACR)

Address offset: 0x0024

Reset value: 0x0000_00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
res	res	res	res	res	res	res	res	res	res	res	res	res	res	res	res

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	res	res	res	res	res	res	res	TXDMAE	RXDMAE
														R/W	R/W

[0] RXDMAE – Receive DMA Enable:

0 : DMA for the receive FIFO is disabled.

1 : DMA for the receive FIFO is enabled.

[1] TXDMAE – Transmit DMA Enable:

0 : DMA for the transmit FIFO is disabled.

1 : DMA for the transmit FIFO is enabled.

23.7 Register map

The following Table 42 summarizes the SSP1 registers.

Table 42 SSP1 register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	비고
0x00	SSPCR0																	SCR								SPH	SPO			DSS				Control register 0
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x04	SSPCR1																													SOD	MS	SSE	LBM	Control register 1
	reset value																													0	0	0	0	
0x08	SSPDR																	Data																Data register
	reset value																	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0C	SSPSR																												BSY	RFF	RNE	TNF	TFE	Status register
	reset value																												0	0	0	1	1	
0x10	SSPCPSR																									CPSDVSR								Clock prescale register
	reset value																									0	0	0	0	0	0	0	0	
0x14	SSPIMSC																													TXIM	RXIM	RTIM	RORIM	Interrupt Mask set or clear register
	reset value																													0	0	0	0	
0x18	SSPRIS																													TXRIS	RXRIS	RTRIS	RORRIS	Raw interrupt status register
	reset value																													1	0	0	0	
0x1C	SSPMIS																													TXMIS	RXMIS	RTMIS	RORMIS	Masked interrupt status register
	reset value																													0	0	0	0	
0x20	SSPICR																															RTIC	RORIC	Interrupt clear register
	reset value																															0	0	
0x24	SSPDMACR																															TXDMAE	RXDMAE	DMA control regsiter
	reset value																															0	0	

Document History Information

Version	Date	Descriptions
Ver. 1.0.0	07SEP2015	Initial Release
Ver. 1.0.1	08JAN2016	1. Bit rate in SPI interface changed ‘up to 2MHz and higher’ to ‘up to 20MHz’. 2. Bit rate generation example changed in 23.3.11 Programming the SSPCR1 Control Register
Ver. 1.0.2	05FEB2016	Modified the problem with none mention of 2nd Function on PB_06 in Table 8 functional description table
Ver. 1.0.3	08MAR2016	In 2.2.2Memory map, GPIO0,1,2,3 changed to GPIOA,B,C,D

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