Table of Contents

1. GENERAL DESCRIPTION 6
2. FEATURES 7
3. PIN CONFIGURATION 8
3.1 Ballout 1-CS Non-Merged Mode (Top View, MF=0) 8
3.2 Ballout 2-CS Non-Merged Mode (Top View, MF=0) 9
3.3 Ballout Merged Mode (Top View, MF=0) 10
4. PIN DESCRIPTION 11
4.1 Signal Description 11
4.2 Addressing 12
5. STATE DIAGRAM 13
5.1 State Diagram for One Activated Bank 13
5.1.1 State diagram for one bank 13
5.1.2 Function Truth Table for more than one Activated Bank 14
5.1.2.1 Function Truth Table 14
5.1.3 Function Truth Table for CKE 15
5.2 Functional Block Diagram in 1-CS Mode 16
5.3 Functional Block Diagram in 2-CS Mode 17
6. FUNCTIONAL DESCRIPTION 18
6.1 System Configurations 18
6.1.1 System Configurations in 1-CS Mode and 2-CS Mode 18
6.1.2 Initialization in 1– CS mode 19
6.1.3 Initialization in 2– CS mode 20
6.1.3.1 Power Up Sequence 21
.2 Mirror Function 22
6.2.1 Ball Assignment with Mirror Function 22
6.3 Commands 23
6.3.1 Command Overview for 1-CS mode 23
6.3.2 Command Overview for 2-CS mode 24
6.3.3 Description of Command 25
6.3.4 Minimum delay from RD/A and WR/A to any other command (to another bank) with concurrent AP 28
6.4 Boundary Scan 28
6.4.1 General Description 28
6.4.2 Disabling the scan feature 28
6.4.2.1 Internal Block Diagram (Reference only) 29
6.4.2.2 Boundary Scan Exit Order 29
6.4.2.3 Scan Pin Description 30
6.4.2.4 Scan DC Electrical Characteristics and Operating Condition 30
6.4.2.5 Scan Capture Timing 31

6.4.2.6 Scan Shift Timing 31
6.4.2.7 Scan AC Electrical Characteristic 32
6.4.3 Scan Initialization 32
6.4.3.1 Scan Initialization for Stand-Alone Mode 32
6.4.3.2 Scan Initialization for Stand-Alone mode 33
6.4.4 Scan Initialization in regular SGRAM operation 33
6.4.4.1 Scan Initialization Sequence within regular SGRAM Mode 34
6.4.5 Scan Exit Sequence 35
6.4.5.1 Boundary Scan Exit Sequence 35
6.4.5.2 Scan AC Electrical Parameter 35
6.5 Programmable impedance output drivers and active terminations 36
6.5.1 GDDR3 IO Driver and Termination 36
6.5.1.1 Output Deiver simplified schematic 37
6.5.1.2 Range of external resistance ZQ 37
6.5.1.3 Termination Types and Activation 37
6.5.2 Self Calibration for Driver and Termination 38
6.5.2.1 Termination update Keep Out time after Autorefresh command 38
6.5.2.2 Number of Legs used for Terminator and Driver Self Calibration 39
6.5.2.3 Self Calibration of PMOS and NMOS Legs 39
6.5.3 Dynamic Switching of DQ terminations 40
6.5.3.1 ODT Disable Timing during a READ command 40
6.5.4 Output impedance and Termination DC Electrical Characteristics 41
6.5.4.1 DC Electrical Characteristic 41
6.6 Mode Register Set Command (MRS) 42
6.6.1 Mode Register Set Command 42
6.6.2 Mode Registers 42
6.6.2.1 Mode Register (MRS) 42
6.6.2.2 Mode Register (MRS) 43
6.6.2.3 Mode Register Set Timing 43
6.6.3 Burst Length and Burst Type 44
6.6.3.1 Burst Length 44
6.6.3.2 Burst type 44
6.6.4 CAS Latency 44
6.6.5 Write Latency 44
6.6.6 DLL Reset 45
6.6.7 Test mode 45
6.7 Extended Mode Register Set Command (EMRS1) 45
6.7.1 Extended Mode Register Set Command 46
6.7.2 Extended Mode Register 1 (EMRS1) 46
6.7.2.1 Extended Mode Register 1 (EMRS1) 47
6.7.2.2 Extended Mode Register Set Timing 48
6.7.3 Chip Select Mode 48
6.7.4 DLL 48
6.7.5 Write Recovery 48

6.7.6 Termination Rtt 48
6.7.7 Impedance Autocalibration of Output Buffer and Active Terminator 49
6.7.7.1 Impedance Options 49
6.7.7.2 Timing of Vendor Code and Revision ID Generation on DQ[7:0] 49
6.7.8 Output Driver Impedance 50
6.7.9 Data Termination 50
6.7.10 Address command termination 50
6.8 Extended Mode Register 2 Set Command (EMRS2) 50
6.8.1 Extended Mode Register 2 Set Command 51
6.8.2 Extended Mode Register 2 (EMRS2) 51
6.8.2.1 Extended Mode Register 2 (EMRS2) 52
6.8.2.2 Impedance Offsets 52
6.8.2.3 Merged Mode 52
6.8.3 OCD Pull Down Offset 52
6.8.4 ODT Pull Up Offset 52
6.9 Extended Mode Register 3 (EMRS3) 53
6.10 Vendor Code and Revision ID 53
6.10.1 Vendor ID Code 53
6.11 Bank / Row Activation (ACT) 54
6.11.1 Activating a specific row 54
6.11.2 Bank Activation Timing 55
6.11.3 Bank Activation Timing on different rank in 2-CS mode 55
6.11.4 Four Window Active tFAW 55
6.11.5 Clock, CKE and command / Address Timings 56
6.12 Bank Activations with REFRESH 56
6.12.1 Bank Activations with REFRESH Command 56
6.13 Writes (WR) 57
6.13.1 Write - Basic Information 57
6.13.1.1 Write Command 58
6.13.1.2 Mapping of WDQS and DM Signals 58
6.13.1.3 Basic Write Burst / DM Timing 59
6.14 Write - Basic Sequence 60
6.15 Write - Consecutive Bursts 61
6.15.1Gapless Bursts 61
6.15.1.1 Gapless Write Bursts 61
6.15.2 Bursts with Gaps 62
6.15.2.1 Consecutive Write Bursts with Gaps 62
6.15.3 Write with Autoprecharge 63
6.15.4 Write followed by Read 64
6.15.5 Write followed by Read on different ranks in 2-CS mode 65
6.15.6 Write followed by DTERDIS 66
6.15.7 Write with Autoprecharge followed by Read / Read with Autoprecharge on another bank 67
6.15.8 Write followed by Precharge on same bank 68

6.16 Reads (RD) 69
6.16.1 Read - Basic Information 69
6.16.1.1 Read Command 70
6.16.1.2 Basic Read Burst Timing 71
6.16.2 Read - Basic Sequence 72
6.16.2.1 Read Burst 72
6.16.3 Consecutive Read Bursts 73
6.16.3.1 Gapless Bursts 73
6.16.4 Bursts with Gaps 74
6.16.4.1 Consecutive Read Bursts with Gaps 74
6.16.5 Read followed by DTERDIS 75
6.16.6 Read with Autoprecharge 76
6.16.7 Read followed by Write 77
6.16.8 Read followed by Precharge on the same Bank 78
6.17 Data Termination Disable (DTERDIS) 79
6.17.1 Data Terminal Disable Command 79
617.1.1 DTERDIS Timing 80
6.17.2 DTERDIS followed by DTERDIS 81
6.17.3 DTERDIS followed by READ 82
6.17.4 DTERDIS followed by Write 83
6.18 Precharge (PRE/PREALL) 84
6.18.1 Precharge Command 84
6.18.2 BA2, BA1 and BA0 precharge bank selection within one rank 85
6.18.3 Precharge Timing 85
6.19 Auto Refresh Command (AREF) 86
6.19.1 Auto Refresh Command 86
6.19.2 Auto Refresh Cycle 87
6.20 Self-Refresh 87
6.20.1 Self-Refresh Entry (SREFEN) 87
6.20.1.1 Self-Refresh Entry Command 88
6.20.1.2 Self Refresh Entry 89
6.21 Self-Refresh Exit (SREFEX) 89
6.21.1 Self Refresh Exit Command 90
6.21.2 Self Refresh Exit 90
6.22 Power-Down 91
6.22.1 Power Down Command 91
6.22.2 Power-Down Mode 92
7 ELECTRICAL CHARACTERISTICS 93
7.1 Absolute Maximum Ratings and Operation Conditions 93
7.1.1 Absolute Maximum Rating 93
7.2 DC Operation Conditions 93
7.2.1 Recommended Power & DC Operation Conditions 93

7.2.1.1 Power & DC Operation Conditions (0 °C ≤ T_C ≤ 105 °C) 93
7.3 DC & AC Logic Input Levels 94
7.3.1 DC & AC Logic Input Levels (0 °C ≤ T_C ≤ 105 °C) 94
7.4 Differential Clock DC and AC Levels 95
7.4.1 Differential Clock DC and AC Input conditions (0 °C ≤ T_C ≤ 105°C) 95
7.5 Output Test Conditions 95
7.6 Pin Capacitances 96
7.6.1 Pin Capacitances (VDDQ = 1.8 V, TA = 25°C, f = 1 MHz) 96
7.7 Driver current characteristics 96
7.7.1 Driver IV characteristics at 40 Ohms 96
7.7.1.1 40 Ohm Driver Pull-Down and Pull-up Characteristics 96
7.7.1.2 Programmed Driver IV Characteristics at 40 Ohm 97
7.8 Termination current characteristics 97
7.8.1 Termination IV Characteristic at 60 Ohms 97
7.8.1.1 60 Ohm Active Termination Characteristic 98
7.8.1.2 Programmed Terminator Characteristics at 60 Ohm 98
7.8.2 Termination IV Characteristic at 120 Ohms 99
7.8.2.1 120 Ohm Active Termination Characteristic 99
7.8.2.2 Programmed Terminator Characteristics of 120 Ohm 100
7.8.3 Termination IV Characteristic at 240 Ohms 100
7.8.3.1 240 Ohm Active Termination Characteristic 100
7.8.3.2 Programmed Terminator Characteristics at 240 Ohm 101
7.9 Operating Current Ratings 102
7.10 AC Timings 103
8. PACKAGE SPECIFICATION 106
9. ORDERING INFORMATION 107
10. REVISION HISTORY 108

1. GENERAL DESCRIPTION

The W641GG2JB 1-Gbit GDDR3 GRAPHICS SDRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. It contains 1,073,741,824 bits. The device can be configured to operate in two different modes:

- in 2-CS mode the chip is organized as two 512 Mbit memories of 8 banks each, with 4096 row locations and 512 column locations per bank.
- in 1-CS mode the chip is organized as one 1 Gbit memory, with 8192 row locations and 512 column locations per bank.

The GDDR3 GRAPHICS SDRAM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the GDDR3 GRAPHICS SDRAM effectively consists of a 4n data transfer every two clock cycles at the internal DRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Unidirectional data strobes are transmitted externally, along with data, for use in data capture at the receiver. RDQS is a strobe transmitted by the GDDR3 GRAPHICS SDRAM during READs. WDQS is the data strobe sent by the memory controller during WRITEs. RDQS is edge-aligned with data for READs and WDQS is center-aligned with data for WRITEs.

The GDDR3 GRAPHICS SDRAM operates from a differential clock (CLK and CLK#; the crossing of CLK going High and CLK# going Low will be referred to as the positive CLK edge). Commands (address and control signals) are registered at the positive CLK edge. Input data is registered at both edges of WDQS, and output data is referenced to both edges of RDQS, as well as to both edges of CLK.

Read and write accesses to the GDDR3 GRAPHICS SDRAM are burst oriented. The burst length can be programmed to 4 or 8 and the two least significant bits of the burst address are “Don’t Care” and internally set to LOW. Accesses start at a selected location and continue for a total of four or eight locations. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

2. FEATURES

- Density: 1Gbit
- Power supply (VDD, VDDQ): 1.8V ± 0.1V
- Organization: 1 Chip Select x 8 banks x 4M words x 32 bits (1-CS mode) and 2 Chip Select x 8 banks x 2M words x 32 bits (2-CS mode)
- Eight internal banks per Chip Select for concurrent operation
- 4n prefetch architecture: 128 bit per array Read or Write access
- Double-data rate architecture: two data transfers per clock cycle
- Single ended interface for data, address and command
- Differential clock inputs CLK, CLK#
- Commands entered on each positive CLK edge
- Single ended Read strobe (RDQS) per byte, edge-aligned with Read data
- Single ended Write strobe (WDQS) per byte, center-aligned with Write data
- Write data mask (DM) function
- DLL aligns DQ and RDQS transitions with CLK clock edges for Reads
- Burst length (BL): 4 or 8
- Sequential burst type only
- Programmable CAS latency: 7 to 14
- Programmable Write latency: 3 to 7
- Auto precharge option for each burst access
- Pseudo open drain outputs with 40Ω pulldown, 40Ω pullup
- ODT: nom. values of 60Ω, 120Ω or 240Ω
- Programmable termination and driver strength offsets
- Refresh cycles: 8192 cycles/32ms
- Auto-refresh and self-refresh modes
- ODT and output drive strength auto-calibration with external resistor ZQ pin (240Ω)
- Programmable IO interface including on chip termination (ODT)
- tRAS lockout support
- Vendor ID for device identification
- Mirror function with MF pin
- Boundary Scan function with SEN pin
- t_{WR} programmable for Writes with Auto-Precharge
- Calibrated output drive. Active termination support
- Short RAS to CAS timing for Writes
- Operating case temperature range:
  Tcase = 0°C to +105°C
- Package: 136-ball TFBGA.
- RoHS Compliant Product

3. PIN CONFIGURATION

3.1 Ballout 1-CS Non-Merged Mode (Top View, MF=0)

1	2	3	4	5	6	7	8	9	10	11	12
V_{DDQ}	V_{DD}	V_{SS}	ZQ		A			MF	V_{SS}	V_{DD}	V_{DDQ}
V_{SSQ}	DQ0	DQ1	V_{SSQ}		B			V_{SSQ}	DQ9	DQ8	V_{SSQ}
V_{DDQ}	DQ2	DQ3	V_{DDQ}		C			V_{DDQ}	DQ11	DQ10	V_{DDQ}
V_{SSQ}	WDQS0	RDQS0	V_{SSQ}		D			V_{SSQ}	RDQS1	WDQS1	V_{SSQ}
V_{DDQ}	DQ4	DM0	V_{DDQ}		E			V_{DDQ}	DM1	DQ12	V_{DDQ}
V_{DD}	DQ6	DQ5	CAS#		F			CS0#	DQ13	DQ14	V_{DD}
V_{SS}	V_{SSQ}	DQ7	BA0		G			BA1	DQ15	V_{SSQ}	V_{SS}
V_{REF}	A1	RAS#	CKE		H			WE#	BA2	A5	V_{REF}
V_{SS}	A12	RAR	V_{DDQ}		J			V_{DDQ}	CLK#	CLK	V_{SS}
V_{DD}	A10	A2	A0		K			A4	A6	A8/AP	V_{DD}
V_{SS}	V_{SSQ}	DQ25	A11		L			A7	DQ17	V_{SSQ}	V_{SS}
V_{DD}	DQ24	DQ27	A3		M			A9	DQ19	DQ16	V_{DD}
V_{DDQ}	DQ26	DM3	V_{DDQ}		N			V_{DDQ}	DM2	DQ18	V_{DDQ}
V_{SSQ}	WDQS3	RDQS3	V_{SSQ}		P			V_{SSQ}	RDQS2	WDQS2	V_{SSQ}
V_{DDQ}	DQ28	DQ29	V_{DDQ}		R			V_{DDQ}	DQ21	DQ20	V_{DDQ}
V_{SSQ}	DQ30	DQ31	V_{SSQ}		T			V_{SSQ}	DQ23	DQ22	V_{SSQ}
V_{DDQ}	V_{DD}	V_{SS}	SEN		U			RES	V_{SS}	V_{DD}	V_{DDQ}

3.2 Ballout 2-CS Non-Merged Mode (Top View, MF=0)

1	2	3	4	5	6	7	8	9	10	11	12
V_{DDQ}	V_{DD}	V_{SS}	ZQ		A			MF	V_{SS}	V_{DD}	V_{DDQ}
V_{SSQ}	DQ0	DQ1	V_{SSQ}		B			V_{SSQ}	DQ9	DQ8	V_{SSQ}
V_{DDQ}	DQ2	DQ3	V_{DDQ}		C			V_{DDQ}	DQ11	DQ10	V_{DDQ}
V_{SSQ}	WDQS0	RDQS0	V_{SSQ}		D			V_{SSQ}	RDQS1	WDQS1	V_{SSQ}
V_{DDQ}	DQ4	DM0	V_{DDQ}		E			V_{DDQ}	DM1	DQ12	V_{DDQ}
V_{DD}	DQ6	DQ5	CAS#		F			CS0#	DQ13	DQ14	V_{DD}
V_{SS}	V_{SSQ}	DQ7	BA0		G			BA1	DQ15	V_{SSQ}	V_{SS}
V_{REF}	A1	RAS#	CKE		H			WE#	BA2	A5	V_{REF}
V_{SS}	RAR	CS1#	V_{DDQ}		J			V_{DDQ}	CLK#	CLK	V_{SS}
V_{DD}	A10	A2	A0		K			A4	A6	A8/AP	V_{DD}
V_{SS}	V_{SSQ}	DQ25	A11		L			A7	DQ17	V_{SSQ}	V_{SS}
V_{DD}	DQ24	DQ27	A3		M			A9	DQ19	DQ16	V_{DD}
V_{DDQ}	DQ26	DM3	V_{DDQ}		N			V_{DDQ}	DM2	DQ18	V_{DDQ}
V_{SSQ}	WDQS3	RDQS3	V_{SSQ}		P			V_{SSQ}	RDQS2	WDQS2	V_{SSQ}
V_{DDQ}	DQ28	DQ29	V_{DDQ}		R			V_{DDQ}	DQ21	DQ20	V_{DDQ}
V_{SSQ}	DQ30	DQ31	V_{SSQ}		T			V_{SSQ}	DQ23	DQ22	V_{SSQ}
V_{DDQ}	V_{DD}	V_{SS}	SEN		U			RES	V_{SS}	V_{DD}	V_{DDQ}

3.3 Ballout Merged Mode (Top View, MF=0)

1	2	3	4	5	6	7	8	9	10	11	12
V_{DDQ}	V_{DD}	V_{SS}	ZQ		A			MF	V_{SS}	V_{DD}	V_{DDQ}
V_{SSQ}	DQ0	DQ1	V_{SSQ}		B			V_{SSQ}	DQ9	DQ8	V_{SSQ}
V_{DDQ}	DQ2	DQ3	V_{DDQ}		C			V_{DDQ}	DQ11	DQ10	V_{DDQ}
V_{SSQ}	WDQS0	RDQS0	V_{SSQ}		D			V_{SSQ}	RDQS1	WDQS1	V_{SSQ}
V_{DDQ}	DQ4	DM0	V_{DDQ}		E			V_{DDQ}	DM1	DQ12	V_{DDQ}
V_{DD}	DQ6	DQ5	CAS#		F			CS0#	DQ13	DQ14	V_{DD}
V_{SS}	V_{SSQ}	DQ7	BA0		G			BA1	DQ15	V_{SSQ}	V_{SS}
V_{REF}	A1	RAS#	CKE		H			WE#	BA2	A5	V_{REF}
V_{SS}	RFU	A12/ CS1#	V_{DDQ}		J			V_{DDQ}	CLK#	CLK	V_{SS}
V_{DD}	A10	A2	A0		K			A4	A6	A8/AP	V_{DD}
V_{SS}	V_{SSQ}	DQ25	A11		L			A7	DQ17	V_{SSQ}	V_{SS}
V_{DD}	DQ24	DQ27	A3		M			A9	DQ19	DQ16	V_{DD}
V_{DDQ}	DQ26	DM3	V_{DDQ}		N			V_{DDQ}	DM2	DQ18	V_{DDQ}
V_{SSQ}	WDQS3	RDQS3	V_{SSQ}		P			V_{SSQ}	RDQS2	WDQS2	V_{SSQ}
V_{DDQ}	DQ28	DQ29	V_{DDQ}		R			V_{DDQ}	DQ21	DQ20	V_{DDQ}
V_{SSQ}	DQ30	DQ31	V_{SSQ}		T			V_{SSQ}	DQ23	DQ22	V_{SSQ}
V_{DDQ}	V_{DD}	V_{SS}	SEN		U			RES	V_{SS}	V_{DD}	V_{DDQ}

4. PIN DESCRIPTION

4.1 Signal Description

Ball	Type	Detailed Function
CLK, CLK#	Input	**Clock:**CLK and CLK# are differential clock inputs. Command and address inputs are latched on the rising edge of CLK. All latencies are referenced to CLK. CLK and CLK# are not internally terminated.
CKE	Input	**Clock Enable:**CKE High activates and CKE Low deactivates internal clock, device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operations (all banks idle), or Active Power-Down (row active in any bank). CKE is synchronous for Power-Down entry and exit and for Self Refresh entry. CKE must be maintained High throughout READ, WRITE and bus snoop bursts. Input buffers excluding CLK, CLK# and CKE are disabled during Power-Down. Input buffers excluding CKE are disabled during Self Refresh. The value of CKE latched at power-up with RES going High determines the termination value of the address and command inputs.
CS0#,CS1#	Input	**Chip Select:**Chip Select: CS# Low enables, and CS# High disables the command decoder. All commands except DTERDIS are masked when CS# is registered High, but internal command execution continues. CS# provides for individual device selection on memory channels with multiple memory devices. CS# is considered part of the command code. In 1-CS mode only CS0# is available. In 2-CS mode both CS0# and CS1# are available, and CS0# is exclusively used for Mode Register or Extended Mode Register programming and self refresh entry.
RAS#,CAS#, WE#	Input	**Command Inputs:**Command inputs: RAS#, CAS# and WE# (along with CS0# or CS1#) define the command to be entered.
BA0-BA2	Input	**Bank Address Inputs:**BA0-BA2 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0-BA2 also determine which Mode Register or Extended Mode Register is accessed with a MODE REGISTER SET command.
A0-A11 (A12)	Input	**Address Inputs:**Address inputs: provide the row address for ACTIVE commands and the column address and auto precharge function (A8) for READ and WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 Low, bank selected by BA0- BA2) or all banks (A8 High). The address inputs also provide the op-code during an MODE REGISTER SET command. A12 is the MSB row address in 1-CS mode.
DQ0-DQ31	I/O	**Data Inputs/Outputs:**Data Input/Output: 32 bit data bus
DM0-DM3	Input	**Input Data Masks:**Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled High along with that input data during a WRITE access. DM is sampled on the rising and falling edges of WDQS. DM0 is associated with DQ0-DQ7, DM1 with DQ8-DQ15, DM2 with DQ16-DQ23 and DM3 with DQ24-DQ31.
RDQS0-RDQS3	Output	**Read Data Strobes:** Output with read data. RDQS is edge-aligned with read data. RDQS0 is associated with DQ0-DQ7, RDQS1 with DQ8-DQ15, RDQS2 with DQ16-DQ23 and RDQS3 with DQ24-DQ31.
WDQS0-WDQS3	Input	**Write Data Strobes:**WRITE Data strobe: Input with write data. WDQS is center-aligned to the input data. WDQS0 is associated with DQ0-DQ7, WDQS1 with DQ8-DQ15, WDQS2 with DQ16-DQ23 and WDQS3 with DQ24-DQ31.
ZQ	Reference	**ODT Impedance Reference:** The ZQ ball is used to control the ODT impedance.

RES	Input	**Reset pin:**The RES pin is a Vddq CMOS input. RES is not internally terminated. When RES is at LOW state the chip goes into full reset. The chip stays in full reset until RES goes to HIGH state. The Low to High transition of the RES signal is used to latch the CKE value to set the value of the termination resistors of the address and command inputs. After exiting the full reset a complete initialization is required since the full reset sets the internal settings to default, including mode register bits.
MF	Input	**Mirror function :**MF is a VDDQ CMOS input. This pin must be hardwired on board either to a power or to a ground plane. With MF set to HIGH, the command and address pins are reassigned in order to allow for an easier routing on board for a back to back memory arrangement.
SEN	Input	**Scan Enable:**SEN is a VDDQ CMOS input. Must be tied to Ground when not in use.
V_{REF}	Supply	Reference voltage for command, address and data inputs.
V_{DDQ}	Supply	Isolated power for the input and output buffers .
V_{SSQ}	Supply	Isolated ground for the input and output buffers.
V_{DD}	Supply	Power Supply
V_{SS}	Supply	Ground
RFU		Reserved
RAR		Reserved for alternate rank (see ballouts)

4.2 Addressing

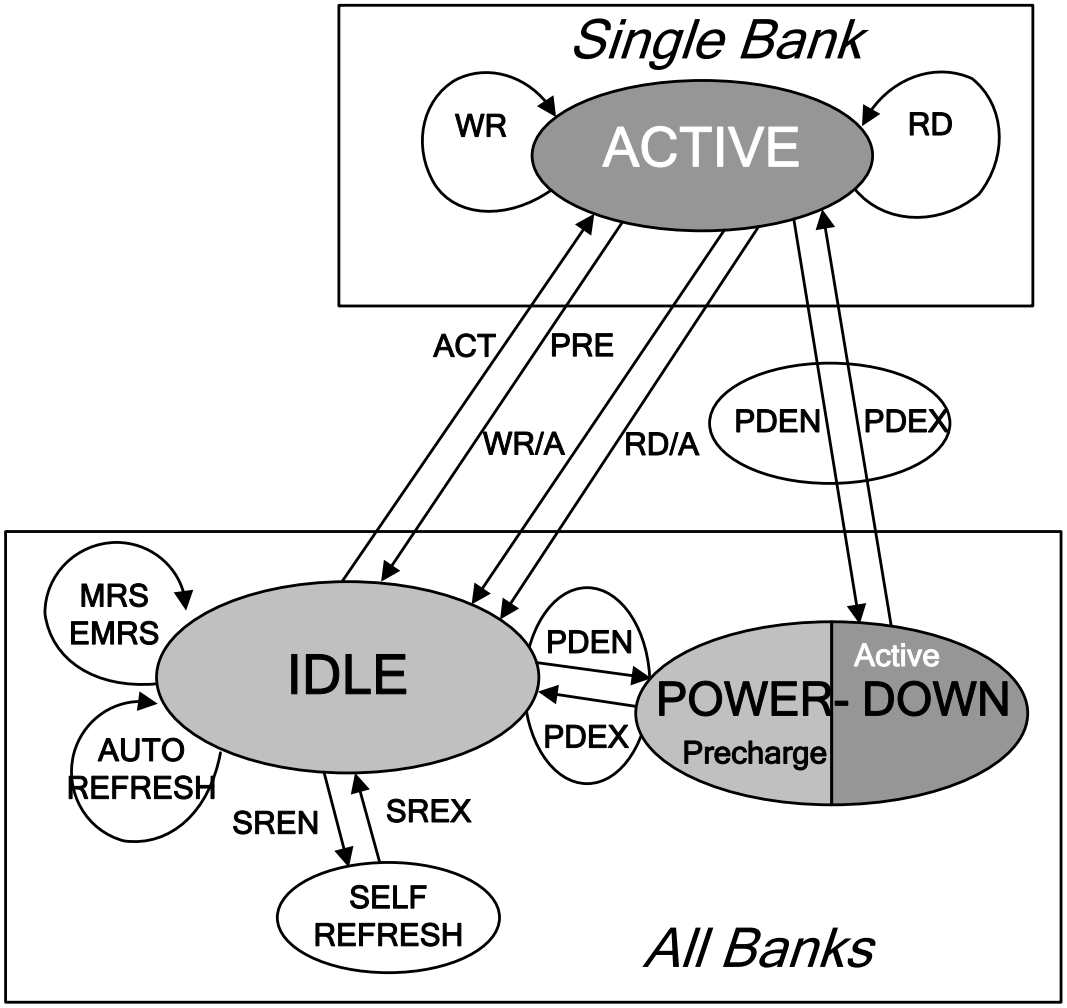
	2-CS Mode (CS0#,CS1#)	1-CS Mode (CS0#)
Number of ranks	2	1
Row Address	A0-A11	A0-A12
Column addresses	A2-A7,A9	A2-A7,A9
Bank address	BA0-BA2	BA0-BA2
Auto precharge	A8/AP	A8/AP
Page size	2 KB	2 KB
Refresh	8K/32 mS	8K/32 mS

5. STATE DIAGRAM

5.1 State Diagram for One Activated Bank

The following diagram shows all possible states and transitions for one activated bank. The other 37 banks of the Graphics SDRAM are assumed to be in idle state.

5.1.1 State diagram for one bank



5.1.2 Function Truth Table for more than one Activated Bank

If there is more than one bank activated in the Graphics SDRAM, some commands can be performed in parallel due to the chip's multibank architecture. The following table defines for which commands such a scheme is possible. All other transitions are illegal. Notes 1-11 define the start and end of the actions belonging to a submitted command. This table is based on the assumption that there are no other actions ongoing on bank n or bank m. If there are any actions ongoing on a third bank t_{RRD}, t_{RTW} and t_{WTR} have to be taken always into account.

5.1.2.1 Function Truth Table

Current State	Ongoing action on bank n	Possible action in parallel on bank m
ACTIVE	ACTIVATE[1]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[2]
	WRITE[3]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[4]
	WRITE/A	ACT, PRE, WRITE, WRITE/A, READ[6]
	READ[7)]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[8]
	READ/A[9)]	ACT, PRE, WRITE, WRITE/A, READ, READ/A [8]
	PRECHARGE[10]	ACT, PRE, WRITE, WRITE/A, READ, READ/A[11]
	PRECHARGE ALL [10]	-
	POWER DOWN ENTRY[12]	-
IDLE	ACTIVATE 1)	ACT
	POWER DOWN ENTRY [12]	-
	AUTO REFRESH[13]	-
	SELF REFRESH ENTRY [12]	-
	MODE REGISTER SET (MRS)[14]	-
	EXTENDED MRS [14]	-
	EXTENDED MRS 2[14]	-
POWER DOWN	POWER DOWN EXIT[15]	-
SELF REFRESH	SELF REFRESH EXIT[16]	-

Notes :

1. Action ACTIVATE starts with issuing the command and ends after t_{RCD}.
2. During action ACTIVATE an ACT command on another bank is allowed considering t_{RRD} or t_{RRD_RR}, a PRE command on another bank is allowed any time. WR, WR/A, RD and RD/A are always allowed.
3. Action WRITE starts with issuing the command and ends tWR after the first pos. edge of CLK following the last falling WDQS edge.
4. During action WRITE an ACT or a PRE command on another bank is allowed any time. A new WR or WR/A command on another bank must be separated by at least one NOP from the ongoing WRITE. RD or RD/A are not allowed before t_{WTR} or t_{WTR_RR} is met.
5. Action WRITE/A starts with issuing the command and ends tWR after the first positive edge of CLK following the last falling WDQS edge.
6. During action WRITE/A an ACT or a PRE command on another bank is allowed any time. A new WR or WR/A command on another bank has to be separated by at least one NOP from the ongoing command. RD is not allowed before or t_{WTR} or t_{WTR_RR} is met. RD/A is not allowed during an ongoing WRITE/A action.
7. Action READ starts with issuing the command and ends with the first positive edge of CLK following the last falling edge of RDQS.
8. During action READ and READ/A an ACT or a PRE command on another bank is allowed any time. A new RD or RD/A command on another bank has to be separated by at least one NOP from the ongoing command. A WR or WR/A command on another bank has to meet t_{RTW}.
9. Action READ/A starts with issuing the command and ends with the first positive edge of CLK following the last falling edge of RDQS.
10. Action PRECHARGE and PRECHARGE ALL start with issuing the command and ends after t_{RP}.

11. During Action ACTIVE an ACT command on another banks is allowed considering t_{RRD} or t_{RRD_RR}. A PRE command on another bank is allowed any time. WR, WR/A, RD and RD/A are always allowed.
12. During POWER DOWN and SELF REFRESH only the EXIT commands are allowed.
13. AUTO REFRESH starts with issuing the command and ends after t_{RFC}.
14. Actions MODE REGISTER SET, EXTENDED MODE REGISTER SET and EXTENDED MODE REGISTER 2 SET start with issuing the command and ends after t_{MRD}.
15. Action POWER DOWN EXIT starts with issuing the command and ends after t_{XPN}.
16. Action SELF REFRESH EXIT starts with issuing the command and ends after t_{XSC}.

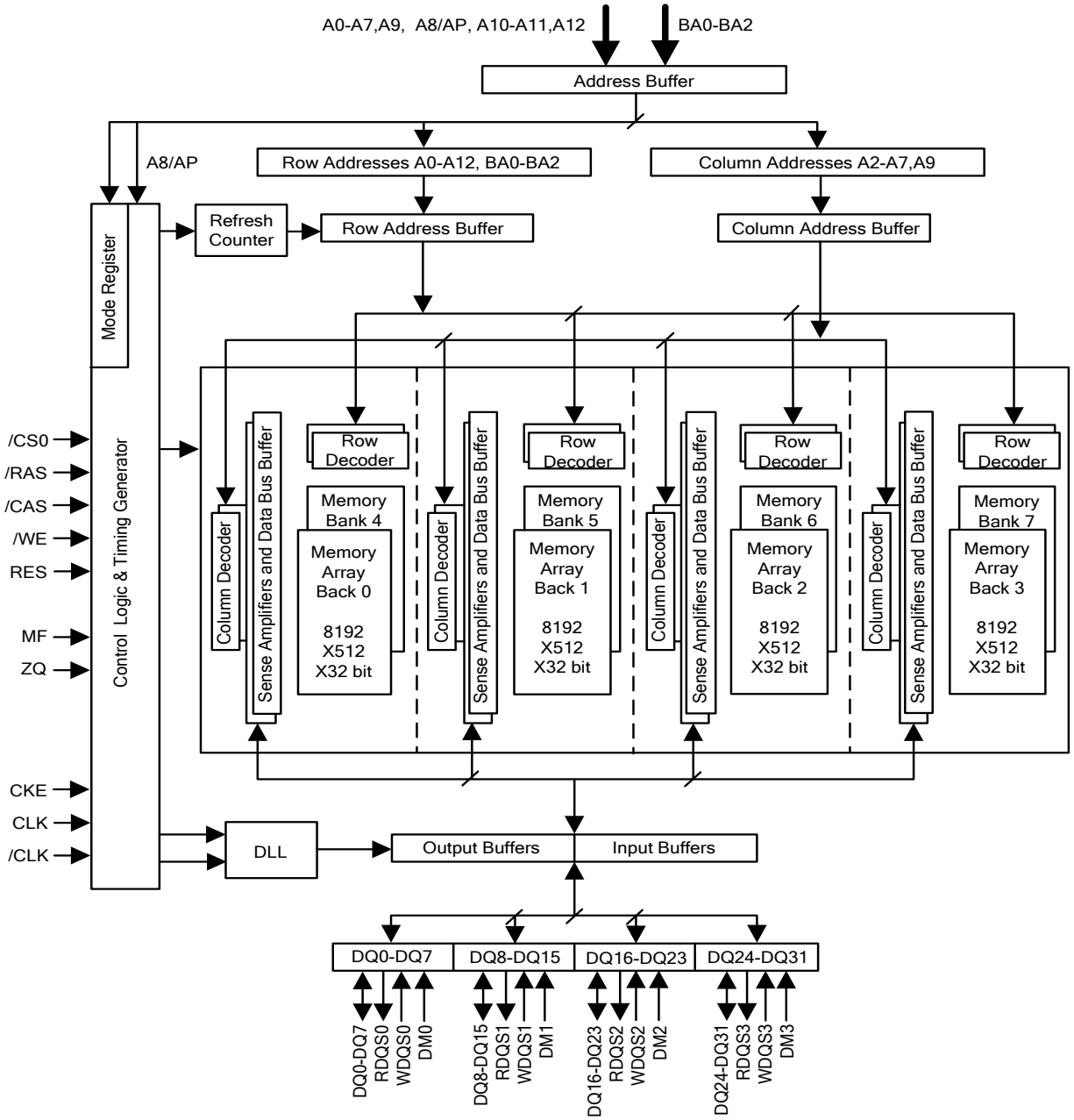
5.1.3 Function Truth Table for CKE

CKE N-1	CKE n	CURRENT STATE	COMMAND	ACTION
L	L	Power Down	X	Stay in Power Down
		Self Refresh	X	Stay in Self Refresh
L	H	Power Down	DESEL or NOP	Exit Power Down
		Self Refresh	DESEL or NOP	Exit Self Refresh [5]
H	L	All Banks Idle	DESEL or NOP	Entry Precharge Power Down
		Bank(s) Active	DESEL or NOP	Entry Active Power Down
		All Banks Idle	Auto Refresh	Entry Self Refresh

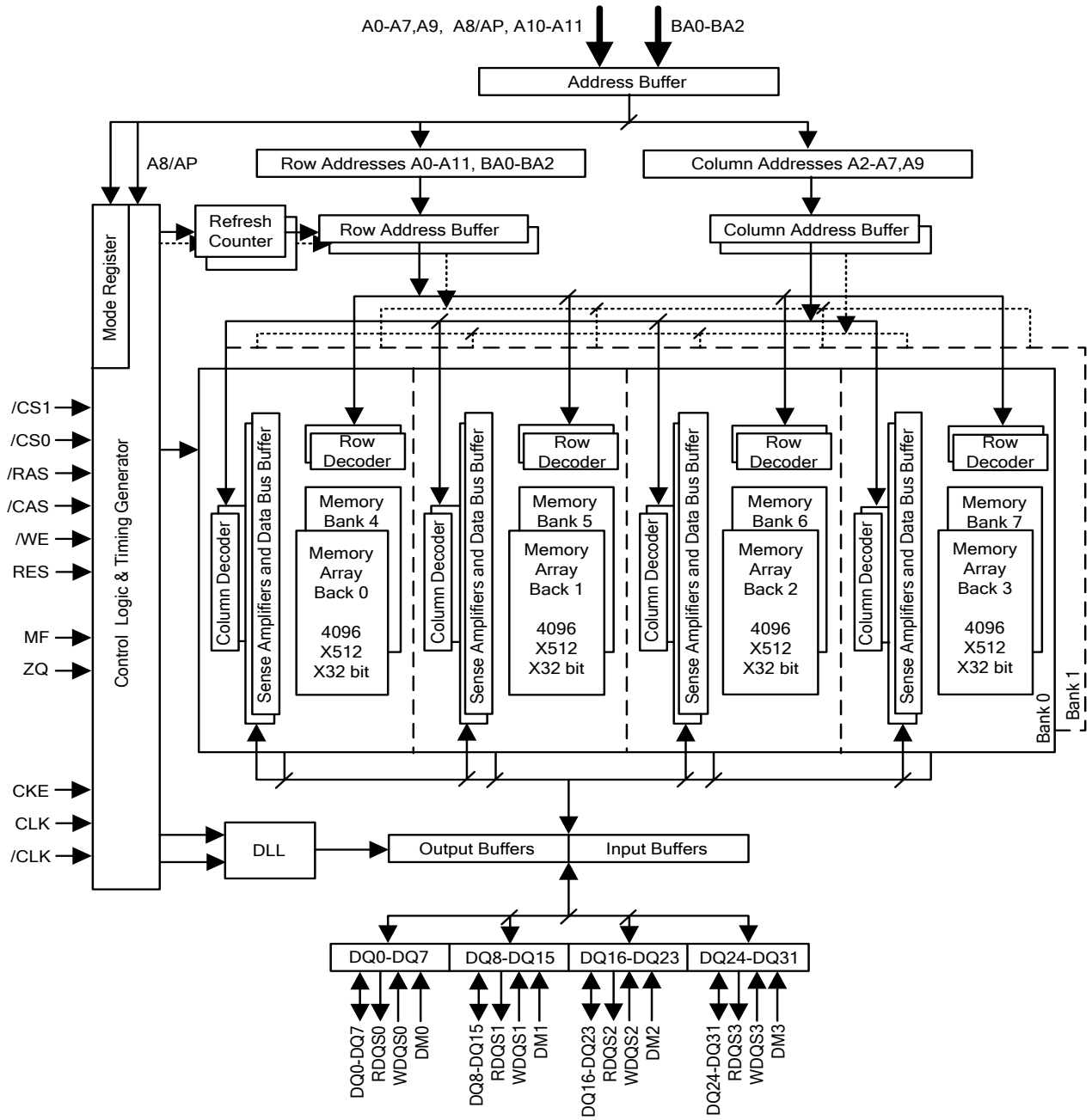
Notes :

1. CKEn is the logic step at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the GDDR3 Graphics RAM immediately prior to clock edge n.
3. COMMAND is the command registered at clock edge n, and ACTION is a result of COMMAND.
4. All states and sequences not shown are illegal or reserved.
5. DESEL or NOP commands should be issued on any clock edges occurring during the t_{XSR} period. A minimum of 1000 clock cycles is required before applying any other valid command.

5.2 Functional Block Diagram in 1-CS Mode



5.3 Functional Block Diagram in 2-CS Mode



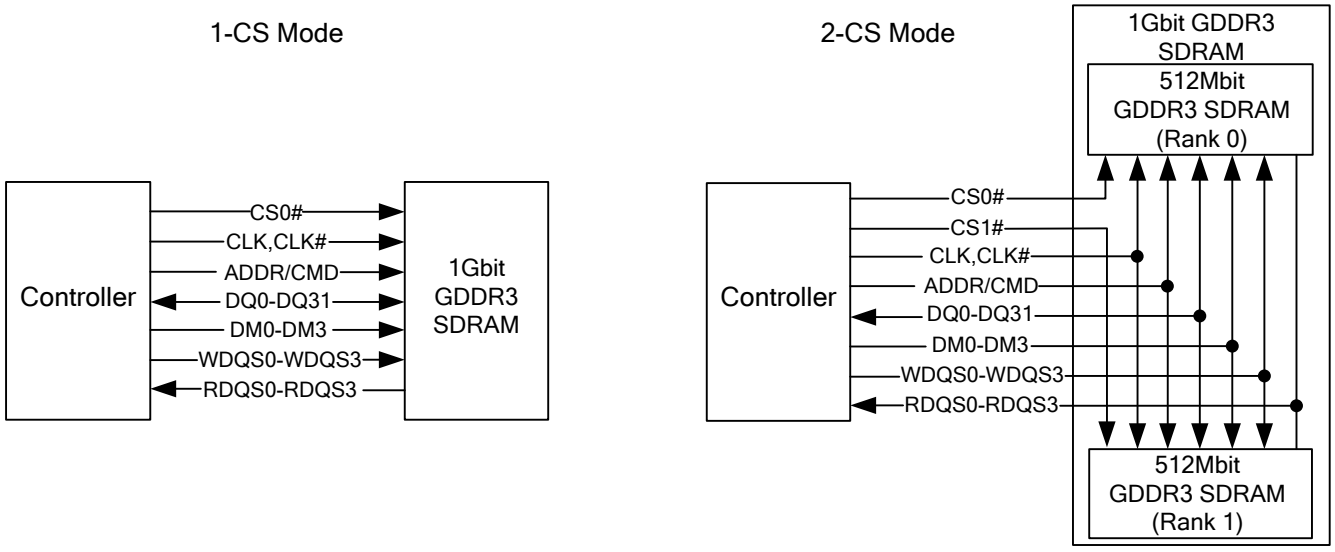
6. FUNCTIONAL DESCRIPTION

This section describe the unitization sequence of the GDRAM. It has been divided in to parts for each of the operations modes (1-CS or 2-CS). In the initialization, and before the choice of the operation mode by Mode Registration Set command, the default mode is 1-CS this implies a common initialization sequence up to point 7.

6.1 System Configurations

Figure shows typical system configurations for 1-CS mode and 2-CS mode.
2-CS mode is equivalent to a clamshell configuration with two 512Mbit devices (rank 0 and rank 1) sharing a common interface; it benefits from the single physical pin load of this monolithic solution.
In 1-CS mode the device is addressed as a single 8-bank device, and the MSB row address A12 selects between the upper and lower half of the die.

6.1.1 System Configurations in 1-CS Mode and 2-CS Mode



6.1.2 Initialization in 1– CS mode

The GDDR3 GRAPHICS SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation or permanent damage to the device.The following sequence is highly recommended for Power-Up:

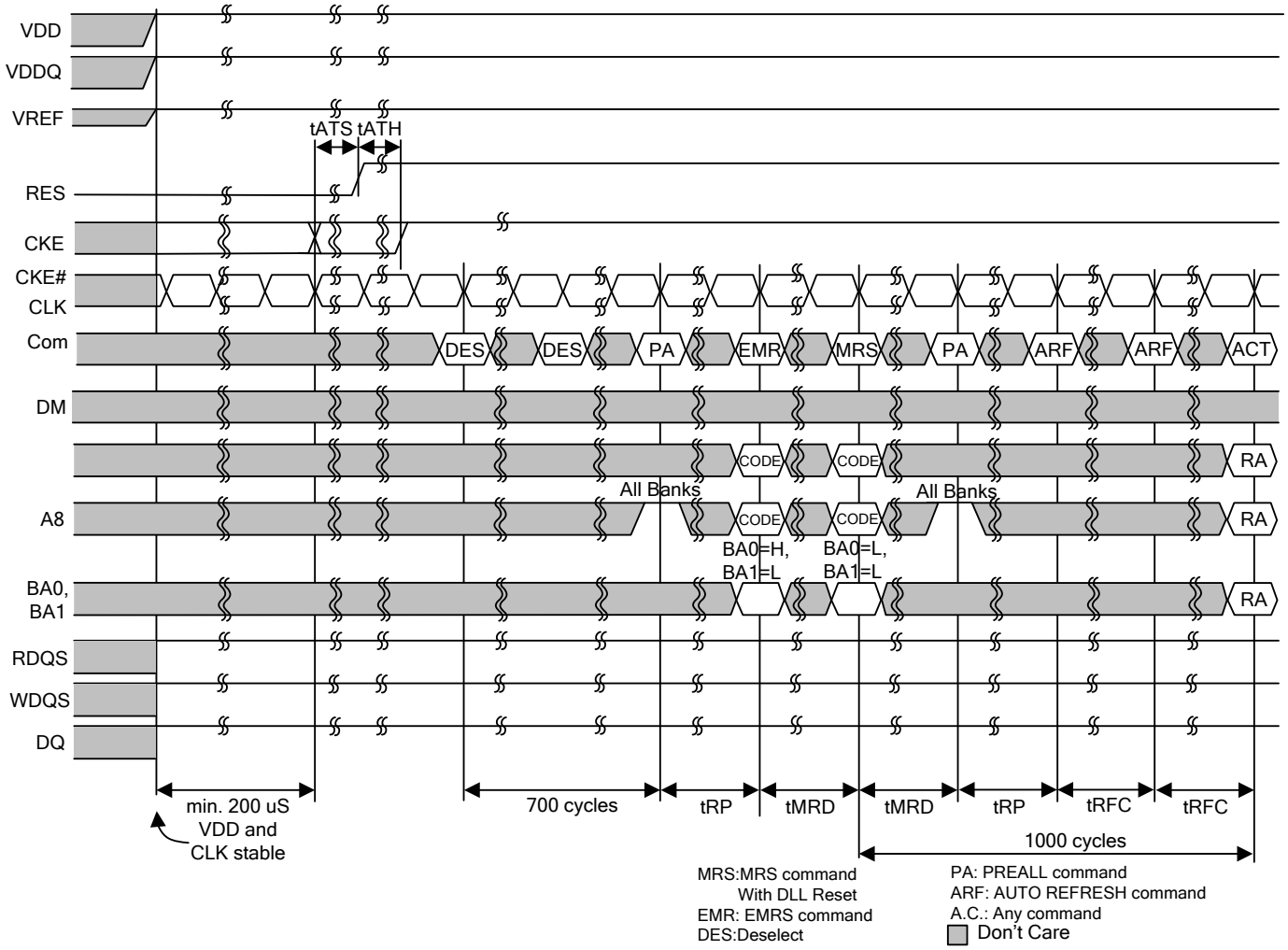
1. Apply power (V_{DD}, V_{DDQ}, V_{REF}). Apply V_{DD} before or at the same time as V_{DDQ}, apply V_{DDQ} before or at the same time as V_{REF}. Maintain RES = Low and CS0 = High to ensure that all the DQ outputs will be in HiZ state, all active terminations off and the DLL off. All other pins may be undefined.
2. Maintain stable conditions for 200 µs minimum for the GDDR3 to power up.
3. After clock is stable, set CKE to High or Low. After t_{ATS} minimum set RES to high. On the rising edge of RES, the CKE value is latched to determine the address and command bus termination value. If CKE is sampled LOW the address termination value is set to ZQ / 2. If CKE is sampled HIGH, the address and command bus termination is set to ZQ.
4. After t_{ATH} minimum, set CKE to high.
5. Wait a minimum of 700 cycles to calibrate and update the address and command termination impedances. Issue DESELECT on the command bus during these 700 cycles.
6. Apply a PRECHARGE ALL command by holding CS0 low and wait for t_{RP} to expire.
7. Issue an Extended Mode Register Set command to set the mode to 1-CS and activate the DLL. The mode selection will be done using the bank address BA2 that will be set to low level for 1-CS mode (in Dual Rank Mode).
8. Issue an Mode Register Set command after t_{MRD} is met to reset the DLL and define the operating parameters.
9. Wait 1000 cycles of clock input to lock the DLL. No Read command can be applied during this time. Since the impedance calibration is already completed, the DLL mimic circuitry can use the actual programmed driver impedance value.
10. Issue a PRECHARGE ALL command to each of the programmed ranks or issue single bank precharge commands to each of the 8 banks to place the chip in an idle state.
11. Issue or more AUTO REFRESH commands.

6.1.3 Initialization in 2– CS mode

The GDDR3 GRAPHICS SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation or permanent damage to the device.The following sequence is highly recommended for Power-Up:

1. Apply power (V_{DD}, V_{DDQ}, V_{REF}). Apply V_{DD} before or at the same time as V_{DDQ}, apply V_{DDQ} before or at the same time as V_{REF}. Maintain RES = Low and CS0 = High to ensure that all the DQ outputs will be in HiZ state, all active terminations off and the DLL off. All other pins may be undefined.
2. Maintain stable conditions for 200 µs minimum for the GDDR3 to power up.
3. After clock is stable, set CKE to High or Low. After t_{ATS} minimum set RES to high. On the rising edge of RES, the CKE value is latched to determine the address and command bus termination value. If CKE is sampled LOW the address termination value is set to ZQ / 2. If CKE is sampled HIGH, the address and command bus termination is set to ZQ
4. After tATH minimum, set CKE to high.
5. Wait a minimum of 700 cycles to calibrate and update the address and command termination impedances. Issue DESELECT on the command bus during these 700 cycles.
6. Apply a PRECHARGE ALL command by holding CS0 low and wait for t_{RP} to expire.
7. Issue an Extended Mode Register Set command to set the mode to 2-CS and activate the DLL. The mode selection will be done using the bank address BA2 that will be set to high level for 2-CS mode (in Single Rank Mode).
8. Issue an Mode Register Set command after t_{MRD} is met to reset the DLL and define the operating parameters.
9. Wait 1000 cycles of clock input to lock the DLL. No Read command can be applied during this time. Since the impedance calibration is already completed, the DLL mimic circuitry can use the actual programmed driver impedance value.
10. Issue a PRECHARGE ALL command to each of the programmed ranks or issue single bank precharge commands to each of the 16 banks in 2-CS Mode, to place the chip in an idle state.
11. Issue or more AUTO REFRESH commands.

6.1.3.1 Power Up Sequence



.2 Mirror Function

The GDDR3 GRAPHICS SDRAM provides a mirror function (MF) pin to change the physical location of the command and address pins assisting in routing devices back to back. The MF ball should be tied directly to VSSQ or VDDQ depending on the control line orientation desired. The pins affected by this Mirror Function mode are listed in Table . The CS1# and A12 pins are not affected by Mirror Function.

6.2.1 Ball Assignment with Mirror Function

	Signal			Signal			Signal			Signal	
Ball	**MF=0**	**MF=1**	**Ball**	**MF=0**	**MF=1**	**Ball**	**MF=0**	**MF=1**	**Ball**	**MF=0**	**MF=1**
F4	CAS#	CS0#	H3	RAS#	BA2	K2	A10	A8/AP	K11	A8/AP	A10
F9	CS0#	CAS#	H4	CKE	WE#	K3	A2	A6	L4	A11	A7
G4	BA0	BA1	H9	WE#	CKE	K4	A0	A4	L9	A7	A11
G9	BA1	BA0	H10	BA2	RAS#	K9	A4	A0	M4	A3	A9
H2	A1	A5	H11	A5	A1	K10	A6	A2	M9	A9	A3

6.3 Commands

In the following table CKEn refers to the positive edge of CLK corresponding to the clock cycle when the command is given to the Graphics SDRAM. CKEn-1 refers to the previous positive edge of CLK. For all command and address inputs CKEn is implied.

All input states or sequences not shown are illegal or reserved.

6.3.1 Command Overview for 1-CS mode

Operation	Code	CKE n-1	CKE n	CS0#	RAS#	CAS#	WE#	BA0	BA1	BA2	A8	A2-7 A9-11/12	Note
Device Delselect	DESEL	H	H	H	L X H	X X H	X L H	X	X	X	X	X	1
Data Terminator Disable	DTERDIS	H	H	H	H	L	H	X	X	X	X	X	1,2
No Operation	NOP	H	H	L	H	H	H	X	X	X	X	X	
Mode Register Set	MRS	H	H	L	L	L	L	0	0	0	OPCODE		
Extended Mode Register Set	EMRS	H	H	L	L	L	L	1	0	OPCODE			
Extended Mode Register Set 2	EMRS2	H	H	L	L	L	L	0	1	0	OPCODE		
Bank Activate	ACT	H	H	L	L	H	H	BA	BA	BA	Row Adress		1,3
Read	RD	H	H	L	H	L	H	BA	BA	BA	L	Col.	
Read w/ Autoprecharge	RD/A	H	H	L	H	L	H	BA	BA	BA	H	Col.	
Write	WR	H	H	L	H	L	L	BA	BA	BA	L	Col.	1,4
Write w/ Autoprecharge	WR/A	H	H	L	H	L	L	BA	BA	BA	H	Col.	
Precharge	PRE	H	H	L	L	H	L	BA	BA	BA	L	X	1,4
Precharge All	PREALL	H	H	L	L	H	L	X	X	X	H	X	
Auto Refresh	AREF	H	H	L	L	L	H	X	X	X	X	X	1,5
Power Down Mode Entry	PWDNEN	H	L	H L	X H	X H	X H	X	X	X	X	X	1,6
Power Down Mode Exit	PWDNEX	L	H	X	X	X	X	X	X	X	X	X	1,7
Self Refresh Entry	SREFEN	H	L	L	L	L	H	X	X	X	X	X	1,8
Self Refresh Exit	SREFEX	L	H	X	X	X	X	X	X	X	X	X	1,9

Notes :

1. X represents “Don’t Care”.
2. This command is invoked when a Read is issued on another DRAM rank placed on the same command bus. Cannot be in power-down or self-refresh state. The Read command will cause the data termination to be disabled.
3. BA0 - BA2 provide bank address, A0 - A11, A12 provide the row address.
4. BA0 - BA2 provide bank address, A2 - A7, A9 provide the column address, A8/AP controls Auto Precharge.
5. Auto Refresh and Self Refresh Entry differ only by the state of CKE.
6. PWDNEN is selected by issuing a DESEL or NOP at the first positive CLK edge following the HIGH to LOW transition of CKE.
7. First possible valid command after t_{XPN}. During t_{XPN} only NOP or DESEL commands are allowed.
8. Self Refresh is selected by issuing AREF at the first positive CLK edge following the HIGH to LOW transition of CKE.
9. First possible valid command after t_{XSC}. During t_{XSC} only NOP or DESEL commands are allowed.

6.3.2 Command Overview for 2-CS mode

Operation	Code	Ranks	CKE n-1	CKE	CS0#	CS1#	RAS#	CAS#	WE#	BA0	BA1	BA2	A8	A2-7 A9-11	Note
Device Deselect	DESEL		H	H	H	H	L X H	X X H	X L H	X	X	X	X	X	1
Data Terminator Disable	DTERDIS		H	H	H	H	H	L	H	X	X	X	X	X	1,2
No Operation	NOP		H	H	L X	X L	H	H	H	X	X	X	X	X	
Mode Register Set	MRS		H	H	L	X	L	L	L	0	0	0	OPCODE		
Extended Mode Register Set	EMRS		H	H	L	X	L	L	L	1	0	OPCODE			
Extended Mode Register Set 2	EMRS2		H	H	L	X	L	L	L	0	1	0	OPCODE		
Bank Activate	ACT	MemBlock 1	H	H	L	H	L	H	H	BA	BA	BA	Row Address		1,3
		MemBlock 2	H	H	H	L	L	H	H	BA	BA	BA	Row Address		
Read	RD	MemBlock 1	H	H	L	H	H	L	H	BA	BA	BA	L	Col.	1,4
		MemBlock 2	H	H	H	L	H	L	H	BA	BA	BA	L	Col.	
Read w/ Autoprecharge	RD/A	MemBlock 1	H	H	L	H	H	L	H	BA	BA	BA	H	Col.	1,4
		MemBlock 2	H	H	H	L	H	L	H	BA	BA	BA	H	Col.	
Write	WR	MemBlock 1	H	H	L	H	H	L	L	BA	BA	BA	L	Col.	1,4
		MemBlock 2	H	H	H	L	H	L	L	BA	BA	BA	L	Col.	
Write w/ Autoprecharge	WR/A	MemBlock 1	H	H	L	H	H	L	L	BA	BA	BA	H	Col.	1,4
		MemBlock 2	H	H	H	L	H	L	L	BA	BA	BA	H	Col.	
Precharge	PRE	MemBlock 1	H	H	L	H	L	H	L	BA	BA	BA	L	X	1
		MemBlock 2	H	H	H	L	L	H	L	BA	BA	BA	L	X	
		Both	H	H	L	L	L	H	L	BA	BA	BA	L	X	
Precharge All	PREALL	MemBlock 1	H	H	L	H	L	H	L	X	X	X	H	X	1
		MemBlock 2	H	H	H	L	L	H	L	X	X	X	H	X	
		Both	H	H	L	L	L	H	L	X	X	X	H	X	
Auto Refresh	AREF	MemBlock 1	H	H	L	H	L	L	H	X	X	X	X	X	1,5
		MemBlock 2	H	H	H	L	L	L	H	X	X	X	X	X	
		Both	H	H	L	L	L	L	H	X	X	X	X	X	
Power Down Mode Entry	PWDNEN		H	L	H X L	H L X	X H	X H	X H	X	X	X	X	X	1,6
Power Down Mode Exit	PWDNEX		L	H	X	X	X	X	X	X	X	X	X	X	1,7
Self Refresh Entry	SREFEN		H	L	L	L	L	L	H	X	X	X	X	X	1,8
Self Refresh Exit	SREFEX		L	H	X	X	X	X	X	X	X	X	X	X	1,9

Notes :
1. X represents “Don’t Care”.
2. This command is invoked when a Read is issued on another DRAM rank placed on the same command bus. Cannot be in power-down or self-refresh state. The Read command will cause the data termination to be disabled. Refer to Figure (Self Calibration of PMOS and NMOS legs) for timing.
3. BA0 - BA2 provide bank address, A0 - A11, A12 provide the row address.
4. BA0 - BA2 provide bank address, A2 - A7, A9 provide the column address, A8/AP controls Auto Precharge.
5. Auto Refresh and Self Refresh Entry differ only by the state of CKE.
6. PWDNEN is selected by issuing a DESEL or NOP at the first positive CLK edge following the HIGH to LOW transition of CKE.
7. First possible valid command after t_{XPN}. During t_{XPN} only NOP or DESEL commands are allowed.
8. Self Refresh is selected by issuing AREF at the first positive CLK edge following the HIGH to LOW transition of CKE.
9. First possible valid command after t_{XSC}. During t_{XSC} only NOP or DESEL commands are allowed.

6.3.3 Description of Command

Command	Description
DESEL	The DESEL function prevents new commands from being executed by the Graphics SDRAM. The Graphics SDRAM is effectively deselected. Operations in progress are not affected.
NOP	The NOP command is used to perform a no operation to the Graphics SDRAM, which is selected (corresponding CS is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.
MRS	The Mode Register is loaded via address inputs A0 - A11. For more details see **“**Mode Register Set Command (MRS)” . The MRS command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.
EMRS	The Extended Mode Register is loaded via address inputs A0 - A11. For more details see section Extended Mode Register Commands EMRS1-3 . The EMRS commands can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.
ACT	The ACT command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0 - BA2 inputs selects the bank, and the address provided in inputs A0 - A11/A12 selects the row. This row remains active (or open) for accesses until a precharge (PRE, RD/A, or WR/A command) is issued to that bank. A precharge must be issued before opening a different row in the same bank.
RD	The RD command is used to initiate a burst read access to an active row. The value on the BA0 - BA2 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The row will remain open for subsequent accesses. For RD commands the value on A8 is set LOW.
RD/A	The RD/A command is used to initiate a burst read access to an active row. The value on the BA0 - BA2 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The value on input A8 is set HIGH. The row being accessed will be precharged at the end of the read burst. The same individual-bank precharge function is performed like it is described for the PRE command. Auto precharge ensures that the precharge is initiated at the earliest valid stage within the burst. The user must not issue a new ACT command to the same bank until the precharge time (t_{RP}) is completed. This time is determined as if an explicit PRE command was issued at the earliest possible time as described in section “Reads (RD)” .

WR	The WR command is used to initiate a burst write access to an active row. The value on the BA0 - BA2 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The row will remain open for subsequent accesses. For WR commands the value on A8 is set LOW. Input data appearing on the DQs is written to the memory array depending on the value on the DM input appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to the memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed for that byte / column location.
WR/A	The WR/A command is used to initiate a burst write access to an active row. The value on the BA0, BA1and BA2 inputs selects the bank, and the address provided on inputs A2-A7, A9 selects the column location. The value on input A8 is set HIGH. The row being accessed will be precharged at the end of the write burst. The same individual-bank precharge function is performed which is described for the PRE command. Auto precharge ensures that the precharge is initiated at the earliest valid stage within the burst. The user is not allowed to issue a new ACT to the same bank until the precharge time (t_{RP}) is completed. This time is determined as if an explicit PRE command was issued at the earliest possible time as described in section "Writes (WR)" . Input data appearing on the DQs is written to the memory array depending on the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to the memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.
PRE	The PRE command is used to deactivate the open row in a particular bank. The bank will be available for a subsequent row access a specified time (t_{RP}) after the PRE command is issued. Inputs BA0 - BA2 select the bank to be precharged. A8/AP is set to LOW. Once a bank has been precharged, it is in the idle state and must be activated again prior to any RD or WR commands being issued to that bank. A PRE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.
PREALL	The PREALL command is used to deactivate all open rows in the memory device. The banks will be available for a subsequent row access a specified time (t_{RP}) after the PREALL command is issued. Once the banks have been precharged, they are in the idle state and must be activated prior to any read or write commands being issued. The PREALL command will be treated as a NOP for those banks where there is no open row, or if a previously open row is already in the process of precharging. PREALL is issued by a PRE command with A8/AP set to HIGH.
AREF	The AREF is used during normal operation of the GDDR3 Graphics RAM to refresh the memory content. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AREF command. The GDDR3 GRAPHICS SDRAM requires AREF cycles at an average periodic interval of t_{REFI}(max). To improve efficiency a maximum number of eight AREF commands can be posted to one memory device (with t_{RFC} from AREF to AREF) as described in section "Auto Refresh Command (AREF)". This means that the maximum absolute interval between any AREF command is 8 x t_{REFI}(max). This maximum absolute interval is to allow the GDDR3 Graphics RAM output drivers and internal terminators to recalibrate, compensating for voltage and temperature changes. All banks must be in the idle state before issuing the AREF command. They will be simultaneously refreshed and return to the idle state after AREF is completed. t_{RFC} is the minimum required time between an AREF command and a following ACT/AREF command.

SREFEN	The Self Refresh function can be used to retain data in the GDDR3 Graphics RAM even if the rest of the system is powered down. When entering the Self Refresh mode by issuing the SREFEN command, the GDDR3 Graphics RAM retains data without external clocking. The SREFEN command is initiated like an AREF command except CKE is disabled (LOW). The DLL is automatically disabled upon entering Self Refresh mode and automatically enabled and reset upon exiting Self Refresh. (1000 cycles must then occur before a RD or DTERDIS command can be issued) The active terminations remain enabled during Self Refresh. Input signals except CKE are "Don't Care". If two GDDR3 Graphics RAMs share the same Command and Address bus, Self Refresh may be entered only for the two devices at the same time. In 2-CS mode, both memories may only enter Self-Refresh, in parallel.
SREFEX	The SREFEX command is used to exit the Self Refresh mode. The DLL is automatically enabled and reset upon exiting. The procedure for exiting Self Refresh requires a sequence of commands. First CLK and CLK# must be stable prior to CKE going from LOW to HIGH. Once CKE is HIGH, the GDDR3 Graphics RAM must receive only NOP/DESEL commands until t_{XSC} is satisfied. This time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and output calibration is to apply NOPs for 1000 cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.
PWDNEN	The PWDNEN command enables the power down mode. It is entered when CKE is set low together with a NOP/DESEL. The CKE signal is sampled at the rising edge of the clock. Once the power down mode is initiated, all of the receiver circuits except CLK and CKE are gated off to reduce power consumption. The DLL remains active (unless disabled before with EMRS). All banks can be set to idle state or stay active. During Power Down Mode, refresh operations cannot be performed; therefore the refresh conditions of the chip have to be considered and if necessary Power Down state has to be left to perform an Auto Refresh cycle. If two GDDR3 Graphics RAMs share the same Command and Address bus, Power down may be entered only for the two devices at the same time.
PWDNEX	A CKE HIGH value sampled at a low to high transition of CLK is required to exit power down mode. Once CKE is HIGH, the GDDR3 Graphics RAM must receive only NOP/DESEL commands until t_{XPN} is satisfied. After t_{XPN} any command can be issued, but it has to comply with the state in which the power down mode was entered.
DTERDIS	Data Termination Disable (Bus snooping for RD commands): The Data Termination Disable Command is detected by the device by snooping the bus for RD commands excluding CS. The GDDR3 Graphics RAM will disable its Data terminators when a RD command is detected. The terminators are disabled starting at CL - 1 clocks after the RD command is detected and the duration is 4 clocks. In a 2CS system, both DRAM devices will snoop the bus for RD commands to either device and both will disable their terminators if a RD command is detected. The command and address terminators are always enabled. See Figure (ODT Disable Timing during a READ command) for an example of when the data terminators are disabled during a RD command.

6.3.4 Minimum delay from RD/A and WR/A to any other command (to another bank) with concurrent AP

From Command	To Command	Minimum delay to another bank (with concurrent auto precharge)	Note
WR/A	RD or RD/A	$(WL + 2) \times t_{CK} + t_{WTR}$	
	WR or WR/A	$2 \times t_{CK}$	
	PRE	t_{CK}	
	ACT	t_{CK}	
RD/A	RD or RD/A	$2 \times t_{CK}$	
	WR or WR/A	$(CL + 4 - WL) \times t_{CK}$	
	PRE	t_{CK}	
	ACT	t_{CK}	

6.4 Boundary Scan

6.4.1 General Description

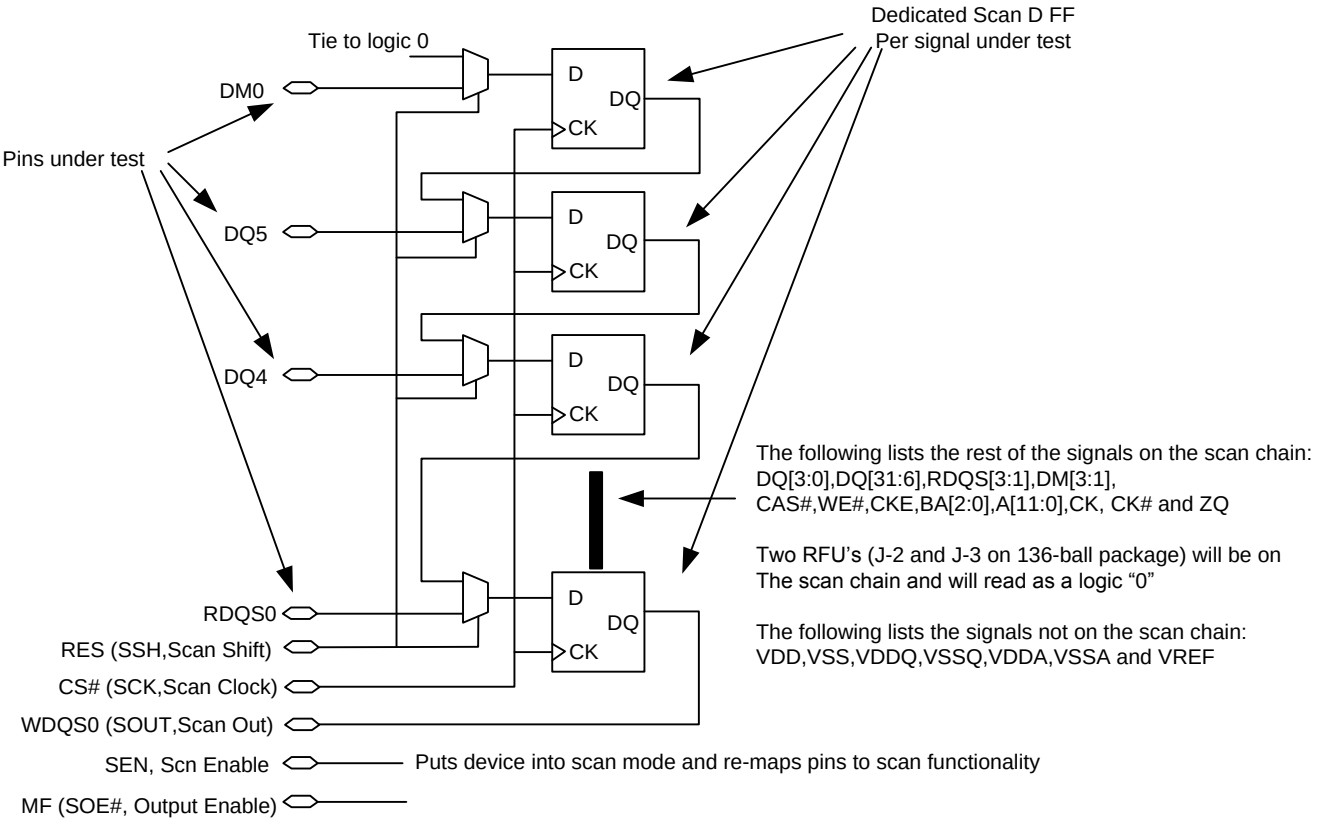
The 1-Gbit GDDR3 incorporates a modified boundary scan test mode. This mode doesn't operate in accordance with IEEE Standard 1149.1-1990. To save the current GDDR3 ball-out, this mode will scan the parallel data input and output the scanned data through the WDQS0 pin controlled by SEN.

Note: Both pads CS1# and A12 will be activated and could be accessed during Boundary Scan.

6.4.2 Disabling the scan feature

It is possible to operate the GDDR3 without using the boundary scan feature. SEN (at U-4 of 136- ball package) should be tied LOW(VSS) to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode, RES, MF, WDQS0 and CS will be operating at normal GDDR3 functionalities when SEN is deasserted.

6.4.2.1 Internal Block Diagram (Reference only)



6.4.2.2 Boundary Scan Exit Order

BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL
1	D-3	13	E-10	25	K-11	37	R-10	49	L-3	61	G-4
2	C-2	14	F-10	26	K-10	38	T-11	50	M-2	62	F-4
3	C-3	15	E-11	27	K-9	39	T-10	51	M-4	63	F-2
4	B-2	16	G-10	28	M-9	40	T-3	52	K-4	64	G-3
5	B-3	17	F-11	29	M-11	41	T-2	53	K-3	65	E-2
6	A-4	18	G-9	30	L-10	42	R-3	54	K-2	66	F-3
7	B-10	19	H-9	31	N-11	43	R-2	55	L-4	67	E-3
8	B-11	20	H-10	32	M-10	44	P-3	56	J-3		
9	C-10	21	H-11	33	N-10	45	P-2	57	J-2		
10	C-11	22	J-11	34	P-11	46	N-3	58	H-2		
11	D-10	23	J-10	35	P-10	47	M-3	59	H-3		
12	D-11	24	L-9	36	R-11	48	N-2	60	H-4		

Notes :

1. When the device is in scan mode, the mirror function will be disabled and none of the pins are remapped.
2. Since the other input of the MUX for DM0 tied to GND, the device will output the continuous zeros after scanning a bit #67, if the chip stays in scan shift mode.
3. An unconnected CS1# and A12 on the board will be read as undefined.

6.4.2.3 Scan Pin Description

PACKAGE BALL	SYMBOL	NORMAL FUNCTION	TYPE	DESCRIPTION
V-9	SSH	RES	Input	**Scan Shift:** Capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
F-9	SCK	CS	Input	**Scan Clock:** Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to rising edge of the scan clock
D-2	SOUT	WDQS0	Output	**Scan Output**
V-4	SEN	SEN	Input	**Scan Enable:** Logic HIGH enables the device into scan mode and will be disabled at logic LOW. Must be tied to GND when not in use.
A-9	SOE	MF	Input	**Scan Output Enable:** Enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to V_{DD} or GND through a resistor (typically 1 KΩ for normal operation). Tester needs to overdrive this pin to guarantee the required input logic level in scan mode.

Notes :

1. When SEN is asserted, no commands are to be executed by the GDDR3. This applies both to user commands and manufacturing commands which may exist while RES is deasserted.
2. The Scan Function can be used right after bringing up V_{DD} / V_{DDQ} of the device. No initialization sequence of the device is required. After leaving the Scan Function it is required to run through the complete initialization sequence.
3. In Scan Mode all terminations for CMD/ADD and DQ, DM, RDQS and WDQS are switched off.
4. In a double-load clam-shell configuration, SEN will be asserted to both devices. Separate two SOE's should be provided to top and bottom devices to access the scanned output. When either of the devices is in scan mode, SOE for the other device which is not in a scan will be disabled.

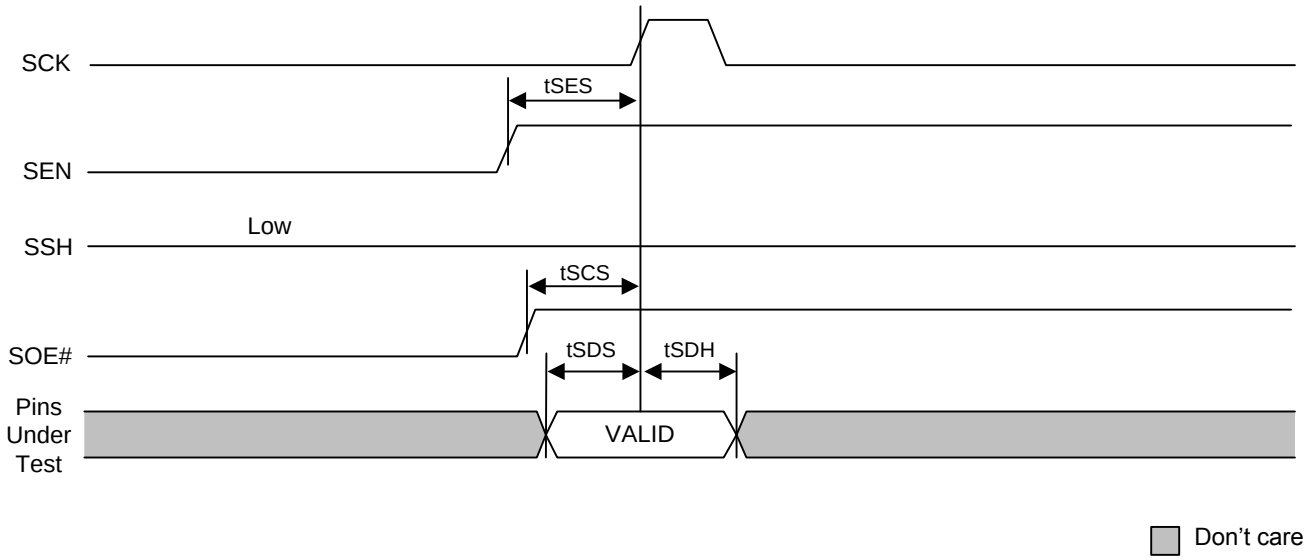
6.4.2.4 Scan DC Electrical Characteristics and Operating Condition

PARAMETER/CONDITION	Symbol	Min.	Max.	Units	Note
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF}+0.15	—		1,2
Input Low (Logic 0) Voltage -	V_{IL}(DC)	—	V_{REF}-0.15 V		1,2

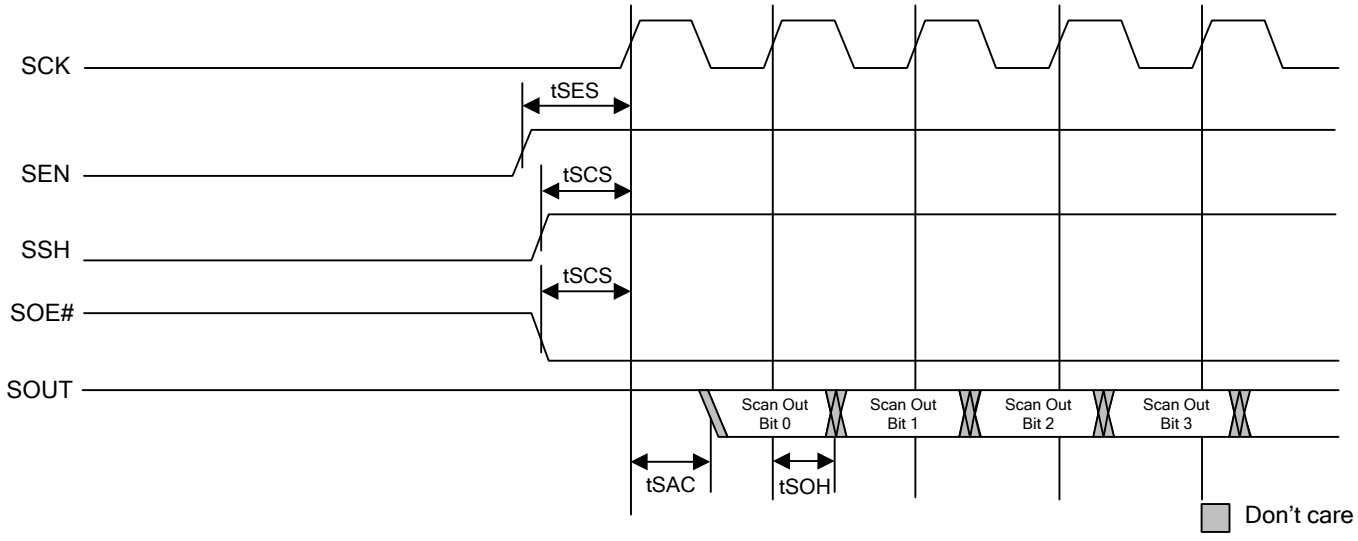
Notes :

1. The parameter applies only when SEN is asserted.
2. All voltages referenced to GND.

6.4.2.5 Scan Capture Timing



6.4.2.6 Scan Shift Timing



6.4.2.7 Scan AC Electrical Characteristic

Parameter/Condition	Symbol	Min.	Max.	Units	Note
Clock					
Clock cycle time	t_{SCK}	40	—	ns	1
Scan Command Time					
Scan enable setup time	t_{SES}	20	—	ns	1,2
Scan enable hold time	t_{SEH}	20	—	ns	2
Scan command setup time for SSH, SOE and SOUT	t_{SCS}	14	—	ns	1
Scan command hold time for SSH, SOE and SOUT	t_{SCH}	14	—	ns	1
Scan Capture Time					
Scan capture setup time	t_{SDS}	10	—	ns	1
Scan capture hold time	t_{SDH}	10	—	ns	1
Scan Shift Time					
Scan clock to valid scan output	t_{SAC}	—	10	ns	1
Scan clock to scan output hold	t_{SOH}	1.5	—	ns	1

Notes:

1. The parameter applies only when SEN is asserted.
2. Scan Enable should be issued earlier than other Scan Commands by 6 ns.

6.4.3 Scan Initialization

The Initialization sequence for the boundary scan functionality depends on the intended SGRAM operation mode. There are two modes to distinguish. The first mode is the Stand-Alone mode. In the Stand-Alone mode the SGRAM is supposed to support the Boundary Scan functionality only, the user does not intend to operate the DRAM in its ordinary functionality after or prior to the entering of the Boundary Scan functionality. The purpose of the Stand-Alone mode could be a connectivity test at the manufacturing site.

The second mode is the regular SGRAM functionality. With this common mode the boundary scan functionality can be enabled after the SGRAM has been initialized by the regular power-up and SGRAM Initialization sequence. When the boundary scan functionality is left the regular SGRAM initialization sequence has to be re-iterated.

6.4.3.1 Scan Initialization for Stand-Alone Mode

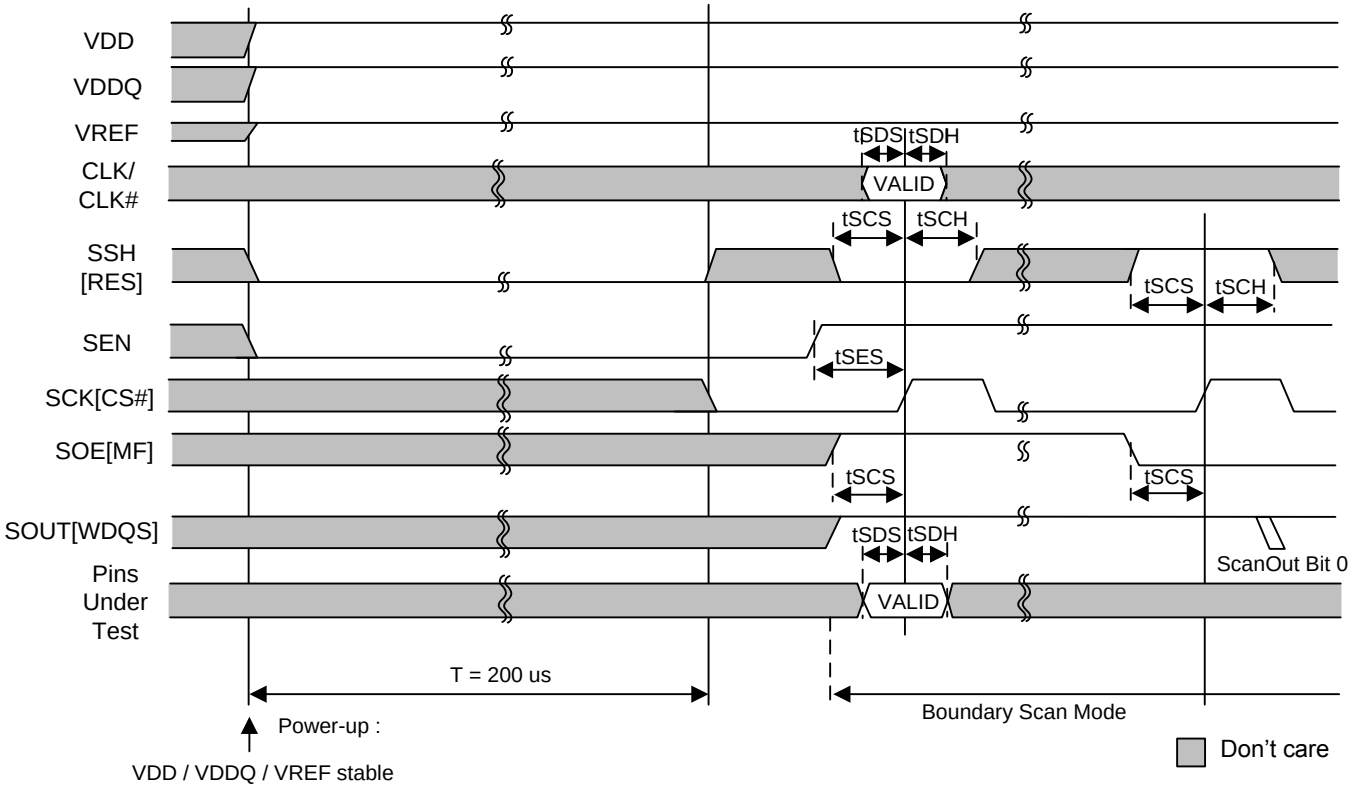
The SGRAM needs to follow the given sequence to support the boundary scan functionality in the Stand-Alone mode.
There is no external clock for the whole sequence needed.

Sequence Flow:

1. External Voltages (VDD/VDDQ/VREF) need to be stable for 200µs, SEN has to be kept low.
2. Bring SEN up to high state to enter boundary scan functionality.
3. Operate boundary scan functionality according to the scan features given in Chapter.
4. Boundary scan can be exited by bringing SEN low or simply by switching power off.

The Scan initialization sequence for the Stand-Alone Mode is shown in Figure.

6.4.3.2 Scan Initialization for Stand-Alone mode



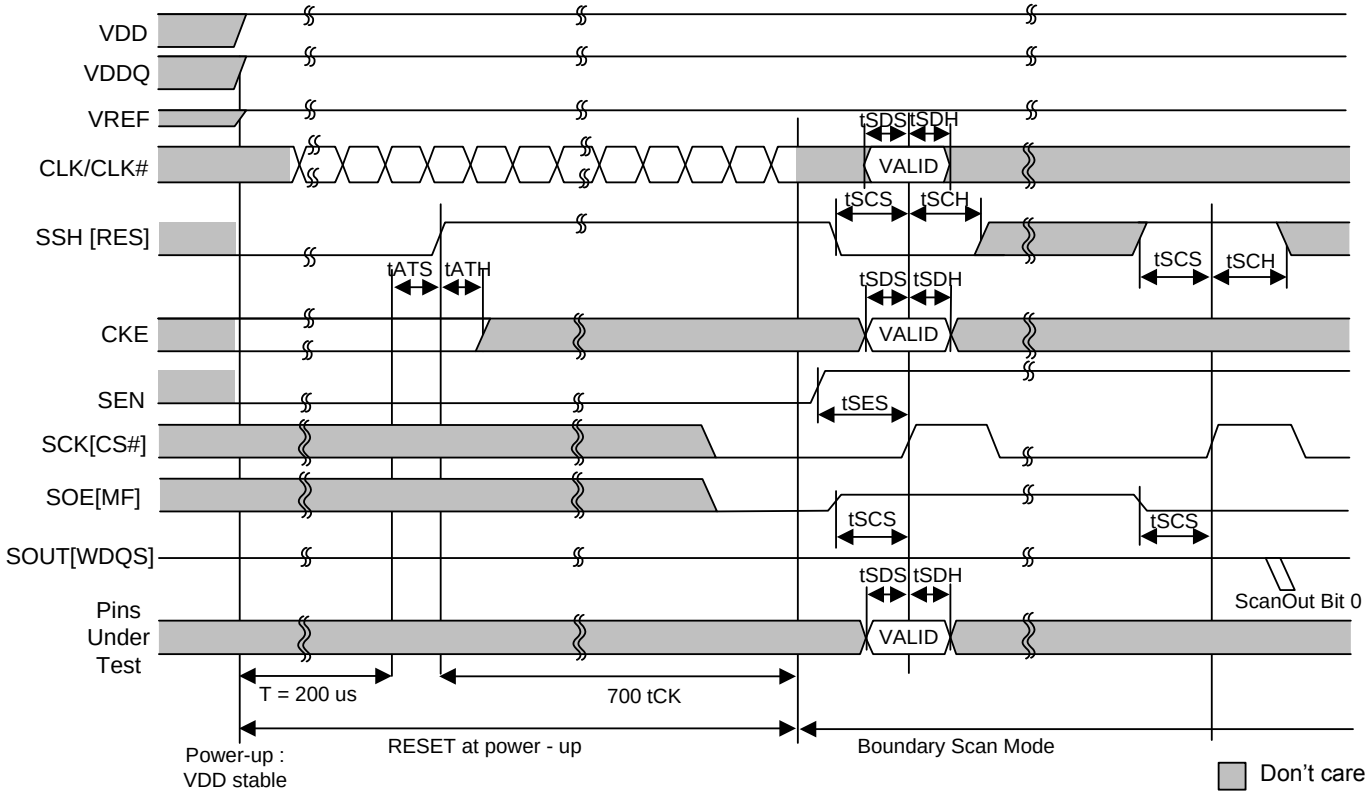
6.4.4 Scan Initialization in regular SGRAM operation

The Initialization sequence of the boundary scan functionality in regular SGRAM operation has to follow the given sequence. Sequence Flow:

1. External Voltages (V_{DD}/V_{DDQ}/V_{REF}) need to be stable for 200 µs, RES has to be kept low, external clock has to be stable prior to RES goes high
2. Bring RES high and keep clock stable for 700tcks, CKE will be latched by rising RES edge, keep t_{ATH}/t_{ATS}
3. Bring SEN up to high state to enter boundary scan functionality
4. Operate boundary scan functionality accordingly to the scan features given in Chapter**.**
5. Boundary scan can be exited by bringing SEN low
6. Wait t_{SN} for bringing up RES, prior to bringing RES to high state external has to be stable
7. After RES is at high state wait 700tck
8. Continue with regular Initialization sequence (PRE-ALL, EMRS, MRS)

The steps 1 and 2 are necessary to enable the termination for the command/address pins. They are part of the regular SGRAM Initialization. They are required if the user wants to issue commands between to entering of the boundary scan functionality and the power-up sequence. The entering of the boundary scan mode is resetting the command/address termination values and all EMRS/MRS settings. Therefore they have to be initialized again after the boundary scan functionary has been left. Figure (Boundary Scan Exit Sequence)shows the scan initialization sequence for regular SGRAM operation.

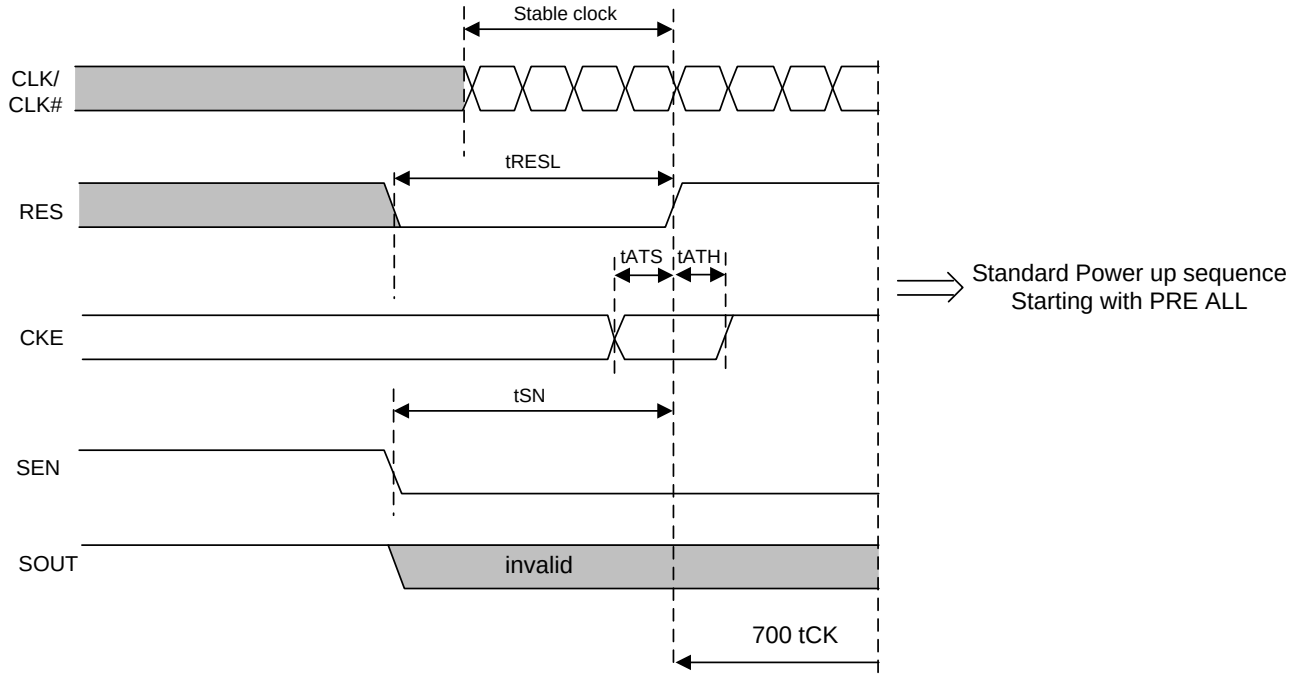
6.4.4.1 Scan Initialization Sequence within regular SGRAM Mode



6.4.5 Scan Exit Sequence

Figure shows the Scan exit Sequence. This figure show the exiting of the boundary scan functionality in conjugation with the appended regular SGRAM initialization sequence to bring the SGRAM again in a well defined state.

6.4.5.1 Boundary Scan Exit Sequence



6.4.5.2 Scan AC Electrical Parameter

Parameter	Symbol	Limit Values		Unit	Note
		Min	Max.		
t_{RESL}	t_{RESL}	20	-	ns	
t_{SN}	t_{SN}	20	-	ns	

6.5 Programmable impedance output drivers and active terminations

6.5.1 GDDR3 IO Driver and Termination

The GDDR3 GRAPHICS SDRAM is equipped with programmable impedance output buffers and active terminations. This allows the user to match the driver impedance to the system impedance.

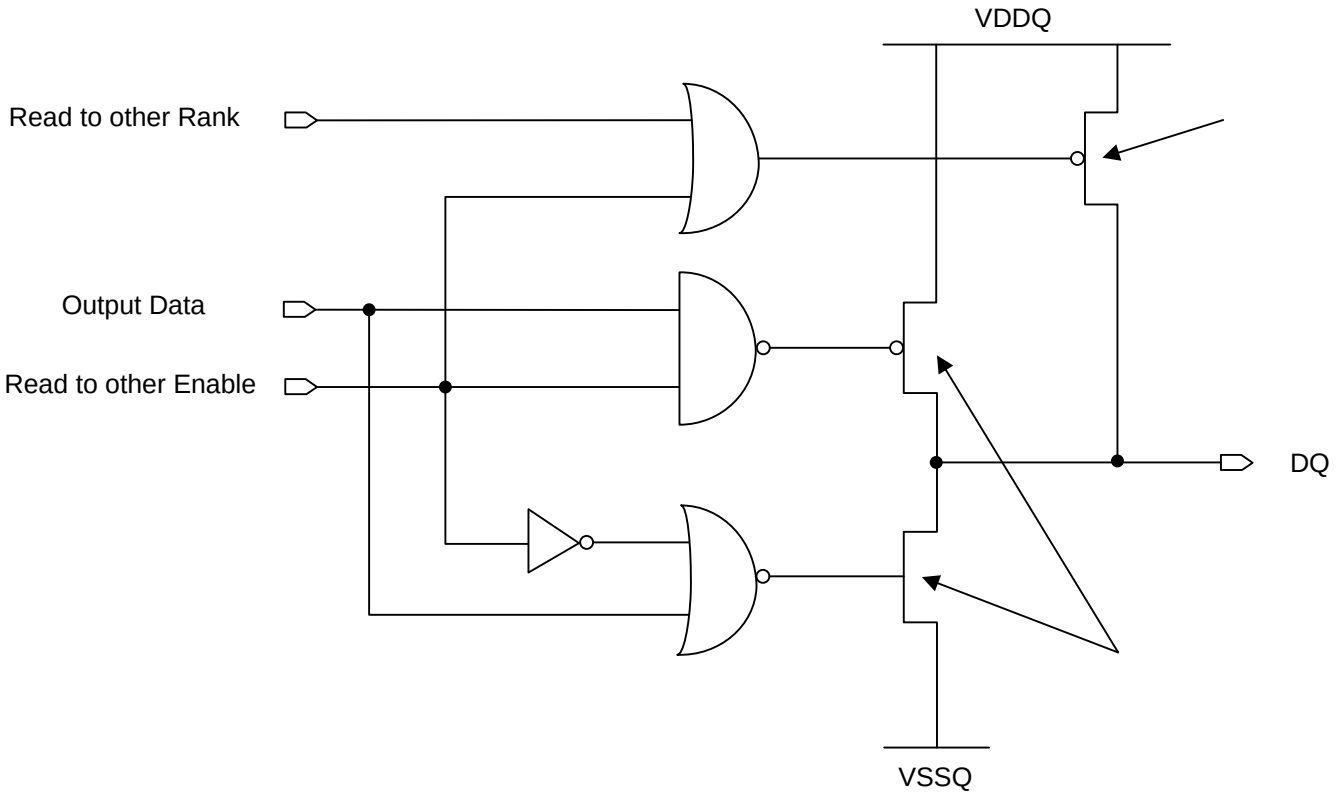
To adjust the impedance of DQ[0:31] and RDQS[0:3], an external precision resistor (ZQ) is connected between the ZQ pin and VSS. The value of the resistor must be six times the value of the desired impedance. For example, a 240 Ω resistor is required for an output impedance of 40 Ω. The range of ZQ is 210 Ω to 270 Ω, giving an output impedance range of 35 Ω to 45 Ω (one sixth the value of ZQ within 10%).

The value of ZQ is used to calibrate the internal DQ termination resistors of DQ[0:31], WDQS[0:3] and DM[0:3]. The two termination values that are selectable using EMRS[3:2] are ZQ / 4 and ZQ / 2.

The value of ZQ is also used to calibrate the internal address command termination resistors. The inputs terminated in this manner are A[0:11], A[12],CKE#, CS0#, CS1#, RAS#, CAS#, WE#. The two termination values that are selectable upon por up (CKE latched LOW to HIGH transition of RES) are ZQ / 4 and ZQ / 2.. RES, MF , CLK and CLK# are not internally terminated.

If no resistance is connected to ZQ, an internal default value of 240 Ω will be used. In this case, no calibration will be performed.

6.5.1.1 Output Deiver simplified schematic



6.5.1.2 Range of external resistance ZQ

Parameter	Symbol	Min.	Nom.	Max.	Units	Note
External resistance value	ZQ	210	240	270	Ω	

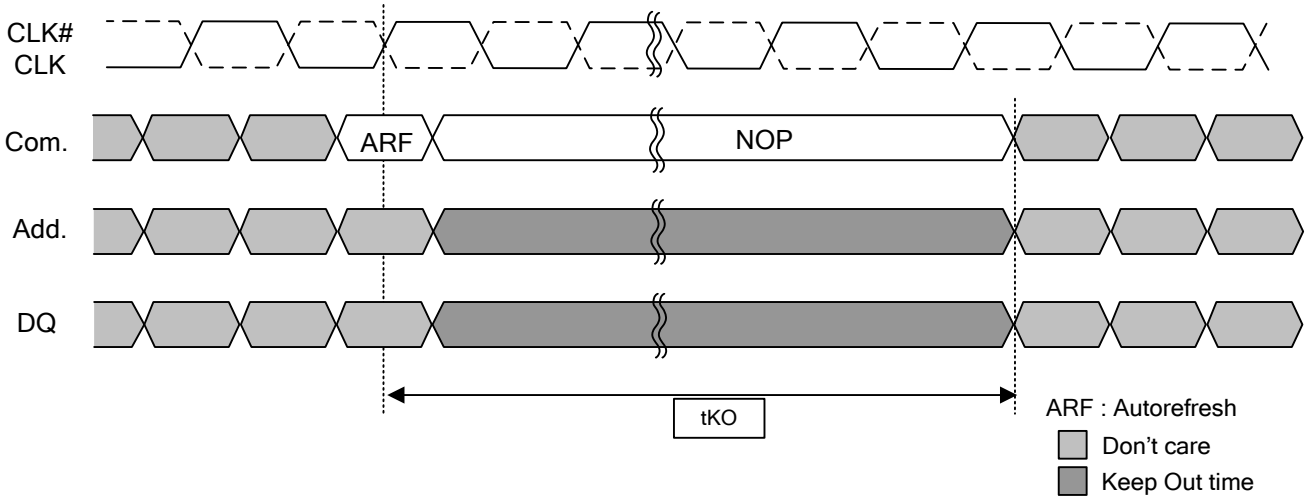
6.5.1.3 Termination Types and Activation

Ball	Termination type	Termination activation
CLK, CLK#, RDQS[0:3], ZQ, RES, MF	No termination	
CKE, CS0#, CS1#, RAS#, CAS#, WE#, BA0 - BA2 , A[0:11], A[12]	Add / CMDs	Always ON
DM[0:3], WDQS[0:3]	DQ	Always ON
DQ[0:31]	DQ	CMD bus snooping

6.5.2 Self Calibration for Driver and Termination

The output impedance is updated during all AREF commands. These updates are used to compensate for variations in supply voltage and temperature. Impedance updates do not affect device operation. No activity on the Address, command and data bus is allowed during a minimum Keep Out time t_{KO} after the Autorefresh command has been issued.

6.5.2.1 Termination update Keep Out time after Autorefresh command



To guarantee optimum driver impedance after power-up, the GDDR3 GRAPHICS SDRAM needs 700 cycles after the clock is applied and stable to calibrate the impedance upon power-up. The user can operate the part with fewer than 700 cycles, but optimal output impedance will not be guaranteed.

The GDDR3 Graphics RAM proceeds in the following manner for Self Calibration:

The PMOS device is calibrated against the external ZQ resistor value. First one PMOS leg is calibrated against ZQ. The number of legs used for the terminators (DQ and ADD/CMD) and the PMOS driver is represented in Table . Next, one NMOS leg is calibrated against the already calibrated PMOS leg. The NMOS driver uses 6 NMOS legs.

6.5.2.2 Number of Legs used for Terminator and Driver Self Calibration

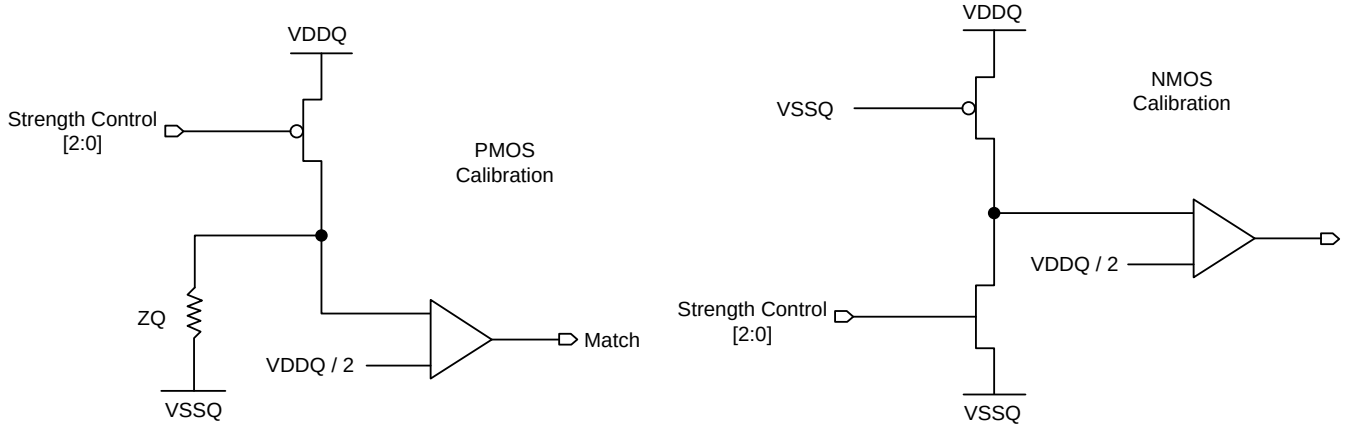
		CKE (at RES)	Termination	Number of Legs	Note
Terminator	ADD / CMD	0	ZQ/2	2	
		1	ZQ	1	
		EMRS[3:2]			
	DQ	00	Disabled	0	1
		10	ZQ/4	4	
		11	ZQ/2	2	
Driver	PMOS		ZQ/6	6	
	NMOS		ZQ/6	6	

Note :

1. EMRS[3:2] = 00 disables the ADD and CMD terminations as well.

Figure represents a simplified schematic of the calibration circuits. First, the strength control bits are adjusted in such a way that the VDDQ voltage is divided equally between the PMOS device and the ZQ resistor. The best bit pattern will cause the comparator to switch the PMOS Match signal output value. In a second step, the NFET is calibrated against the already calibrated PFET. In the same manner, the best control bit combination will cause the comparator to switch the NMOS Match signal output value.

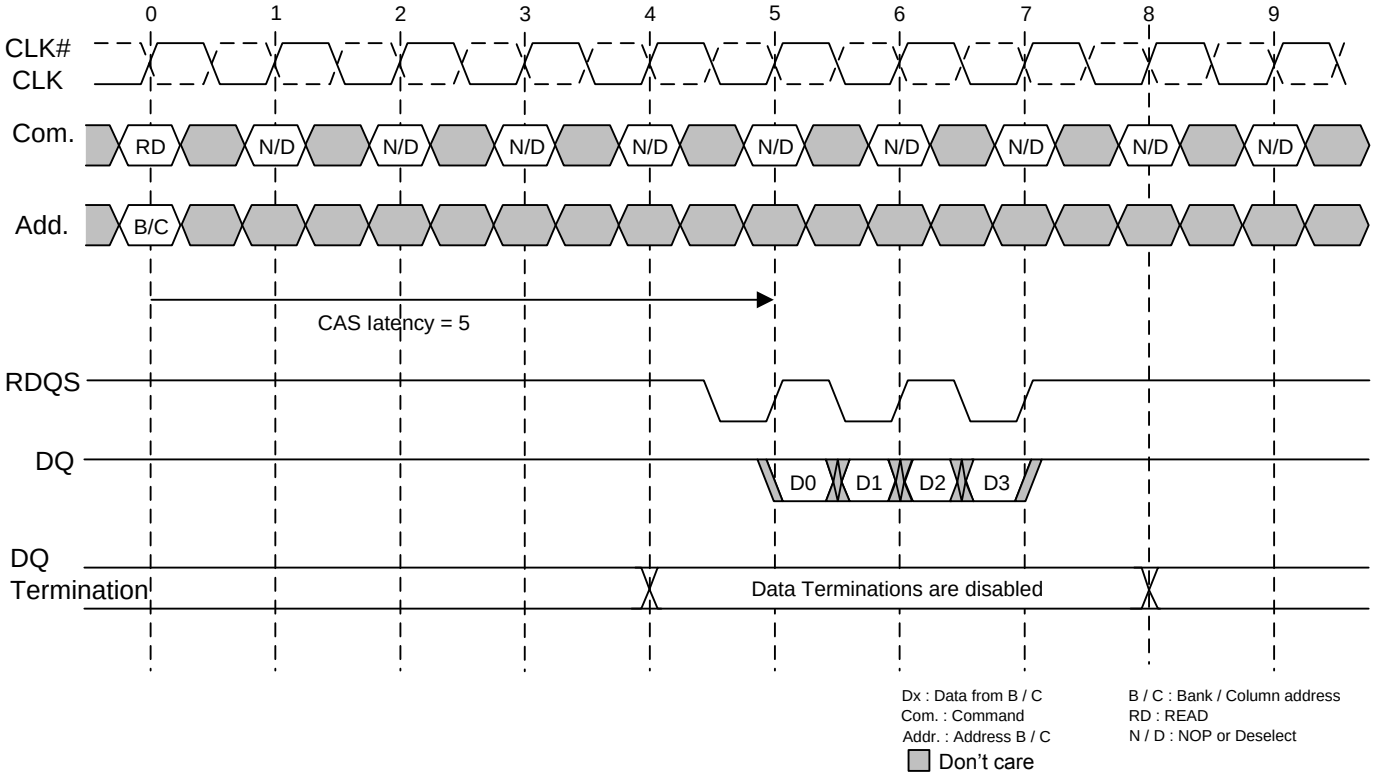
6.5.2.3 Self Calibration of PMOS and NMOS Legs



6.5.3 Dynamic Switching of DQ terminations

The GDDR3 Graphics RAM will disable its data terminators when a READ or DTERDIS command is detected. The terminators are disabled starting at CL - 1 Clocks after the READ / DTERDIS command is detected and the duration is 4 clocks. In a two rank system, both devices will snoop the bus for a READ / DTERDIS command to either device and both will disable their terminators if a READ / DTERDIS command is detected. The address and command terminators are always enabled.

6.5.3.1 ODT Disable Timing during a READ command



6.5.4 Output impedance and Termination DC Electrical Characteristics

The Driver and Termination impedances are determined by applying $V_{DDQ/2}$ nominal at the corresponding input/output and by measuring the current flowing into or out of the device. V_{DDQ} is set to the nominal value.

I_{OH} is the current flowing out of DQ when the Pull-Up transistor is activated and the DQ termination disabled. I_{OL} is the current flowing into DQ when the Pull-Down transistor is activated and the DQ termination disabled. $I_{TCAH(ZQ)}$ is the current flowing out of the Termination of Commands and Addresses for a ZQ termination value.

6.5.4.1 DC Electrical Characteristic

Parameter	ZQ Value	Limit Values		Unit	Note
		240			
		Min.	Max.		
I_{OH}	ZQ/6	20.5	25.0	mA	1,2
I_{OL}	ZQ/6	20.5	25.0	mA	1,2
$I_{TCAH(ZQ)}$	ZQ	3.4	4.2	mA	1,2

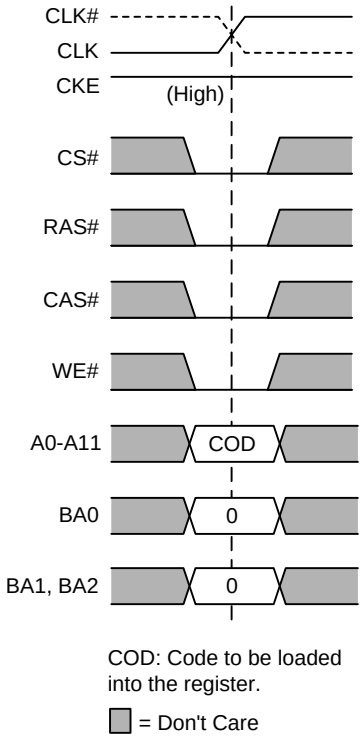
Notes :

1. Measurement performed with V_{DDQ} (nominal) and by applying $V_{DDQ/2}$ at the corresponding Input / Output. 0° C ≤ Tc ≤105° C
2. for 1.8 V V_{DD}/V_{DDQ} power supply

6.6 Mode Register Set Command (MRS)

The Mode Register stores the data for controlling the operation modes of the memory. It programs CAS latency, test mode, DLL Reset, the value of the Write Latency and the Burst length. The Mode Register must be written after power up to operate the SGRAM. During a Mode Register Set command the address inputs are sampled and stored in the Mode Register. The mode Register content can only be set or changed when the chip is in idle state. For non-READ commands following a Mode Register Set a delay of tMRD must be met.
To apply an MRS command, CS0 has to be used.

6.6.1 Mode Register Set Command



6.6.2 Mode Registers

Three Mode Registers MRS, EMRS1 and EMRS2 define the specific mode of operation. All Mode Registers are initialized upon power-up as indicated below.
All functions controlled by Mode Register EMRS3 and some high-speed options in the other registers as outlined below shall be deactivated or deleted such that programming of the respective register bits has no effect.

6.6.2.1 Mode Register (MRS)

The Mode Register controls operating modes such as Burst Length, Burst Type, CAS latency, Write Latency, DLL Reset and Test Mode as shown in Figure . The register is programmed via the MODE REGISTER SET command with BA0=0, BA1=0 and BA2=0.

6.6.2.2 Mode Register (MRS)

BA2	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	WL			DLL	TM	CAS Latency			BT	BL		

Write Latency

A1	A10	A9	WL
0	1	1	3*
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Test Mode

A7	mode
0	Normal*
1	Test mode

Burst Length

A2	A1	A0	BL
0	1	0	4*
0	1	1	8
All others			RFU

DLL Reset

A8	DLL Reset
0	No*
1	Yes

CAS Latency

A6	A5	A4	Latency
0	0	0	8*
0	0	1	9
0	1	0	10
0	1	1	11
1	0	0	12
1	0	1	13
1	1	0	14
1	1	1	7

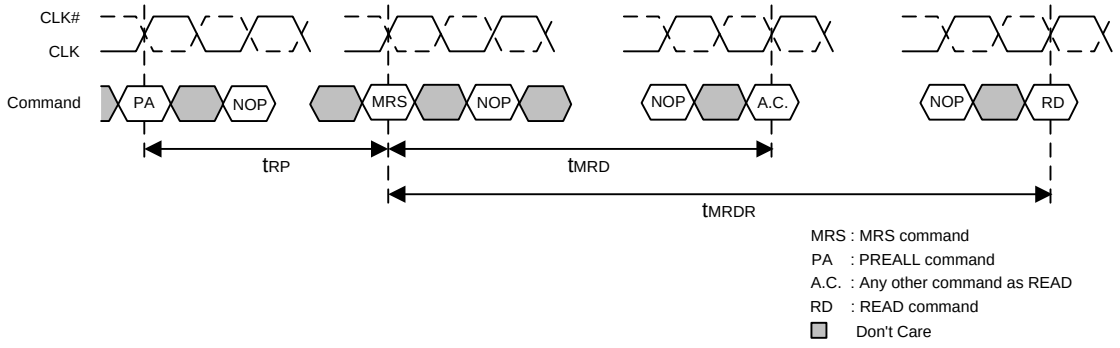
Burst Type

A3	BT
0	Sequential*
1	RFU

Note: The DLL Reset bit is self-clearing

*** Default value at power-up**

6.6.2.3 Mode Register Set Timing



6.6.3 Burst Length and Burst Type

6.6.3.1 Burst Length

Read and write accesses to the GDDR3 GRAPHICS SDRAM are burst-oriented, with a burst length of 4 or 8 as programmed inbits A0-A2.
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected.
All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundaryis reached. The block is uniquely selected by address bits A2-A7,A9.
The access order within a burst is fixed, and address bits A0 and A1 are ignored as shown in Table.

The only supported burst type is sequential.

6.6.3.2 Burst type

Accesses within a given bank must be programmed to be sequential. This is done using the Mode Register Set command (A3). This device does not support the burst interleave mode.

6.6.3.2.1 Burst Definition

Burst Length	Column Address			Order of Accesses within a Burst
	A2	A1	A0	
4	—	X	X	0-1-2-3
8	0	X	X	0-1-2-3-4-5-6-7
	1	X	X	4-5-6-7-0-1-2-3

The value applied at the balls A0 and A1 for the column address is “Don’t care”.

6.6.4 CAS Latency

The READ latency, or CAS latency, is the delay between the registration of a READ command and the availability of the first piece of output data. The latency is set using bits A4-A6.
If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m.
The high-speed option for CAS latencies of 13 to 20 shall be deleted or deactivated.

6.6.5 Write Latency

The WRITE latency (WL) is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data. The latency is set using bits A9-A11.
If a WRITE command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m.

6.6.6 DLL Reset

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A8 set to zero, and bits A0-A7 and A9-A11 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bit A8 set to one, and bits A0-A7 and A9-A12 set to the desired values. The register bit is self clearing meaning that it returns back to the value '0' after the DLL reset function has been issued.

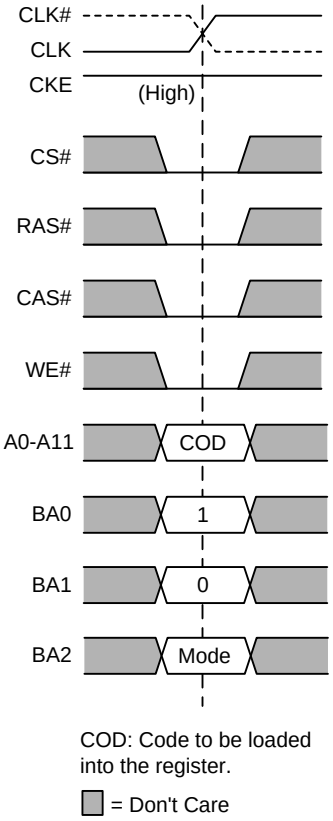
6.6.7 Test mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A7 set to '0', and bitsA0-A6 and A8-A11 set to the desired values. Programming bit A7 to '1' places the device into a test mode that isonly to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.

6.7 Extended Mode Register Set Command (EMRS1)

The Extended Mode Register is used to control multiple operation modes of the device. The most important one is the organization as a 1-CS or a 2-CS device. Furthermore, it is used to set the output driver impedance value, the termination impedance value, the Write Recovery time value for Write with Autoprecharge. It is used as well to enable/disable the DLL, to issue the Vendor ID. There is no default value for the Extended Mode Register. Therefore it must be written after power up to operate the GDDR3 Graphics RAM. The Extended Mode Register can be programmed by performing a normal Mode Register Set operation and setting the BA0 bit to HIGH. All other bits of the EMR register are reserved and should be set to LOW. The Extended Mode Register must be loaded when all banks are idle and no burst are in progress. The controller must wait the specified time t_{MRD} before initiating any subsequent operation (Figure : Extended Mode Register 1).
The timing of the EMRS command operation is equivalent to the timing of the MRS command operation.To apply an EMRS command, CS0 has to be used.

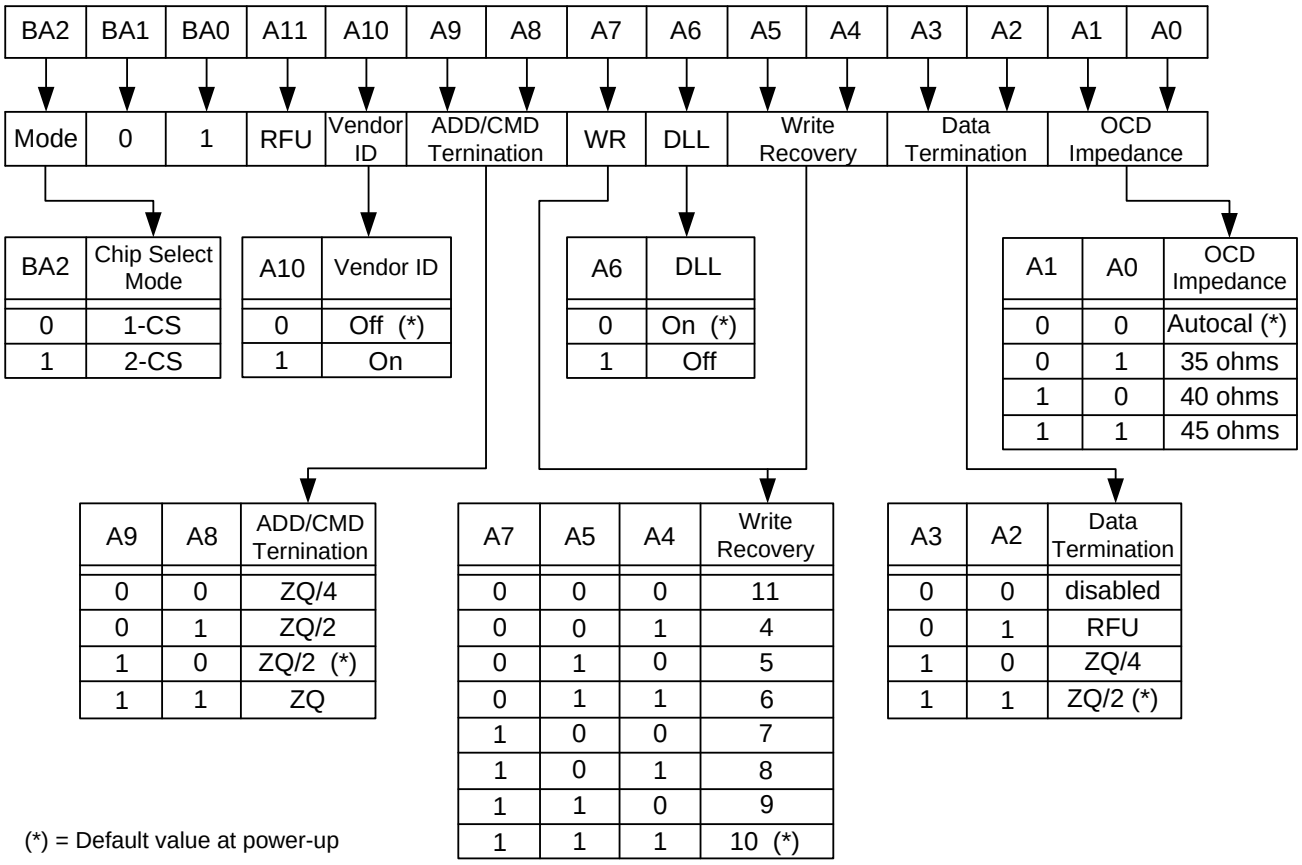
6.7.1 Extended Mode Register Set Command



6.7.2 Extended Mode Register 1 (EMRS1)

The Extended Mode Register 1 controls operating modes such as output driver impedance, data termination, address/command termination, DLL on/off, Write recovery and Vendor ID as shown in Figure. It also selects between 1-CS mode and 2-CS mode configuration. The register is programmed via the MODE REGISTER SET command with BA0=1, BA1=0 and BA2 set to the desired configuration.

6.7.2.1 Extended Mode Register 1 (EMRS1)



BA2	Chip Select Mode
0	1-CS
1	2-CS

A10	Vendor ID
0	Off (*)
1	On

A6	DLL
0	On (*)
1	Off

A1	A0	OCD Impedance
0	0	Autocal (*)
0	1	35 ohms
1	0	40 ohms
1	1	45 ohms

A9	A8	ADD/CMD Ternination
0	0	ZQ/4
0	1	ZQ/2
1	0	ZQ/2 (*)
1	1	ZQ

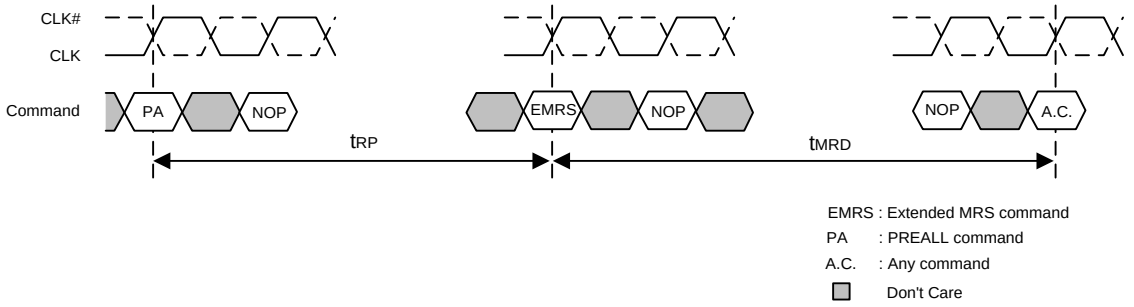
A7	A5	A4	Write Recovery
0	0	0	11
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	7
1	0	1	8
1	1	0	9
1	1	1	10 (*)

A3	A2	Data Termination
0	0	disabled
0	1	RFU
1	0	ZQ/4
1	1	ZQ/2 (*)

(*) = Default value at power-up

Notes :
1. Default termination values at Power Up.
2. The ODT disable function disables all terminators on th device.
3. If the user activates bits in the extended mode register in an optional field, either the optional field is activated (if option implemented in the device) or no action is taken by the device (if option not implemented).
4. WR (write recovery time for auto precharge) in clock cycles is calculated by dividing tWR (in ns) and rounding up to the next integer (WR[cycles] = tWR[ns] / tCK[ns]). The mode register must be programmed to this value.

6.7.2.2 Extended Mode Register Set Timing



6.7.3 Chip Select Mode

Mode	EMRS1[BA2]	EMRS2[A5]	Pin for CS1#	Pin for A12
1-CS Mode, non-merged	0	0	NA	J-2
2-CS Mode	0	1	J-3	NA
	1	0		
1-CS Mode, merged	1	1	NA	J-3

6.7.4 DLL

The DLL is enabled by default. If DLL-off operation is desired, the DLL must be disabled by setting bit A6 to '1'. Once enabled, the DLL requires 1000 cycles to lock.

6.7.5 Write Recovery

The programmed WR value is used for the auto precharge feature along with tRP to determine tDAL. WR must be programmed with a value greater than or equal to [RU{tWR/tCK}], where RU stands for round up, tWR is the analog value and tCK is the operating clock cycle time.

The high-speed option for Write Recovery values of 11 to 20 shall be deleted or deactivated.

6.7.6 Termination Rtt

The data termination, Rtt, is used to set the value of the internal termination resistors. The GDDR3 DRAM supports ZQ / 4 and ZQ / 2 termination values. The termination may also be disabled for testing and other purposes. Data -, address - and command - termination are disabled in parallel. The Termination Rtt are controlled independently from the Output Driver Impedance values.

6.7.7 Impedance Autocalibration of Output Buffer and Active Terminator

GDDR3 GRAPHICS SDRAMs offer autocalibrating impedance output buffers and on-die terminations (ODT). This enables auser to match the driver impedance and terminations to the system within a given range. To adjust the impedance, an external precision resistor shall be connected between the ZQ pin and VSSQ. A nominal resistor value of 240 is equivalent to 40 Pulldown, 40 Pullup and 60 ODT nominal impedances. If no resistance is connected to the ZQ pin, a default value of 240 is assumed and no calibration is performed.

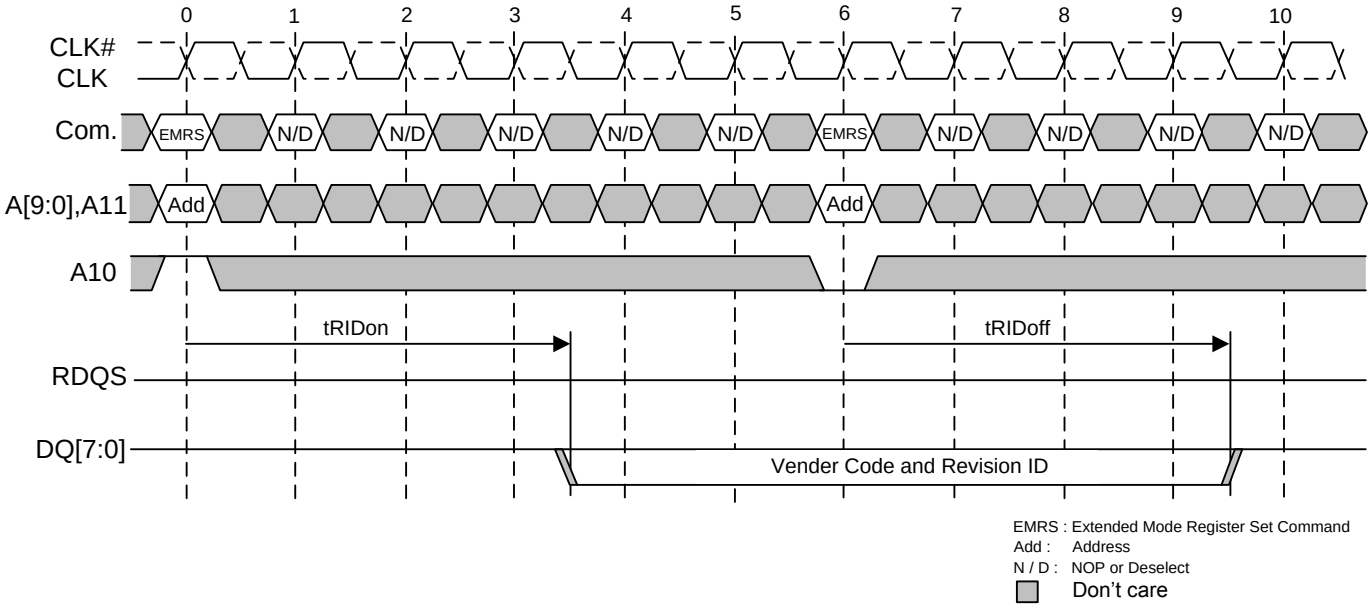
The output driver and on-die termination impedances are updated during all REFRESH commands to compensate for variations in supply voltage and temperature. The impedance updates are transparent to the system.

Table provides an overview of the ODT settings controlled by EMRS1.

6.7.7.1 Impedance Options

Signal	ODT Activation	EMRS1 Control Bits
CLK,CLK#,RES,MF,SEN	No ODT	-
CKE,CS0#,CS1#,RAS#,CAS#,WE#,BA0-BA2,A0-A12	Always on	A8-A9
DM0-DM3,WDQS0-WDQS3	Always on	A2-A3
DQ0-DQ31	Always on except for Reads (bus snooping)	A2-A3
RDQS0-RDQS3	No ODT	-

6.7.7.2 Timing of Vendor Code and Revision ID Generation on DQ[7:0]



6.7.8 Output Driver Impedance

Bits A0 and A1 define the driver strength. The Auto Calibration setting enables the Auto-Calibration functionality for the Pulldown, Pullup and Termination over process, temperature and voltage changes. The 35Ω, 40Ω and 4Ω5 options enable factory settings for the Pulldown, Pullup driver strength and termination.
With any of those options enabled, driver strength and termination are expected to change with process, voltage and temperature. AC timings are only guaranteed with Auto Calibration.

6.7.9 Data Termination

Bits A2 and A3 define the data termination value for the on-die termination (ODT) for the DQ pins in combination with the driver strength setting. The termination can be set to a value of ZQ/4 or ZQ/2; it may also be turned off.

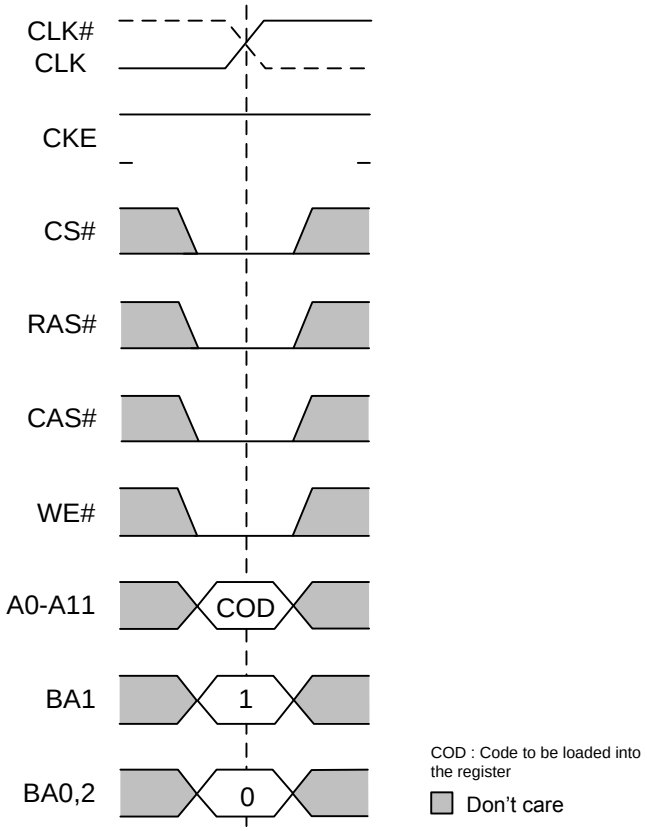
6.7.10 Address command termination

Bits A8 and A9 define the address/command termination. The termination can be set to a value of ZQ/4, ZQ/2 or ZQ. The setting overwrites the value defined upon power-up initialization.

6.8 Extended Mode Register 2 Set Command (EMRS2)

The Extended Mode Register 2 is used to control OCD/ODT impedance offsets. It can be programmed by performing a normal Mode Register Set operation and setting the BA1 bit to HIGH and BA0, BA2 bits to LOW. The Extended Mode Register 2 must be loaded when all banks are idle and no burst are in progress. The controller must wait the specified time t_{MRD} before initiating any subsequent operation. The timing of the EMRS2 command operation is equivalent to the timing of the MRS command operation.

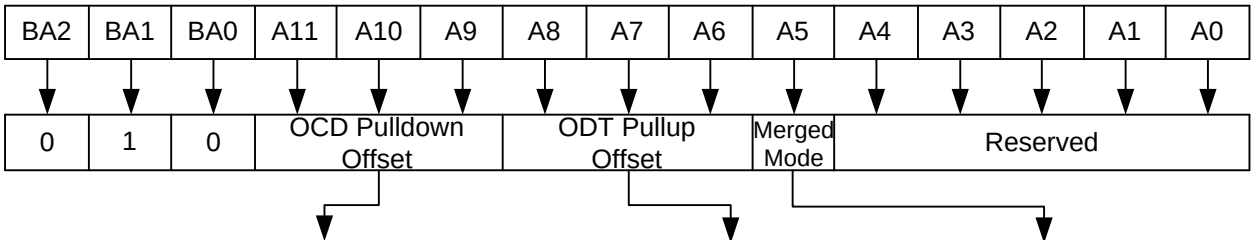
6.8.1 Extended Mode Register 2 Set Command



6.8.2 Extended Mode Register 2 (EMRS2)

The Extended Mode Register 2 controls output driver and termination offsets and Merged Mode as shown in Figure. The register is programmed via the MODE REGISTER SET command with BA0=0, BA1=1 and BA2=0.
The Application Mode function (mid range vs. high speed) on bit A0 and the temperature sensor self refresh function on bit A1 shall be deleted or deactivated.

6.8.2.1 Extended Mode Register 2 (EMRS2)



A11	A10	A9	OCD PD Offset
0	0	0	0 (*)
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	RFU
1	0	1	-3
1	1	0	-2
1	1	1	-1

A8	A7	A6	ODT PU Offset
0	0	0	0 (*)
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	RFU
1	0	1	-3
1	1	0	-2
1	1	1	-1

A5	Merged Mode
0	Non-Merged (*)
1	Merged

(*) = Default value at power-up

6.8.2.2 Impedance Offsets

The driver and termination impedances may be offset individually for output driver and data termination. The offset impedance step values correspond to a nominal value of TBD. With negative offset steps the drive strengths will be decreased and Ron will be increased. With positive offset steps the drive strengths will be increased and Ron will be decreased.

6.8.2.3 Merged Mode

Merged Mode combines the specific pins of 1-CS Mode (A12) and 2-CS Mode (CS1#) on a single physical pin (J-3).

6.8.3 OCD Pull Down Offset

The 1G GDDR3 add the ability to add an offset to the Output impedance driver set using the bit A[1:0] of the EMRS. A range from -3 to +3 can be chosen using A[11:9]. Each steps correspond to an approximate change of 1 Ohms. The offset will be applied also on Autocal value if selected. The offset will be applied also on Autocal value if selected. With negative offset steps the Driver Strength will be decreased and the Ron will be increased. With positive offset steps the Driver Strength will be increased and Ron will be decreased.

6.8.4 ODT Pull Up Offset

The 1G GDDR3 add the ability to add an offset to the ODT set using the bit A[3:2] of the EMRS. A range from -3 to +3 can be chosen using A[8:6]. Each steps correspond to an approximate change of 1.5 Ohms. With negative offset steps the Termination value will be increased. With positive offset steps the Termination value will be decreased.

6.9 Extended Mode Register 3 (EMRS3)

All functions originally controlled by EMRS3 like alternate CL/WR, RDBI, WDBI and Multi-Cycle Preamble (MPR) shall be deleted or deactivated, or shall be permanentely set (autocal enabled, nominal VINT).

6.10 Vendor Code and Revision ID

When the Vendor Code function is enabled by bit A10, the GDDR3 GRAPHICS SDRAM will provide the vendor code on DQ[3:0] and the revision identification on DQ[7:4] as shown in Table.

The Revision ID shall be made programmable on a single metal layer (TBD).

6.10.1 Vendor ID Code

Default Revision ID (DQ7-DQ4)	Manufacturer ID (DQ3-DQ0)
0000	1000

6.11 Bank / Row Activation (ACT)

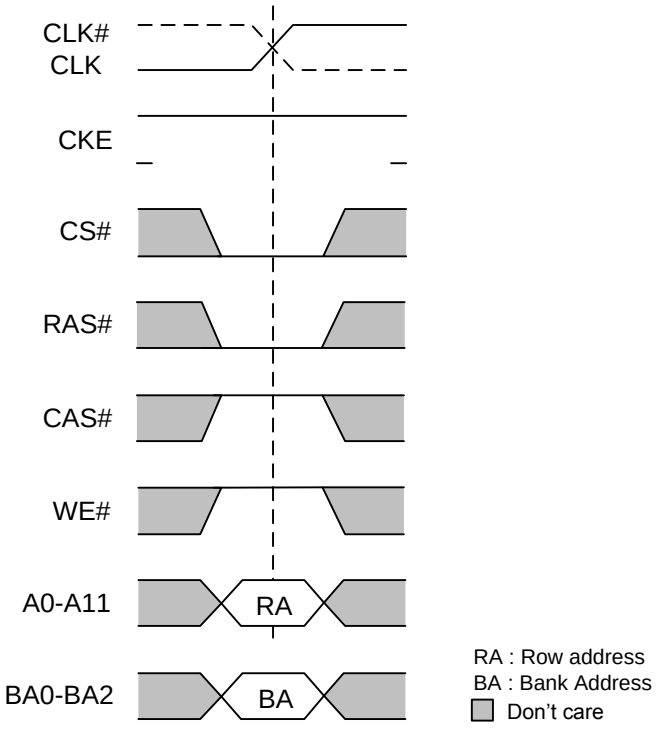
Before a READ or WRITE command can be issued to a bank, a row in that bank must be opened. This is accomplished via the ACT command, which selects both the bank and the row to be activated.After opening a row by issuing an ACT command, a READ command may be issued after t_{RCDRD} to that row or a WRITE command after t_{RCDWR}.

A subsequent ACT command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACT commands to the same bank is defined by t_{RC}.

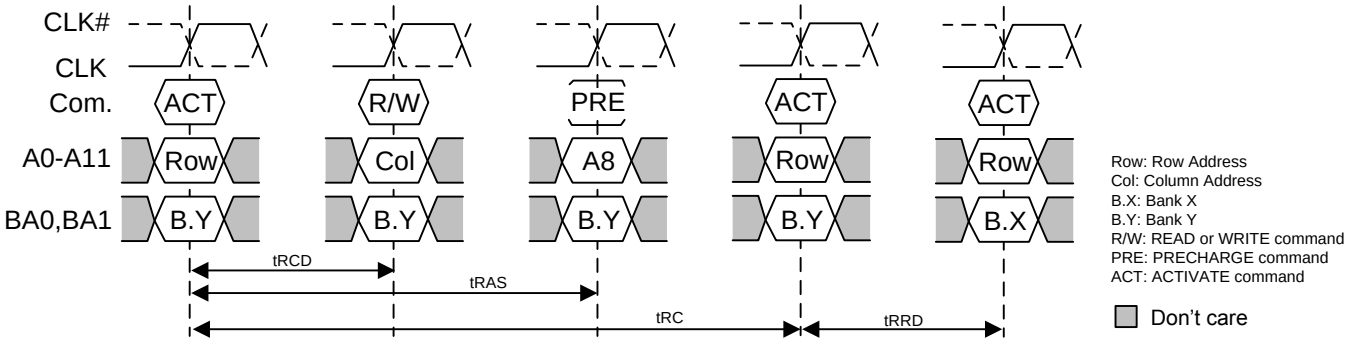
A subsequent ACT command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACT commands to ACT commands to banks in the same rank is defined by t_{RRD}, and to banks in different ranks by t_{RRD_RR} (see Figure:Bank Activation Timing on different rank in 2-CS mode).There is a minimum time t_{RAS} between opening and closing a row.

For the 1-CS Mode (1Gb) an additional address bit is available (A12). Internally this additional address bit is converted into a selection signal for one or the other internal rank representing the first or the second half of the 512 Mb. Subsequent column accesses to the activated bank are steered to the internal rank as selected by A12 during activation of the bank.

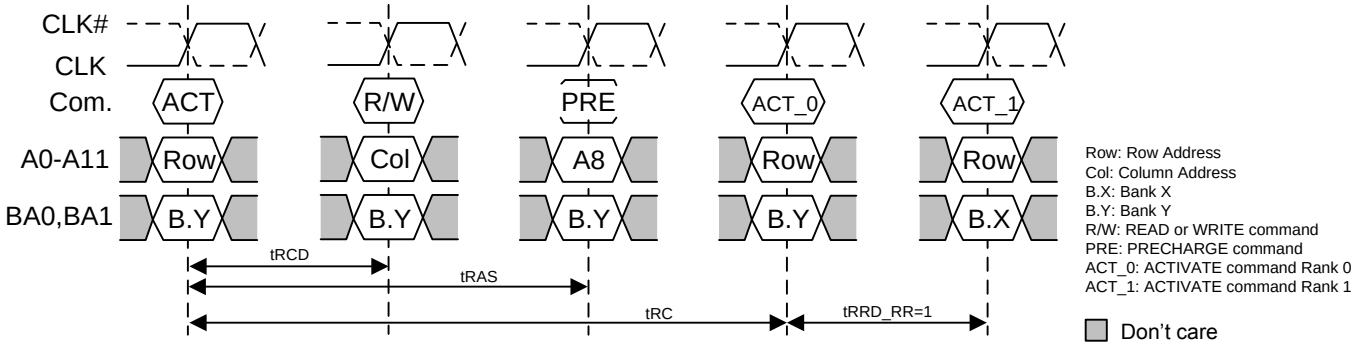
6.11.1 Activating a specific row



6.11.2 Bank Activation Timing

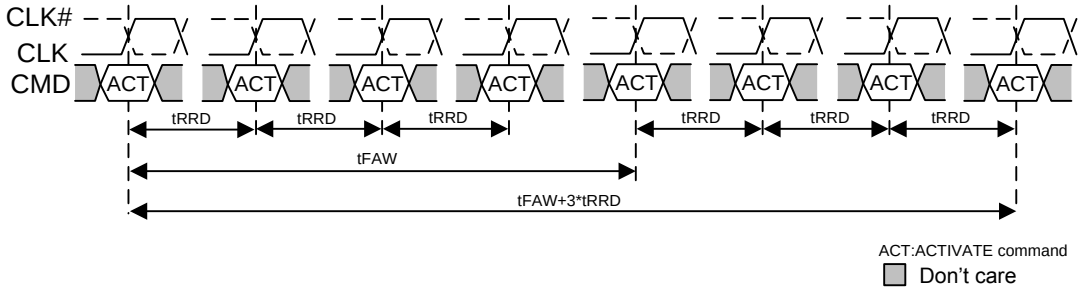


6.11.3 Bank Activation Timing on different rank in 2-CS mode

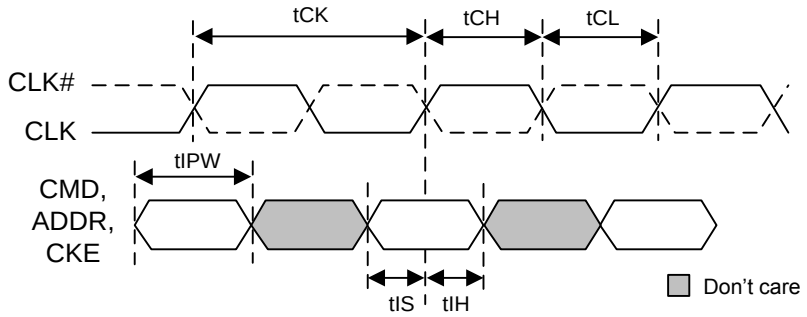


For eight bank GDDR3 devices, there may be a need to limit the number of activates in a rolling window to ensure that the instantaneous current supplying capability of the devices is not exceeded. To reflect the true capability of the DRAM instantaneous current supply, the parameter t_{FAW} (four activate window) is defined. No more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW} (ns) by t_{CK} (ns) and rounding up the next integer value. As an example of the rolling window, if (t_{FAW} / t_{CK}) rounds up to 10 clocks, and an activate command is issued in clock n, no more than three further activate commands may be issued in clocks n+1 through n+9. t_{FAW} is only valid within one rank. There is no further restriction between ranks.

6.11.4 Four Window Active tFAW



6.11.5 Clock, CKE and command / Address Timings



Setup and Hold Timing for CKE is equal to CMD and ADDR Setup and Hold Timing.

6.12 Bank Activations with REFRESH

6.12.1 Bank Activations with REFRESH Command

Operating Mode	2X REF Mode	Bank Refreshed per REF Command	Effective tRET
1-CS Mode	off	4 even or 4 odd banks in all 4 quedrants	32ms
	on	All 8 banks in all 4 quadrants	16ms
2-CS Mode	off	4 even or 4 odd banks in selected rank (rank 0 or rank 1) or in both ranks	32ms
	on	All 8 banks in selected rank (rank 0 or rank 1) or in both ranks	16ms

6.13 Writes (WR)

6.13.1 Write - Basic Information

Write bursts are initiated with a WR command, as shown in Figure. The column and bank addresses are provided with the WR command, and Auto Precharge is either enabled or disabled for that access. The length of the burst initiated with a WR command is four or eight depending on the mode register setting. There is no interruption of WR bursts. The two least significant address bits A0 and A1 are “Don’t Care”.

For WR commands with Autoprecharge the row being accessed is precharged $t_{WR/A}$ after the completion of the burst. If t_{RAS}(min) is violated the begin of the internal Autoprecharge will be performed one cycle after t_{RAS}(min) is met. WR, the write recovery time for write with Autoprecharge can be programmed in the Mode Register. Choosing high values for WR will prevent the chip to delay the internal Autoprecharge in order to meet t_{RAS}(min).

During WR bursts data will be registered with the edges of WDQS. The write latency can be programmed during Extended Mode Register Set. The first valid data is registered with the first valid rising edge of WDQS following the WR command. The externally provided WDQS must switch from HIGH to LOW at the beginning of the preamble. There is also a postamble requirement before the WDQS returns to HIGH. The WDQS signal can only transition when data is applied at the chip input and during pre- and postambles. t_{DQSS} is the time between WR command and first valid rising edge of WDQS. Nominal case is when WDQS edges are aligned with edges of external CLK. Minimum and maximum values of t_{DQSS} define early and late WDQS operation. Any input data will be ignored before the first valid rising WDQS transition.

t_{DQSL} and t_{DQSH} define the width of low and high phase of WDQS. The sum of t_{DQSL} and t_{DQSH} has to be t_{CK}. Back to back WR commands are possible and produce a continuous flow of input data.

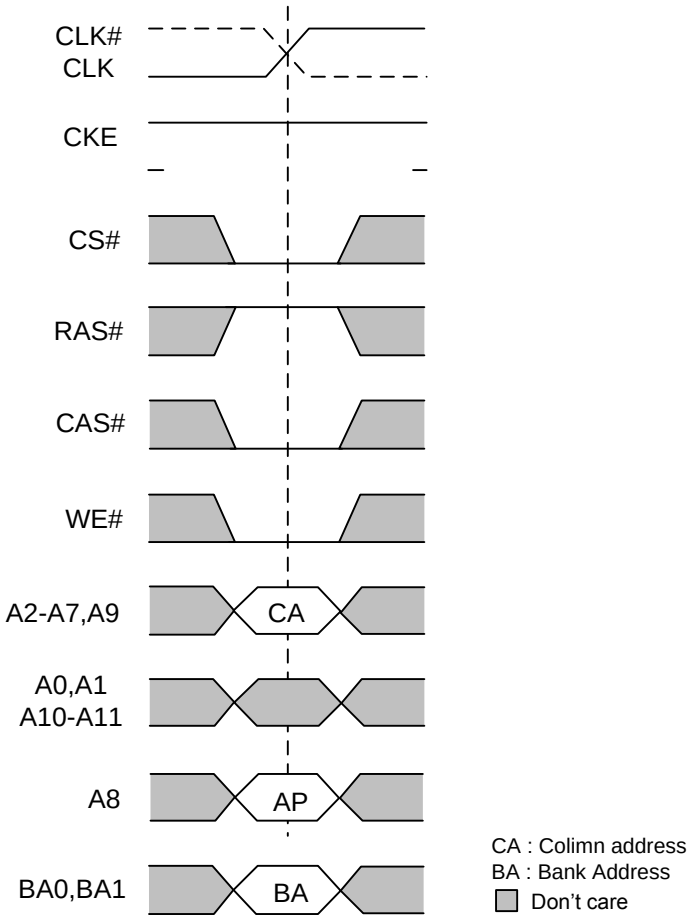
For back to back WR, t_{CCD} has to be met. Any WR burst may be followed by a subsequent RD command. Figure (Write followed by Read) shows the timing requirements for a WR followed by a RD. In this case the delay between the WR command and the following RD may be zero for access across the two 8 bank segments (t_{WTR_RR} = 1 t_{CK}) as shown in Figure (Write followed by Read on different ranks in 2-CS mode).

A WR may also be followed by a PRE command to the same bank. t_{WR} has to be met as shown in Figure (Write followed by Precharge on same bank).

Setup and hold time for incoming DQs and DMs relative to the WDQS edges are specified as t_{DS} and t_{DH}. DQ and DM input pulse width for each input is defined as t_{DIPW}. The input data is masked if the corresponding DM signal is high.

All iming parameters are defined with graphics DRAM terminations on.

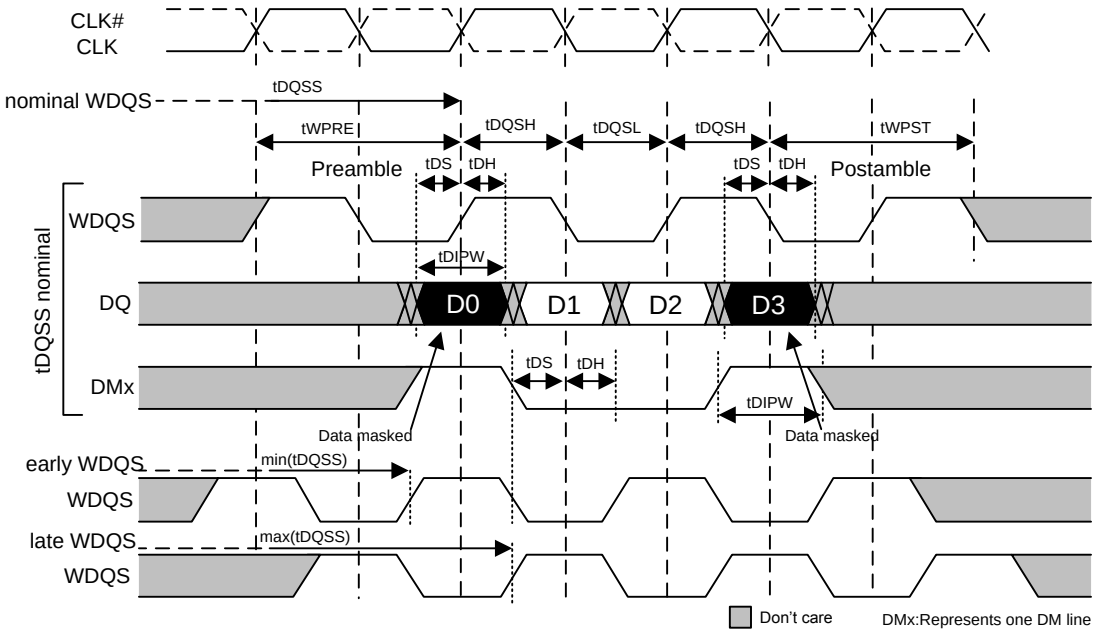
6.13.1.1 Write Command



6.13.1.2 Mapping of WDQS and DM Signals

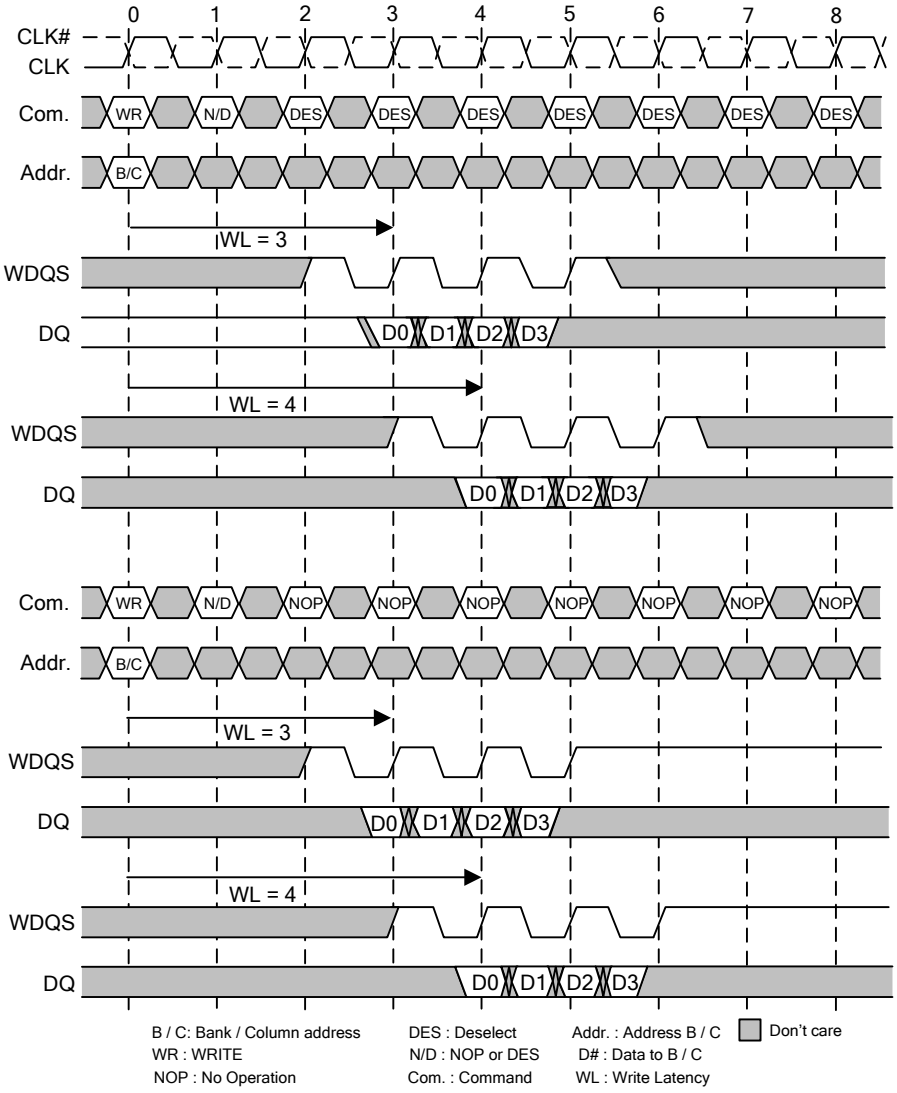
WDQS	Data mask signal	Controlled DQs
WDQS0	DM0	DQ0 - DQ7
WDQS1	DM1	DQ8 - DQ15
WDQS2	DM2	DQ16 - DQ23
WDQS3	DM3	DQ24 - DQ31

6.13.1.3 Basic Write Burst / DM Timing



Note: WDQS can only transition when data is applied at the chip input and during pre- and postambles.

6.14 Write - Basic Sequence



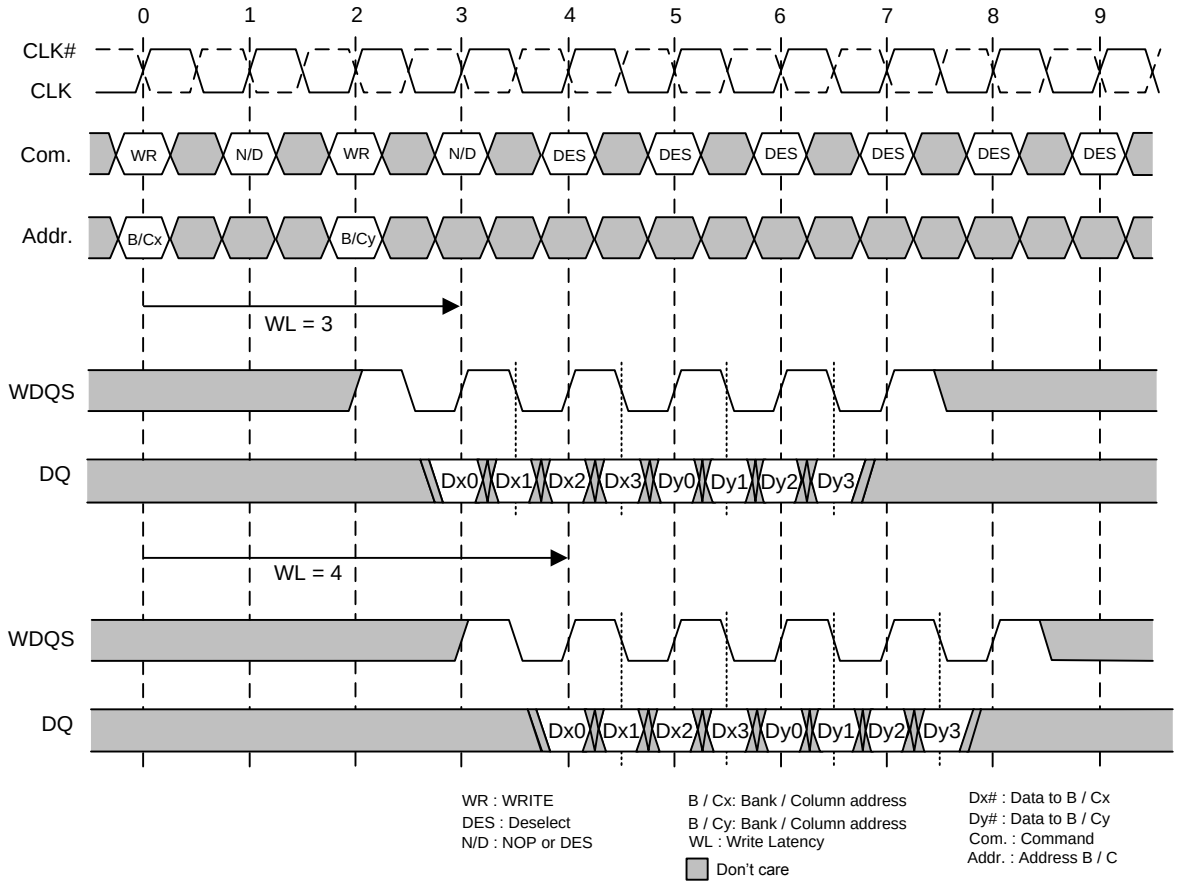
Notes :

1. Shown with nominal value of t_{DQSS}.
2. WDQS can only transition when data is applied at the chip input and during pre- and postambles.
3. When NOPs are applied on the command bus, the WDQS and the DQ busses remain stable High.
4. When DESs are applied on the command bus, the status of the WDQS and DQ busses is unknown.

6.15 Write - Consecutive Bursts

6.15.1Gapless Bursts

6.15.1.1 Gapless Write Bursts

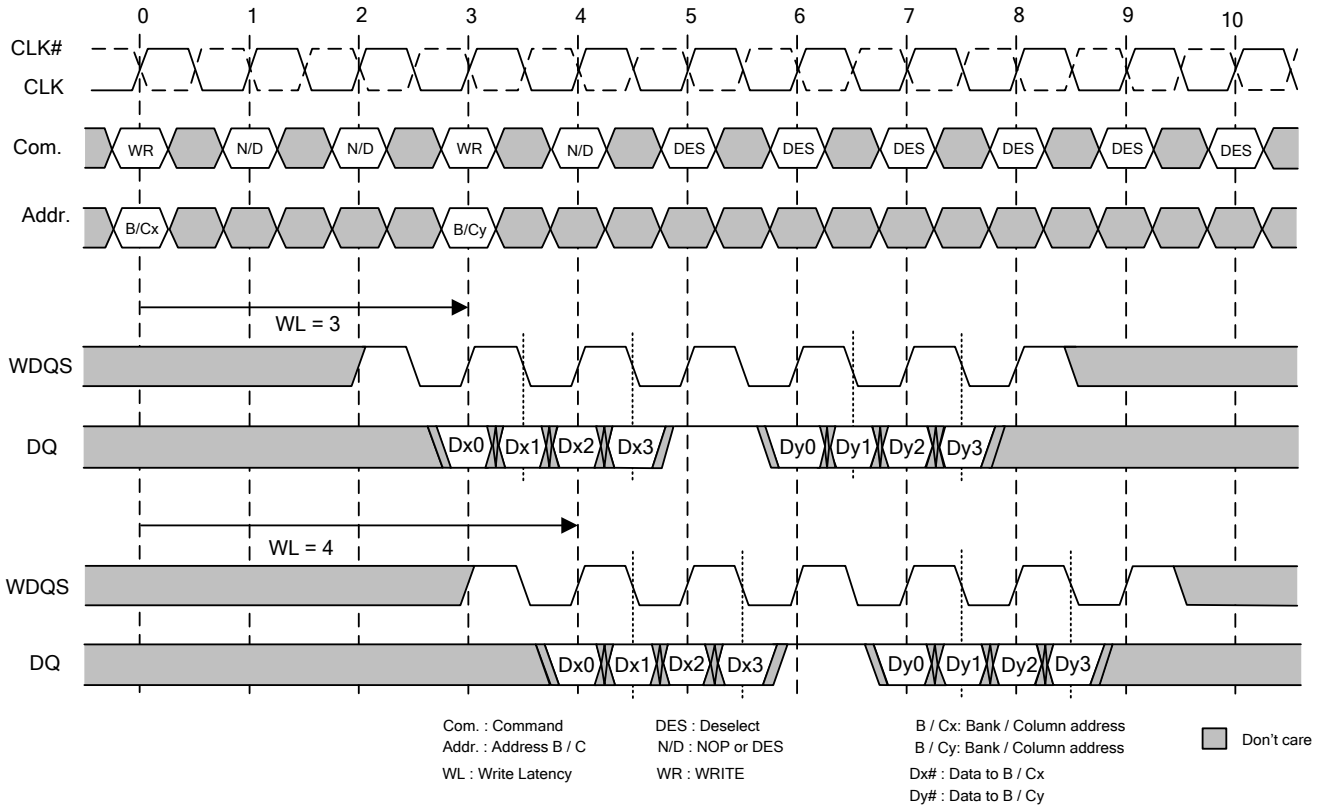


Notes :

1. Shown with nominal value of t_{DQSS}.
2. The second WR command may be either for the same bank or another bank.
3. WDQS can only transition when data is applied at the chip input and during pre- and postambles.

6.15.2 Bursts with Gaps

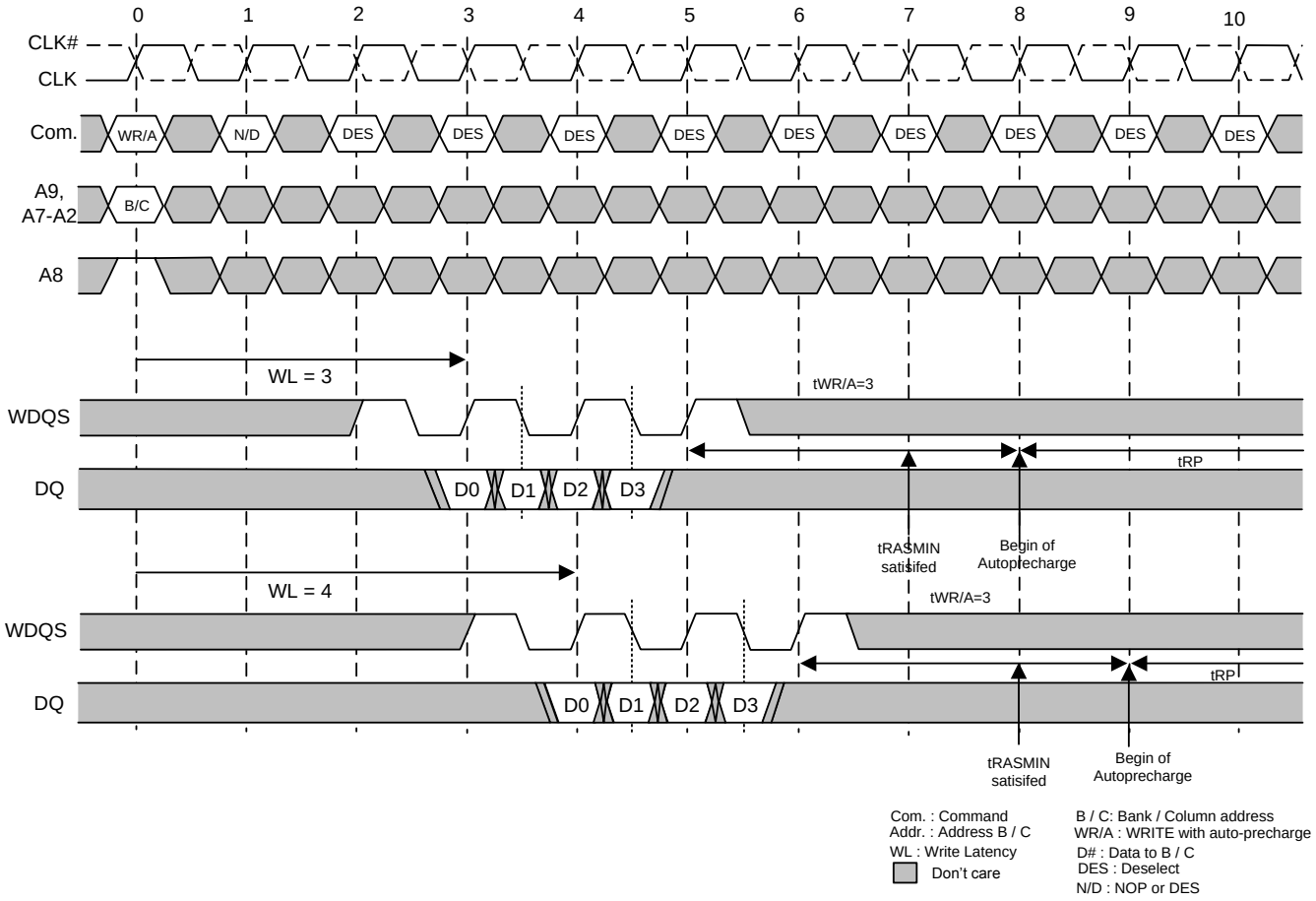
6.15.2.1 Consecutive Write Bursts with Gaps



Notes :

1. Shown with nominal value of t_{DQSS}.
2. The second WR command may be either for the same bank or another bank.
3. WDQS can only transition when data is applied at the chip input and during pre- and postambles.

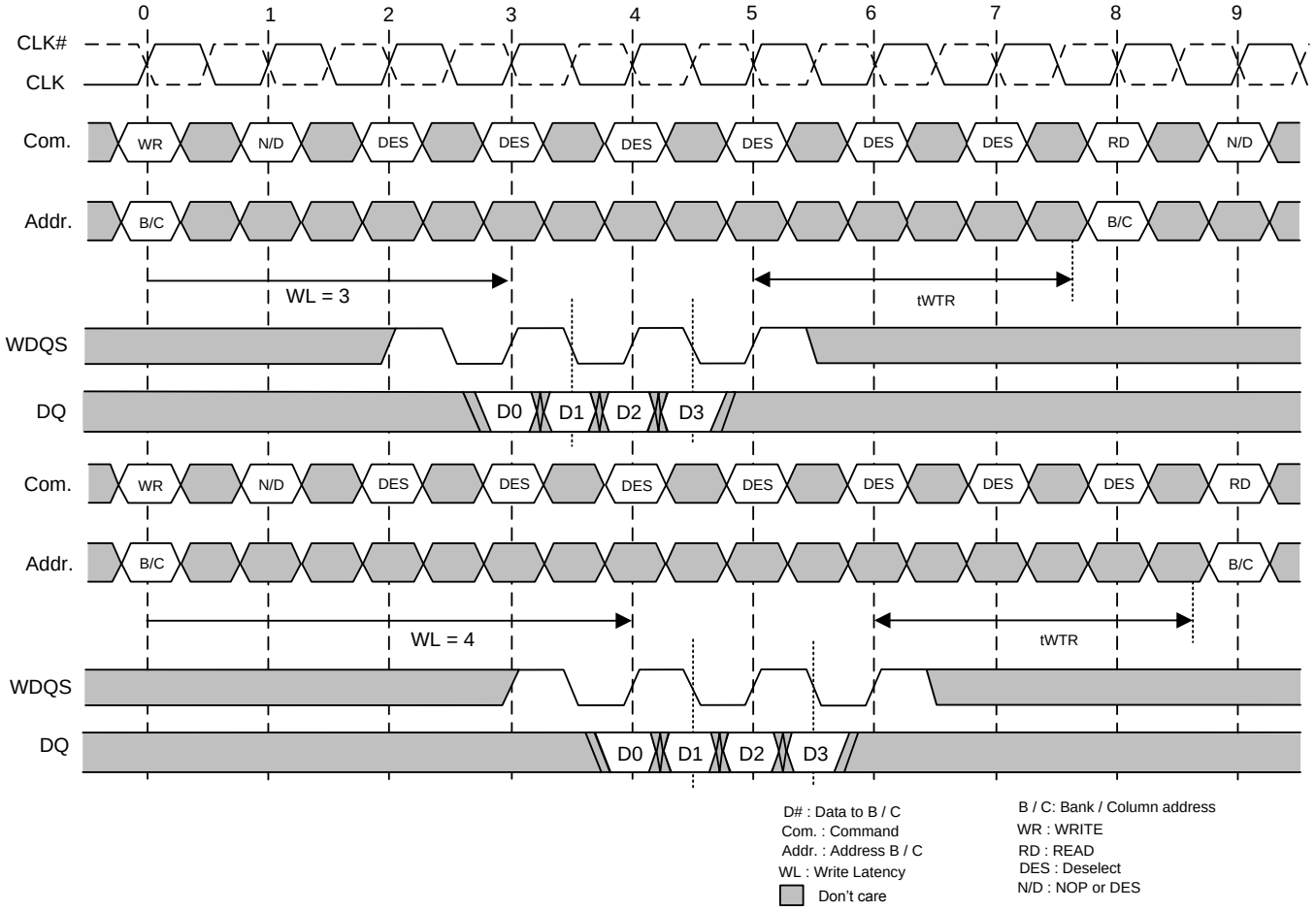
6.15.3 Write with Autoprecharge



Notes :

1. Shown with nominal value of t_{DQSS}.
2. $t_{WR/A}$ starts at the first rising edge of CLK after the last valid edge of WDQS.
3. t_{RP} starts after $t_{WR/A}$ has been expired.
4. When issuing a WR/A command please consider that the t_{RAS} requirement also must be met at the beginning of t_{RP}.
5. $t_{WR/A} \geq t_{WR}$.
6. WDQS can only transition when data is applied at the chip input and during pre- and postambles.

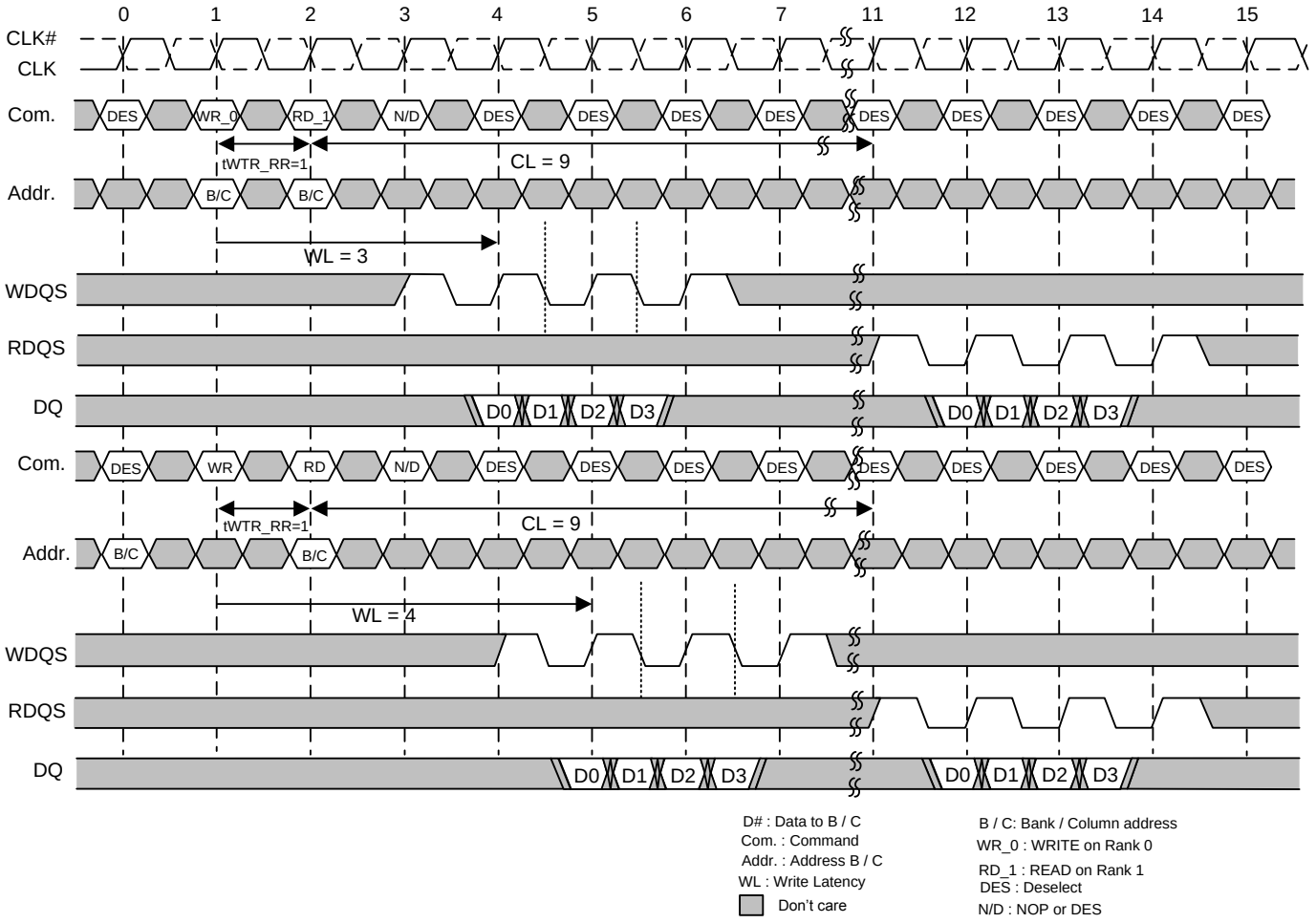
6.15.4 Write followed by Read



Notes :

1. Shown with nominal value of t_{DQSS}.
2. The RD command may be either for the same bank or another bank.
3. WDQS can only transition when data is applied at the chip input and during pre- and postambles.

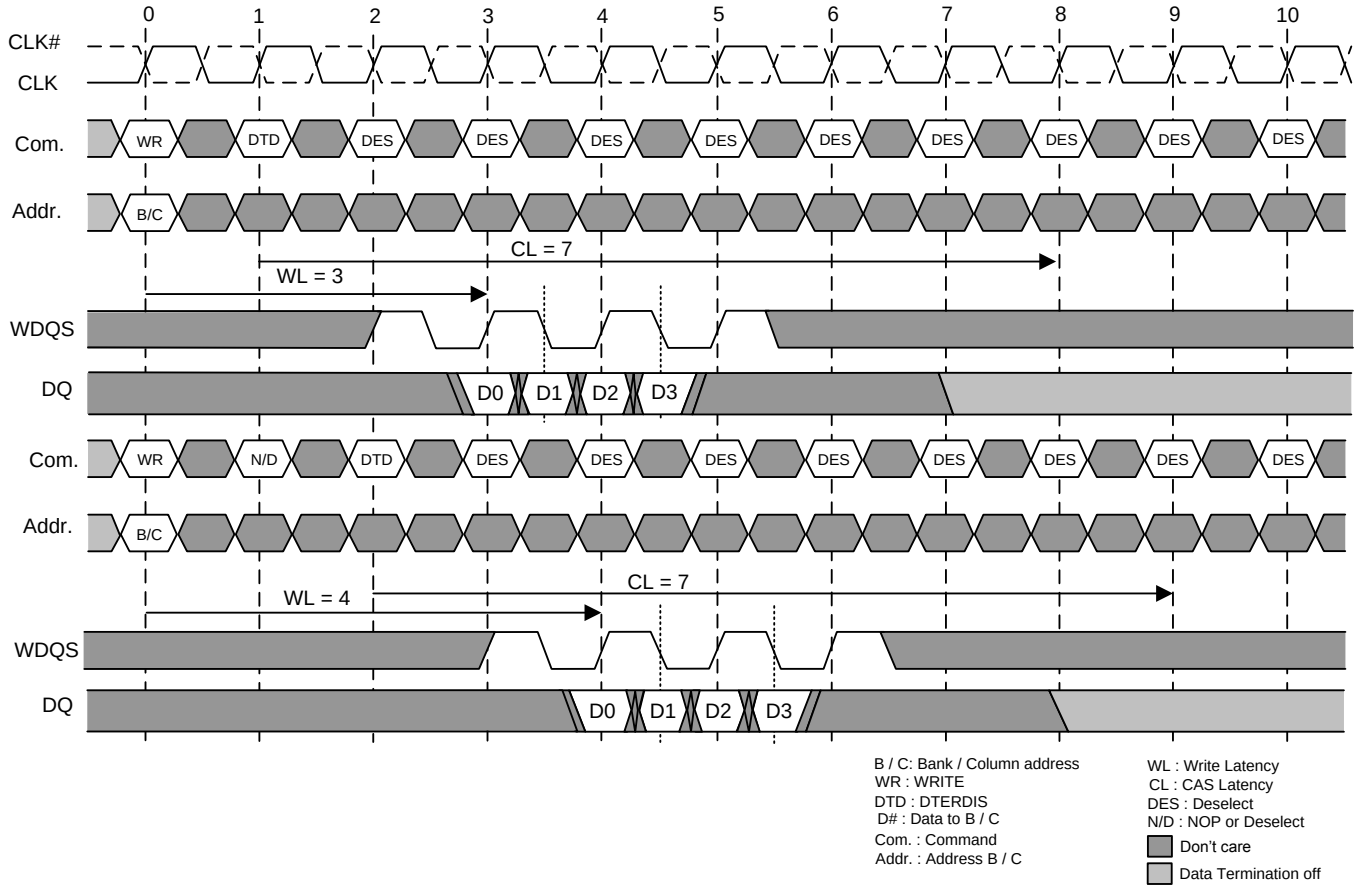
6.15.5 Write followed by Read on different ranks in 2-CS mode



Notes :

1. t_{WTR_RR} is defined between write and read command on different rank.
2. Shown with nominal value of t_{DQSS}.
3. The RD command may be either for the same bank or another bank.
4. WDQS can only transition when data is applied at the chip input and during pre- and postamble.

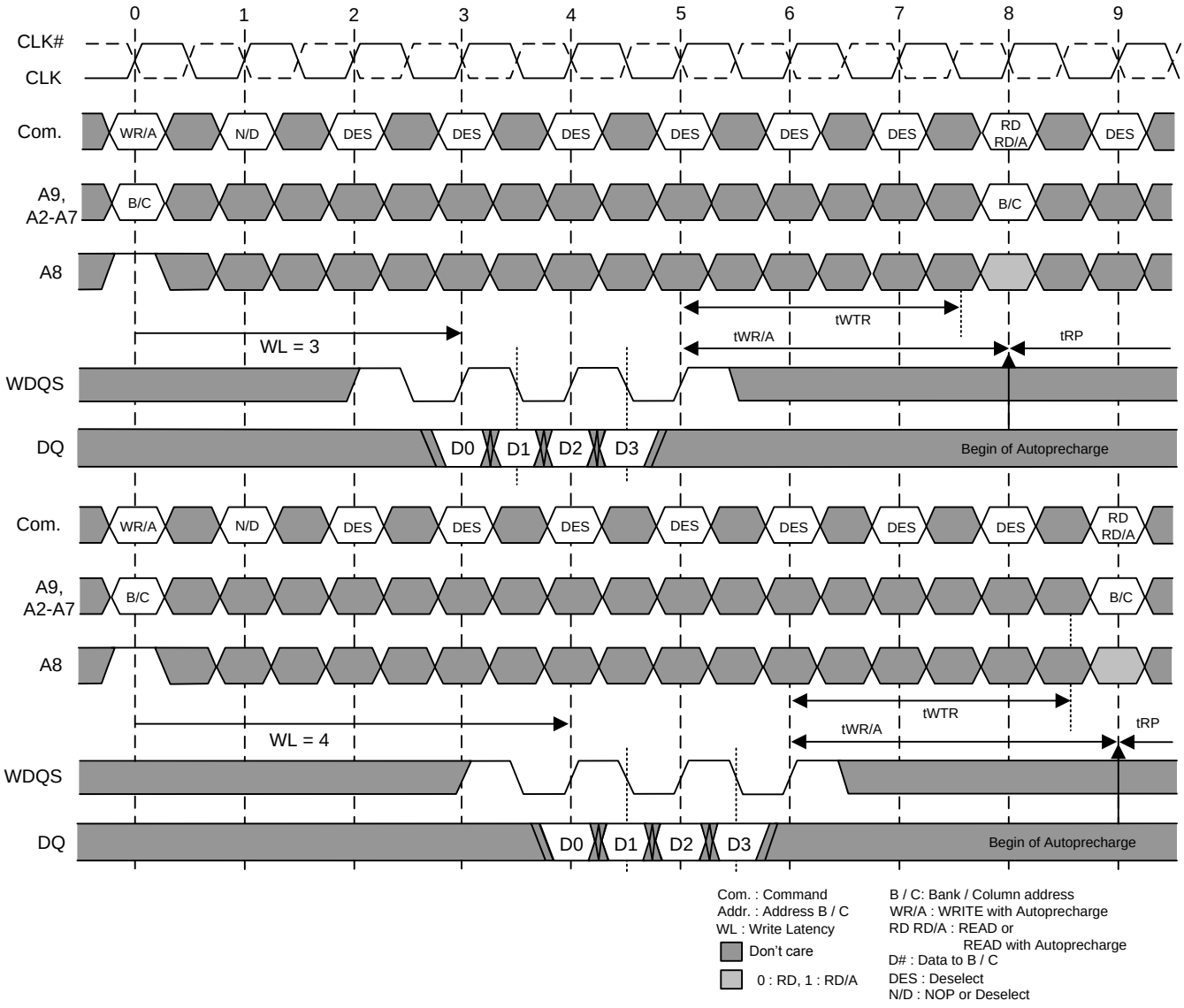
6.15.6 Write followed by DTERDIS



Notes :

1. Shown with nominal value of t_{DQSS}.
2. WDQS can only transition when data is applied at the chip input and during pre- and postambles.
3. A margin of one clock has been introduced in order to make sure that the data termination are still on when the last Write data reaches the memory.
4. The minimum distance between Write and DTERDIS is one clock.

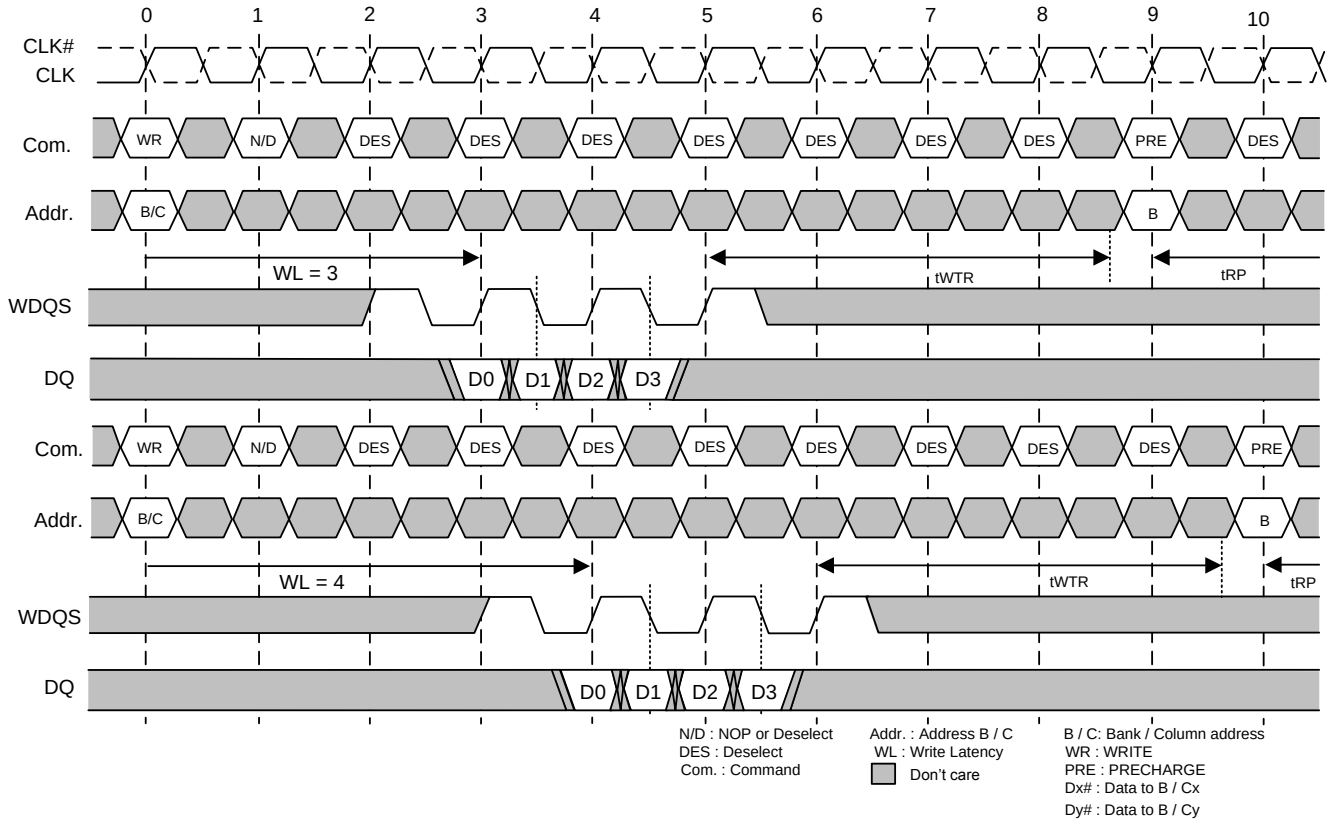
6.15.7 Write with Autoprecharge followed by Read / Read with Autoprecharge on another bank



Notes :

1. Shown with nominal value of t_{DQSS}.
2. The RD command is only allowed for another activated bank.
3. $t_{WR/A}$ is set to 4 in this example.
4. WDQS can only transition when data is applied at the chip input and during pre- and postambles.

6.15.8 Write followed by Precharge on same bank



Notes :

1. Shown with nominal value of t_{DQSS}.
2. WR and PRE commands are to same bank.
3. t_{RAS} requirement must also be met before issuing PRE command.
4. WDQS can only transition when data is applied at the chip input and during pre- and postambles.

6.16 Reads (RD)

6.16.1 Read - Basic Information

Read bursts are initiated with a RD command, as shown in Figure (Basic Read Burst Timing). The column and bank addresses are provided with the RD command and Autoprecharge is either enabled or disabled for that access. The length of the burst initiated with a RD command is 4 or 8. There is no interruption of RD bursts. The two least significant start address bits are “Don’t Care”.

If Autoprecharge is enabled, the row being accessed will start internal precharge at the latter of either the completion of bits prefetch or one cycle after $t_{RAS(min)}$ is met.

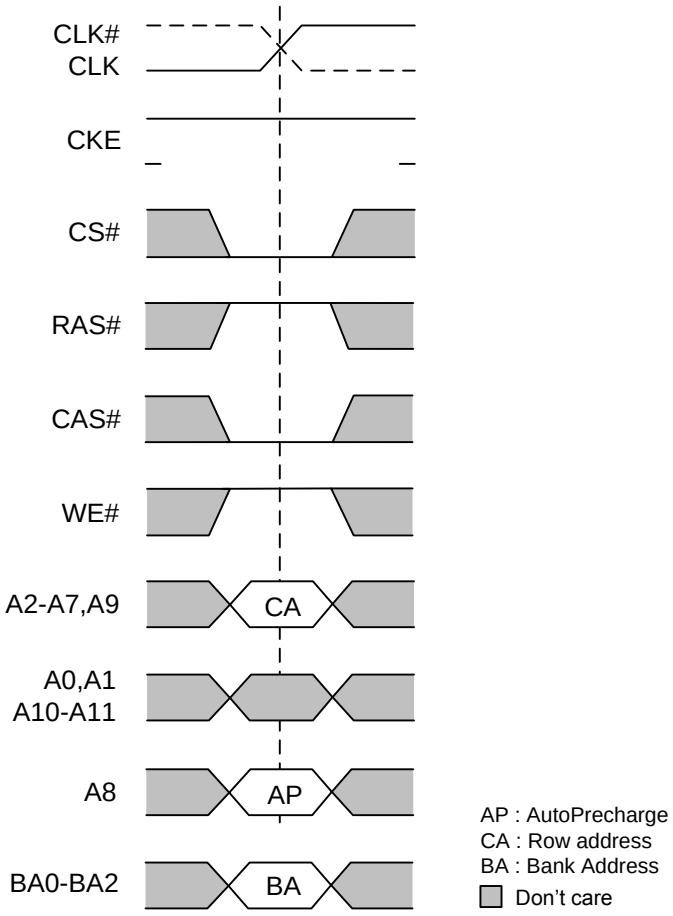
During RD bursts the memory device drives the read data edge aligned with the RDQS signal which is also driven by the memory. After a programmable CAS latency of 7, 8, 9 or 10 the data is driven to the controller. RDQS leaves HIGH state one cycle before its first rising edge (RD preamble t_{RPRE}). After the last falling edge of RDQS a postamble of t_{RPST} is performed. t_{AC} is the time between the positive edge of CLK and the appearance of the corresponding driven read data. The skew between RDQS and the crossing point of CLK/CLK# is specified as t_{DQSCK}. t_{AC} and t_{DQSCK} are defined relatively to the positive edge of CLK. t_{DQSQ} is the skew between a RDQS edge and the last valid data edge belonging to the RDQS edge. t_{DQSQ} is derived at each RDQS edge and begins with RDQS transition and ends with the last valid transition of DQs. t_{QHS} is the data hold skew factor and t_{QH} is the time from the first valid rising edge of RDQS to the first conforming DQ going non-valid and it depends on t_{HP} and t_{QHS}. t_{HP} is the minimum of t_{CL} and t_{CH}. t_{QHS} is effectively the time from the first data transition (before RDQS) to the RDQS transition. The data valid window is derived for each RDQS transition and is defined as t_{QH} minus t_{DQSQ}.

After completion of a burst, assuming no other commands have been initiated, data will go HIGH and RDQS will go HIGH. Back to back RD commands are possible producing a continuous flow of output data. For back to back RD, t_{CCD} has to be met.

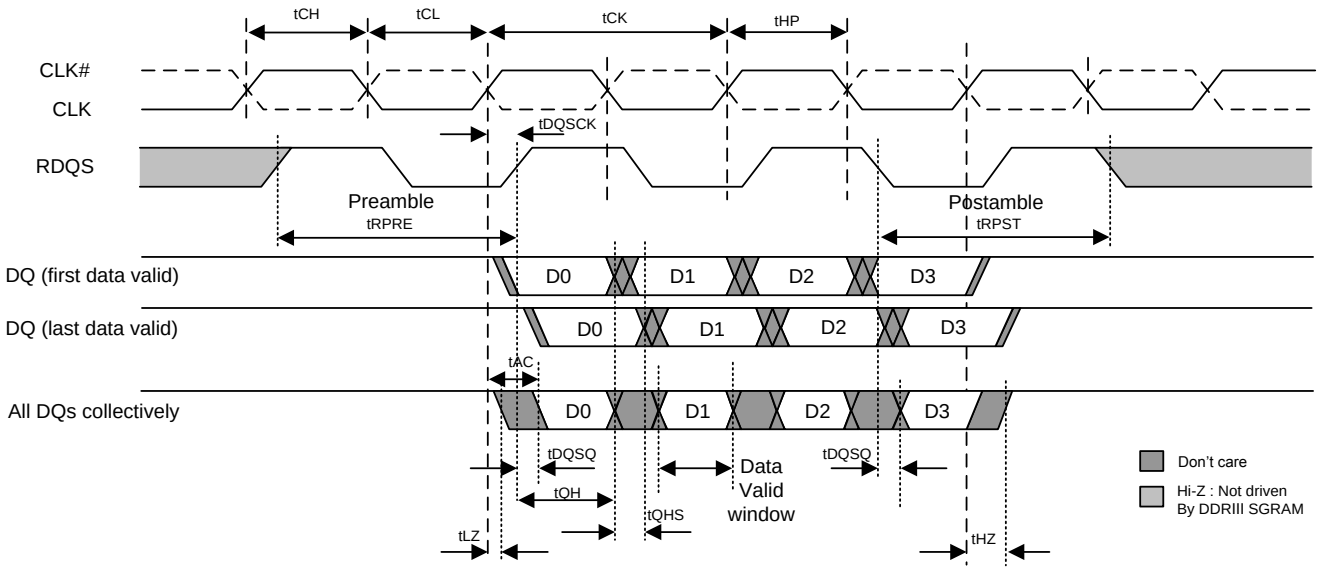
Any RD burst may be followed by a subsequent WR command. The minimum required number of NOP commands between the RD command and the WR command (t_{RTW}) depends on the programmed CAS latency and the programmed Write latency $t_{RTW(min)}$= (CL+4-WL) , the timing requirements for RD followed by a WR with some combinations of CL and WL. A RD may also be followed by a PRE command. Since no interruption of bursts is allowed the minimum time between a RD command and a PRE is two clock cycles .

All timing parameters are defined with controller terminations on.

6.16.1.1 Read Command



6.16.1.2 Basic Read Burst Timing

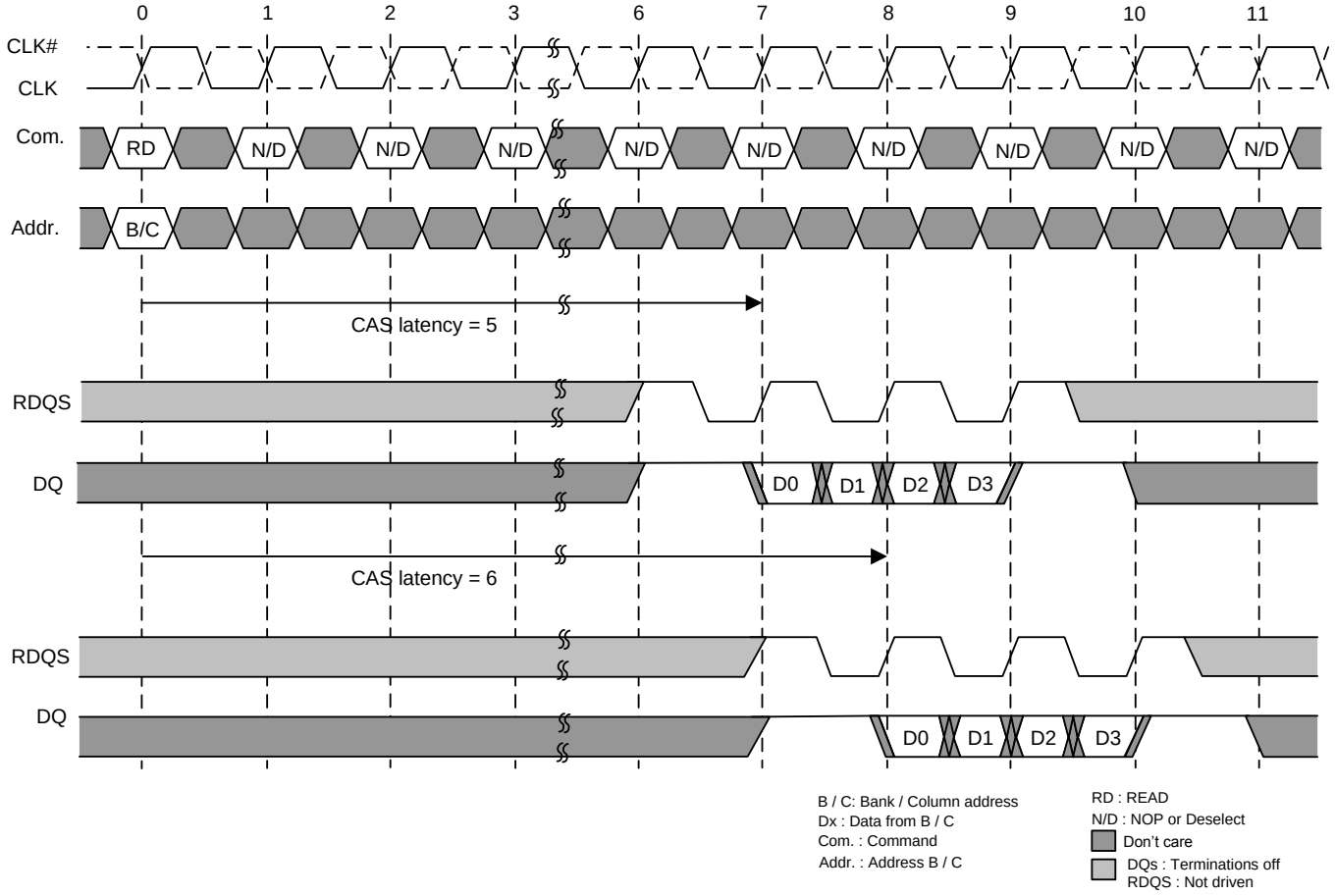


Notes :

1. The GDDR3 GRAPHICS SDRAM switches off the DQ terminations one cycle before data appears on the bus and drives the data bus HIGH.
2. The GDDR3 GRAPHICS SDRAM drives the data bus HIGH one cycle after the last data driven on the bus before switching the termination on again.

6.16.2 Read - Basic Sequence

6.16.2.1 Read Burst



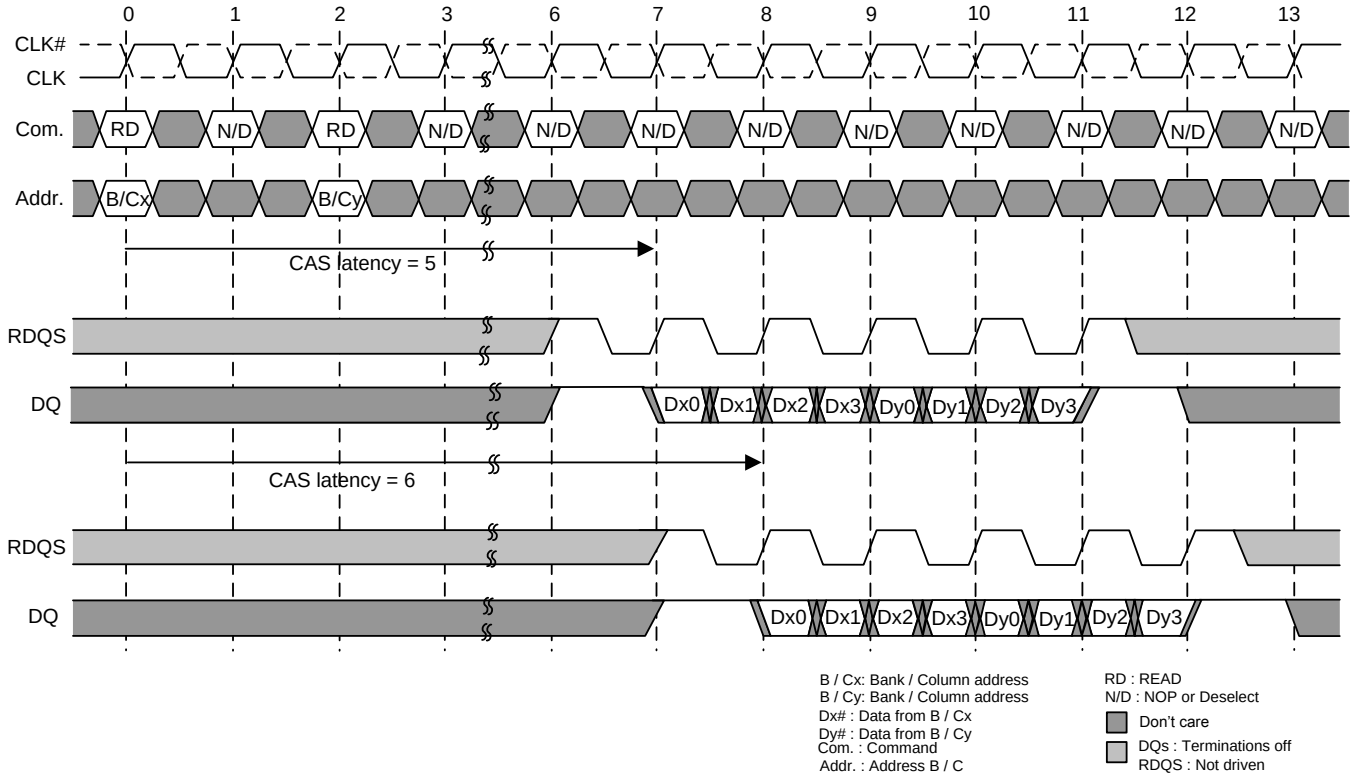
Notes :

1. Shown with nominal t_{AC} and t_{DQSQ}.
2. RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.
3. The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.

6.16.3 Consecutive Read Bursts

6.16.3.1 Gapless Bursts

6.16.3.1.1 Gapless Consecutive Read Bursts

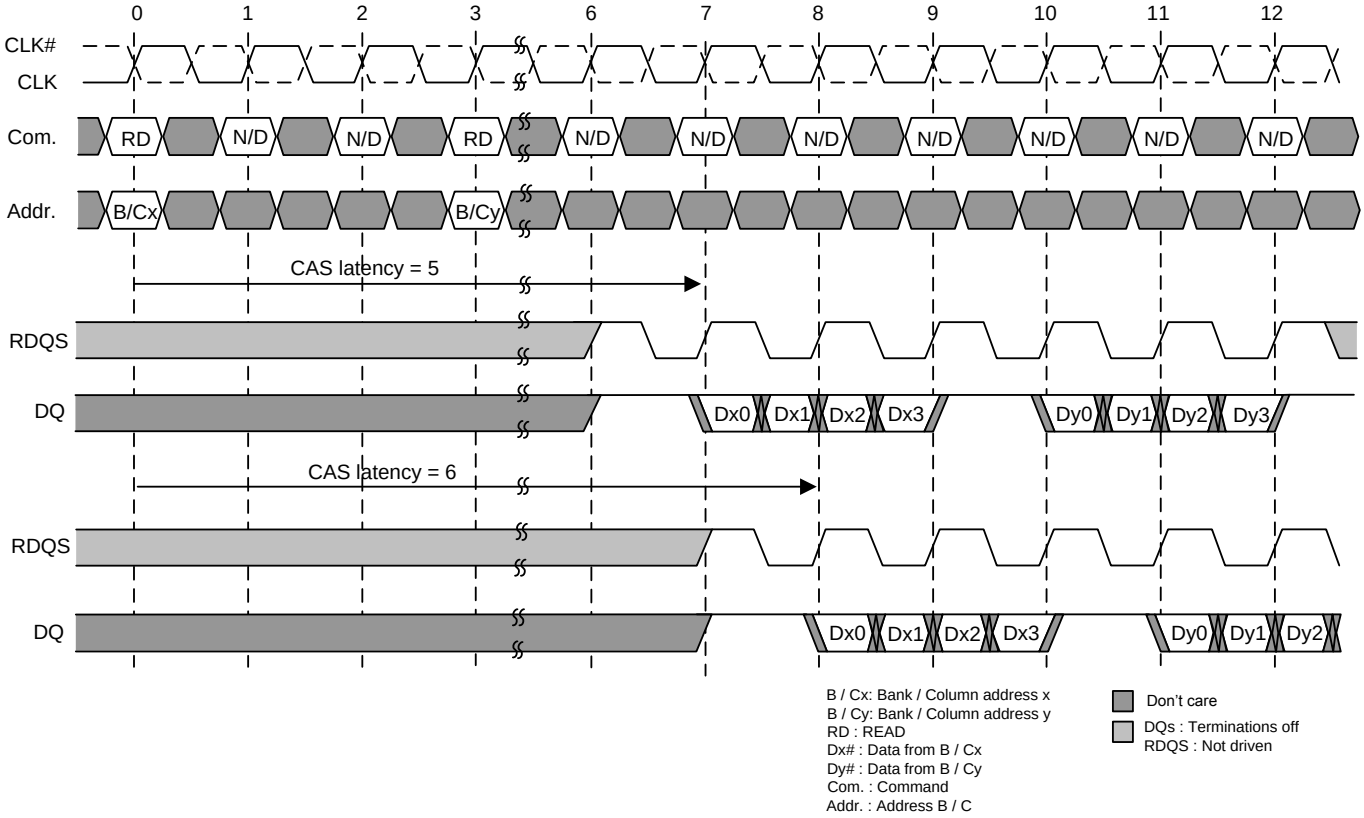


Notes :

1. The second RD command may be either for the same bank or another bank.
2. Shown with nominal t_{AC} and t_{DQSQ}.
3. Example applies only when READ commands are issued to same device.
4. RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.
5. The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.

6.16.4 Bursts with Gaps

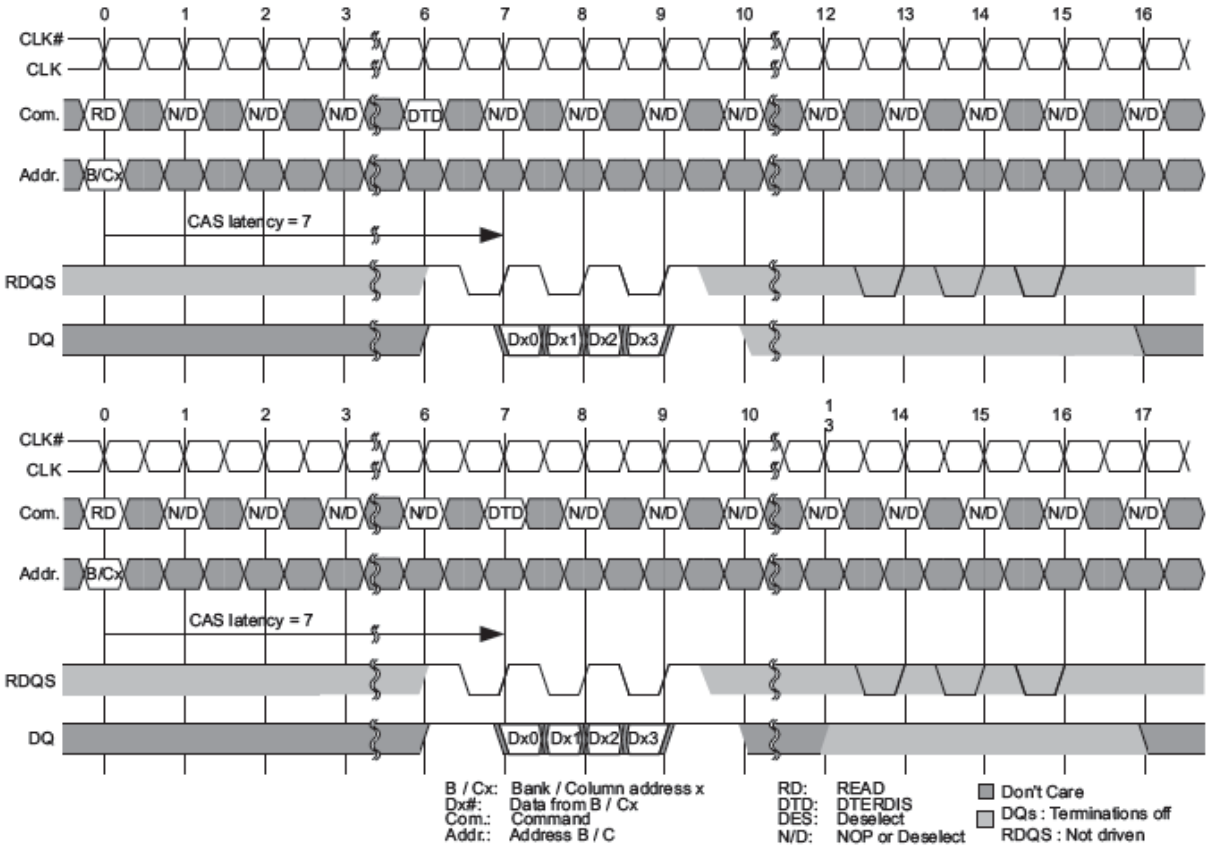
6.16.4.1 Consecutive Read Bursts with Gaps



Notes :

1. The second RD command may be either for the same bank or another bank.
2. RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.
3. The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.

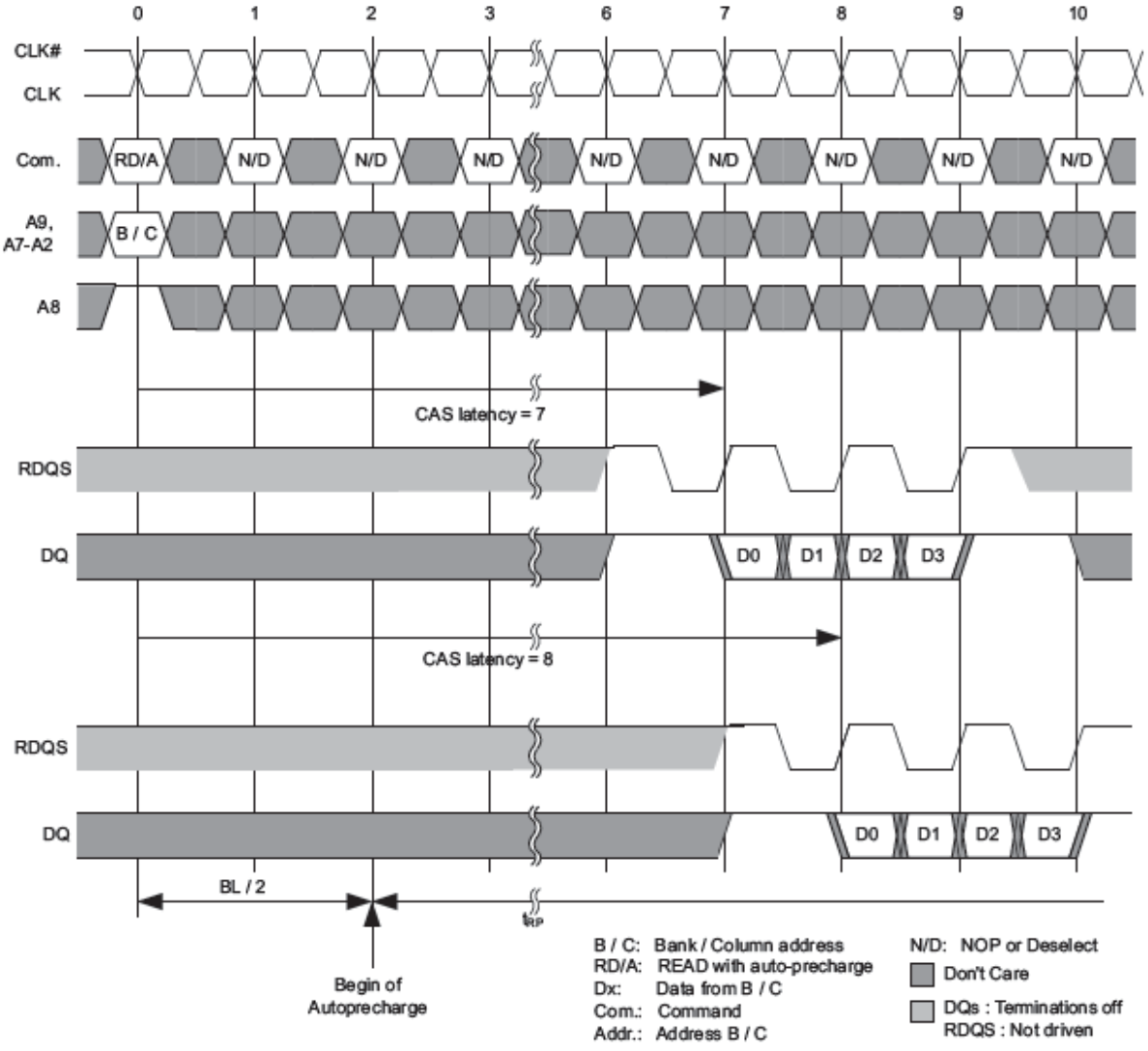
6.16.5 Read followed by DTERDIS



Notes :

1. At least BL/2+1 NOPs are required between a READ command and a DTERDIS command in order to avoid contention on the RDQS bus in a 2 memories system.
2. CAS Latency 7 is used as an example.
3. The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of BL/2+2 clocks.
4. The dashed lines (RDQS bus) describe the RDQS behavior in the case where the DTERDIS command corresponds to a Read command applied to the second Graphics DRAM in a 2 memories system. In this case, RDQS would be driven by the second Graphics DRAM.

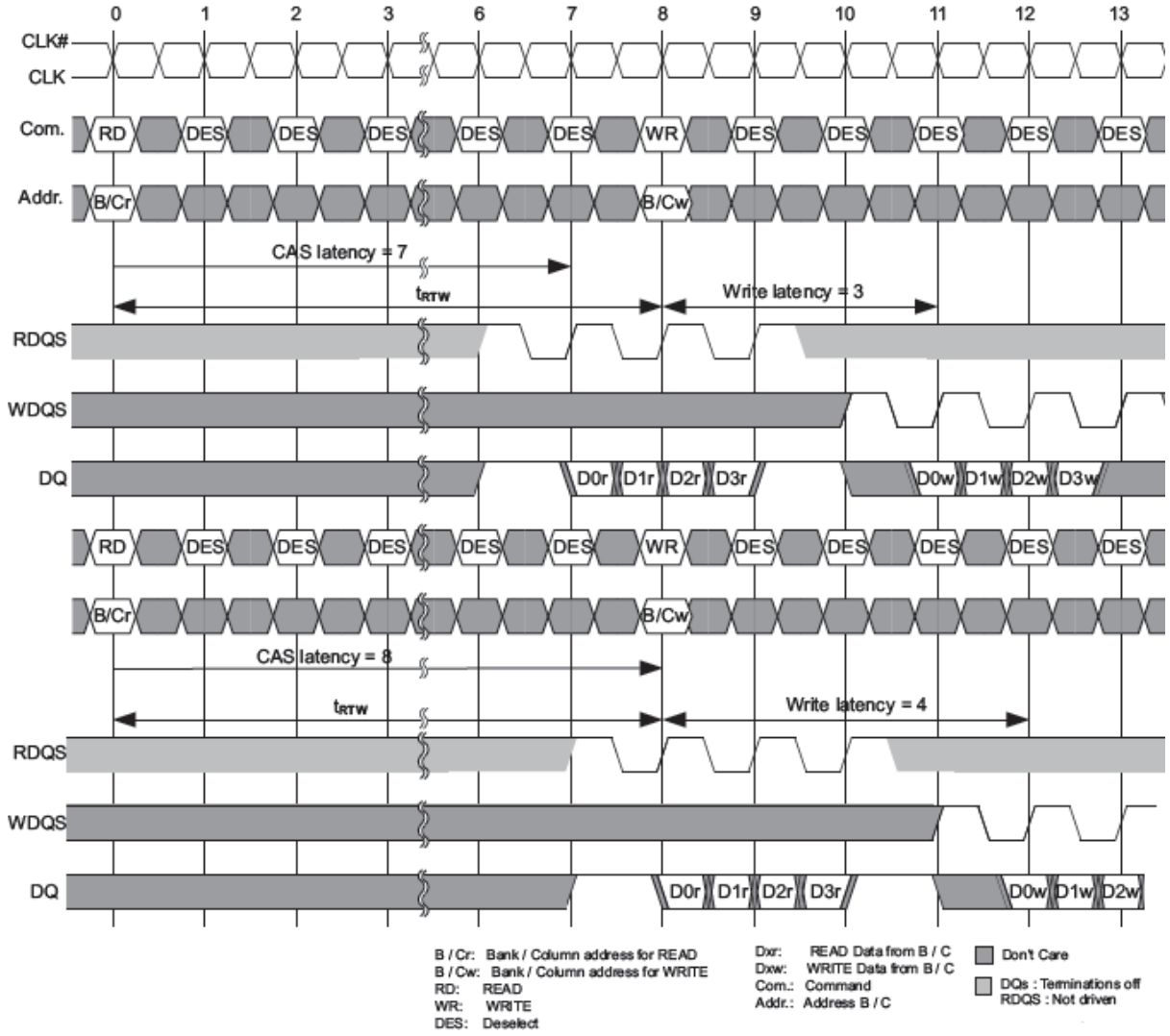
6.16.6 Read with Autoprecharge



Notes :

1. When issuing a RD/A command, the t_{RAS} requirement must be met at the beginning of Autoprecharge.
2. Shown with nominal t_{AC} and t_{DQSQ}
3. RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.
4. The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.
5. t_{RAS} Lockout support.

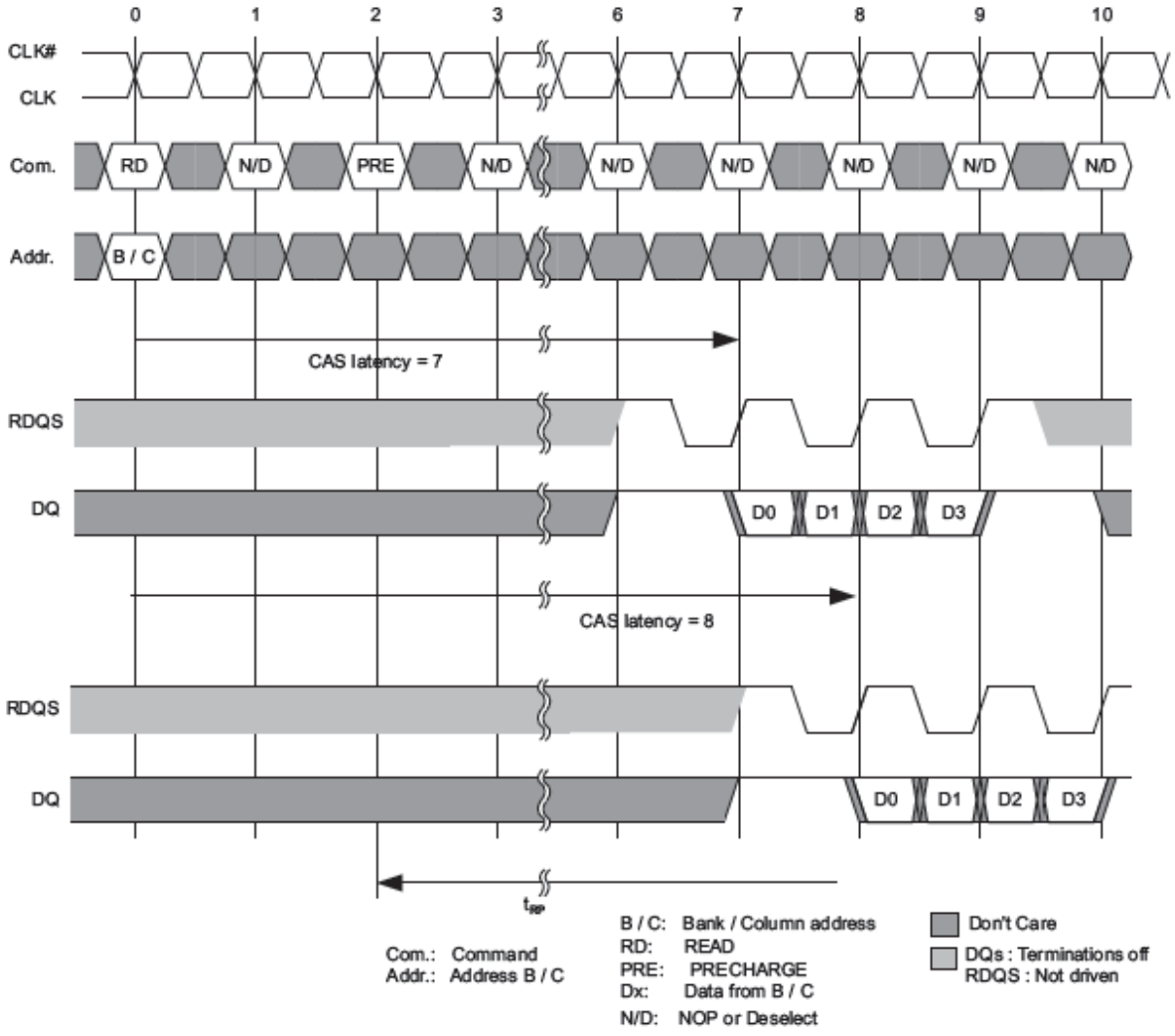
6.16.7 Read followed by Write



Notes :

1. Shown with nominal t_{AC}, t_{DQSQ} and t_{DQSS}.
2. RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.
3. The DQ terminations are switched off 1 cycle before the first Read Data and on again 1 cycle after the last Read data.
4. WDQS can only transition when data is applied at the chip input and during pre- and postambles.
5. The Write command may be either on the same bank or on another bank.

6.16.8 Read followed by Precharge on the same Bank



Notes :

1. t_{RAS} requirement must also be met before issuing PRE command.
2. RD and PRE commands are applied to the same bank.
3. Shown with nominal t_{AC} and t_{DQSQ}.
4. RDQS will start driving high 1/2 cycle prior to the first falling edge and stop 1/2 cycle after the last rising edge of RDQS.

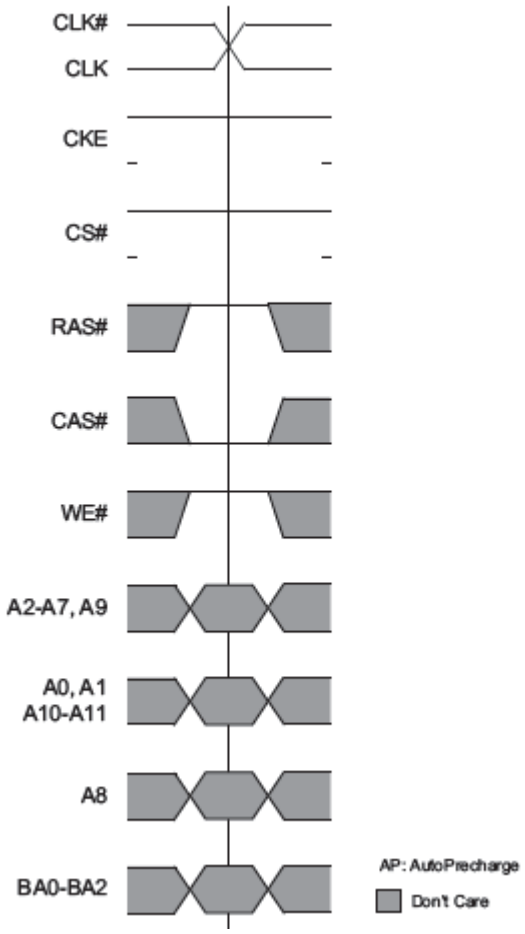
6.17 Data Termination Disable (DTERDIS)

The Data Temination Disable command is detected by the device by snooping the bus for Read commands when CS is high. The terminators are disabled starting at CL - 1 clocks after the DTERDIS command is detected and the duration is 4 clocks. The command and address terminators are always enabled.

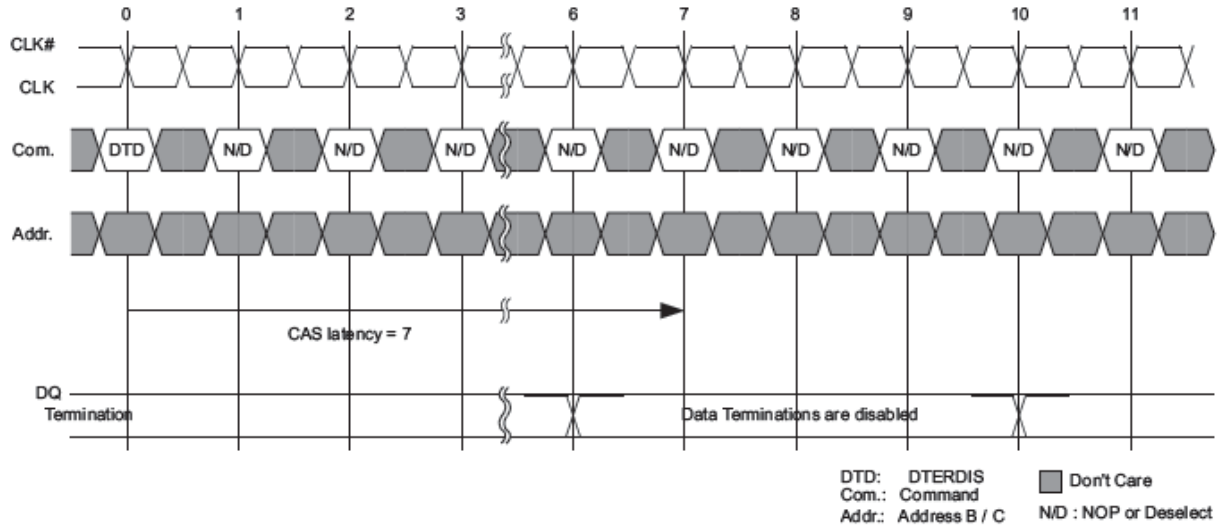
DTERDIS may only be applied to the GDDR3 Graphics memory if it is not in the Power Down or in the Self Refresh state.

The timing relationship between DTERDIS and other commands is defined by the constraint to avoid contention on the RDQS bus (i.e Read to DTERDIS transition) or the necessity to have a defined termination on the data bus during Write (i.e. Write to DTERDIS transition). ACT and PRE/PREALL may be applied at any time before or after a DTERDIS command.

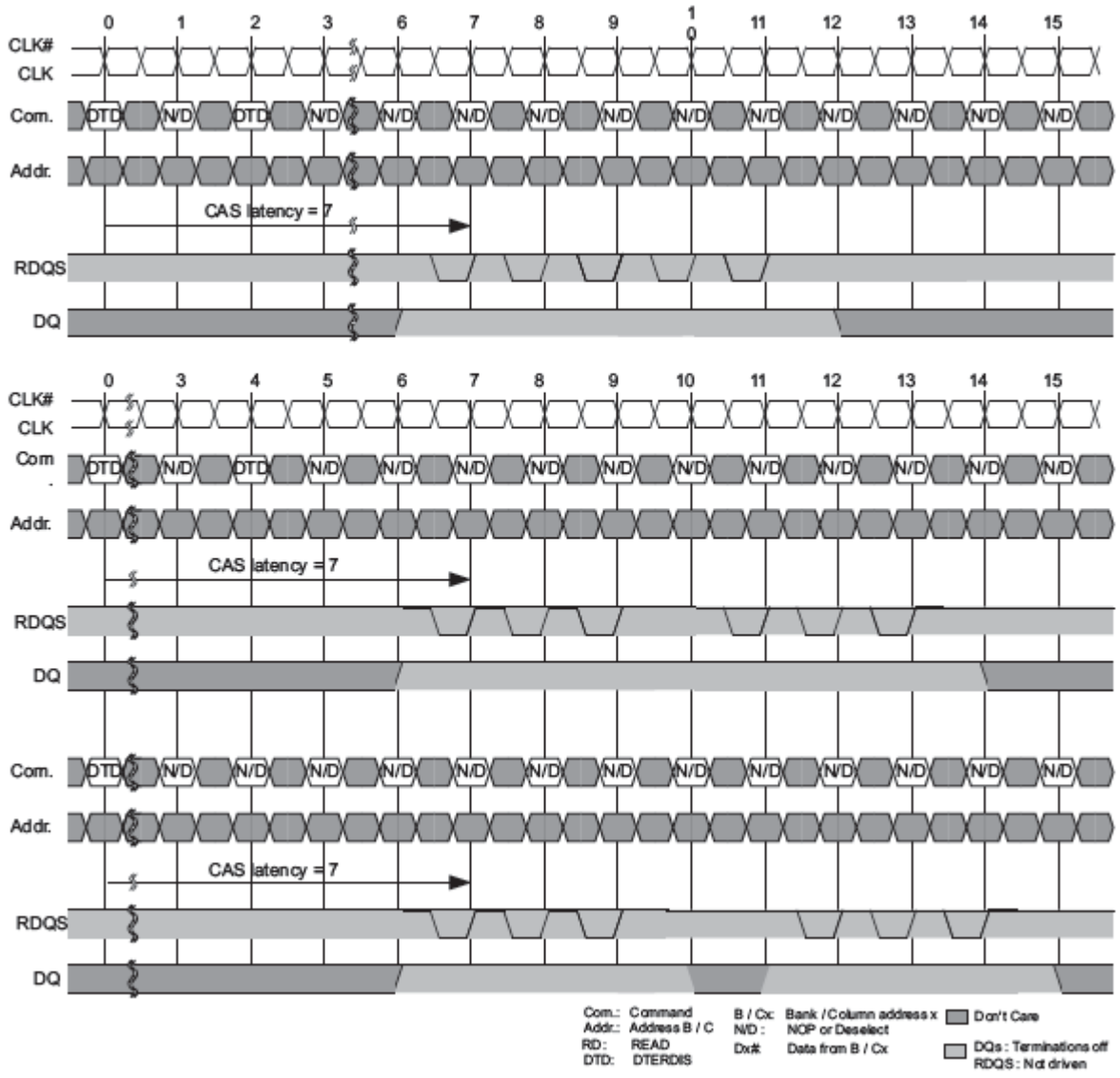
6.17.1 Data Terminal Disable Command



617.1.1 DTERDIS Timing



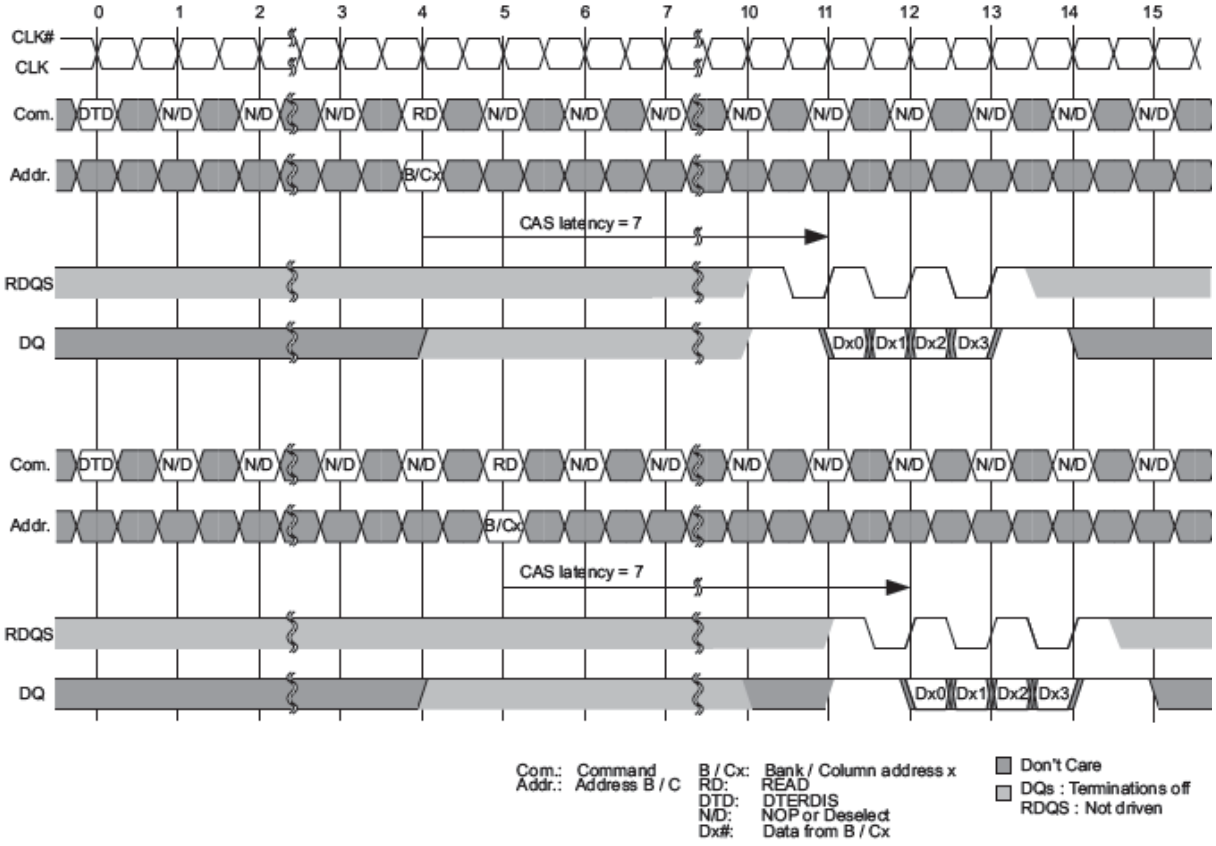
6.17.2 DTERDIS followed by DTERDIS



Notes :

1. At least 1NOP is required between 2 DTERDIS commands. This correspond to a Read to Read transition on the other memory in a 2 memories system.
2. CAS Latency 7 is used as an example.
3. The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of 4 clocks.
4. The dashed lines (RDQS bus) describe the RDQS behavior in the case where the DTERDIS command corresponds to a Read command applied to the second Graphics DRAM in a 2 memories system. In this case, RDQS would be driven by the second Graphics DRAM.

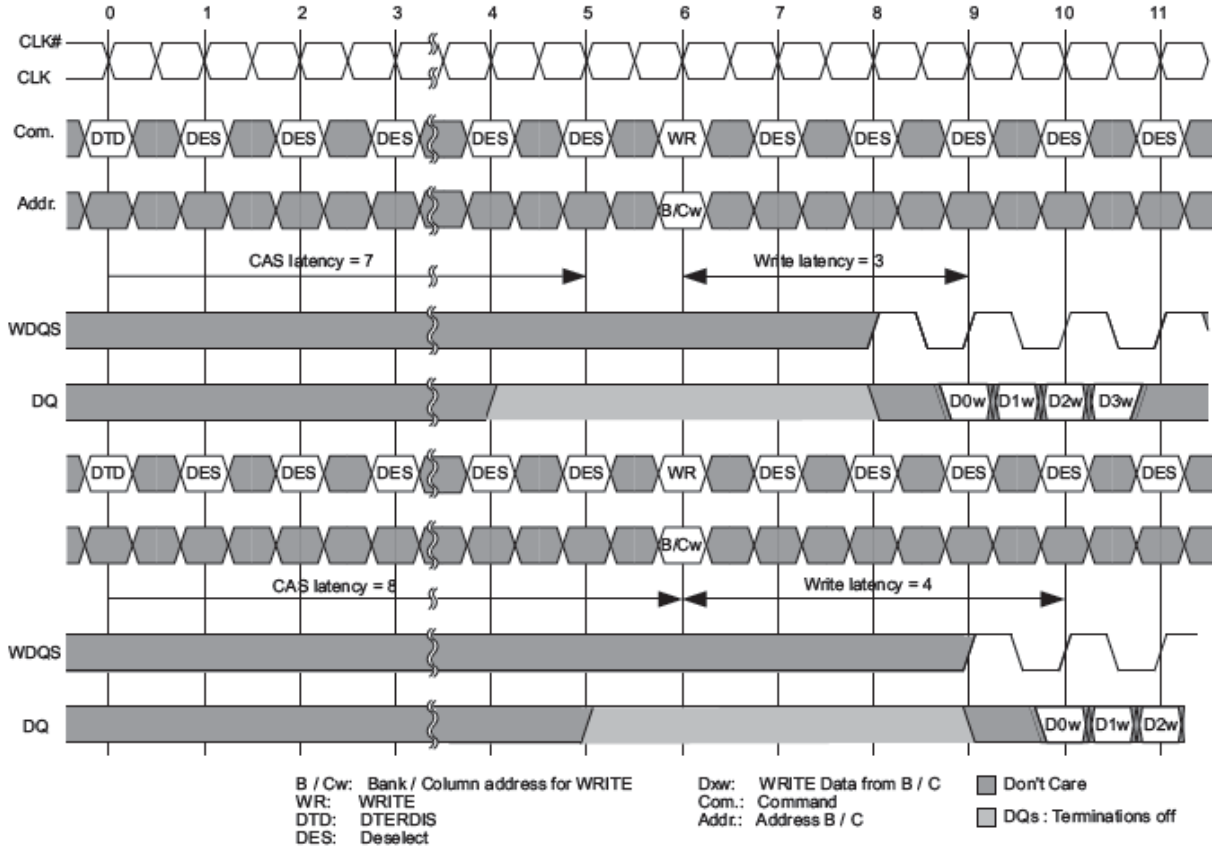
6.17.3 DTERDIS followed by READ



Notes :

1. At least BL/2+1 NOPs are required between a DTERDIS command and a READ command in order to avoid contention on the RDQS bus in a 2 memories system.
2. CAS Latency 7 is used as an example.
3. The DQ terminations are switched off (CL-1) clock periods after the DTERDIS command for a duration of 4 clocks.

6.17.4 DTERDIS followed by Write



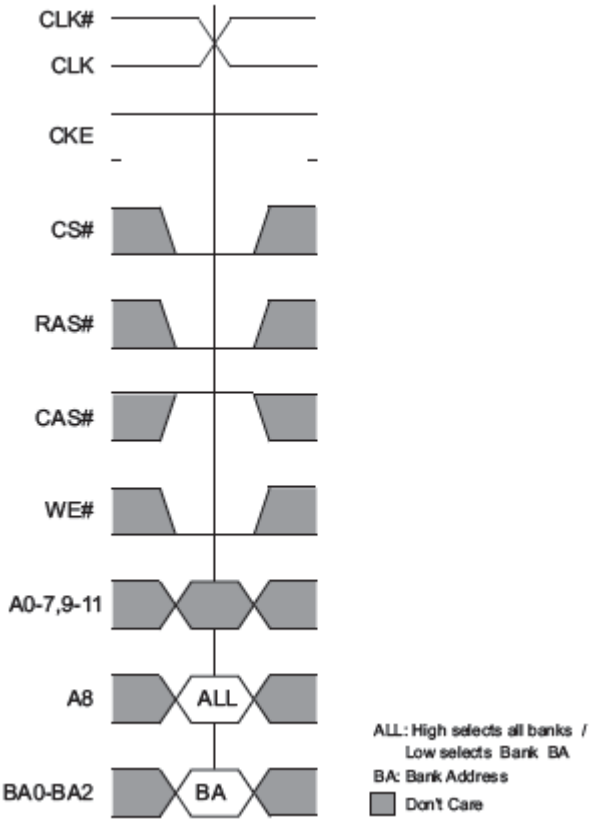
Notes :

1. Write shown with nominal value of t_{DQSS}.
2. WDQS can only transition when data is applied at the chip input and during pre- and postambles.
3. The minimum distance between DTERDIS and Write is (CL - WL + BL/2 +2) clocks.

6.18 Precharge (PRE/PREALL)

The Precharge command is used to deactivate the open row in a particular bank (PRE) or the open rows in all banks (PREALL). The bank(s) will enter the idle state and be available again for a new row access after the time t_{RP}. A8/AP sampled with the PRE command determines whether one or all banks are to be precharged. For PRE commands BA0, BA1 and BA2 select the bank. For PREALL inputs BA0, BA1 and BA2 are “Don’t Care”. The PRE/PREALL command may not be given unless the t_{RAS} requirement is met for the selected bank (PRE), or for all banks within one rank (PREALL).

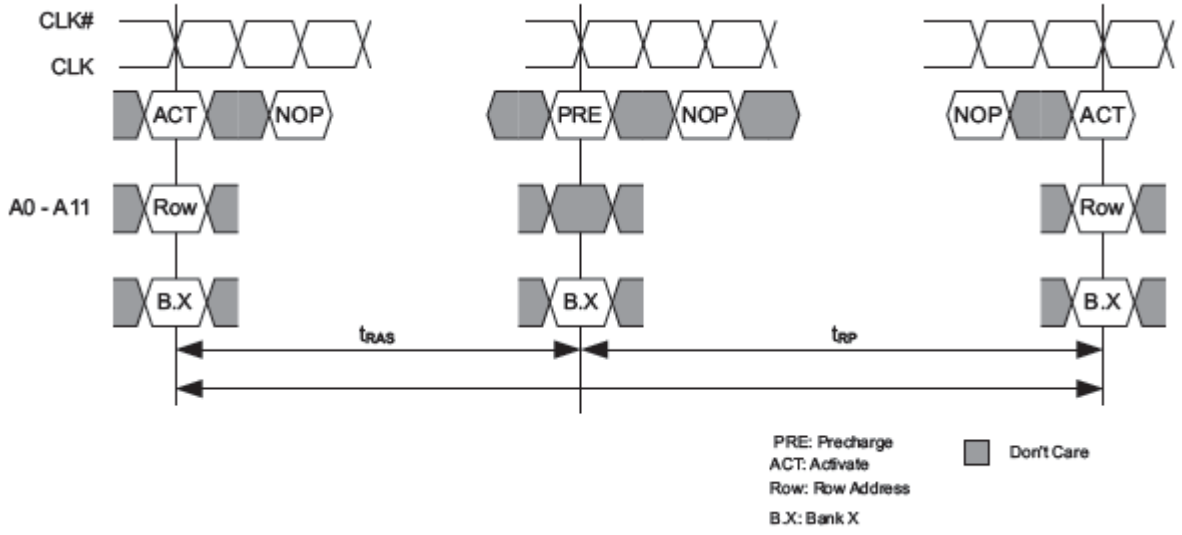
6.18.1 Precharge Command



6.18.2 BA2, BA1 and BA0 precharge bank selection within one rank

A8 / AP	BA2	BA1	BA0	Precharged bank(s)
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	X	X	X	All banks within one rank

6.18.3 Precharge Timing



6.19 Auto Refresh Command (AREF)

AREF is used to do a refresh cycle on one row in each bank. The addresses are generated by an internal refresh controller; external address pins are “DON’T CARE”. All banks within the ranks must be idle before the AREF command can be applied. The delay between the AREF command and the next ACT or subsequent AREF must be at least t_{RFC}(min). The refresh period starts when the AREF command is entered and ends t_{RFC} later at which time all banks will be in the idle state.

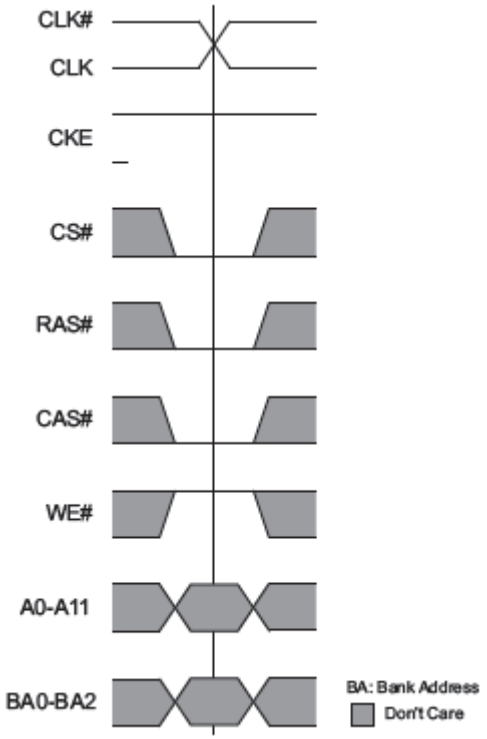
Within a period of t_{REF} the whole memory has to be refreshed. The average periodic interval time from AREF to AREF is then t_{REFI}.

To improve efficiency bursts of AREF commands can be used. Such bursts may consist of maximum 8 AREF commands. t_{RFC}(min) is the minimum required time between two AREF commands inside of one AREF burst. According to the number of AREF commands in one burst the average required time from one AREF burst to the next can be increased. Example: If the AREF bursts consists of 8 AREF commands, the average time from one AREF burst to the next is 8 * t_{REFI}.

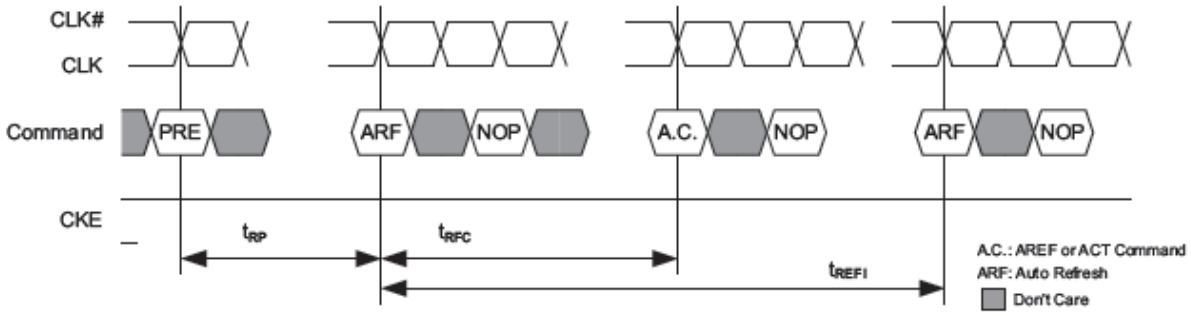
The AREF command generates an update of the OCD output impedance and of the addresses, commands and DQ terminations. The timing parameter t_{KO}.

AREF affects one rank, only. Therefore, accesses to the other rank in the 2-CS-mode are allowed after t_{KO} has expired.

6.19.1 Auto Refresh Command



6.19.2 Auto Refresh Cycle



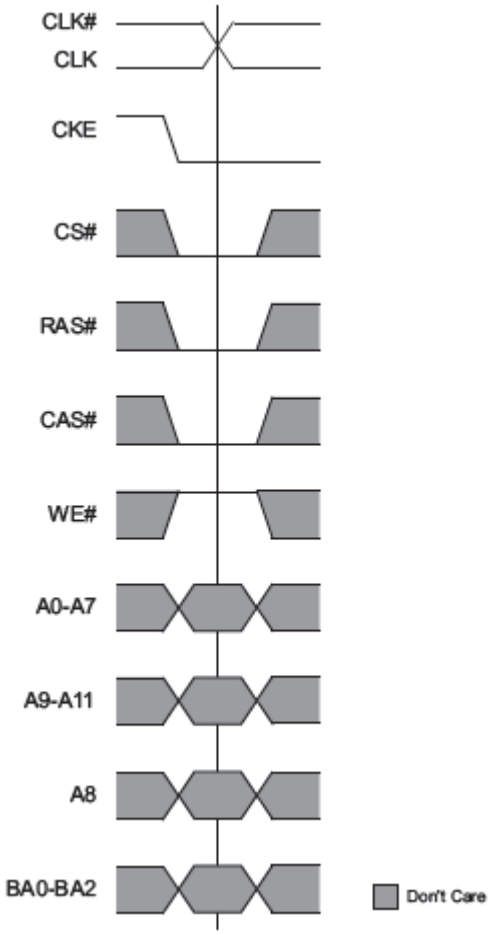
6.20 Self-Refresh

6.20.1 Self-Refresh Entry (SREFEN)

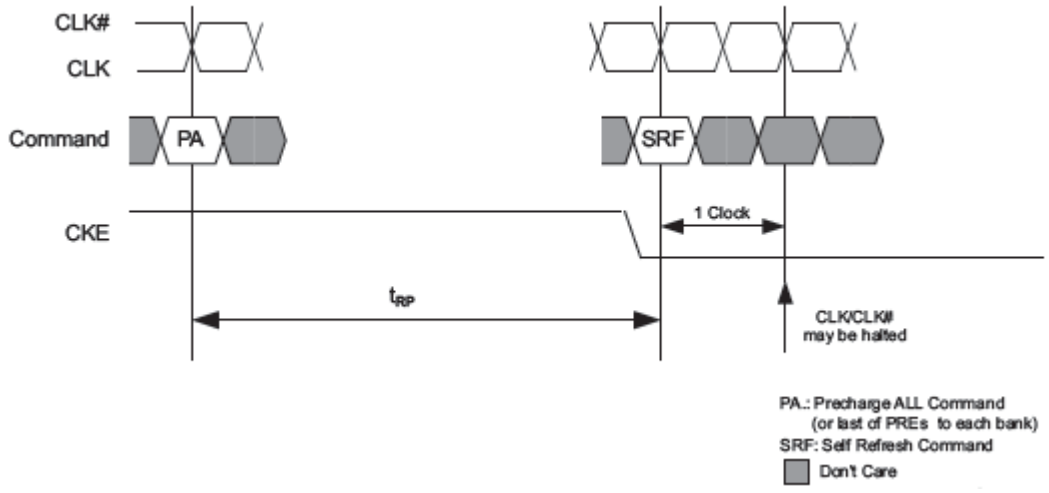
The Self-Refresh mode can be used to retain data in the GDDR3 Graphics RAM even if the rest of the system is powered down. When in the Self-Refresh mode, the GDDR3 Graphics RAM retains data without external clocking. The Self-Refresh command is initiated like an Auto-Refresh command except CKE is disabled (LOW). Self Refresh Entry is only possible if all banks are precharged and t_{RP} is met.The GDDR3 Graphics RAM has a build-in timer to accommodate Self-Refresh operation. The Self-Refresh command is defined by having CS#, RAS#, CAS# and CKE held low with WE# high at the rising edge of the clock. Once the command is registered, CKE must be held LOW to keep the device in Self- Refresh mode. When the GDDR3 Graphics RAM has entered the Self-Refresh mode, all external control signals, except CKE are disabled. For power saving, the DLL and the clock are internally disable; and the address and command terminators are turned off. But the Data terminators remain on. The user may halt the external clock while the device is in Self-Refresh mode the next clock after Self-Refresh entry, however the clock must be restarted before the device can exit Self-Refresh operation.

In 2-CS-mode, SR may only be entered for both ranks in parallel. Therefore CS0# and CS1# will have to be set to Low Level.

6.20.1.1 Self-Refresh Entry Command



6.20.1.2 Self Refresh Entry

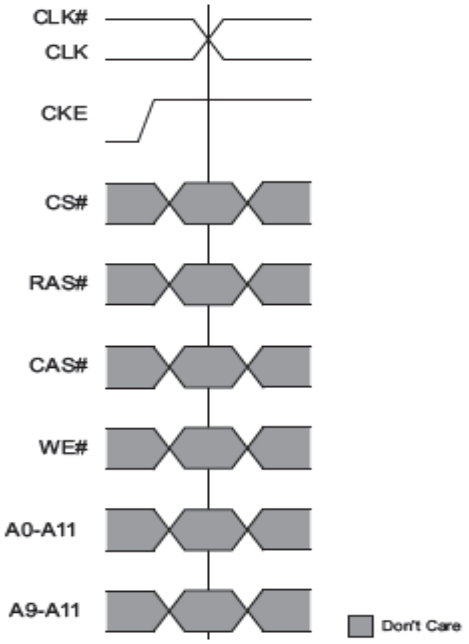


6.21 Self-Refresh Exit (SREFEX)

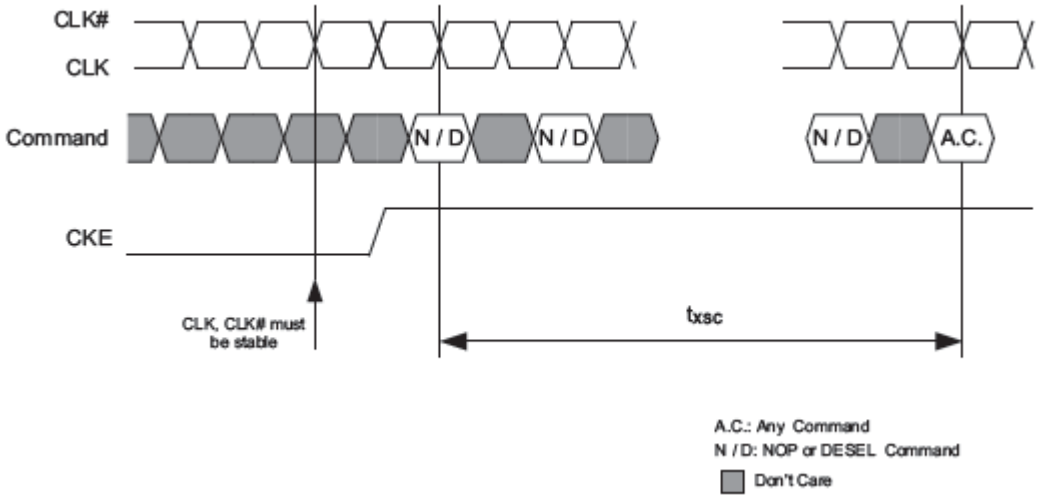
To exit the Self Refresh Mode, a stable external clock is needed before setting CKE high asynchronously. Once the Self-Refresh Exit command is registered, a delay equal or longer than t_{XSRD} must be satisfied before a read command can be applied. During this time, the DLL is automatically enabled, reset and calibrated.

CKE must remain HIGH for the entire Self-Refresh exit period and commands must be gated off with CS# held HIGH. Alternately, NOP commands may be registered on each positive clock edge during the Self Refresh exit interval.

6.21.1 Self Refresh Exit Command



6.21.2 Self Refresh Exit



6.22 Power-Down

The GDDR3 requires CKE to be active at all times an access is in progress: From the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined after the rising edge of the Read Postamble. For Writes, a burst completion is defined one clock after the rising edge of the Write Postamble.

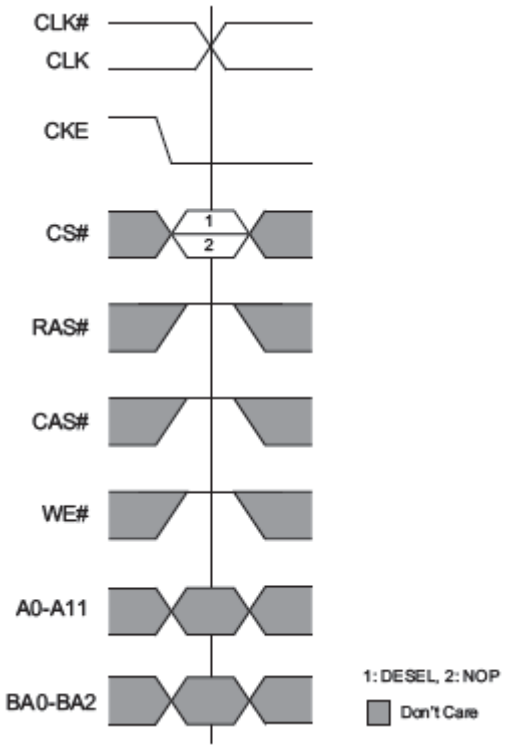
For Read with Autoprecharge and Write with Autoprecharge, the internal Autoprecharge must be completed before entering Power-Down.

Power-Down is entered when CKE is registered LOW. (No access can be in progress. "Access" means as well READ or WRITE to a second memory sharing the data bus in a dual rank system.) If Power-Down occurs when all banks are idle, this mode is referred to as Precharge Power-Down; if Power- Down occurs when there is a row active in any bank, this mode is referred to as Active Power-Down. Entering power- down deactivates the input and output buffers, excluding CLK, CLK# and CKE. For maximum power saving, the user has the option of disabling the DLL prior to entering power- down. In that case the DLL must be enabled and reset after exiting power-down, and 1000 cycles must occur before a READ command can be issued.

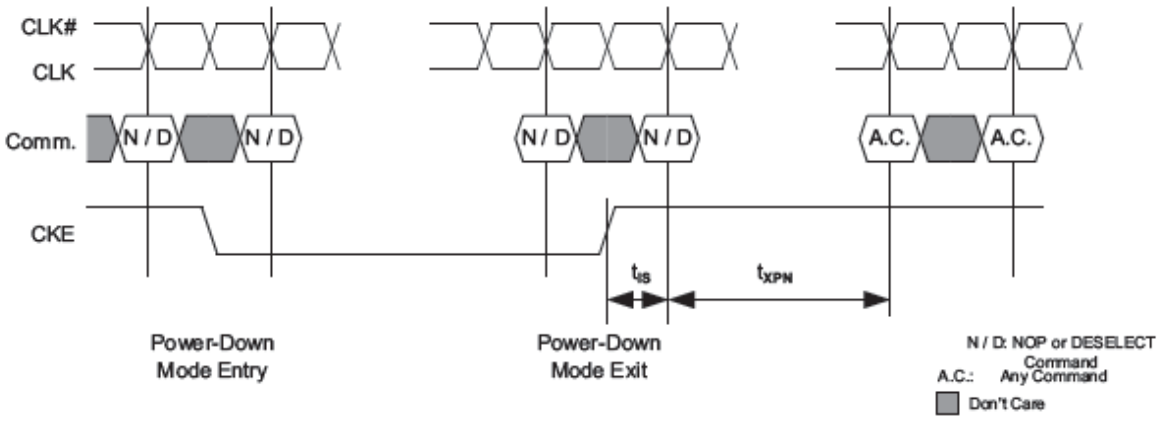
In Power-Down mode, CKE low and a stable clock signal must be maintained at the inputs of the GDDR3 Graphics RAM, all the other input signals are “Don’t Care”. Power down duration is limited by the refresh requirements of the device.

The Power-Down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESEL command). A valid executable command may be applied t_{XPN} later.

6.22.1 Power Down Command



6.22.2 Power-Down Mode



7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings and Operation Conditions

7.1.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power Supply Voltage	V_{DD}	-0.5	2.5	V
Power Supply Voltage for Output Buffer	V_{DDQ}	-0.5	2.5	V
Input Voltage	V_{IN}	-0.5	2.5	V
Output Voltage	V_{OUT}	-0.5	2.5	V
Storage Temperature	T_{STG}	-55	+150	°C
Junction Temperature	T_J	—	+125	°C
Case Temperature	Tcase	0	+105	°C
Short Circuit Output Current	I_{OUT}	—	50	mA

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

7.2 DC Operation Conditions

7.2.1 Recommended Power & DC Operation Conditions

7.2.1.1 Power & DC Operation Conditions (0 °C ≤ T_c ≤ 105 °C)

Parameter	Symbol	Limit Values			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD} / V_{DDQ}	1.7	1.8	1.9	V	1,2,3
Reference Voltage	V_{REF}	0.69*V_{DDQ}	—	0.71*V_{DDQ}	V	4
Output Low Voltage	$V_{OL(DC)}$	—	—	0.8	V	3
Input leakage current	I_{IL}	–5.0	—	+5.0	µA	5
CLK Input leakage current	I_{ILC}	–5.0	—	+5.0	µA	
Output leakage current	I_{OL}	–5.0	—	+5.0	µA	5

Notes :

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. for 1.8 V V_{DD}/V_{DDQ} power supply.
4. V_{REF} is expected to equal 70% of V_{DDQ} for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±2% V_{REF} (DC). Thus, from 70% of V_{DDQ}, V_{REF} is allowed ± 19mV for DC error and an additional ± 27mV for AC noise.
5. I_{IL} and I_{OL} are measured with ODT disabled.

7.3 DC & AC Logic Input Levels

7.3.1 DC & AC Logic Input Levels (0 °C ≤ T_c ≤ 105 °C)

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Input logic high voltage, DC	V_{IH}(DC)	V_{REF} + 0.15	—	V	1,2
Input logic low voltage, DC	V_{IL}(DC)	—	V_{REF} -0.15	V	1,2
Input logic high voltage, AC	V_{IH}(AC)	V_{REF} + 0.25	—	V	1,3,4
Input logic low voltage, AC	V_{IL}(AC)	—	V_{REF} - 0.25	V	1,3,4
Input logic high, DC, RESET pin	V_{IHR}(DC)	0.65 × V_{DDQ}	V_{DDQ} + 0.3	V	
Input logic low, DC, RESET pin	V_{ILR}(DC)	-0.3	0.35 × V_{DDQ}	V	
Input Logic High, DC, MF pin	V_{IHMF}(DC)	V_{DD}	V_{DD} + 0.3	V	5
Input Logic Low,DC, MF pin	V_{ILMF}(DC)	–0.3	0	V	

Notes :

1. for 1.8 V V_{DD}/V_{DDQ} power supply.
2. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level.
3. Input slew rate = 3 V/ns. If the input slew rate is less than 3 V/ns, input timing may be compromised. All slew rates are measured between V_{IL}(AC) and V_{IH}(AC).
4. V_{IH} overshoot: V_{IH}(max) = V_{DDQ}+0.5V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate. V_{IL} undershoot: V_{IL}(min) = 0 V for a pulse width ≤ 500ps and the pulse width cannot be greater than 1/3 of the cycle rate.
5. The MF pin must be hard-wired on board to either V_{DD} or V_{SS}.

7.4 Differential Clock DC and AC Levels

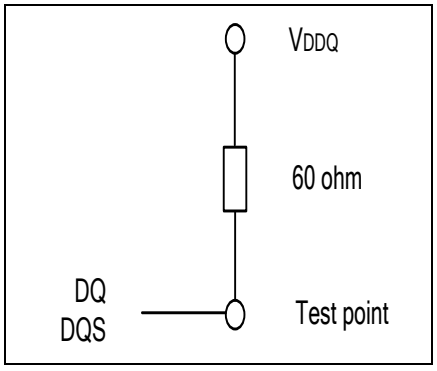
7.4.1 Differential Clock DC and AC Input conditions (0 °C ≤ T_c ≤ 105°C)

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Clock Input Mid-Point Voltage, CLK and CLK#	V_{MP}(DC)	0.7 × V_{DDQ} – 0.10	0.7 × V_{DDQ} + 0.10	V	1
Clock Input Voltage Level, CLK and CLK#	V_{IN}(DC)	0.42	V_{DDQ} + 0.3	V	1,2
Clock DC Input Differential Voltage, CLK and CLK#	V_{ID}(DC)	0.3	V_{DDQ}	V	1
Clock AC Input Differential Voltage, CLK and CLK#	V_{ID}(AC)	0.5	V_{DDQ} + 0.5	V	1,2,3
AC Differential Crossing Point Input Voltage	V_{IX}(AC)	0.7 × V_{DDQ} – 0.15	0.7 × V_{DDQ} + 0.15	V	1,2,4

Notes :

1. All voltages referenced to $V_{SS.}$
2. for 1.8 V V_{DD}/V_{DDQ} power supply.
3. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on CLK#.
4. The value of V_{IX} is expected to equal 0.7 × V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

7.5 Output Test Conditions



7.6 Pin Capacitances

7.6.1 Pin Capacitances (VDDQ = 1.8 V, TA = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit	Note
Input capacitance: A0-A11,A12, , BA0-2, CKE, CS#, CAS#, RAS#, WE#, CKE, RES,CLK,CLK#	CI,CCK	1.0	2.5	pF	
Input capacitance: DQ0-DQ31, RDQS0-RDQS3, WDQS0-WDQS3, DM0-DM3	CIO	2.0	3.0	pF	

7.7 Driver current characteristics

7.7.1 Driver IV characteristics at 40 Ohms

Figure represents the driver Pull-Down and Pull-Up IV characteristics under process, voltage and temperature best and worst case conditions. The actual Driver Pull-Down and Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal driver output impedance to 40 Ω.

7.7.1.1 40 Ohm Driver Pull-Down and Pull-up Characteristics

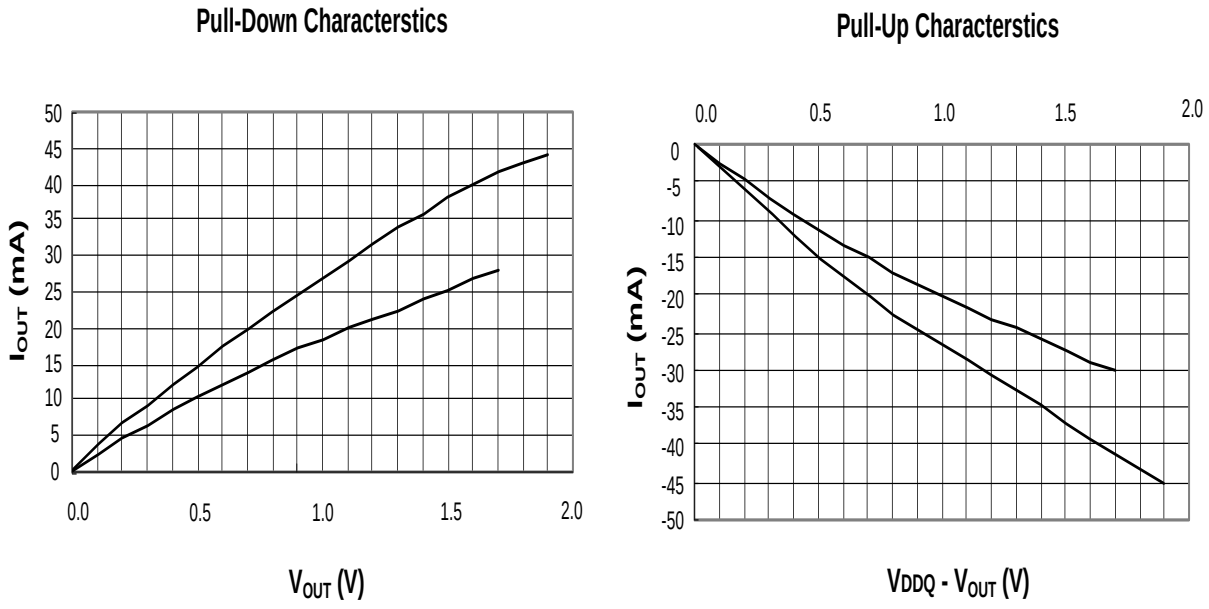


Table lists the numerical values of the minimum and maximum allowed values of the output driver Pull-Down and Pull-Up IV characteristics.

7.7.1.2 Programmed Driver IV Characteristics at 40 Ohm

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Minimum	Maximum	Minimum	Maximum
0.1	2.32	3.04	-2.44	-3.27
0.2	4.56	5.98	-4.79	-6.42
0.3	6.69	8.82	-7.03	-9.45
0.4	8.74	11.56	-9.18	-12.37
0.5	10.70	14.19	-11.23	-15.17
0.6	12.56	16.72	-13.17	-17.83
0.7	14.34	19.14	-15.01	-20.37
0.8	16.01	21.44	-16.74	-22.78
0.9	17.61	23.61	-18.37	-25.04
1.0	19.11	26.10	-19.90	-27.17
1.1	20.53	28.45	.21.34	-29.17
1.2	21.92	30.45	-22.72	-31.25
1.3	23.29	32.73	-24.07	-33.00
1.4	24.65	34.95	-25.40	-35.00
1.5	26.00	37.10	-26.73	-37.00
1.6	27.35	39.15	-28.06	-39.14
1.7	28.70	41.01	-29.37	-41.25
1.8	30.08	42.53	-30.66	-43.29
1.9	—	43.71	—	-45.23
2.0	—	44.89	—	-47.07

7.8 Termination current characteristics

7.8.1 Termination IV Characteristic at 60 Ohms

Figure represents the DQ termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual DQ termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal DQ termination impedance to 60 Ω. (Extended Mode Register programmed to ZQ/4).

7.8.1.1 60 Ohm Active Termination Characteristic

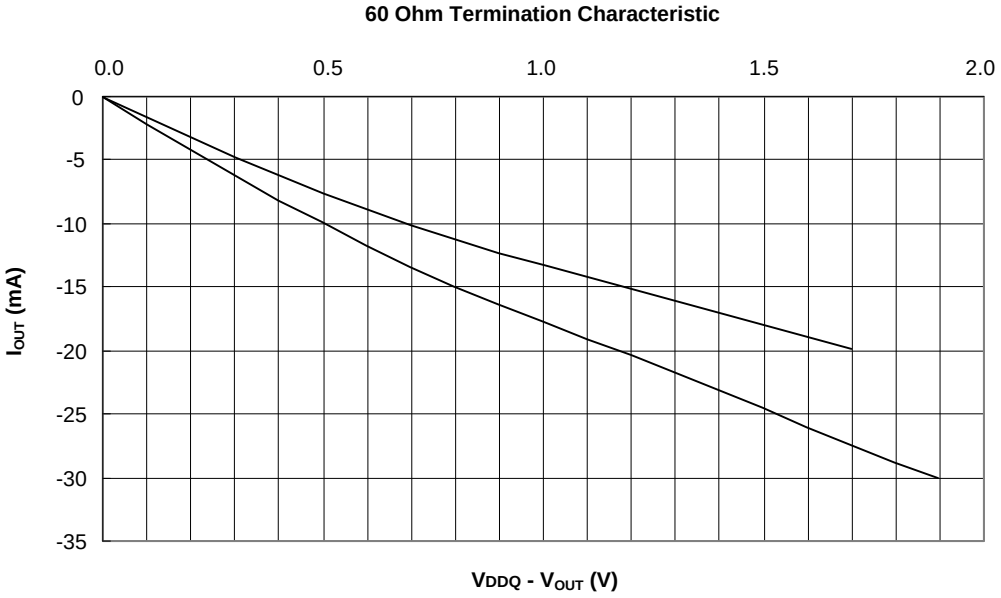


Table lists the numerical values of the minimum and maximum allowed values of the output driver termination IV characteristic.

7.8.1.2 Programmed Terminator Characteristics at 60 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
0.1	-1.63	-2.18		1.1	-14.23	-19.45
0.2	-3.19	-4.28		1.2	-15.14	-20.83
0.3	-4.69	-6.30		1.3	-16.04	-22.00
0.4	-6.12	-8.25		1.4	-16.94	-23.33
0.5	-7.49	-10.11		1.5	-17.82	-24.67
0.6	-8.78	-11.89		1.6	-18.70	-26.09
0.7	-10.01	-13.58		1.7	-19.58	-27.50
0.8	-11.16	-15.19		1.8	-20.44	-28.86
0.9	-12.25	-16.69		1.9	—	-30.15
1.0	-13.27	-18.11		2.0	—	-31.38

7.8.2 Termination IV Characteristic at 120 Ohms

Figure represents the DQ or ADD/CMD termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal termination impedance to 120 Ω. (Extended Mode Register programmed to ZQ/2 for DQ terminations or CKE = 0 at the RES transition during Power-Up for ADD/CMD terminations).

7.8.2.1 120 Ohm Active Termination Characteristic

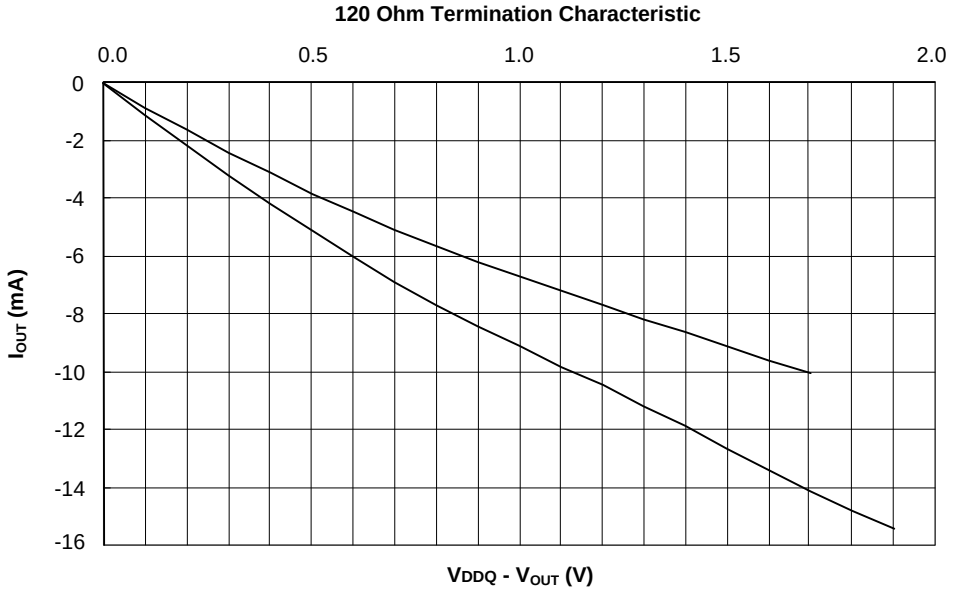


Table lists the numerical values of the minimum and maximum allowed values of the termination IV characteristic.

7.8.2.2 Programmed Terminator Characteristics of 120 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
0.1	-0.81	-1.09		1.1	-7.11	-9.72
0.2	-1.60	-2.14		1.2	-7.57	-10.42
0.3	-2.34	-3.15		1.3	-8.02	-11.00
0.4	-3.06	-4.12		1.4	-8.47	-11.67
0.5	-3.74	-5.06		1.5	-8.91	-12.33
0.6	-4.39	-5.94		1.6	-9.35	-13.05
0.7	-5.00	-6.79		1.7	-9.79	-13.75
0.8	-5.58	-7.59		1.8	-10.22	-14.43
0.9	-6.12	-8.35		1.9	—	-15.08
1.0	-6.63	-9.06		2.0	—	-15.69

7.8.3 Termination IV Characteristic at 240 Ohms

Figure represents the ADD/CMD termination Pull-Up IV characteristic under process, voltage and temperature best and worst case conditions. The actual ADD/CMD termination Pull-Up current must lie between these two bounding curves. The value of the external ZQ resistor is 240 Ω, setting the nominal termination impedance to 240 Ω. (CKE = 1at the RES transition during Power-Up for ADD/CMD terminations).

7.8.3.1 240 Ohm Active Termination Characteristic

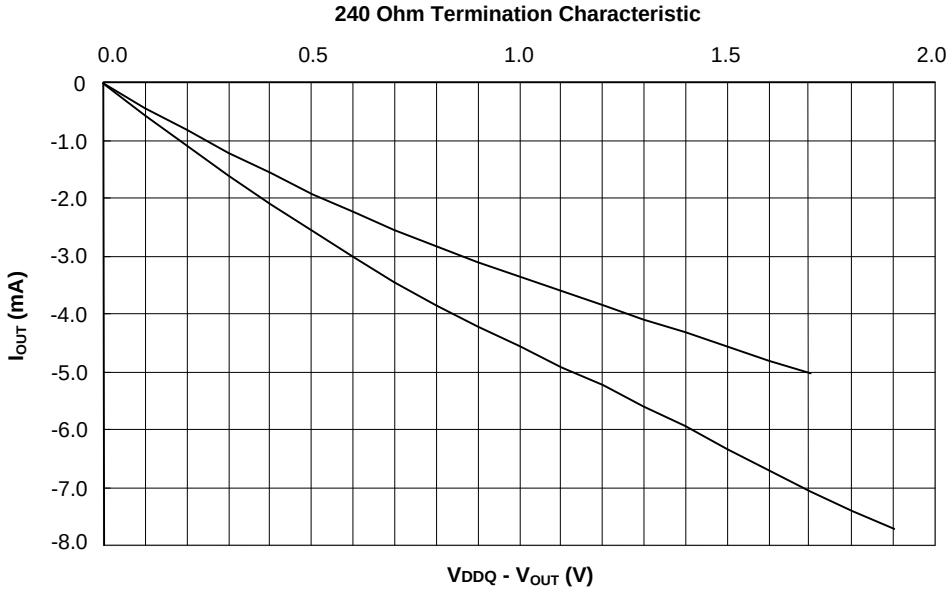


Table lists the numerical values of the minimum and maximum allowed values of the ADD/CMD termination IV characteristic.

7.8.3.2 Programmed Terminator Characteristics at 240 Ohm

Voltage (V)	Terminator Pull-Up Current (mA)			Voltage (V)	Terminator Pull-Up Current (mA)	
	Minimum	Maximum			Minimum	Maximum
0.1	-0.41	-0.55		1.1	-3.56	-4.86
0.2	-0.80	-1.07		1.2	-3.79	-5.21
0.3	-1.17	-1.58		1.3	-4.01	-5.50
0.4	-1.53	-2.06		1.4	-4.23	-5.83
0.5	-1.87	-2.53		1.5	-4.46	-6.17
0.6	-2.20	-2.97		1.6	-4.68	-6.52
0.7	-2.50	-3.40		1.7	-4.90	-6.88
0.8	-2.79	-3.80		1.8	-5.11	-7.21
0.9	-3.06	-4.17		1.9	—	-7.54
1.0	-3.32	-4.53		2.0	—	-7.85

7.9 Operating Current Ratings

SYM.	PARAMETER/CONDITION	TYP.			UNIT	NOTES
		650	700	800		
I_{DD0}	**One Bank Activate Precharge Current:** tCK = tCK(min); tRC = tRC(min); CKE = HIGH; data bus inputs are SWITCHING; address and command inputs are SWITCHING; /CS is HIGH between valid commands	320	335	360	mA	
I_{DD1}	**One Bank Activate Read Precharge Current:** tCK= tCK(min); tRC = tRC(min); CKE = HIGH; 1 bank activated; single read burst with data bus SWITCHING, address and command inputs are SWITCHING; /CS is High between valid commands; Iout = 0mA	330	345	380	mA	2
I_{DD2P}	**Precharge Power-Down Current:** tCK = tCK(min); all banks idle; CKE = LOW; all other inputs are HIGH	140	150	160	mA	
I_{DD2N}	**Precharge Standby Current in Non Power-down mode.**	190	200	220	mA	
I_{DD3N}	**Active Standby Current:** tCK = tCK(min); 1 bank active; CKE = HIGH; all other inputs are HIGH	285	300	330	mA	
I_{DD4R}	**Burst Read Current:** tCK = tCK(min); CKE = HIGH; continuous read burst across banks with data bus SWITCHING; address and command inputs are SWITCHING; Iout = 0 mA	495	520	550	mA	2
I_{DD4W}	**Write Burst Current:** tCK = tCK(min); CKE = HIGH; continuous write burst across banks with data bus SWITCHING; address and command inputs are SWITCHING	495	520	550	mA	
I_{DD5D}	**Auto Refresh current at tREFI.**	380	400	435	mA	
I_{DD6}	**Self Refresh Current:** CKE = LOW; all other inputs are HIGH	40	40	40	mA	

Notes:
1. IDD specifications are tested after the device is properly initialized.
2. Measured with open outputs and ODT off.
3. LOW is defined as inputs stable at VIL(max).
   HIGH is defined as inputs stable at VIH(min).
   SWITCHING is defined as inputs changing between HIGH and LOW every clock cycle for address and command inputs, and inputs changing with 50% of each data transfer for DQ.

7.10 AC Timings

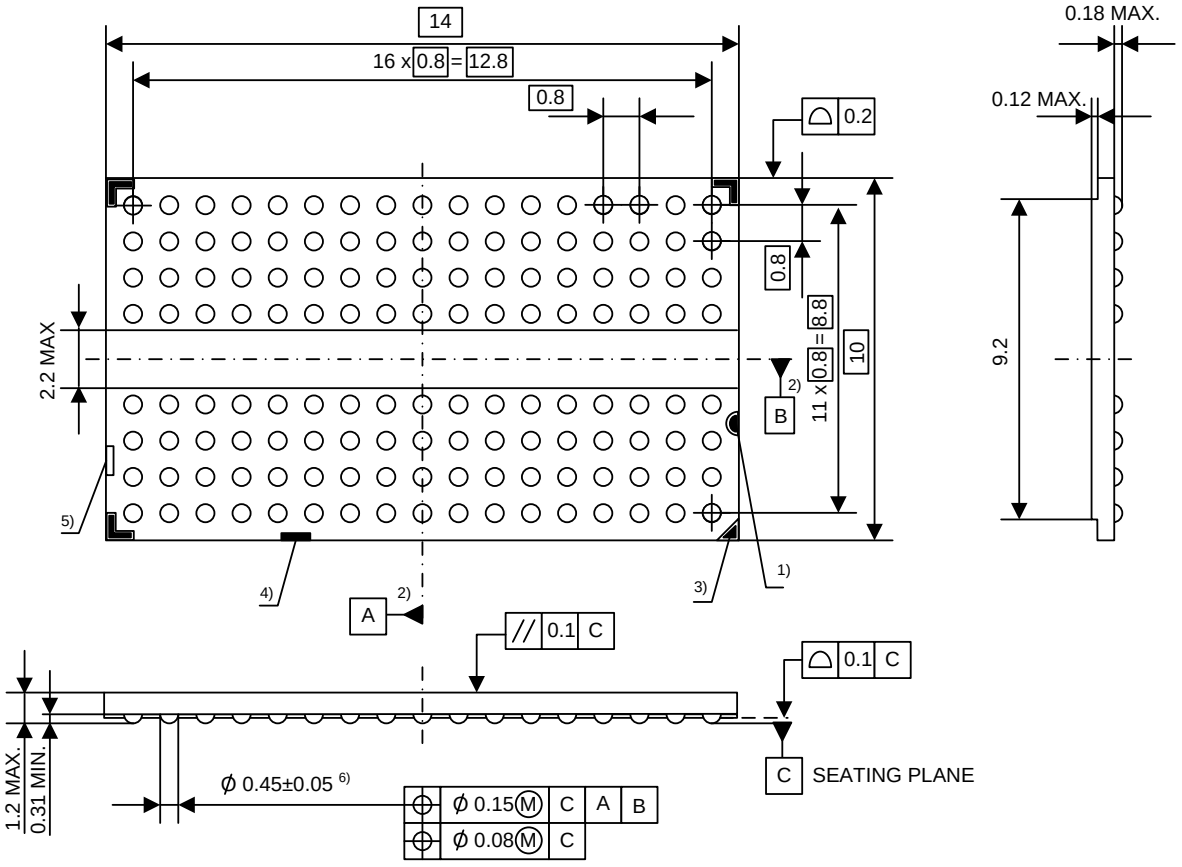
Parameter	CAS latency	Symbol	Limit Values						Unit	Note
			650		700		800		MHz	
			min	max	min	max	min	max		
Clock and Clock Enable										
System frequency	CL =11	f_{CK11}	—	—	450	700	—	—	MHz	1
	CL =10	f_{CK10}	—	—	450	700	450	800	MHz	1
	CL = 9	f_{CK9}	450	650	—	—	—	—	MHz	1
Clock cycle to cycle period jitter		$t_{JIT(cc)}$	0.06		0.06		0.06		t_{CK}	2,3
Clock high level width		t_{CH}	0.45	—	0.45	—	0.45	—	t_{CK}	2,3,4
Clock low level width		t_{CL}	0.45	—	0.45	—	0.45	—	t_{CK}	2,3,4
Minimum clock half period		t_{HP}	0.45	—	0.45	—	0.45	—	t_{CK}	3
Command and Address Setup and Hold Timing										
Address/Command input setup time		t_{IS}	0.35	—	0.35	—	0.35	—	ns	5,6
Address/Command input hold time		t_{IH}	0.35	—	0.35	—	0.35	—	ns	5,6
Address/Command input pulse width		t_{IPW}	0.7	—	0.7	—	0.7	—	t_{CK}	4
Mode Register Set Timing										
Mode Register Set cycle time		t_{MRD}	6	—	6	—	6	—	t_{CK}	7,8
Mode Register Set to READ timing		t_{MRDR}	12	—	12	—	12	—	t_{CK}	7
Row Timing										
Row Cycle Time		t_{RC}	37	—	37	—	37	—	t_{CK}	
Row Active Time		t_{RAS}	27	—	27	—	27	—	t_{CK}	9
ACT(a) to ACT(b) Command period		t_{RRD}	7	—	7	—	8	—	t_{CK}	
ACT(a) to ACT(b) Command period (different rank)		t_{RRD_RR}	1	—	1	—	1	—	t_{CK}	12
Row Precharge Time		t_{RP}	12	—	12	—	14	—	t_{CK}	
Row to Column Delay Time for Reads		t_{RCDRD}	11	—	11	—	13	—	t_{CK}	
Row to Column Delay Time for Writes		t_{RCDWR}	9	—	9	—	9	—	t_{CK}	
Four Active Windows within Rank		t_{FAW}	35	—	35	—	35	—	t_{CK}	
Column Timing										
CAS(a) to CAS(b) Command period		t_{CCD}	BL/2	—	BL/2	—	BL/2	—	t_{CK}	10
Internal write to Read Command Delay		t_{WTR}	6	—	6	—	6	—	t_{CK}	11
Write to Read Command Delay (different rank)		t_{WTR_RR}	1	—	1	—	1	—	t_{CK}	10
Write to Write Command Delay (different rank)		t_{WTW_RR}	2	—	2	—	2	—	t_{CK}	10
Read to Write command delay		t_{RTW}	$t_{RTW(min)}$ = CL + BL/2+ 2 - WL						t_{CK}	14
Read to Read Command Delay (different rank)		t_{RTR_RR}	2	—	2	—	2	—	t_{CK}	10
Write Cycle Timing Parameters for Data and Data Strobe										
Write command to first WDQS latching transition		t_{DQSS}	WL–0.25	WL+0.25	WL–0.25	WL+0.25	WL–0.25	WL+0.25	t_{CK}	

Parameter	CAS latency	Symbol	Limit Values						Unit	Note
			650		700		800		MHz	
			min	max	min	max	min	max		
Data-in and Data Mask to WDQS Setup Time		t_{DS}	0.18	—	0.18	—	0.18	—	ns	5,13
Data-in and Data Mask to WDQS Hold Time		t_{DH}	0.18	—	0.18	—	0.18	—	ns	5,13
Data-in and DM input pulse width (each input)		t_{DIPW}	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS input high pulse width		t_{DQSH}	0.40	—	0.40	—	0.40	—	t_{CK}	
DQS Write Preamble Time		t_{WPRE}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS Write Postamble Time		t_{WPST}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Write Recovery Time		t_{WR}	10	—	10	—	10	—	t_{CK}	11
Read Cycle Timing Parameters for Data and Data Strobe										
Data Access Time from Clock		t_{AC}	–0.25	0.25	–0.25	0.25	–0.25	0.25	ns	
Read Preamble		t_{RPRE}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	4
Read Postamble		t_{RPST}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Data-out high impedance time from CLK		t_{HZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
Data-out low impedance time from CLK		t_{LZ}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ns	
DQS edge to Clock edge skew		t_{DQSCK}	–0.25	0.25	–0.25	0.25	–0.25	0.25	ns	
DQS edge to output data edge skew		t_{DQSQ}	—	0.16	—	0.16	—	0.16	ns	15
Data hold skew factor		t_{QHS}	—	0.16	—	0.16	—	0.16	ns	
Data output hold time from DQS		t_{QH}	t_{HP}–t_{QHS}						ns	
Refresh/Power Down Timing										
Refresh Period (8192 cycles)		t_{REF}	—	32	—	32	—	32	ms	
Average periodic Auto Refresh interval		t_{REFI}	3.9		3.9		3.9		µs	
Delay from AREF to next ACT/ AREF		t_{RFC}	59	—	59	—	59	—	ns	
Self Refresh Exit time		t_{XSC}	1000	—	1000	—	1000	—	t_{CK}	
Power Down Exit time		t_{XPN}	6	—	6	—	6	—	t_{CK}	
Other Timing Parameters										
RES to CKE setup timing		t_{ATS}	10	—	10	—	10	—	ns	
RES to CKE hold timing		t_{ATH}	10	—	10	—	10	—	ns	
Termination update Keep Out timing		t_{KO}	10	—	10	—	10	—	ns	
Rev. ID EMRS to DQ on timing		t_{RIDon}	—	20	—	20	—	20	ns	
REV. ID EMRS to DQ off timing		t_{RIDoff}	—	20	—	20	—	20	ns	

1. f_{CK}(min), f_{CK}(max) for DLL on mode.
2. CLK and CLK# input slew rate must be greater than 3 V/ns.
3. t_{HP} is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CLK,CLK# inputs.
4. Timing is calculated for a clock frequecy of 700 MHz.
5. The input reference level for signals other than CLK and CLK# is V_{REF}.
6. Command/Address input slew rate = 3 V/ns. If the slew rate is less than 3 V/ns, timing is no longer referenced to the midpoint but to the $V_{il(AC)}$ maximum and $V_{iH(AC)}$ minimum points .
7. This value of t_{MRD} applies only to the case where the "DLL reset"' bit is not activated.
8. t_{MRD} is defined from MRS to any other command then READ.
9. $t_{RAS,max}$ is 8*t_{REFi}.
10. t_{CCD} is either for gapless consecutive reads or gapless consecutive writes.
11. WTR and t_{WR} start at the first rising edge of CLK after the last valid (falling) WDQS edge of the slowest WDQS signal.
12. This parameter is defined for commands issued to rank m following rank n where m ≠ n. For all other type of access, standard timing parameters do apply.
13. DQ and DM input slew rates must not deviate from WDQS by more than 10 percent. If the DQ/DM/WDQS slew rate is less than 3 V/ns, timing is no longer referenced to the midpoint but to the $V_{il(AC)}$ maximum and $V_{iH(AC)}$ minimum points.
14. Please round up t_{RTW} to the next integer of t_{CK}.
15. This parameter is defined per byte.
16. tAC +/-290ps when VDDmax.
17. Input slew rate = 2.2V/ns. If tIS/tIH higher than 550ps.

8. PACKAGE SPECIFICATION

Package Outline TFBGA 136 (10x14 mm^2, ball pitch:0.8mm, Ø=0.45mm)



Lead free solder balls (green solder balls)
1) Bad unit marking (BUM) (light = good)
2) Middle of packages edges
3) Package orientation mark A1
4) SBA- fiducial (solder ball attach)
5) Bare core area
6) Solder ball diameter refers to post reflow conduction

9. ORDERING INFORMATION

PART NUMBER	DESCRIPTION
W641GG2JB-14	1Gb GDDR3 SDRAM

Note: For pad information of KGD, please contact sales representative.

10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01-001	03/28/2011	All	Product datasheet for customer.
A01-002	04/22/2011	32 93 102 103,104	Add tSAC value. Add Tcase . Add 800 Mhz in DC table. Add 800 Mhz in AC table.

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