Winbond Electronics Corp.

256K × 8 CMOS FLASH MEMORY

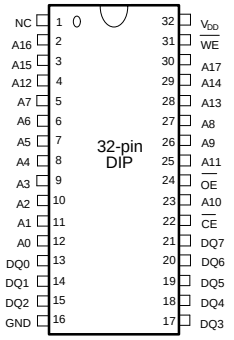
GENERAL DESCRIPTION

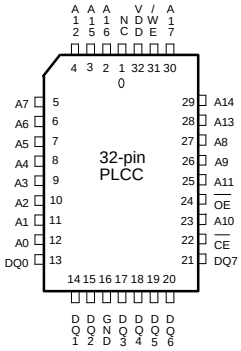
The W49F020 is a 2-megabit, 5-volt only CMOS flash memory organized as 256K × 8 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W49F020 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

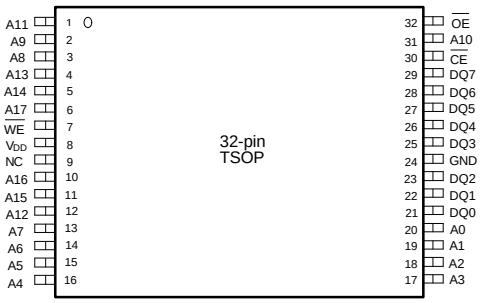
FEATURES

- Single 5-volt operations:
  - 5-volt Read
  - 5-volt Erase
  - 5-volt Program
- Fast Program operation:
  - Byte-by-Byte programming: 50 μS (max.)
- Fast Erase operation: 100 mS (typ.)
- Fast Read access time: 70/90 nS
- Endurance: 1K/10K cycles (typ.)
- Twenty-year data retention
- Hardware data protection
- One 8K byte Boot Block with Lockout protection
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic program and erase timing with internal V_{PP} generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin DIP and 32-pin TSOP and 32-pin-PLCC

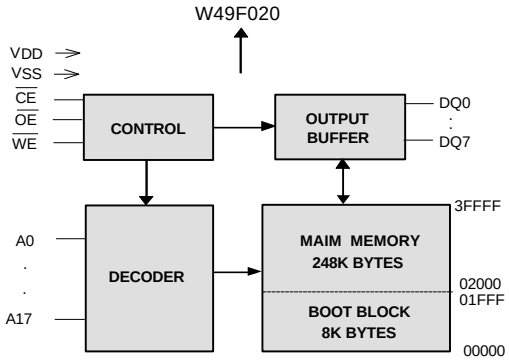
PIN CONFIGURATIONS







BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A17	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VDD	Power Supply
GND	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W49F020 is controlled by $\overline{CE}$ and $\overline{OE}$, both of which have to be low for the host to obtain data from the outputs. $\overline{CE}$ is used for device selection. When $\overline{CE}$ is high, the chip is de-selected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. Refer to the timing waveforms for further details.

Boot Block Operation

There is an 8K-byte boot block in this device, which can be used to store boot code. The boot block locates in the first 8K bytes of the memory with the address range from 0000(hex) to 1FFF(hex). For the specific code, please see Command Codes for Boot Block Lockout Enable.

When the boot block is enabled, data for the designated block cannot be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method. When the boot block programming lockout feature is activated, the chip erase function cannot erase the boot block any longer.

In order to detect whether the boot block feature is set on the 8K-bytes block or not, users can perform software command sequence to check it. First, enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 hex". If the output data is "1," the boot block programming lockout feature is activated; if the output data is "0," the lockout feature is inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-word command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Chip Erase Operation

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. If the boot block programming lockout is activated, only the data in the main memory blocks will be erased to FF(hex), and the data in the boot block will not be erased (remains same as before the chip erase operation). The entire memory array will be erased to FF hex by the chip erase operation if the boot block programming lockout feature is not activated. Once the boot block lockout feature is activated, the chip erase function erase the main memory block but not the boot block. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Program Operation

The W49F020 is programmed on a byte-by-byte basis. Program operation can only change logical data "1" to logical data "0." The erase operation (changed entire data in main memory blocks and/or boot block from "0" to "1") is needed before programming.

The program operation is initiated by a 4-word command cycle (see Command Codes for Byte Programming). The device will internally enter the program operation immediately after the byte-program command is entered. The internal program timer will automatically time-out (50 µS max. -

T_{BP}) when completing programming and return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W49F020 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A $\overline{WE}$ pulse with less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming operation is inhibited when V_{DD} is less than 2.5V typical.

(3) Write Inhibit Mode: Forcing $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ_7)- Write Status Detection

The W49F020 features a data polling function which used to indicate the end of a program or erase cycle. When the W49F020 is in the internal program or erase cycle, any attemption to read DQ_7 of the last word loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ_7 will show the true data. Note that DQ_7 will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has been completed.

Toggle Bit (DQ_6)- Write Status Detection

In addition to data polling, the W49F020 provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In software access mode, a three-word (or JEDEC 3-word) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code DA(hex); and a read from address 0001H outputs the device code 8C(hex) for W49F020. The product ID operation can be terminated by a three-word command sequence or an alternated one-word command sequence (see Command Definition table).

In the hardware access mode, access to the product ID will be activated by forcing $\overline{CE}$ and $\overline{OE}$ low, $\overline{WE}$ high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

(V_{HH} = 12V ± 5%)

MODE	PINS				
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	Din
Standby	V_{IH}	X	X	X	High Z
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}
	X	X	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Product ID	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}; A1–A17 = V_{IL}; A9 = V_{HH}	Manufacturer Code DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}; A1–A17 = V_{IL}; A9 = V_{HH}	Device Code 8C (Hex)

TABLE OF COMMAND DEFINITION

COMMAND DESCRIPTION	NO. OF Cycles	1ST CYCLE	2ND CYCLE	3RD CYCLE	4TH CYCLE	5TH CYCLE	6TH CYCLE
		Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data
Read	1	A_{IN} D_{OUT}					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Byte Program	4	5555 AA	2AAA 55	5555 A0	A_{IN} D_{IN}		
Boot Block Lockout	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit (1)	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit (1)	1	XXXX F0					

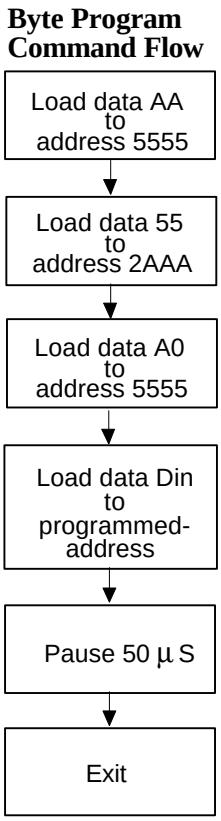
Notes:

1. Address Format: A14–A0 (Hex); Data Format: DQ7-DQ0 (Hex)
2. Either one of the two Product ID Exit commands can be used.

Command Codes for Byte Program

WORD SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	A0H
3 Write	Programmed-Address	Programmed-Data

Byte Program Flow Chart

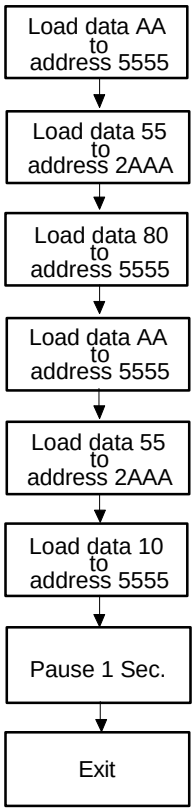


Notes for software program code:
Data Format: DQ7–DQ0 (Hex
Address Format: A14–A0 (Hex)

Command Codes for Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	10H

Chip Erase Acquisition Flow

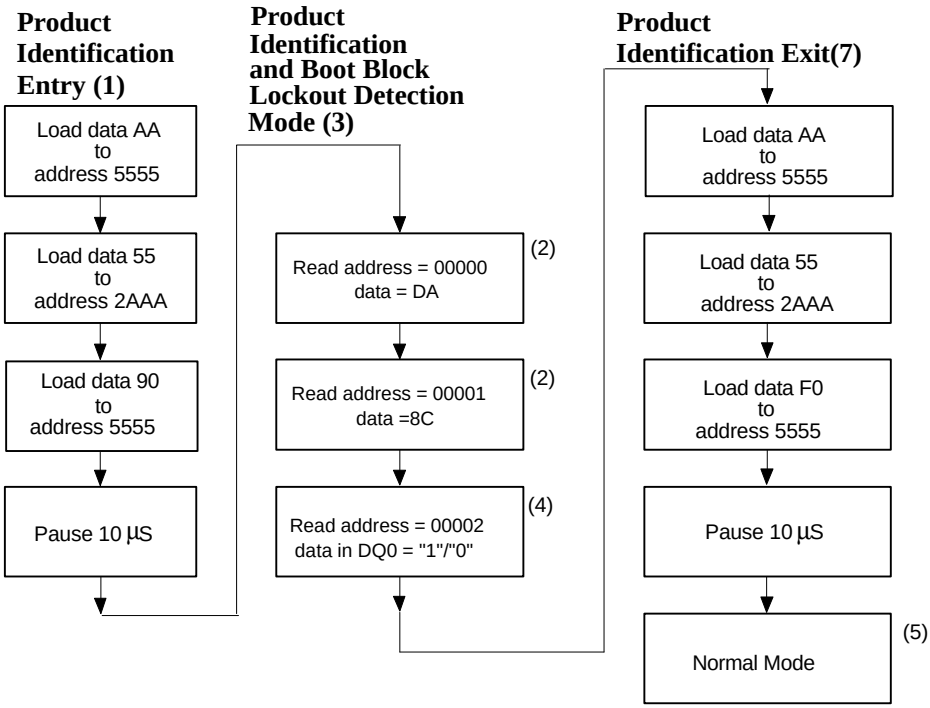


Notes for chip erase:
Data Format: DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

Command Codes for Product Identification and Boot Block Lockout Detection

BYTE SEQUENCE	ALTERNATE PRODUCT (6) IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT (7)	
	ADDRESS	DATA	ADDRESS	DATA
1 Write	5555	AA	5555H	AAH
2 Write	2AAA	55	2AAAH	55H
3 Write	5555	90	5555H	F0H
	Pause 10 µS		Pause 10 µS	

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)

(2) A1–A17 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) If the output data in DQ0= " 1," the boot block programming lockout feature is activated; if the output data in DQ0= " 0," the lockout feature is inactivated and the block can be programmed.

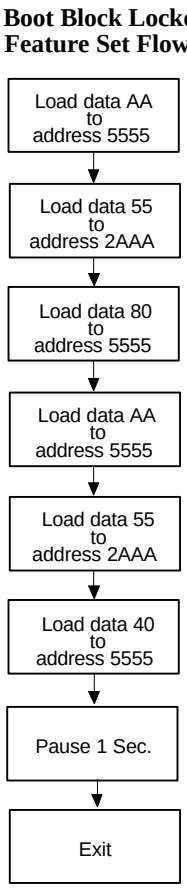
(5) The device returns to standard operation mode.

(6) Optional 1-word cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

Command Codes for Boot Block Lockout Enable

BYTE SEQUENCE	BOOT BLOCK LOCKOUT FEATURE SET	
	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	40H
	Pause 1 Sec.	

Boot Block Lockout Enable Acquisition Flow



Notes for boot block lockout enable:
Data Format: DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except $\overline{OE}$	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on $\overline{OE}$ Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, all DQs open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	25	50	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	$\overline{CE}$ = V_{IH}, all DQs open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	$\overline{CE}$ = V_{DD} -0.3V, all DQs open Other inputs = V_{DD} -0.3V/GND	-	20	100	µA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = GND to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	5	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

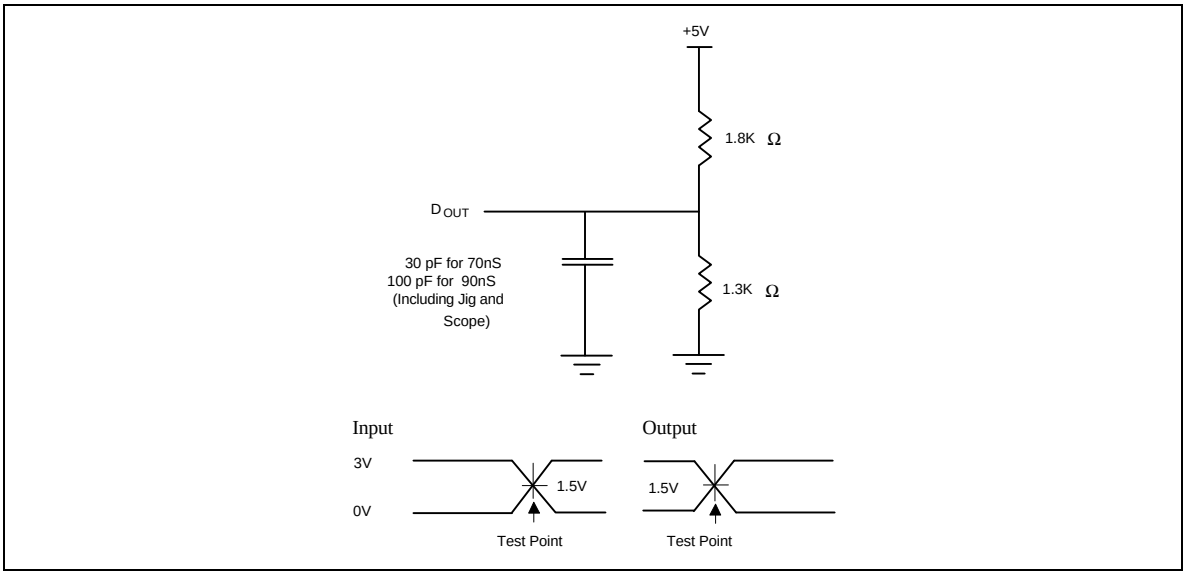
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 100 pF for 90nS C_L = 30 pF for 70nS

AC Test Load and Waveform



AC Characteristics, continued

Read Cycle Timing Parameters

(V_{CC} = 5.0V ±10%, V_{CC} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49F020-70		W49F020-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	90	-	nS
Chip Enable Access Time	T_{CE}	-	70	-	90	nS
Address Access Time	T_{AA}	-	70	-	90	nS
Output Enable Access Time	T_{OE}	-	35	-	40	nS
$\overline{CE}$ Low to Active Output	T_{CLZ}	0	-	0	-	nS
$\overline{OE}$ Low to Active Output	T_{OLZ}	0	-	0	-	nS
$\overline{CE}$ High to High-Z Output	T_{CHZ}	-	25	-	25	nS
$\overline{OE}$ High to High-Z Output	T_{OHZ}	-	25	-	25	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	nS

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	T_{AS}	0	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Setup Time	T_{CS}	0	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Hold Time	T_{CH}	0	-	-	nS
$\overline{OE}$ High Setup Time	T_{OES}	0	-	-	nS
$\overline{OE}$ High Hold Time	T_{OEH}	0	-	-	nS
$\overline{CE}$ Pulse Width	T_{CP}	100	-	-	nS
$\overline{WE}$ Pulse Width	T_{WP}	100	-	-	nS
$\overline{WE}$ High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	0	-	-	nS
Byte programming Time	T_{BP}	-	10	50	µS
Erase Cycle Time	T_{EC}	-	0.1	1	S

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

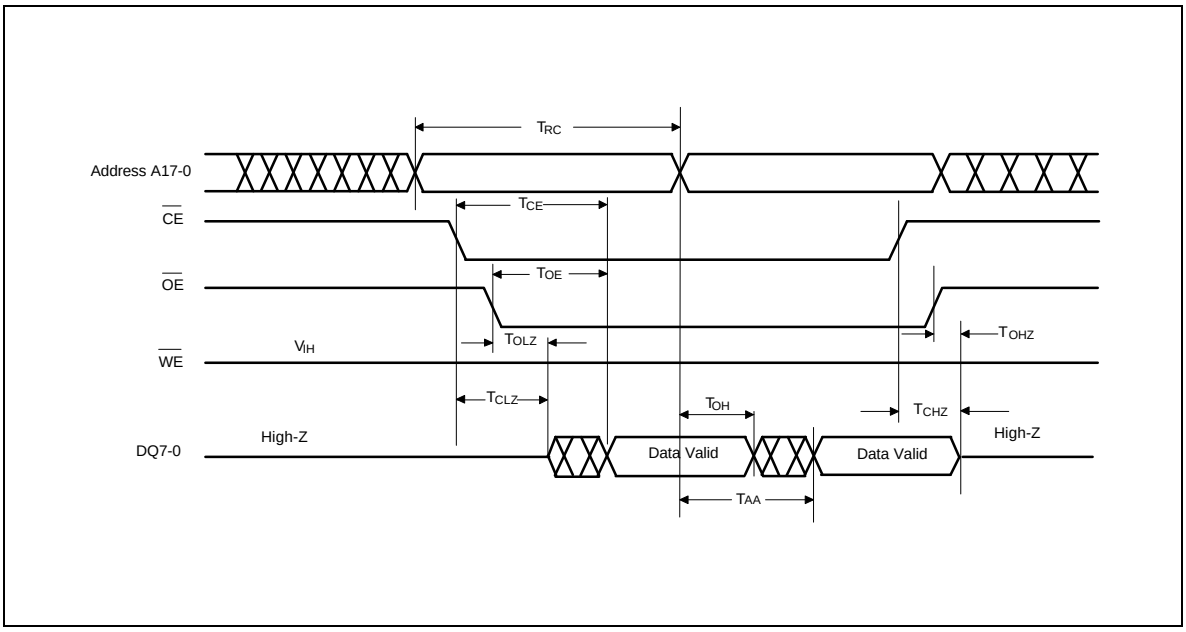
AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W49F020-70		W49F020-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
$\overline{OE}$ to Data Polling Output Delay	TOEP	-	35	-	40	nS
$\overline{CE}$ to Data Polling Output Delay	TCEP	-	70	-	90	nS
$\overline{OE}$ to Toggle Bit Output Delay	TOET	-	35	-	40	nS
$\overline{CE}$ to Toggle Bit Output Delay	TCET	-	70	-	90	nS

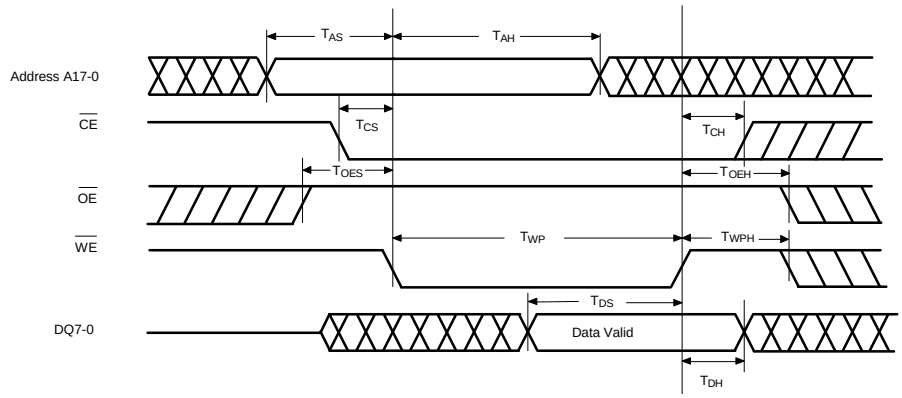
TIMING WAVEFORMS

Read Cycle Timing Diagram

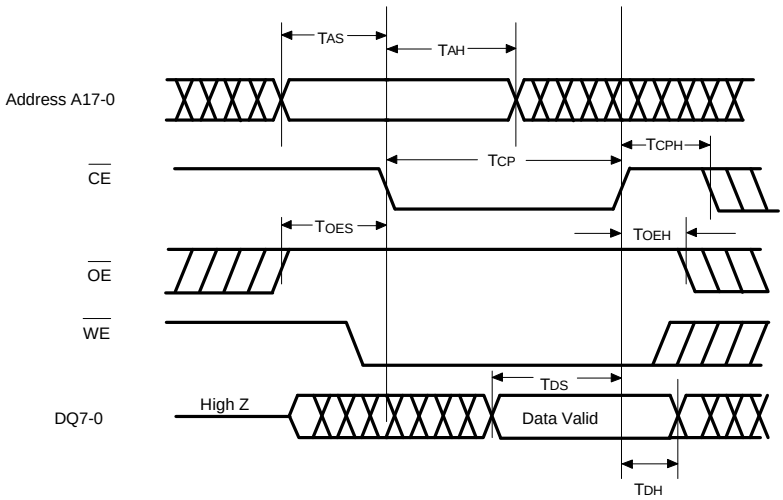


Timing Waveforms, continued

$\overline{WE}$ Controlled Command Write Cycle Timing Diagram

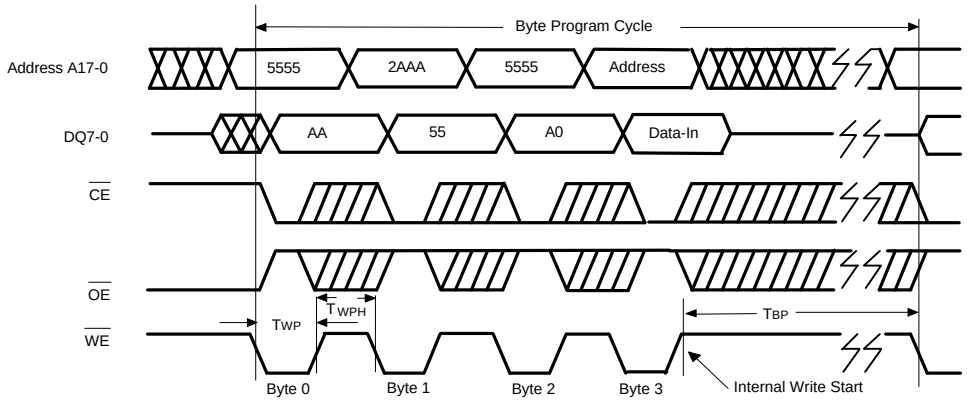


$\overline{CE}$ Controlled Command Write Cycle Timing Diagram

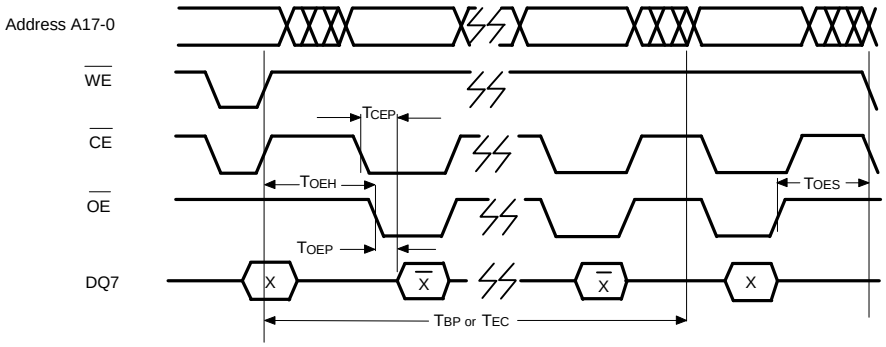


Timing Waveforms, continued

Program Cycle Timing Diagram

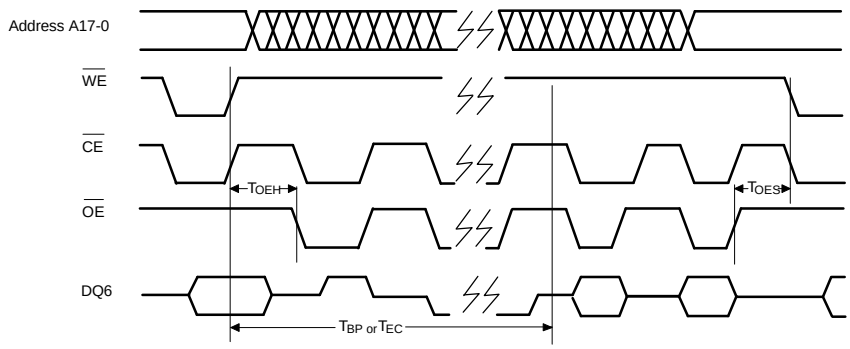


$\overline{\text{DATA}}$ Polling Timing Diagram

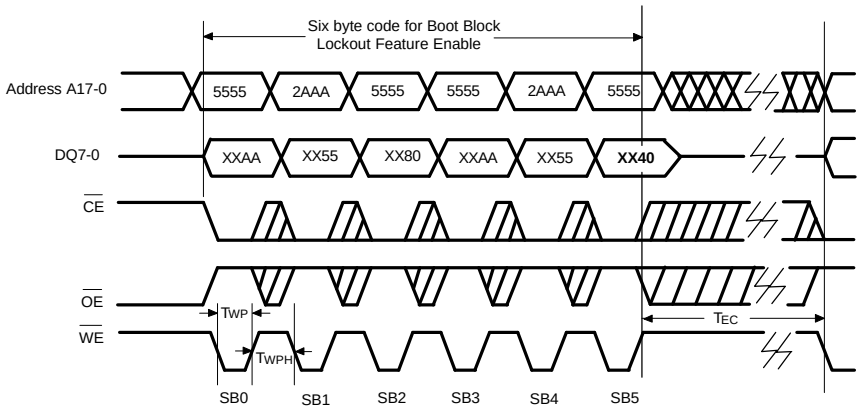


Timing Waveforms, continued

Toggle Bit Timing Diagram

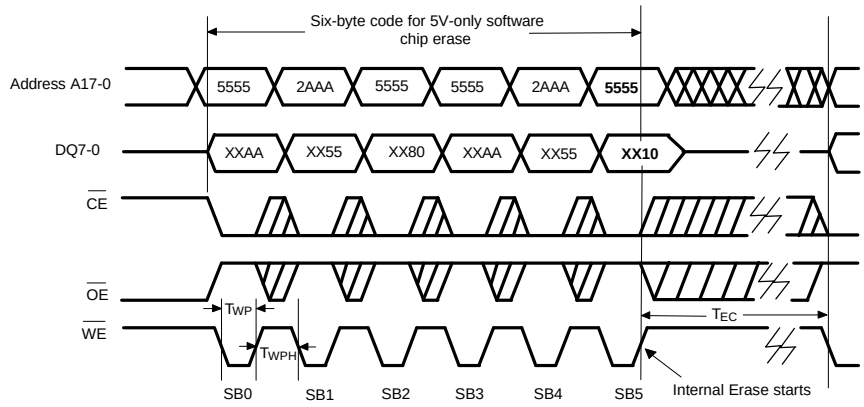


Boot Block Lockout Enable Timing Diagram



Timing Waveforms, continued

Chip Erase Timing Diagram



ORDERING INFORMATION

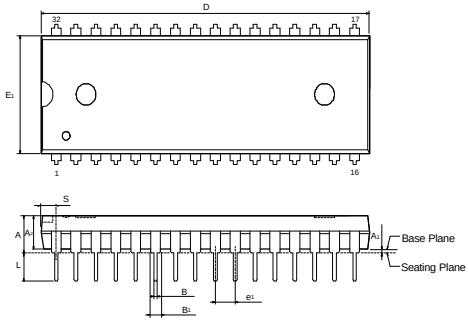
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (mA)	PACKAGE	CYCLE
W49F020-70	70	50	100 (CMOS)	32-pin DIP	1K
W49F020-90	90	50	100 (CMOS)	32-pin DIP	1K
W29F020Q-70	70	50	100 (CMOS)	32-pin TSOP (8 mm × 20 mm)	1K
W29F020Q-90	90	50	100 (CMOS)	32-pin TSOP (8 mm × 20 mm)	1K
W29F020P-70	70	50	100 (CMOS)	32-pin PLCC	1K
W29F020P-90	90	50	100 (CMOS)	32-pin PLCC	1K
W49F020-70B	70	50	100 (CMOS)	32-pin DIP	10K
W49F020-90B	90	50	100 (CMOS)	32-pin DIP	10K
W29F020Q-70B	70	50	100 (CMOS)	32-pin TSOP (8 mm × 20 mm)	10K
W29F020Q-90B	90	50	100 (CMOS)	32-pin TSOP (8 mm × 20 mm)	10K
W29F020P-70B	70	50	100 (CMOS)	32-pin PLCC	10K
W29F020P-90B	90	50	100 (CMOS)	32-pin PLCC	10K

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.
3. There are two kinds of boot block in this device. The part number shown in the Ordering Information table is only for Bottom Boot Block part, which is in the lower address range. For the requirement of the higher address range boot block, the Top Boot Block, please contact Winbond FAE for details.

PACKAGE DIMENSIONS

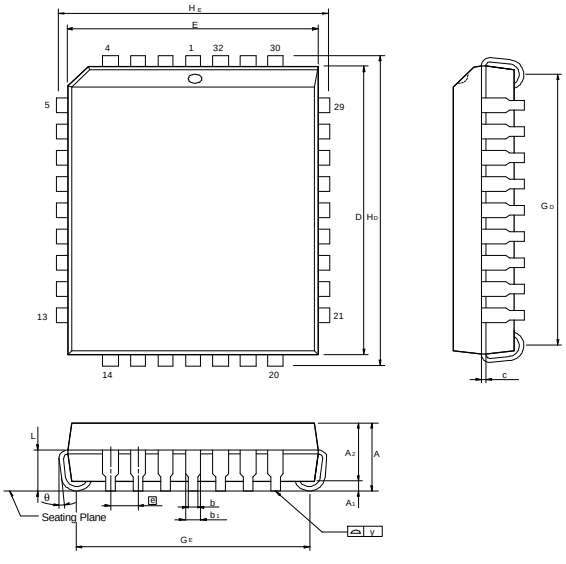
32-pin P-DIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:
1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be based on final visual inspection spec.

32-pin PLCC

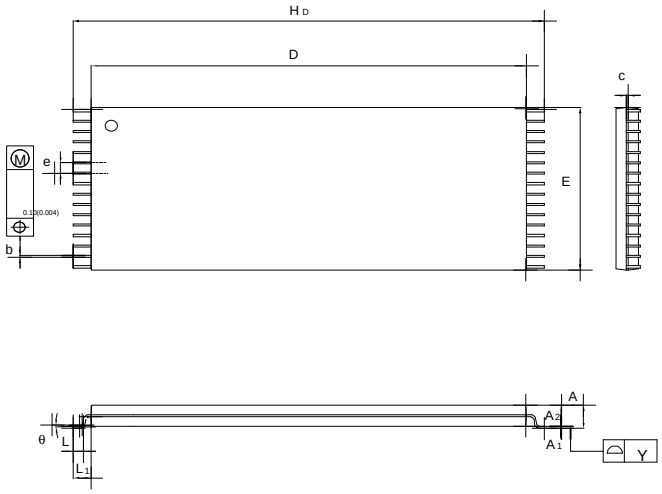


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.51	0.530	12.45	12.9	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.49	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection sepc.

Package Dimensions, continued

32-pin TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:
Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 1999	-	Initial Issued

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Note: All data and specifications are subject to change without notice.