W42C32-05

Spread Spectrum Frequency Timing Generator

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Generates a spread spectrum timing signal**
- **Reduces measured EMI by as much as 12 dB**
- **Integrated loop filter components**
- **Requires a single low-cost fundamental crystal (or other frequency reference) for proper operation**
- **Special spread spectrum control functions**
- **Low-power CMOS design**
- **Available in 16-pin SOIC package, (300 mil)**

Overview

The W42C32 modulates the output of a single PLL in order to 'spread' the bandwidth of a synthesized clock and, more importantly, decrease the peak amplitudes of its fundamental harmonics. Since peak amplitudes are reduced, the radiated electromagnetic emissions of the W42C32-05 are significantly lower than the typical narrow band signal produced by oscillators and most frequency generators. Lowering a signal's amplitude by increasing its bandwidth is a method of reducing EMI called 'spread spectrum frequency timing generation'. This patented technique not only reduces the emissions of the primary clock, but also impacts every signal synchronized to it.

Key Specifications

Cycle-to-Cycle Jitter ..... 250 ps

45/55 Duty Cycle ..... approximately 1.4V

Selectable Frequency spread

2 ns rise/fall time 0.4V to 2.0V, 3.3V supply

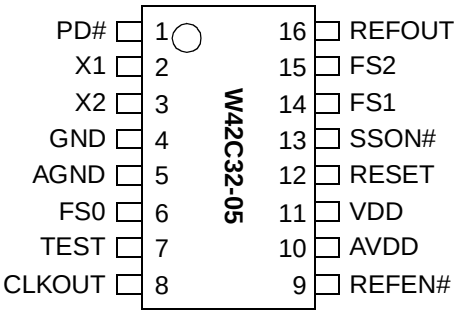
2 ns rise/fall time 0.8V to 2.4V, 5.0V supply

Table 1. Frequency Spread Selection

W42C32-05					
FS2	**FS1**	**FS0**	**REFOUT (MHz)**	**CLKOUT (MHz)**	**VDD (V)**
0	0	0	22.1148	44.2296 ± 2.5%	5.0
0	0	1	22.1148	44.2296 ±1.5%	5.0
0	1	0	14.7456	29.4912 ± 2.5%	5.0
0	1	1	18.432	18.432 ± 2.5%	5.0
1	0	0	14.318	66.66 – 2%	3.3
1	0	1	Reserved		3.3
1	1	0	14.318	100 – 2%	3.3
1	1	1	Reserved		3.3

Pin Configuration

SOIC



Pin Definitions[1]

Pin Name	Pin No.	Pin Type	Pin Description
CLKOUT	8	O	***Output Modulated Frequency**:* Frequency is set using FS0:2 (refer to *Table 1).*
REFOUT	16	O	***Reference Output:*** A buffered version of the input frequency.
X1	2	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as either an external crystal connection, or as an external reference frequency input.
X2	3	I	***Crystal Connection:*** If using an external reference, this pin must be left unconnected.
SSON#	13	I	***Spread Spectrum Control (active LOW):*** Pulling this input signal HIGH turns the internal modulating waveform off. This pin has an internal pull-down resistor.
FS0	6	I	***Frequency Selection Bit 0:*** This pin selects the frequency and spreading characteristics. Refer to *Table 1*. This pin has an internal pull-up resistor.
FS1	14	I	***Frequency Selection Bit 1:*** This pin selects the frequency and spreading characteristics. Refer to *Table 1*. This pin has an internal pull-up resistor.
FS2	15	I	***Frequency Selection Bit 2:*** This pin selects the frequency and spreading characteristics. Refer to *Table 1* (note the V_{DD} specification). This pin has an internal pull-up resistor.
PD#	1	I	***Power-down (active LOW):*** Enabling power-down reduces current consumption and disables the clock outputs. This pin has an internal pull-up resistor.
REFEN#	9	I	***Reference Clock Selection Input:*** Pulling this signal LOW turns the REFOUT clock output on. This pin has an internal pull-up resistor.
RESET	12	I	***Reset:*** A reset starts the spread spectrum modulating frequency at the beginning point of the modulation profile. This pin has an internal pull-down resistor. To reset the spread spectrum modulating frequency, pull this pin from LOW to HIGH.
VDD	11	P	***Power Connection:*** Connected to either 3.3V or 5.0V power supply. V_{DD} and AV_{DD} must be the same voltage level.
AVDD	10	P	***Analog Power Connection:*** Connected to either 3.3V or 5.0V power supply. V_{DD} and AV_{DD} must be the same voltage level.
GND	4	G	***Ground Connection:*** Connect to the common system ground plane.
AGND	5	G	***Analog Ground Connection:*** Connect to the common system ground plane.
TEST	7	I	***Three-state Input:*** Pulling this input pin and REFEN# pin HIGH, CLKOUT will be three-stated. This pin has an internal pull-down resistor.[2]

Notes:
1. Pull-up resistors not CMOS level.
2. Pulling PD# and REFEN# input pins HIGH, REFOUT will be three-stated.

Functional Description

The W42C32-05 uses a phase-locked loop (PLL) to multiply the frequency of a low-cost, low-frequency crystal up to the desired clock frequency. The basic circuit topology is shown in *Figure 1*. An on-chip crystal driver causes the crystal to oscillate at its fundamental. The resulting reference signal is divided by Q and fed to the phase detector. The VCO output is divided by P and also fed back to the phase detector. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency. The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

Frequency Selection With SSFTG

In Spread Spectrum frequency timing generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform in the W42C32 are fixed, the modulation percentage may be varied.

Using frequency select bits (FS2:0 pins), various spreading percentages for different input frequency ranges can be chosen. For example, refer to the W42C32-05 in *Table 1*. If the logic level on FS2:0 = 000, then an input reference frequency between 14 and 24 MHz will produce an output frequency at twice the reference frequency with a spread of ±2.5%.

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentages between ±0.875% and ±2.5% are most common.

Additional Features of the W42C32-05

A RESET pin is available to aid in applications which have multiple PLL clock generators. When a reset is issued, the modulation profile shown in *Figure 3* is reset to its starting point. This feature is necessary for applications in which two spread spectrum systems must synchronize with each other.

The REFOUT out pin provides a buffered version of the input clock frequency.

The SSON# pin disables the spread spectrum function when set to logic HIGH. Otherwise, an internal pull-down resistor leaves this feature enabled.

The PD# pin reduces power consumption and disables the clock outputs when set to logic LOW. Otherwise, an internal pull-up resistor places the W42C32-05 into normal mode.

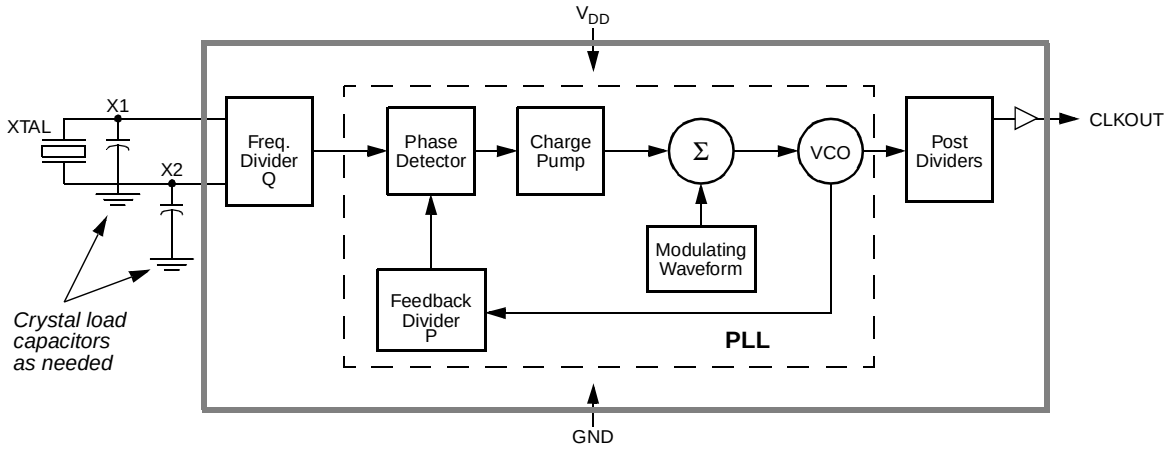


Figure 1. System Block Diagram (Concept, not actual implementation)

Spread Spectrum Frequency Timing Generation

The benefits of using Spread Spectrum Frequency Timing Generation are depicted in *Figure 2*. An EMI emission profile of a clock harmonic is shown.

Contrast the typical clock EMI with the Cypress spread spectrum clock. Notice the spike in the typical clock. This spike can make systems fail quasi-peak EMI testing. The FCC and other regulatory agencies test for peak emissions. With Cypress's Spread Spectrum Frequency Timing Generator (SSFTG), the peak energy is much lower (at least 8 dB) because the energy is spread out across a wider bandwidth.

Modulating Waveform

The shape of the modulating waveform is critical to EMI reduction. The modulation scheme used to accomplish the maximum reduction in EMI is shown in *Figure 3*. The period of the modulation is shown as a percentage of the period length along the X axis. The amount that the frequency is varied is shown along the Y axis, also shown as a percentage of the total frequency spread.

Cypress frequency selection tables express the modulation percentage in two ways. The first method displays the spreading frequency band as a percent of the programmed average output frequency, symmetric about the programmed average frequency. This method is always shown using the expression $f_{Center} \pm X_{MOD}\%$ in the frequency spread selection table.

The second approach is to specify the maximum operating frequency and the spreading band as a percentage of this frequency. The output signal is swept from the lower edge of the band to the maximum frequency. The expression for this approach is $f_{MAX} - X_{MOD}\%$. Whenever this expression is used, Cypress has taken care to ensure that f_{MAX} will never be exceeded. This is important in applications where the clock drives components with tight maximum clock speed specifications.

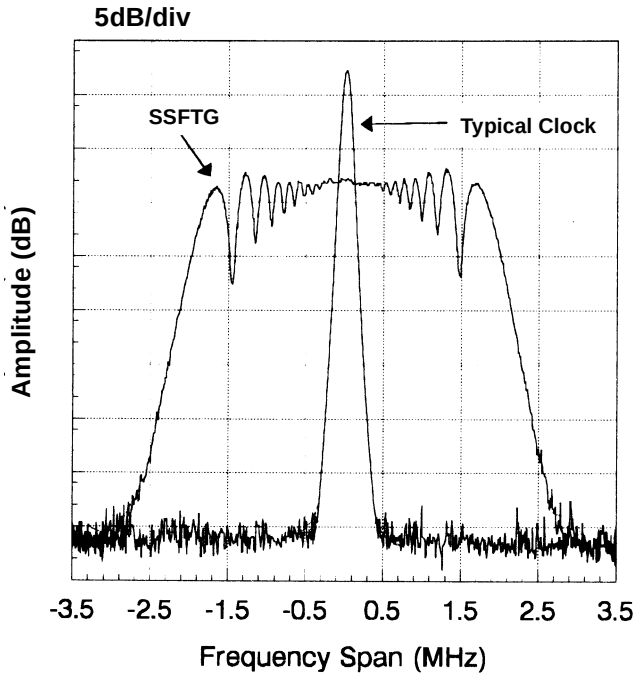


Figure 2. Typical Clock and SSFTG Comparison

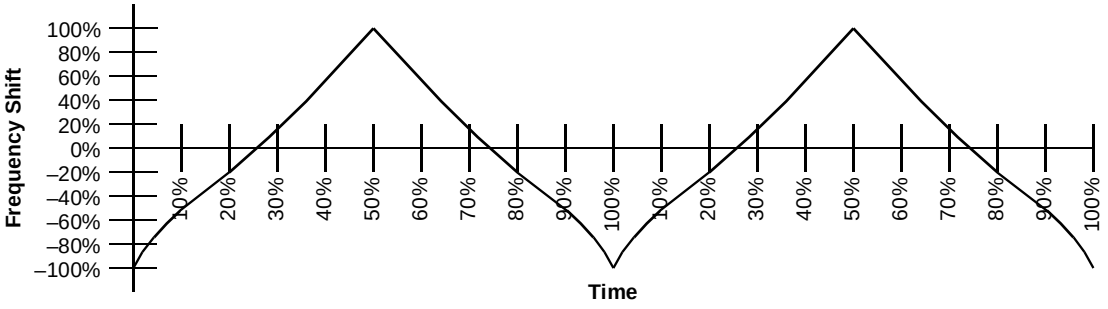


Figure 3. Modulation Waveform Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C

DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 5.0V \pm 10\%, 3.3V \pm 5\%$

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current	V_{DD} = 5.0, 100 MHz		35	45	mA
t_{OFF}	Power Down Time				4	cycles[3]
t_{ON}	Power Up Time	First locked clock cycle after PD# goes HIGH			5	ms
t_{EN}	Enable/Disable Time	Time required for output to be enabled/disabled			4	cycles[3]
V_{IL}	Input Low Voltage	V_{DD} = 5.0V			0.8	V
		V_{DD} = 3.3V			$0.15V_{DD}$	V
V_{IH}	Input High Voltage	V_{DD} = 5.0V	3.0			V
		V_{DD} = 3.3V	$0.7V_{DD}$			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage	V_{DD} = 5.0V	2.4			V
		V_{DD} = 3.3V	2.4			V
I_{IL}	Input Low Current				–100	µA
I_{IH}	Input High Current				10	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 3.3V		2.4		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 3.3V		2.4		mA
C_I	Input Capacitance	All pins except X1, X2			7	pF
C_L	XTAL Load Capacitance	Pins X1, X2			16	pF
R_P	Input Pull-Up Resistor	V_{IN} = 0V		300		kΩ
Z_{OUT}	Clock Output Impedance	Any clock output pin		33		Ω

Note:
3. Cycle refers to input clock cycles supplied by the input crystal or reference.

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 5V±10%. 3.3V±5%

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency		12		28	MHz
f_{OUT}	Output Frequency		18		100	MHz
t_R	Output Rise Time	15-pF load 0.4V–2.4V		1	2	ns
t_F	Output Fall Time	15-pF load 2.4V–0.8V		1	2	ns
t_{OD}	Output Duty Cycle	15-pF load, V_{DD} = 5.0V	45		55	%
t_{OD}	Output Duty Cycle	15-pF load, V_{DD} = 3.3V	40		60	%
t_{ID}	Input Duty Cycle		40		60	%
t_{JCYC}	Jitter, Cycle-to-Cycle			250	300	ps
	Harmonic Reduction	f_{in} = 16 MHz, ninth harmonic measured, reference board, 15-pF load		8		dB

Application Information

Recommended Circuit Configuration

For optimum performance in system applications the power supply decoupling scheme shown in *Figure 4* should be used.

V_{DD} decoupling is important to both reduce phase jitter and EMI radiation. The 0.1-µF decoupling capacitor should be placed as close to the V_{DD} pin as possible, otherwise the increased trace inductance will negate its decoupling capability.

The 10-µF decoupling capacitor shown should be a tantalum type. For further EMI protection, the V_{DD} connection can be made via a ferrite bead, as shown.

The 16-pF XTAL load capacitors can be used to raise the integrated 12-pF capacitors up to a total load of 20 pF on the crystal.

Recommended Board Layout

Figure 4 shows a recommended 2-layer board layout.

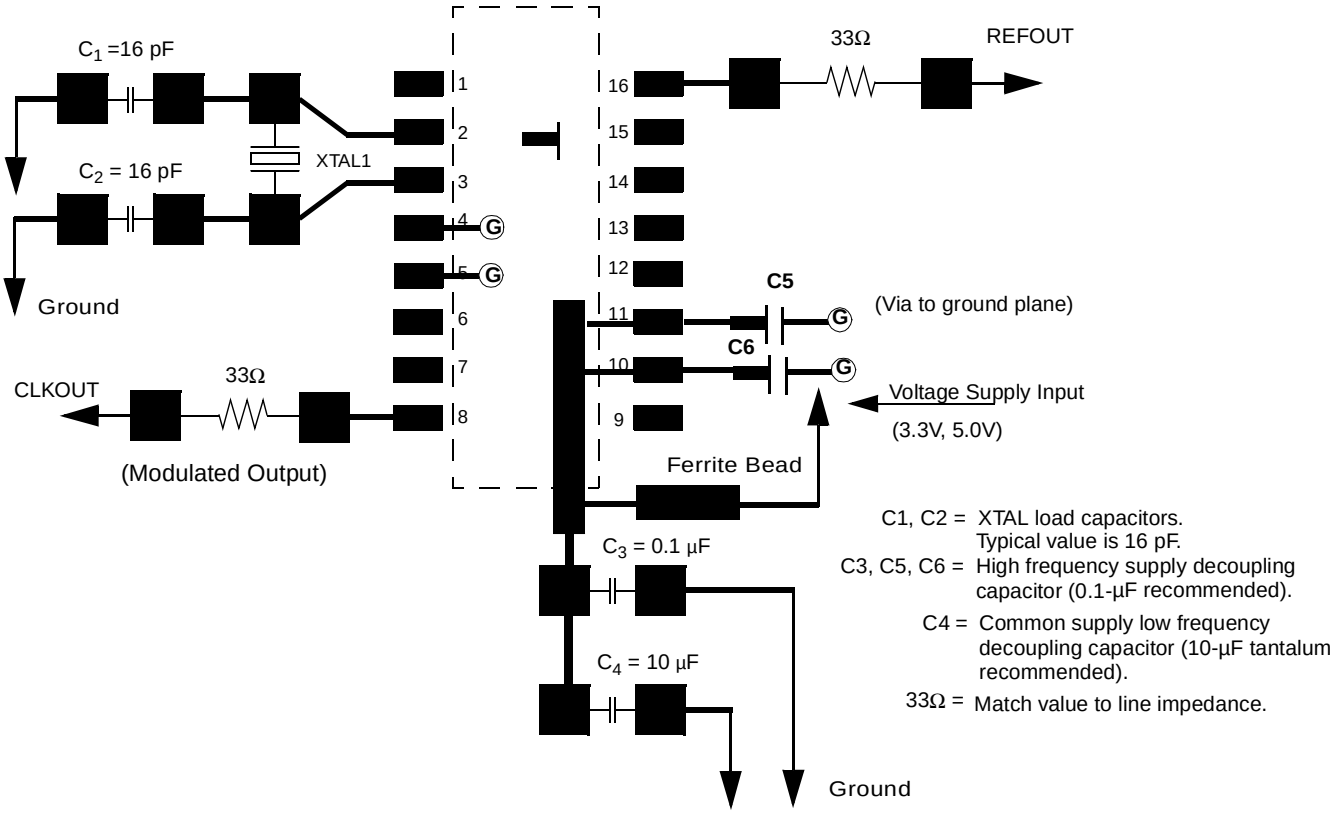


Figure 4. Recommended Board Layout (2-Layer Board)

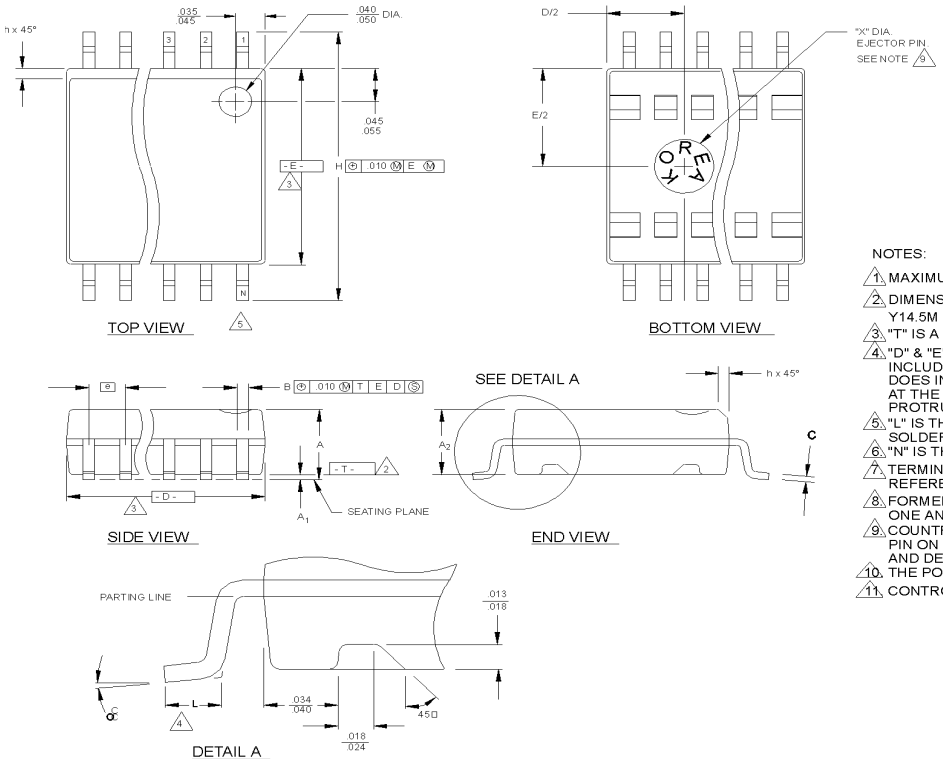
Ordering Information

Ordering Code	Freq. Mask Code	Package Name	Package Type
W42C32	05	G	16-pin Plastic SOIC (300-mil)

Document #: 38-00808

Package Diagram

16-Pin Small Outline Integrated Circuit (SOIC, 300-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCES PER ANSI. Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
10. THE POCKETS ON THE BOTTOM ARE OPTIONAL.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
∝	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
∝	0°	5°	8°						
X	2.16	2.36	2.54						

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