512MB – 2x32Mx72, SDRAM UNBUFFERED

FEATURES

- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- Power Supply: 3.3V ± 0.3V
- JEDEC Standard 168 Pin DIMM Package

DESCRIPTION

The W3DG7267V is organized as a 2x32Mx72 synchronous DRAM module which consists of eighteen 32Mx8 SDRAM components in TSOP II package, and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 168 Pin DIMM multilayer FR4 Substrate.

* This product is under development, is not qualified or characterized and is subject to change without notice.

NOTE: Consult factory for availability of:

- Lead-Free Products
- Vendor source control options
- Industrial temperature options

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	CS1#	142	DQ51
3	DQ1	31	DNU	59	Vcc	87	DQ33	115	RAS#	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF	90	Vcc	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DNU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	Vcc	101	DQ45	129	CS3#	157	Vcc
18	Vcc	46	DQM2	74	DQ28	102	Vcc	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DNU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	Vcc	54	Vss	82	**SDA	110	Vcc	138	Vss	166	**SA1
27	WE#	55	DQ16	83	**SCL	111	CAS#	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vcc	112	DQM4	140	DQ49	168	Vcc

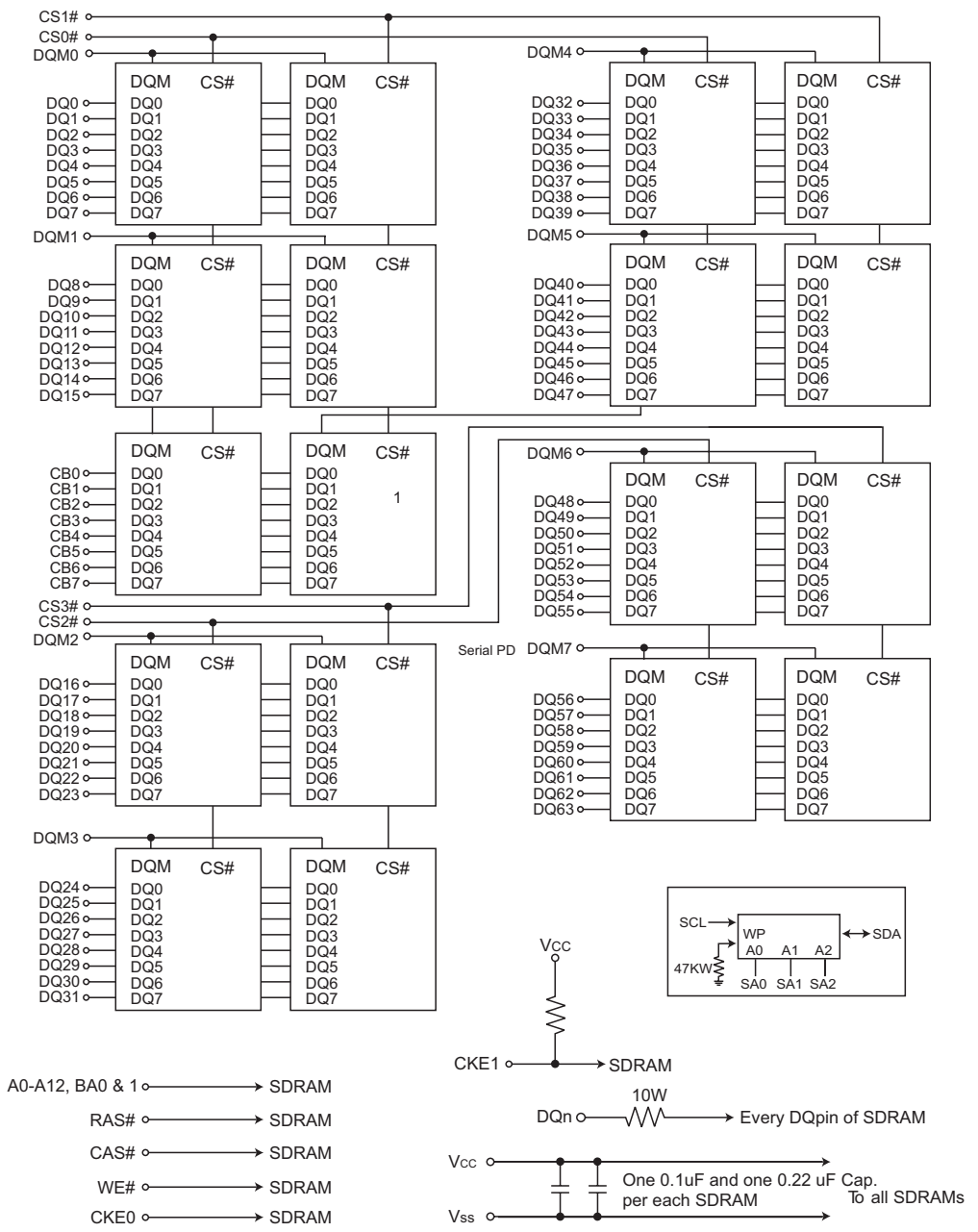
PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CB0-CB7	Check bit (Data-in/data-out)
CK0-CK3	Clock input
CKE0, CKE1	Clock Enable input
CS0#,CS3#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
Vcc	Power Supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0-2	Address in EEPROM
DNU	Do not use
NC	No Connect

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power Dissipation	P_D	18	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, 0°C ≤ T_A ≤ 70°

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{CCQ}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	2
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL}= -2mA
Input Leakage Current	I_{LI}	-10	—	10	µA	3

Note: 1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 25 °C, f = 1MHz, V_{CC} = 3.3V, V_{REF} = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	74	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	74	pF
Input Capacitance (CKE0)	C_{IN3}	74	pF
Input Capacitance (CLK0)	C_{IN4}	16	pF
Input Capacitance (CS0#,CS2#)	C_{IN5}	24	pF
Input Capacitance (DQM0-DQM7)	C_{IN6}	15	pF
Input Capacitance (BA0-BA1)	C_{IN7}	74	pF
Data input/output capacitance (DQ0-DQ63)	C_{OUT}	15	pF
Data input/output capacitance (CB0-CB7)	C_{OUT1}	15	pF

OPERATING CURRENT CHARACTERISTICS

V_{CC} = 3.3V, 0°C ≤ T_A ≤ 70°C

Parameters	Symbol	Conditions	Versions	Units	Note
			133/100		
Operating Current (One bank active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0mA	1620	mA	1
Precharge Standby Current in Power Down Mode	I_{CC2P}	$C_{KE} \leq V_{IL}$(max), t_{CC} = 10ns	36	mA	
	I_{CC2PS}	C_{KE} & CLK ≤ V_{IL}(max), t_{CC} = ∞	36	mA	
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	$C_{KE} \geq V_{IH}$(min), CS ≥ V_{IH}(min), t_{CC} =10ns Input signals are charged one time during 20	360	mA	
	I_{CC2NS}	$C_{KE} \geq V_{IH}$(min), CLK ≤ V_{IL}(max), t_{CC}= ∞ Input signals are stable	180	mA	
Active standby current in power-down mode	I_{CC3P}	$C_{KE} \geq V_{IL}$(max), t_{CC} = 10ns	108	mA	
	I_{CC3PS}	C_{KE} & CLK ≤ V_{IL}(max), t_{CC} = ∞	108		
Active standby in current non power-down mode	I_{CC3N}	$C_{KE} \geq V_{IH}$(min), CS ≥ V_{IH}(min), t_{CC} = 10ns Input signals are charged one time during 20ns	450	mA	
	I_{CC3NS}	$C_{KE} \geq V_{IH}$(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ input signals are stable	450	mA	
Operating current (Burst mode)	I_{CC4}	Io = mA Page burst 4 Banks activated t_{CCD} = 2CLK	2340	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3240	mA	2
Self refresh current	I_{CC6}	$C_{KE} \leq$ 0.2V	54	mA	

Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

V_{CC}, V_{CCQ} = +3.3V ±0.3V

AC CHARACTERISTICS			7		7.5		10			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
Access timefrom CLK (pos.edge)	CL = 3	$t_{AC(3)}$		5.4		5.4		6	ns	27
	CL = 2	$t_{AC(2)}$		5.4		6		6	ns	
Address hold time		t_{AH}	0.8		0.8		1		ns	
Address setup time		t_{AS}	1.5		1.5		2		ns	
CLK high-level width		t_{CH}	2.5		2.5		3		ns	
CLK low-level width		t_{CL}	2.5		2.5		3		ns	
Clock cycle time	CL = 3	$t_{CK(3)}$	7		7.5		8		ns	23
	CL = 2	$t_{CK(2)}$	7.5		10		10		ns	23
CKE hold time		t_{CKH}	0.8		0.8		1		ns	
CKE setup time		t_{CKS}	1.5		1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	0.8		0.8		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	1.5		1.5		2		ns	
Data-in hold time		t_{DH}	0.8		0.8		1		ns	
Data-in setup time		t_{DS}	1.5		1.5		2		ns	
Data-out high-impedance time	CL = 3	$t_{HZ(3)}$		5.4		5.4		6	ns	10
	CL = 2	$t_{HZ(2)}$		5.4		6		6	ns	10
Data-out low-impedance time		t_{LZ}	1		1		1		ns	
Data-out hold time (load)		t_{OH}	2.7		2.7		2.7		ns	
Data-out hold time (no load)		t_{OHN}	1.8		1.8		1.8		ns	28
ACTIVE to PRECHARGE command		t_{RAS}	37	120,000	44	120,000	50	120,000	ns	
ACTIVE to ACTIVE command period		t_{RC}	60		66		66		ns	
ACTIVE to READ or WRITE delay		t_{RCD}	15		20		20		ns	
Refresh period		t_{REF}	64		64		64		ms	
AUTOREFRESH period		t_{RFC}	66		66		66		ns	
PRECHARGE command period		t_{RP}	15		20		20		ns	
ACTIVE bank a to ACTIVE bank b command		t_{RRD}	14		15		15		ns	
Transition time		t_T	0.3	1.2	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		t_{WR}	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7.5ns			24
			14		15		15		ns	25
Exit SELF REFRESH to ACTIVE command		t_{XSR}	67		75		80		ns	20

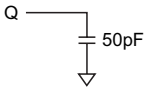
AC FUNCTIONAL CHARACTERISTICS

V_{CC}, V_{CCQ} = +3.3V ±0.3V

PARAMETER		SYMBOL	7	7.5	10	UNITS	NOTES
READ/WRITE command to READ/WRITE command		t_{CCD}	1	1	1	t_{CK}	17
CKE to clock disable or power-down entry mode		t_{CKED}	1	1	1	t_{CK}	14
CKE to clock enable or power-down exit setup mode		t_{PED}	1	1	1	t_{CK}	14
DQM to input data delay		t_{DQD}	0	0	0	t_{CK}	17
DQM to data mask during WRITEs		t_{DQM}	0	0	0	t_{CK}	17
DQMto data high-impedance during READs		t_{DQZ}	2	2	2	t_{CK}	17
WRITE command to input data delay		t_{DWD}	0	0	0	t_{CK}	17
Data-into ACTIVE command		t_{DAL}	4	5	5	t_{CK}	15, 21
Data-into PRECHARGE command		t_{DPL}	2	2	2	t_{CK}	16, 21
Last data-in to burst STOP command		t_{BDL}	1	1	1	t_{CK}	17
Last data-in to new READ/WRITE command		t_{CDL}	1	1	1	t_{CK}	17
Lastdata-into PRECHARGE command		t_{RDL}	2	2	2	t_{CK}	16, 21
LOADMODEREGISTER command to ACTIVE or REFRESH command		t_{MRD}	2	2	2	t_{CK}	26
Data-out to high-impedance from PRECHARGE command	CL = 3	$t_{ROH(3)}$	3	3	3	t_{CK}	17
	CL = 2	$t_{ROH(2)}$	2	2	2	t_{CK}	17

Notes

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC}, V_{CCQ} = +3.3V; T_A = 25°C; pin under test biased at 1.4V; f = 1 MHz.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with mini-mum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{CC} and V_{CCQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume t_T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a mono-tonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are other-wise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by t_{CKS}; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by t_{WR} plus t_{RP}; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by t_{WR}.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on t_{CK} = 10ns for 10, and t_{CK} = 7.5ns for 7 and 7.5.
22. V_{IH} overshoot: V_{IH} (MAX) = V_{CCQ} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} under-shoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including t_{WR}, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (t_{RP}) begins 7ns for 7; 7.5ns for 7.5 and 7.5ns for 10 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC133, PC100 specify three clocks.
27. t_{AC} for 7/7.5 at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.

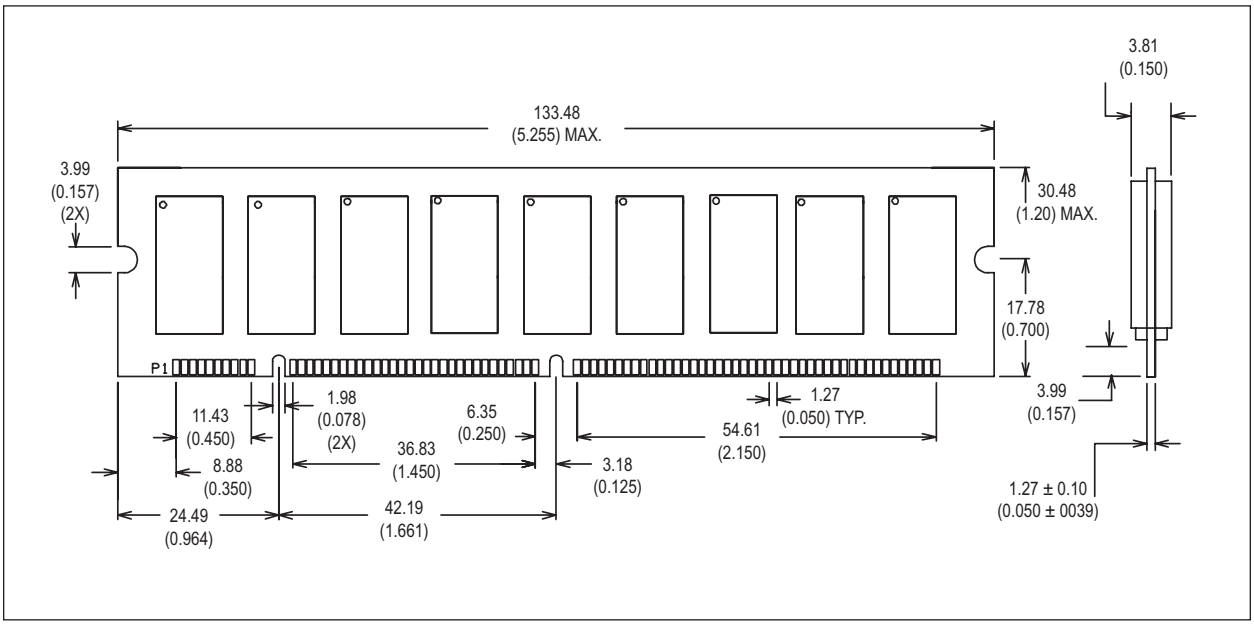
ORDERING INFORMATION

Part Number	Speed	CAS Latency	Height*
W3DG7267V10D2	100MHz	CL=2	30.48 (1.20")
W3DG7267V7D2	133MHz	CL-2	30.48 (1.20")
W3DG7267V75D2	133MHz	CL=3	30.48 (1.20")

NOTES:

- Consult Factory for availability of Lead-Free products. (F = Lead-Free, G = RoHS Compliant)
- Product specific part numbers are available for source control if needed, please consult factory for the correct part number if a specific component vendor is preferred.
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

Document Title

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Revision History

Rev #	History	Release Date	Status
Rev A	Created Datasheet	11-7-01	Advanced
Rev B	Add "Part Number" to order info table	1-17-02	Advanced
Rev 0	0.1 Updated Cap & IDD Spec 0.2 Added package dimentions in millimeters 0.3 Removed "ED" from part number 0.4 Changed from Advanced to Preliminary	6-9-04	Preliminary
Rev 1	1.0 Added lead-free and RoHS notes 1.1 Added source control notes 1.2 Added industrial temperature options 1.3 Added AC specs	1-17-05	Preliminary