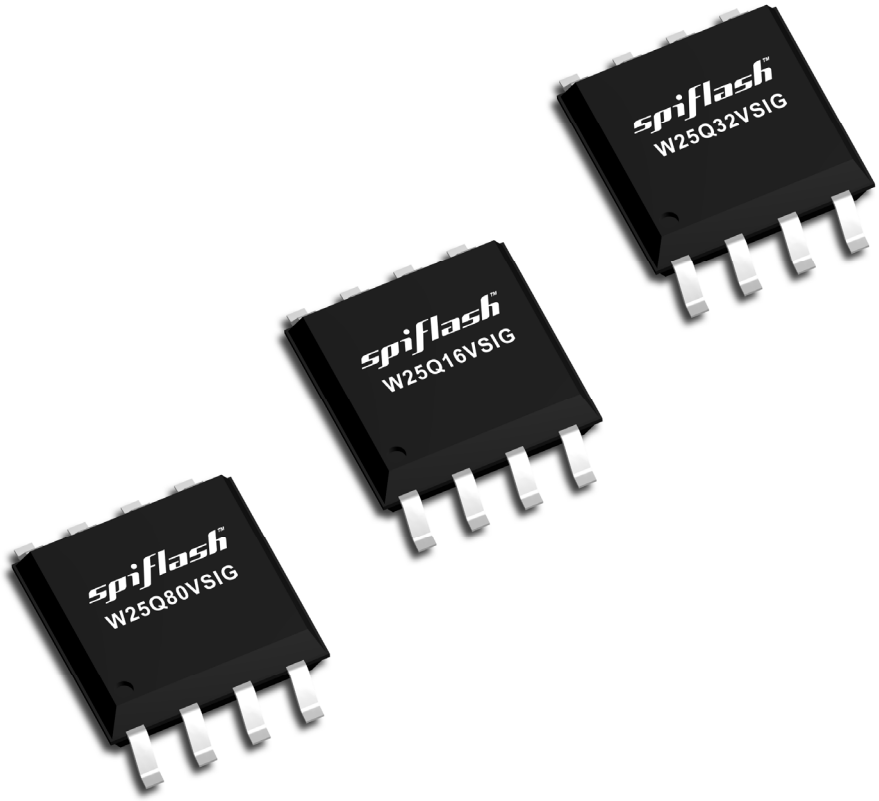
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spiflash®

8M-BIT, 16M-BIT AND 32M-BIT SERIAL FLASH MEMORY WITH DUAL AND QUAD SPI



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1. GENERAL DESCRIPTION

The W25Q80 (8M-bit), W25Q16 (16M-bit), and W25Q32 (32M-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 5mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25Q80/16/32 array is organized into 4,096/8,192/16,384 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased in groups of 16 (sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q80/16/32 has 256/512/1024 erasable sectors and 16/32/64 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25Q80/16/32 supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI using SPI pins: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 80MHz are supported allowing equivalent clock rates of 160MHz for Dual Output and 320MHz for Quad Output when using the Fast Read Dual/Quad Output instructions. These transfer rates are comparable to those of 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of SpiFlash Memories**
  - W25Q80: 8M-bit / 1M -byte (1,048,576)
  - W25Q16: 16M-bit / 2M-byte (2,097,152)
  - W25Q32: 32M-bit / 4M-byte (4,194,304)
  - 256-bytes per programmable page
- **Standard, Dual or Quad SPI**
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
- **Highest Performance Serial Flash**
  - Up to 6X that of ordinary Serial Flash
  - 80MHz clock operation
  - 160MHz equivalent Dual SPI
  - 320MHz equivalent Quad SPI
  - 40MB/S continuous data transfer rate
  - 30MB/S random access (32-byte fetch)
  - Comparable to X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector Erase (4K-bytes)
  - Block Erase (32K and 64K-bytes)
  - Program one to 256 bytes
  - Up to 100,000 erase/write cycles
  - 20-year data retention
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Top or Bottom, Sector or Block selection
  - Lock-Down and OTP protection(1)
  - 64-Bit Unique ID for each device(1)

  Note 1:
  These features are on special order.
  Please contact Winbond for details.
- **Space Efficient Packaging**
  - 8-pin SOIC 208-mil
  - 8-pad WSON 6x5-mm (W25Q80 & W25Q16)
  - 16-pin SOIC 300-mil (W25Q16 & W25Q32)

3. PIN CONFIGURATION SOIC 208-MIL

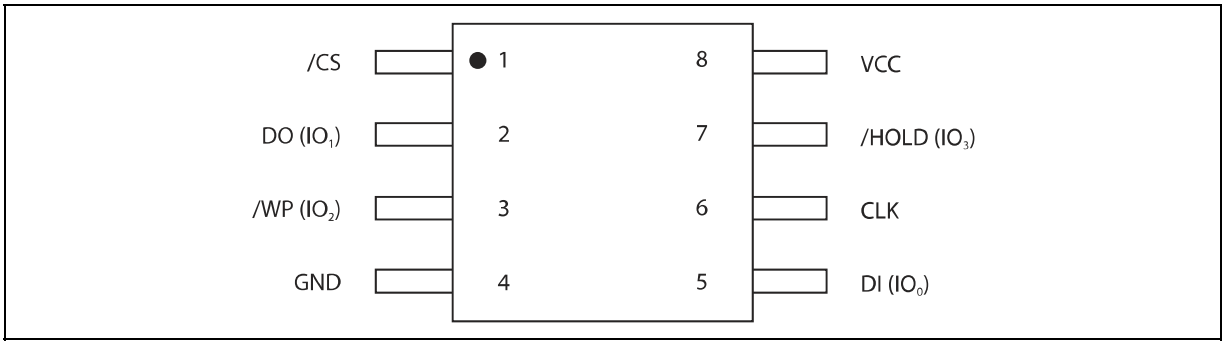


Figure 1a. W25Q80, W25Q16, W25Q32 Pin Assignments, 8-pin SOIC 208-mil (Package Code SS)

4. PAD CONFIGURATION WSON 6X5-MM

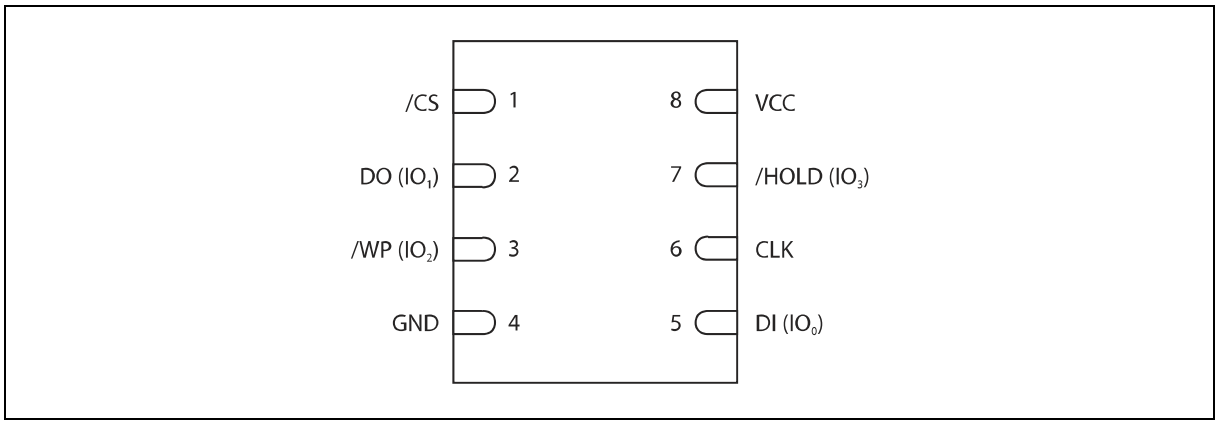


Figure 1b. W25Q80, W25Q16 Pad Assignments, 8-pad WSON (Package Code ZP)

5. PIN DESCRIPTION SOIC 208-MIL, AND WSON 6X5-MM

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)*[1]
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*[2]
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)*[1]
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*[2]
8	VCC		Power Supply

*1 IO0 and IO1 are used for Dual and Quad instructions

*2 IO0 – IO3 are used for Quad instructions

6. PIN CONFIGURATION SOIC 300-MIL

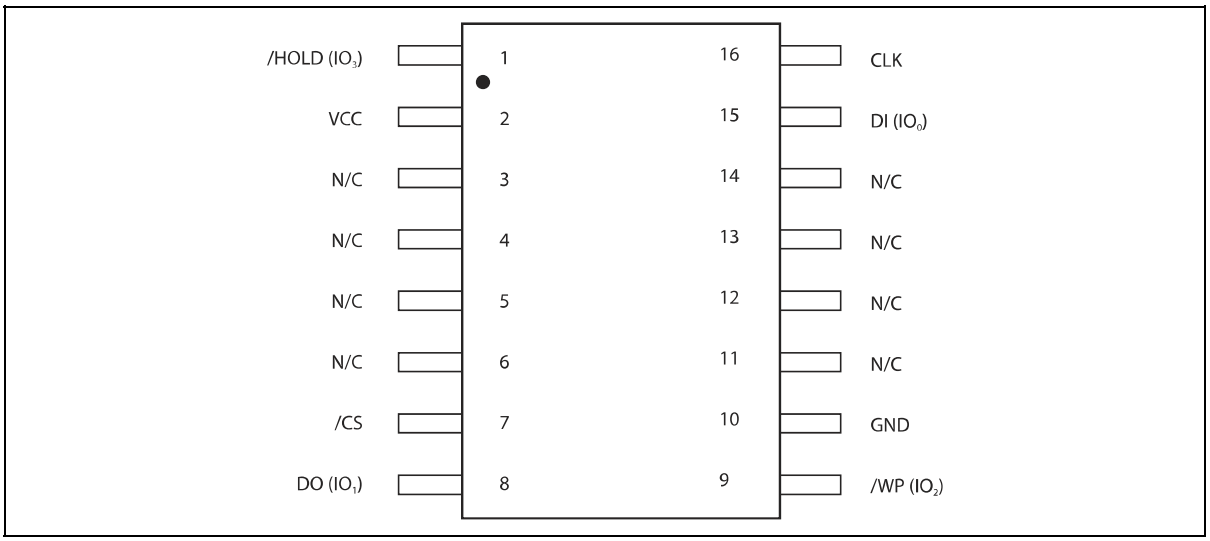


Figure 1c. W25Q16 and W25Q32 Pin Assignments, 16-pin SOIC 300-mil (Package Code SF)

7. PIN DESCRIPTION SOIC 300-MIL

PAD NO.	PAD NAME	I/O	FUNCTION
1	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
2	VCC		Power Supply
3	N/C		No Connect
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
16	CLK	I	Serial Clock Input

*1 IO0 and IO1 are used for Dual and Quad instructions

*2 IO0 – IO3 are used for Quad instructions

7.1 Package Types

W25Q80 is offered in an 8-pin plastic 208-mil width SOIC (package code SS) and 6x5-mm WSON (package code ZP). W25Q16 is offered in an 8-pin plastic 208-mil width SOIC (package code SS) and 6x5-mm WSON as shown in figure 1a, and 1b, respectively. The W25Q16 and W25Q32 are offered in a 16-pin plastic 300-mil width SOIC (package code SF) as shown in figure 1c. Package diagrams and dimensions are illustrated at the end of this datasheet.

7.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 30). If needed a pull-up resister on /CS can be used to accomplish this.

7.3 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q80/16/32 support standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual and Quad SPI instruction use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1 the /WP pin becomes IO2 and /HOLD pin becomes IO3.

7.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin (Hardware Write Protect) function is not available since this pin is used for IO2. See figure 1a, 1b, and 1c for the pin configuration of Quad I/O operation.

7.5 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See figure 1a, 1b, and 1c for the pin configuration of Quad I/O operation.

7.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

8. BLOCK DIAGRAM

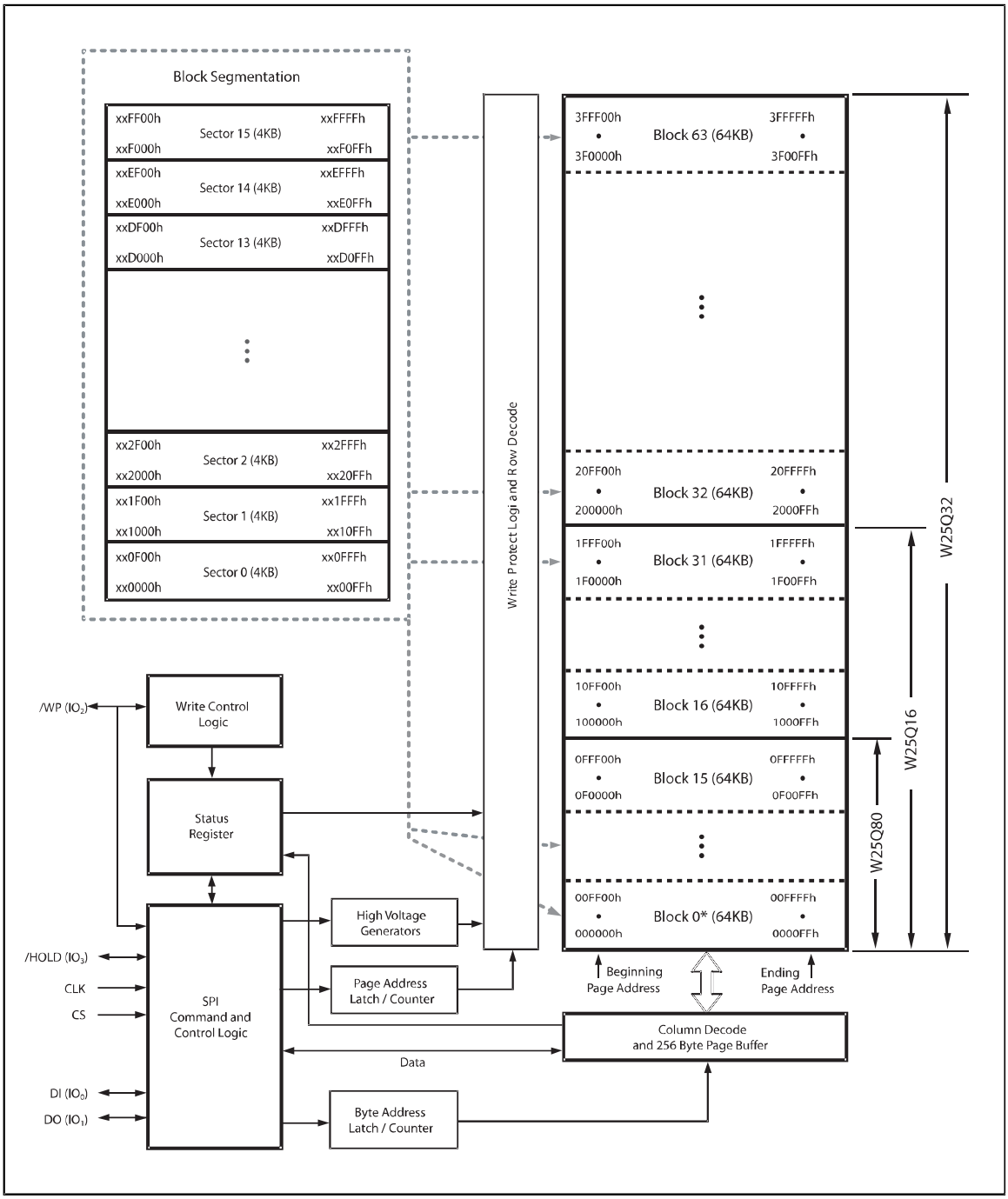


Figure 2. W25Q80, W25Q16 and W25Q32 Block Diagram

9. FUNCTIONAL DESCRIPTION

9.1 SPI OPERATIONS

9.1.1 Standard SPI Instructions

The W25Q80/16/32 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3 the CLK signal is normally high on the falling and rising edges of /CS.

9.1.2 Dual SPI Instructions

The W25Q80/16/32 supports Dual SPI operation when using the "Fast Read Dual Output and Dual I/O" (3B and BB hex) instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins; IO0 and IO1.

9.1.3 Quad SPI Instructions

The W25Q80/16/32 supports Quad SPI operation when using the "Fast Read Quad Output and Fast Read Quad I/O" (6B and EB hex respectively). These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

9.1.4 Hold Function

The /HOLD signal allows the W25Q80/16/32 operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the

/HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

9.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the W25Q80/16/32 provides several means to protect data from inadvertent writes.

9.2.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after program and erase
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection until next power-up(1)
- One Time Program (OTP) write protection(1)

Note 1: These features are available upon special order. Please contact Winbond for details.

Upon power-up or at power-down the W25Q80/16/32 will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 29). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (SEC,TB, BP2, BP1 and BP0) bits. These settings allow a portion or all of the memory to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

10. CONTROL AND STATUS REGISTERS

The Read Status Register-1 and Status Register-2 instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection and the Quad SPI setting. The Write Status Register instruction can be used to configure the devices write protection features and Quad SPI setting. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and in some cases the /WP pin.

10.1 STATUS REGISTER

10.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase Suspend instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

10.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

10.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

10.1.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

10.1.5 Sector/Block Protect (SEC)

The non-volatile Sector protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

10.1.6 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and can not be written to again until the next power-down, power-up cycle.(2)
1	1	X	One Time Program(1)	Status Register is permanently protected and can not be written to.

Note:
1. These features are available upon special order. Please contact Winbond for details.
2. When SRP1, SRP0 = (1,0), a power-down, power-up cycle will change SRP1, SRP0 to (0,0) state.

10.1.7 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad operation. When the QE bit is set to a 0 state (factory default) the /WP pin and /Hold are enabled. When the QE pin is set to a 1 the Quad IO2 and IO3 pins are enabled.

WARNING: The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins are tied directly to the power supply or ground.

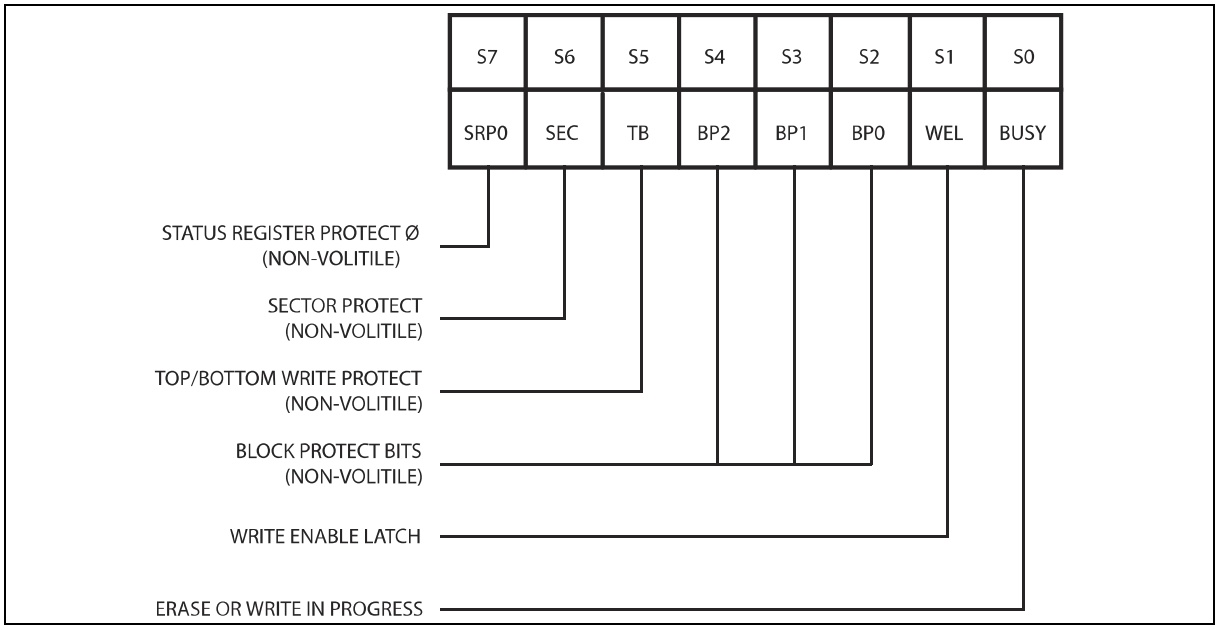


Figure 3a. Status Register-1

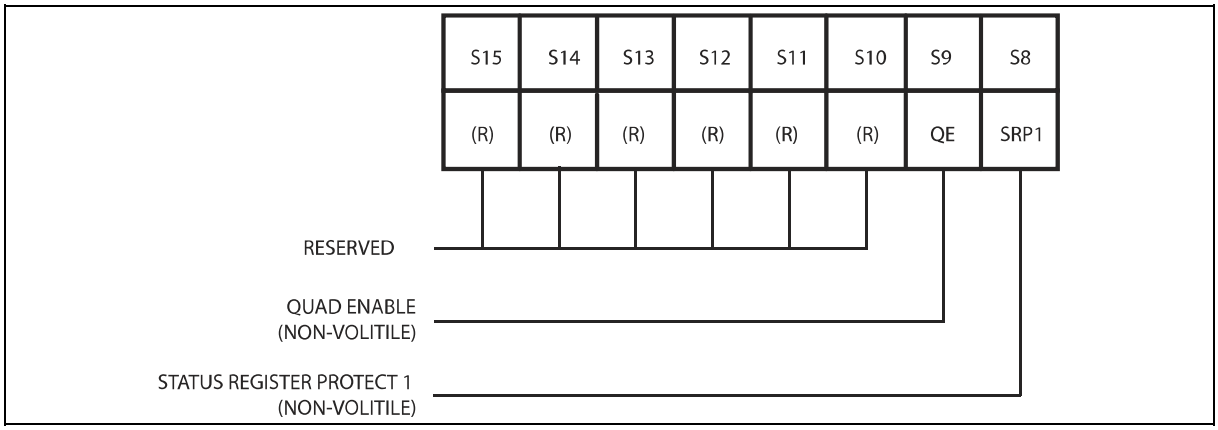


Figure 3b. Status Register-2

10.1.8 Status Register Memory Protection

STATUS REGISTER(1)					W25Q32 (32M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	63	3F0000h - 3FFFFFh	64KB	Upper 1/64
0	0	0	1	0	62 and 63	3E0000h - 3FFFFFh	128KB	Upper 1/32
0	0	0	1	1	60 thru 63	3C0000h - 3FFFFFh	256KB	Upper 1/16
0	0	1	0	0	56 thru 63	380000h - 3FFFFFh	512KB	Upper 1/8
0	0	1	0	1	48 thru 63	300000h - 3FFFFFh	1MB	Upper 1/4
0	0	1	1	0	32 thru 63	200000h - 3FFFFFh	2MB	Upper 1/2
0	1	0	0	1	0	000000h - 00FFFFh	64KB	Lower 1/64
0	1	0	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/32
0	1	0	1	1	0 thru 3	000000h - 03FFFFh	256KB	Lower 1/16
0	1	1	0	0	0 thru 7	000000h - 07FFFFh	512KB	Lower 1/8
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/4
0	1	1	1	0	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/2
X	X	1	1	1	0 thru 63	000000h – 3FFFFFh	4MB	ALL
1	0	0	0	1	63	3FF000h – 3FFFFFh	4KB	Top Block
1	0	0	1	0	63	3FE000h – 3FFFFFh	8KB	Top Block
1	0	0	1	1	63	3FC000h – 3FFFFFh	16KB	Top Block
1	0	1	0	X	63	3F8000h – 3FFFFFh	32KB	Top Block
1	1	0	0	1	0	000000h – 000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h – 001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h – 003FFFh	16KB	Bottom Block
1	1	1	0	X	0	000000h – 007FFFh	32KB	Bottom Block

STATUS REGISTER(1)					W25Q16 (16M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	31	1F0000h - 1FFFFFh	64KB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000h - 1FFFFFh	128KB	Upper 1/16
0	0	0	1	1	28 thru 31	1C0000h - 1FFFFFh	256KB	Upper 1/8
0	0	1	0	0	24 thru 31	180000h - 1FFFFFh	512KB	Upper 1/4
0	0	1	0	1	16 thru 31	100000h - 1FFFFFh	1MB	Upper 1/2
0	1	0	0	1	0	000000h - 00FFFFh	64KB	Lower 1/32
0	1	0	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/16
0	1	0	1	1	0 thru 3	000000h - 03FFFFh	256KB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h - 07FFFFh	512KB	Lower 1/4
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/2
X	X	1	1	X	0 thru 31	000000h – 1FFFFFh	2MB	ALL
1	0	0	0	1	31	1FF000h – 1FFFFFh	4KB	Top Block
1	0	0	1	0	31	1FE000h – 1FFFFFh	8KB	Top Block
1	0	0	1	1	31	1FC000h – 1FFFFFh	16KB	Top Block
1	0	1	0	X	31	1F8000h – 1FFFFFh	32KB	Top Block
1	1	0	0	1	0	000000h – 000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h – 001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h – 003FFFh	16KB	Bottom Block
1	1	1	0	X	0	000000h – 007FFFh	32KB	Bottom Block

STATUS REGISTER[1]					W25Q80 (8M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	15	0F0000h - 0FFFFFh	64KB	Upper 1/16
0	0	0	1	0	14 and 15	0E0000h - 0FFFFFh	128KB	Upper 1/8
0	0	0	1	1	12 thru 15	0C0000h - 0FFFFFh	256KB	Upper 1/4
0	0	1	0	0	8 thru 15	080000h - 0FFFFFh	512KB	Upper 1/2
0	1	0	0	1	0	000000h - 00FFFFh	64KB	Lower 1/16
0	1	0	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/8
0	1	0	1	1	0 thru 3	000000h - 03FFFFh	256KB	Lower 1/4
0	1	1	0	0	0 thru 7	000000h - 07FFFFh	512KB	Lower 1/2
X	X	1	1	X	0 thru 15	000000h – 0FFFFFh	1MB	ALL
1	0	0	0	1	15	0FF000h – 0FFFFFh	4KB	Top Block
1	0	0	1	0	15	0FE000h – 0FFFFFh	8KB	Top Block
1	0	0	1	1	15	0FC000h – 0FFFFFh	16KB	Top Block
1	0	1	0	X	15	0F8000h – 0FFFFFh	32KB	Top Block
1	1	0	0	1	0	000000h – 000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h – 001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h – 003FFFh	16KB	Bottom Block
1	1	1	0	X	0	000000h – 007FFFh	32KB	Bottom Block

Note:
1. x = don't care

10.2 INSTRUCTIONS

The instruction set of the W25Q80/16/32 consists of fifteen basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 19. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

10.2.1 Manufacturer and Device Identification

MANUFACTURER ID	**(M7-M0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7-ID0)**	**(ID15-ID0)**
Instruction	**ABh, 90h**	**9Fh**
W25Q80	13h	4014h
W25Q16	14h	4015h
W25Q32	15h	4016h

10.2.2 Instruction Set Table 1 (1)

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Write Enable	**06h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7–S0) (2)				
Read Status Register-2	**35h**	(S15-S8) (2)				
Write Status Register	**01h**	(S7–S0)	(S15-S8)			
Page Program	**02h**	A23–A16	A15–A8	A7–A0	(D7–D0)	
Quad Page Program	**32h**	A23–A16	A15–A8	A7–A0	(D7–D0, …)(3)	
Block Erase (64KB)	**D8h**	A23–A16	A15–A8	A7–A0		
Block Erase (32KB)	**52h**	A23–A16	A15–A8	A7–A0		
Sector Erase (4KB)	**20h**	A23–A16	A15–A8	A7–A0		
Chip Erase	**C7h/60h**					
Erase Suspend	**75h**					
Erase Resume	**7Ah**					
Power-down	**B9h**					
High Performance Mode	**A3h**	dummy	dummy	dummy		
Mode Bit Reset (4)	**FFh**	FFh				
Release Power down or HPM / Device ID	**ABh**	dummy	dummy	dummy	(ID7-ID0) (5)	
Manufacturer/ Device ID(6)	**90h**	dummy	dummy	00h	(M7-M0)	(ID7-ID0)
Read Unique ID(7)	**4Bh**	dummy	dummy	dummy	Dummy	(ID63-ID0)
JEDEC ID	**9Fh**	(M7-M0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until /CS terminates the instruction.
3. Quad Page Program Input Data
   IO0 = (D4, D0, ……)
   IO1 = (D5, D1, ……)
   IO2 = (D6, D2, ……)
   IO3 = (D7, D3, ……)
4. This instruction is recommended when using the Dual or Quad Mode bit feature. See section 10.2.28 for more information.
5. The Device ID will repeat continuously until /CS terminates the instruction.
6. See Manufacturer and Device Identification table for Device ID information.
7. This feature is available upon special order. Please contact Winbond for details.

10.2.3 Instruction Set Table 2 (Read Instructions)

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Data	**03h**	A23–A16	A15–A8	A7–A0	(D7–D0)	
Fast Read	**0Bh**	A23–A16	A15–A8	A7–A0	dummy	(D7–D0)
Fast Read Dual Output	**3Bh**	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …)(1)
Fast Read Dual I/O	**BBh**	A23-A8(2)	A7-A0, M7-M0(2)	(D7–D0, …)(1)		
Fast Read Quad Output	**6Bh**	A23–A16	A15–A8	A7–A0	dummy	(D7–D0, …)(3)
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0(4)	(x,x,x,x, D7–D0, …)(5)	(D7-D0, …)(3)		

Notes:

1: Dual Output data
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

2: Dual Input Address
IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3: Quad Output Data
IO0 = (D4, D0, …..)
IO1 = (D5, D1, …..)
IO2 = (D6, D2, …..)
IO3 = (D7, D3, …..)

4: Quad Input Address
IO0 = A20, A16, A12, A8 , A4, A0, M4, M0
IO1 = A21, A17, A13, A9 , A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5: Fast Read Quad I/O Data
IO0 = (x, x, x, x, D4, D0, …..)
IO1 = (x, x, x, x, D5, D1, …..)
IO2 = (x, x, x, x, D6, D2, …..)
IO3 = (x, x, x, x, D7, D3, …..)

10.2.4 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

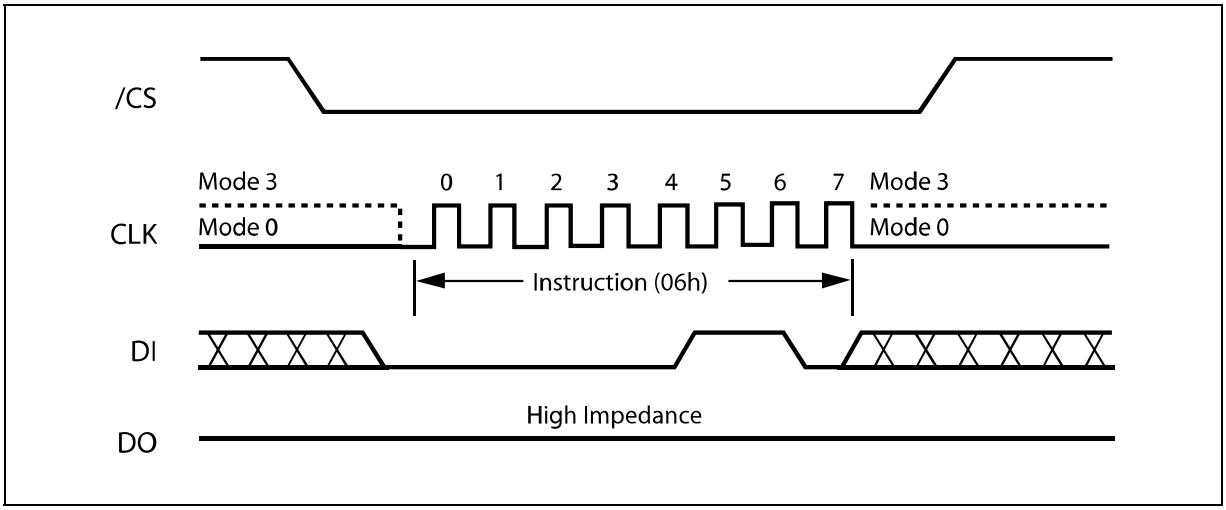


Figure 4. Write Enable Instruction Sequence Diagram

10.2.5 Write Disable (04h)

The Write Disable instruction (Figure 5) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

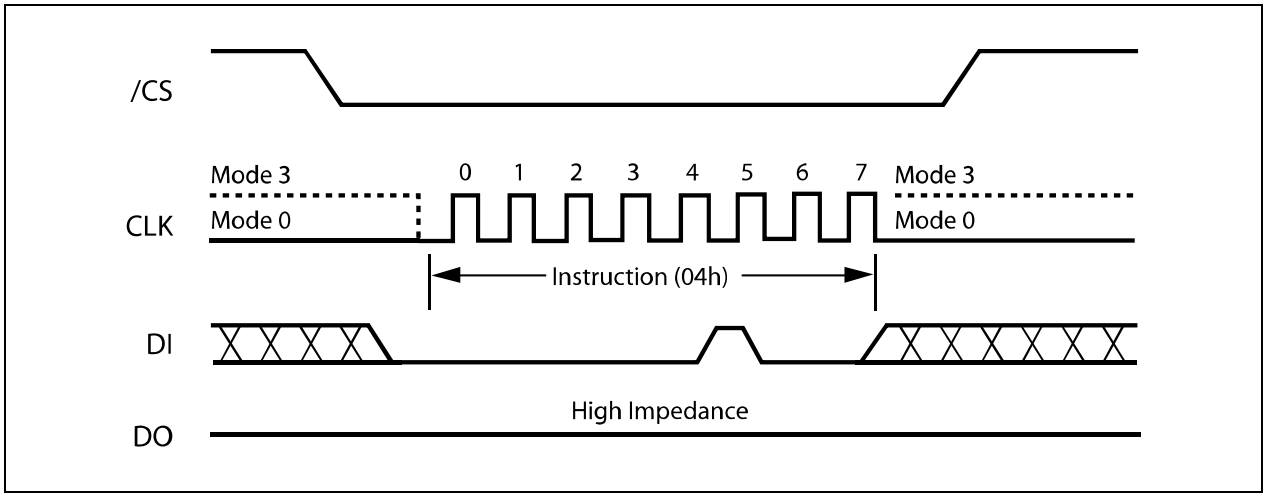


Figure 5. Write Disable Instruction Sequence Diagram

10.2.6 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1 and “35h” for Status Register-2 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3a and 3b and include the BUSY, WEL, BP2-BP0, TB, SEC, SRP0, SRP1 and QE bits (see description of the Status Register earlier in this datasheet).

The Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 6. The instruction is completed by driving /CS high.

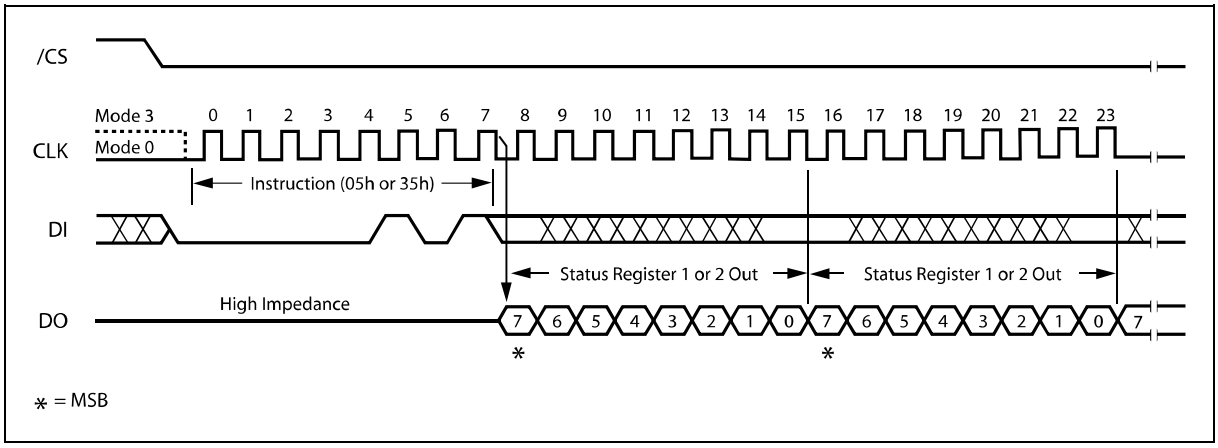


Figure 6. Read Status Register Instruction Sequence Diagram

10.2.7 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 7. The Status Register bits are shown in figure 3 and described earlier in this datasheet.

Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7, 5, 4, 3, 2 of Status Register-1) and QE, SRP1(bits 9 and 8 of Status Register-2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register instruction will not be executed. If /CS is driven high after the eighth clock (compatible with the 25X series) the QE and SRP1 bits will be cleared to 0. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (SEC, TB, BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table and description). The Write Status Register instruction also allows the Status Register Protect bits (SRP0, SRP1) to be set. Those bits are used in conjunction with the Write Protect (/WP) pin, Lock out or OTP features to disable writes to the status register. Please refer to 10.1.16 for detailed descriptions regarding Status Register protection methods. Factory default for all status Register bits are 0.

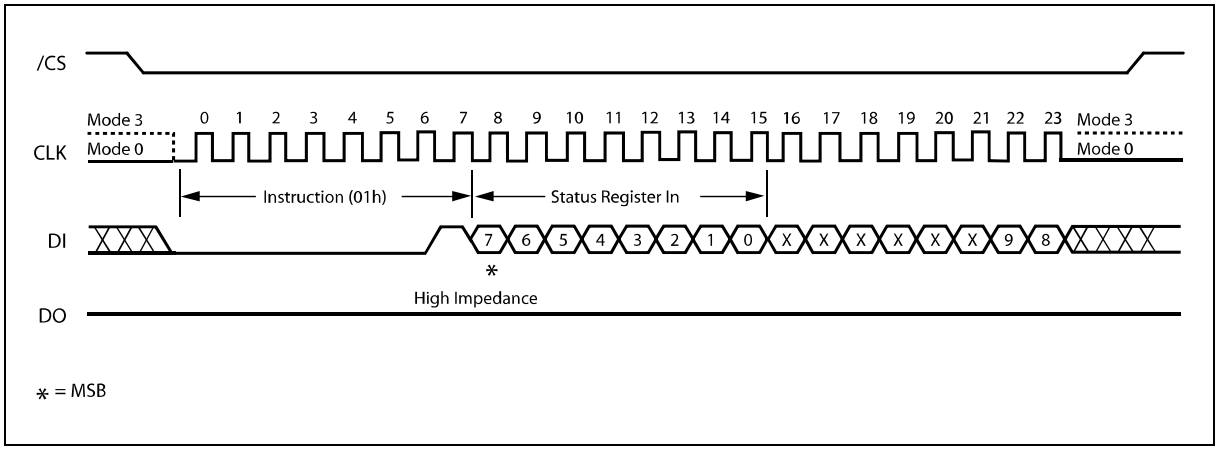


Figure 7. Write Status Register Instruction Sequence Diagram

10.2.8 Read Data (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The Read Data instruction sequence is shown in figure 8. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

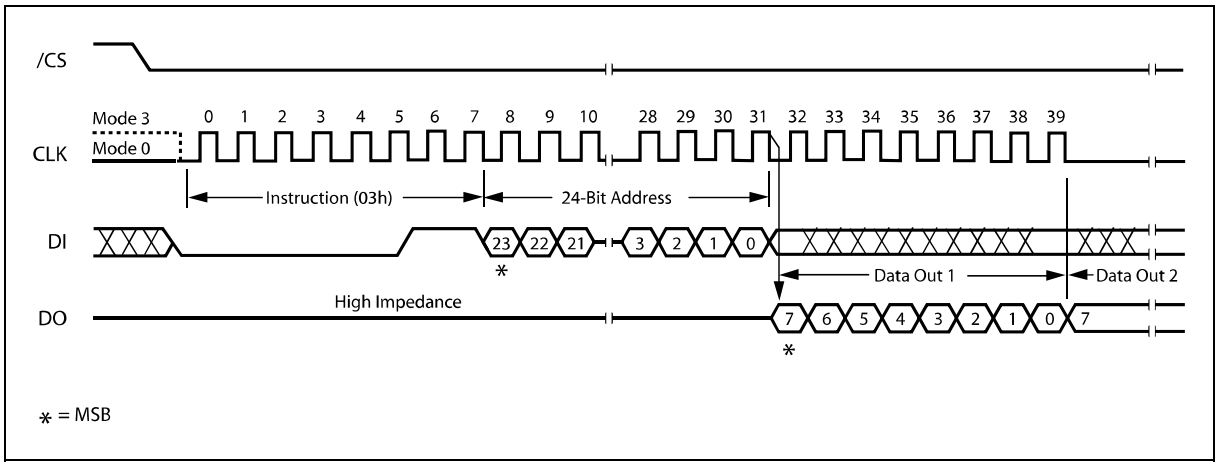


Figure 8. Read Data Instruction Sequence Diagram

10.2.9 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 9. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

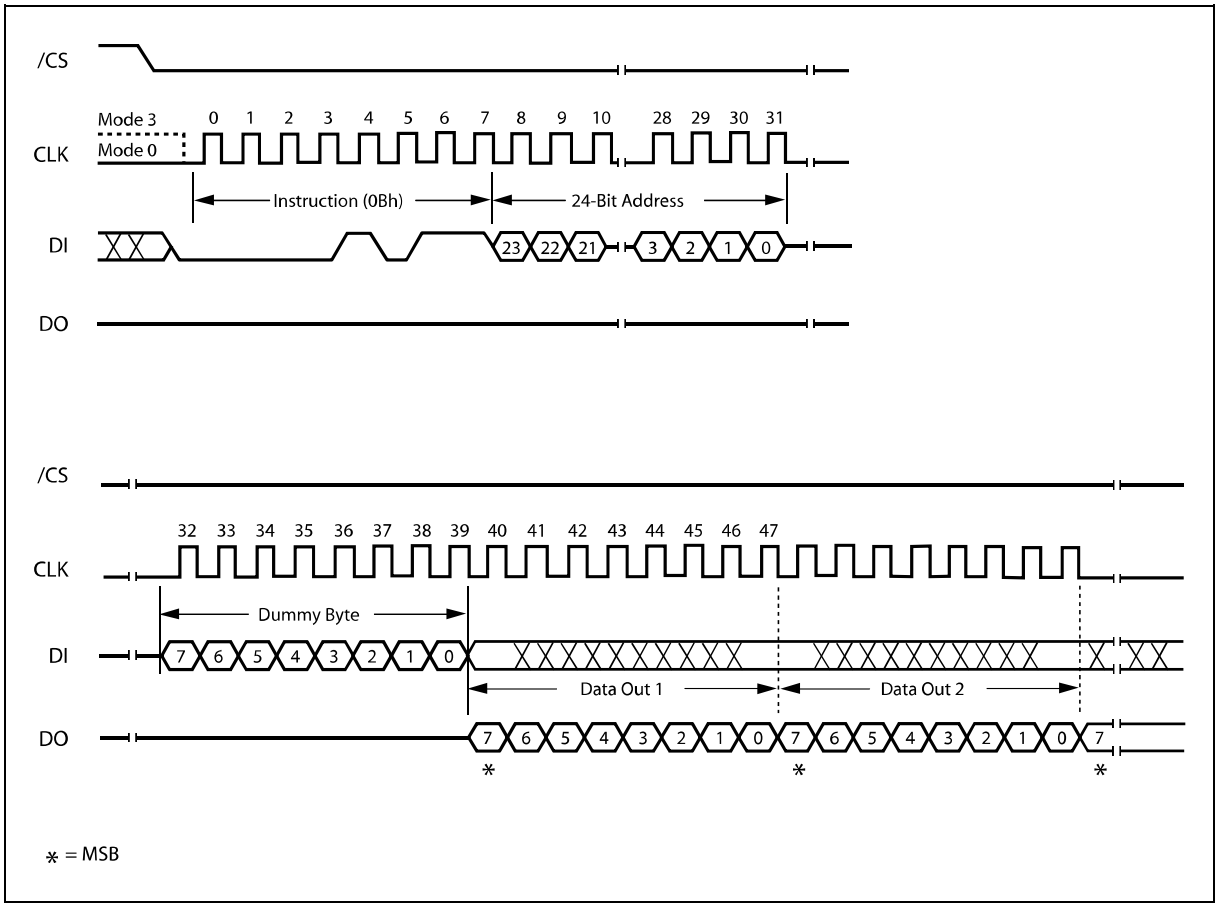


Figure 9. Fast Read Instruction Sequence Diagram

10.2.10 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred from the W25Q80/16/32 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

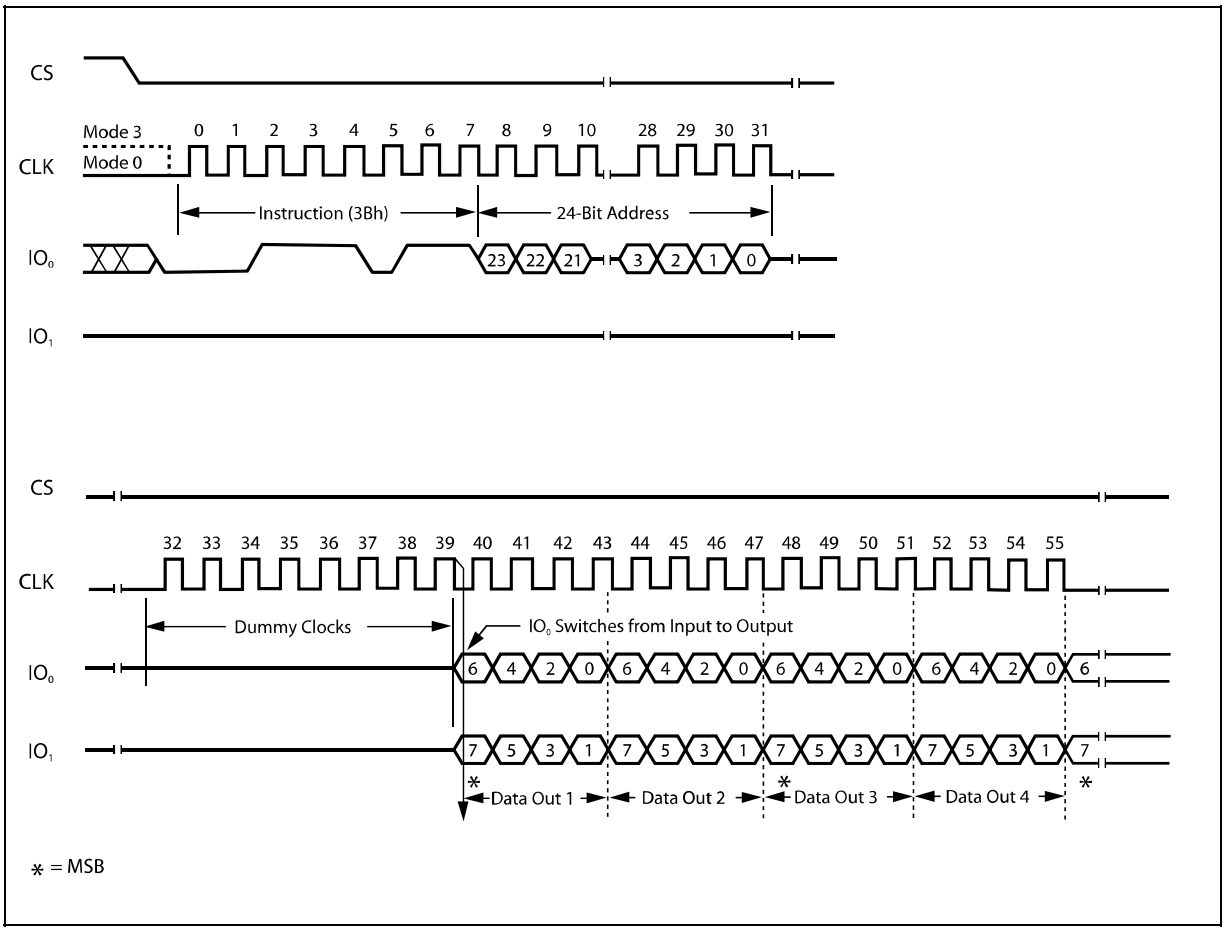


Figure 10. Fast Read Dual Output Instruction Sequence Diagram

10.2.11 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Instruction (Status Register bit QE must equal 1). The Fast Read Quad Output Instruction allows data to be transferred from the W25Q80/16/32 at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

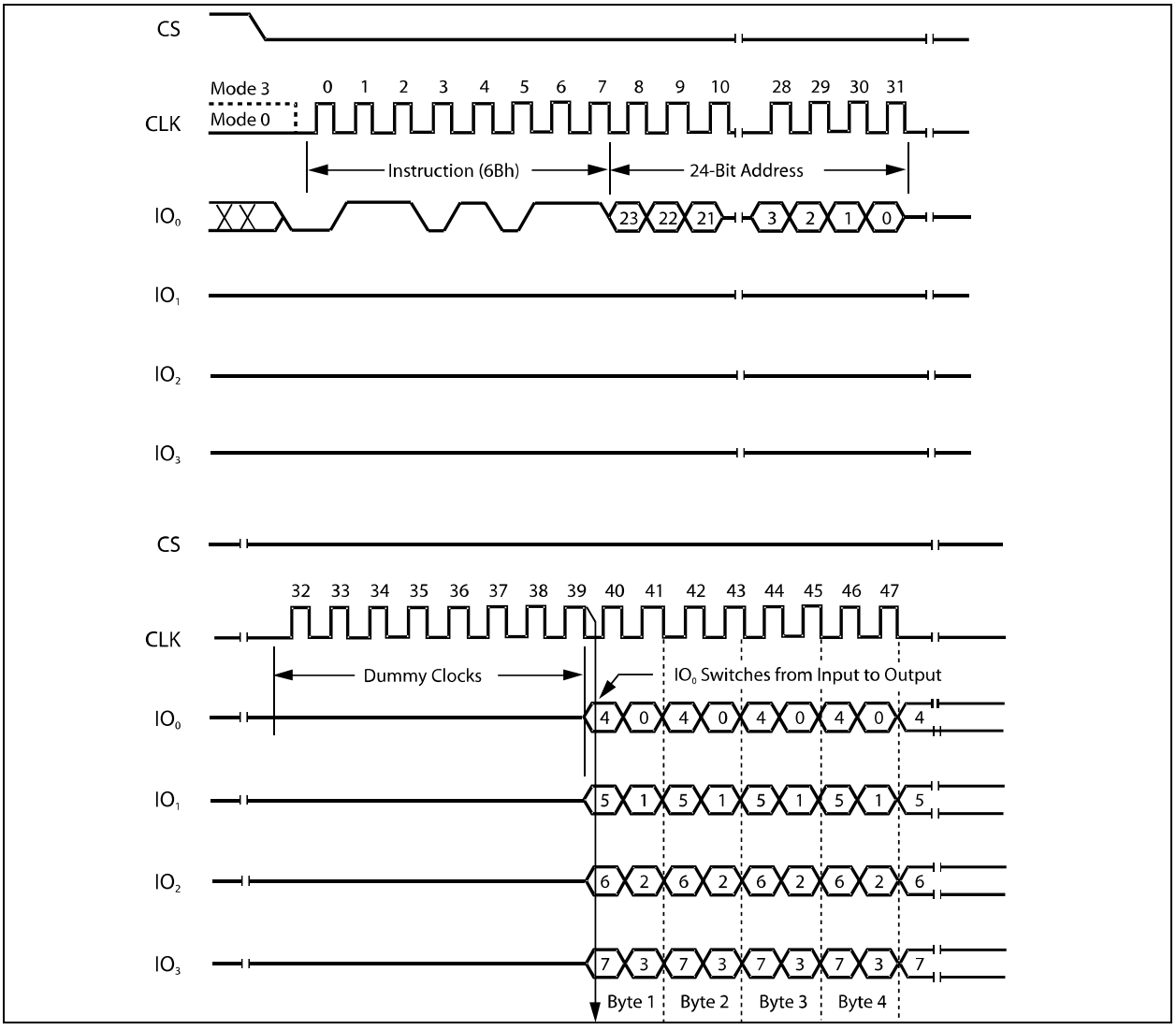


Figure 11. Fast Read Quad Output Instruction Sequence Diagram

10.2.12 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications. To ensure optimum performance the High Performance Mode (HPM) instruction (A3h) must be executed once, prior to the Fast Read Dual I/O Instruction.

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the Mode bits (M7-0) after the input Address bits (A23-0), as shown in figure 12a. The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Mode bits (M7-0) equals "Ax" hex, then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in figure 12b.. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after /CS is asserted low. If the Mode bits (M7-0) are any value other than "Ax" hex, the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A Mode Bit Reset instruction can be used to reset Mode Bits (M7-0) before issuing normal instructions (See 10.2.28 for detailed descriptions).

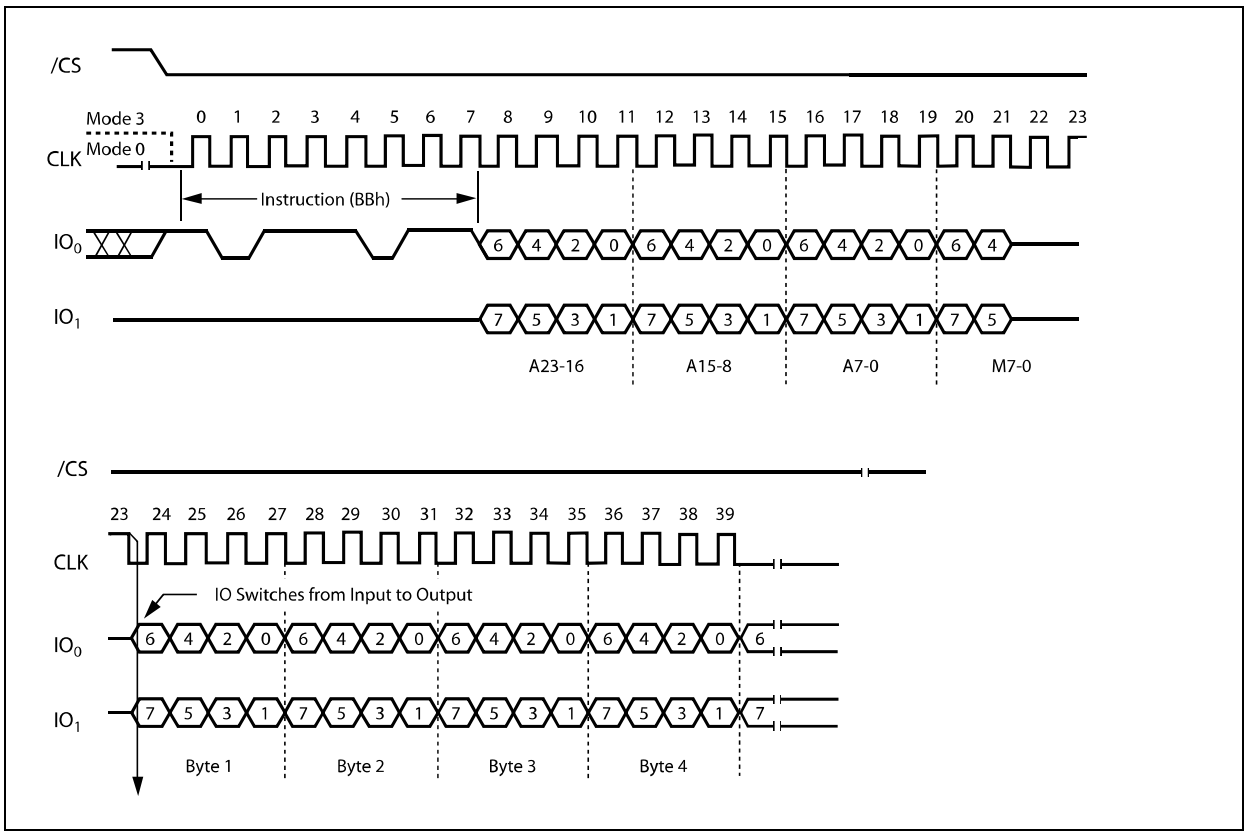


Figure 12a. Fast Read Dual Input/Output Instruction Sequence Diagram (M7-0 = 0xh or NOT Axh)

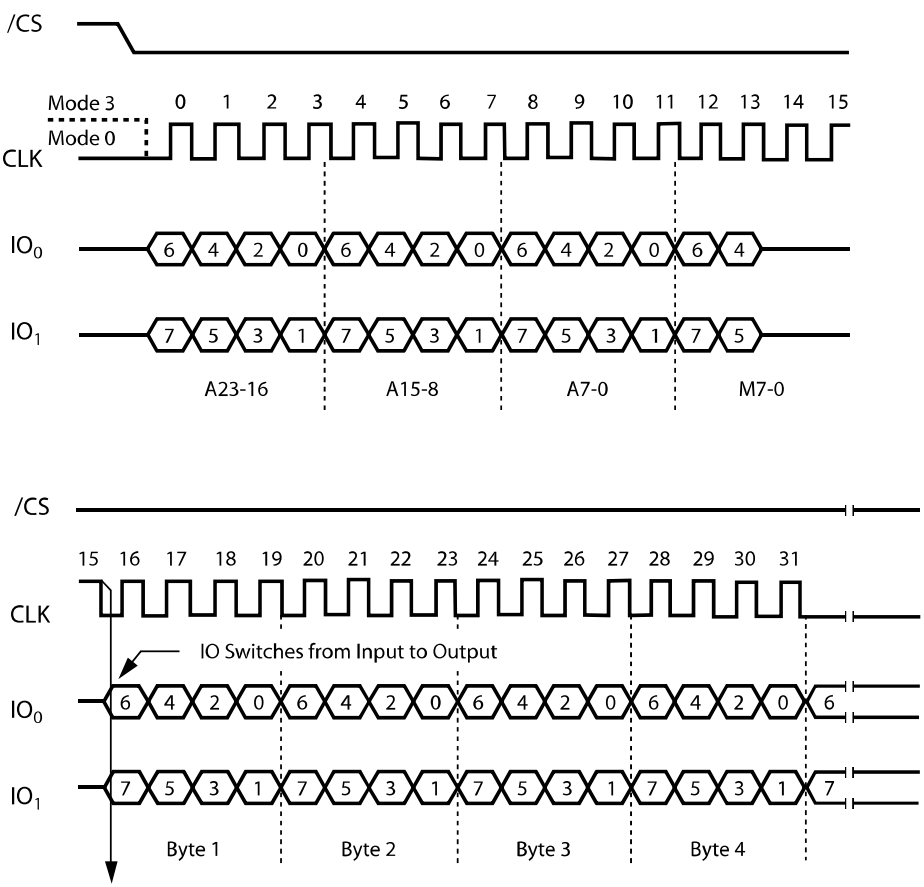


Figure 12b. Fast Read Dual Input/Output Instruction Sequence Diagram (M7-0 = Axh)

10.2.13 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clock are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast read Quad I/O Instruction. To ensure optimum performance the High Performance Mode (HPM) instruction (A3h) must be executed once, prior to the Fast Read Quad I/O Instruction.

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Mode bits (M7-0) after the input Address bits (A23-0), as shown in figure 13a. The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Mode bits (M7-0) equals "Ax" hex, then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in figure 13b. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after /CS is asserted low. If the Mode bits (M7-0) are any value other than "Ax" hex, the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A Mode Bit Reset instruction can be used to reset Mode Bits (M7-0) before issuing normal instructions (See 10.2.28 for detailed descriptions).

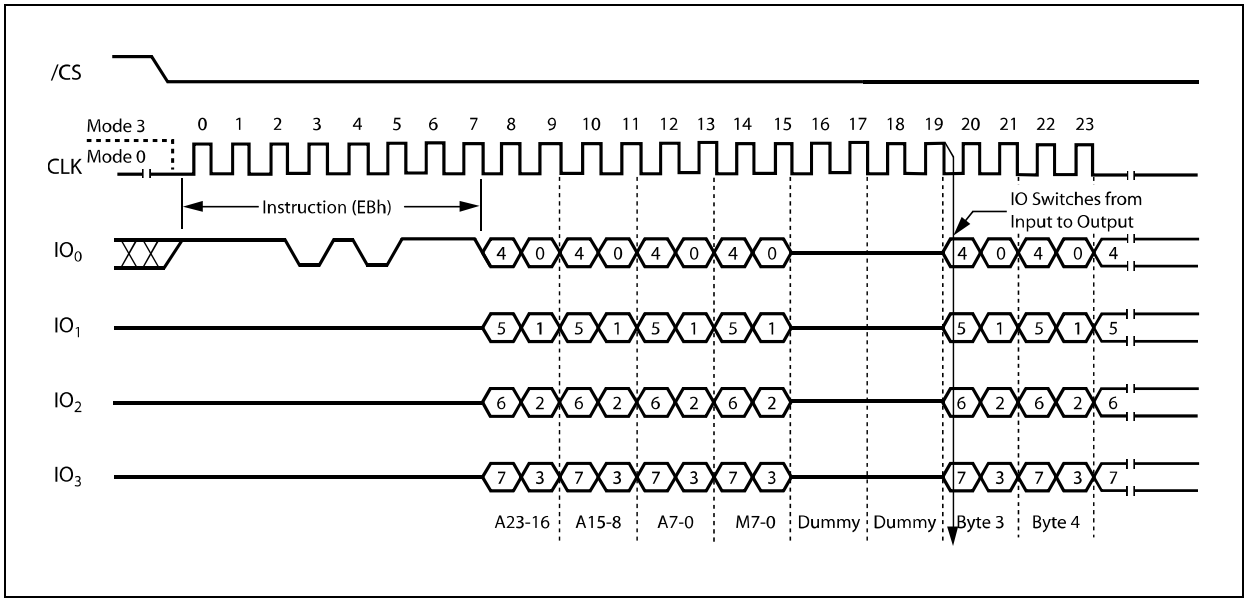


Figure 13a. Fast Read Quad Input/Output Instruction Sequence Diagram (M7-0 = 0xh or NOT Axh)

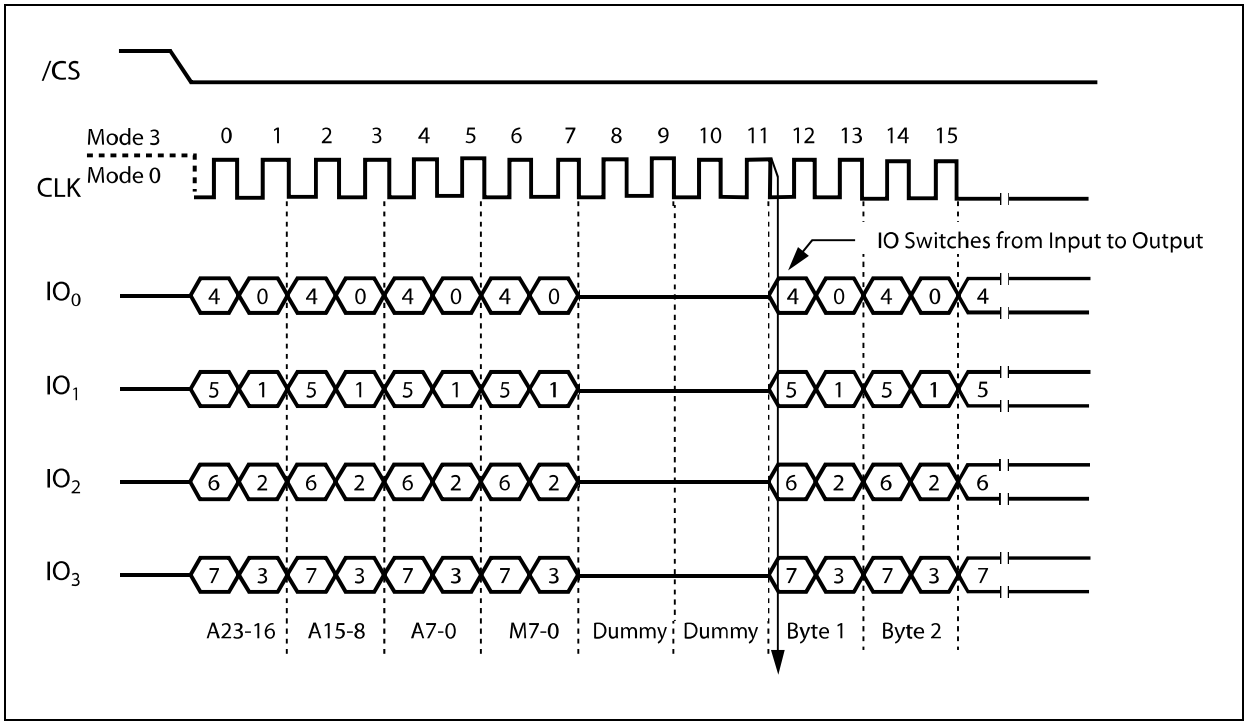


Figure 13b. Fast Read Quad Input/Output Instruction Sequence Diagram (M7-0 = Axh)

10.2.14 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in figure 14.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits.

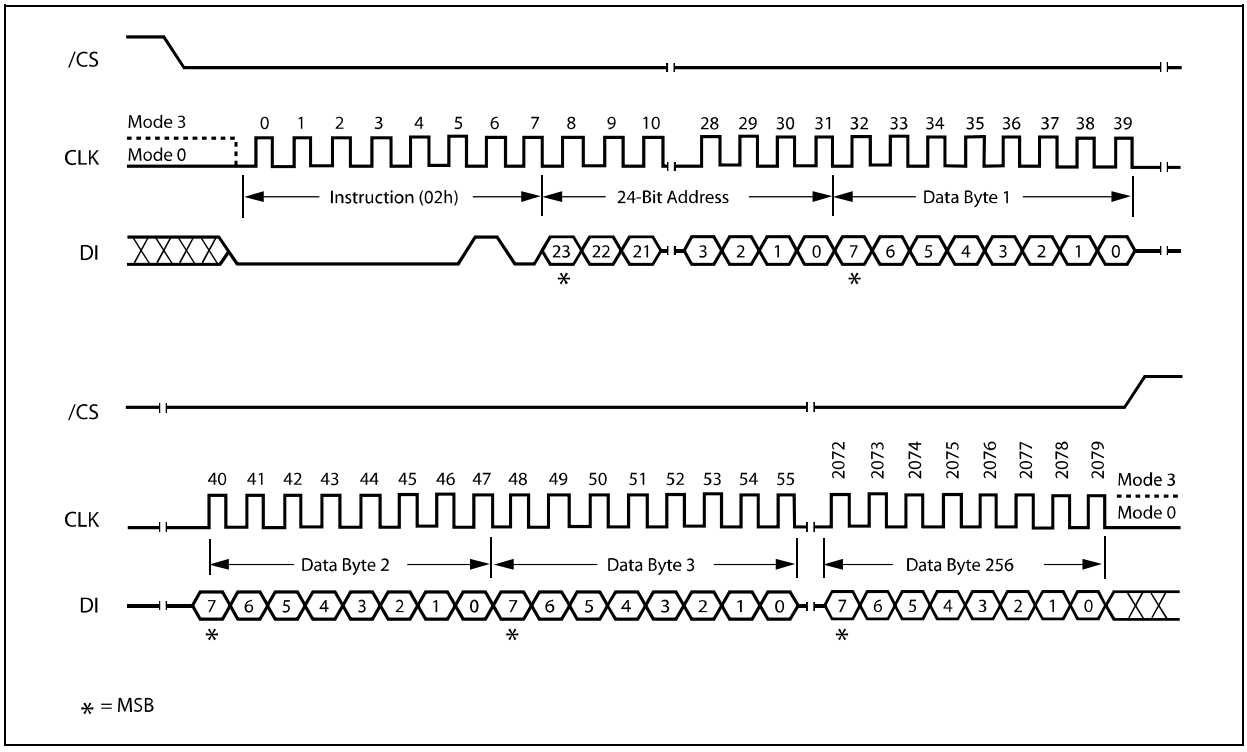


Figure 14. Page Program Instruction Sequence Diagram

10.2.15 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO_0, IO_1, IO_2, and IO_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in figure 15.

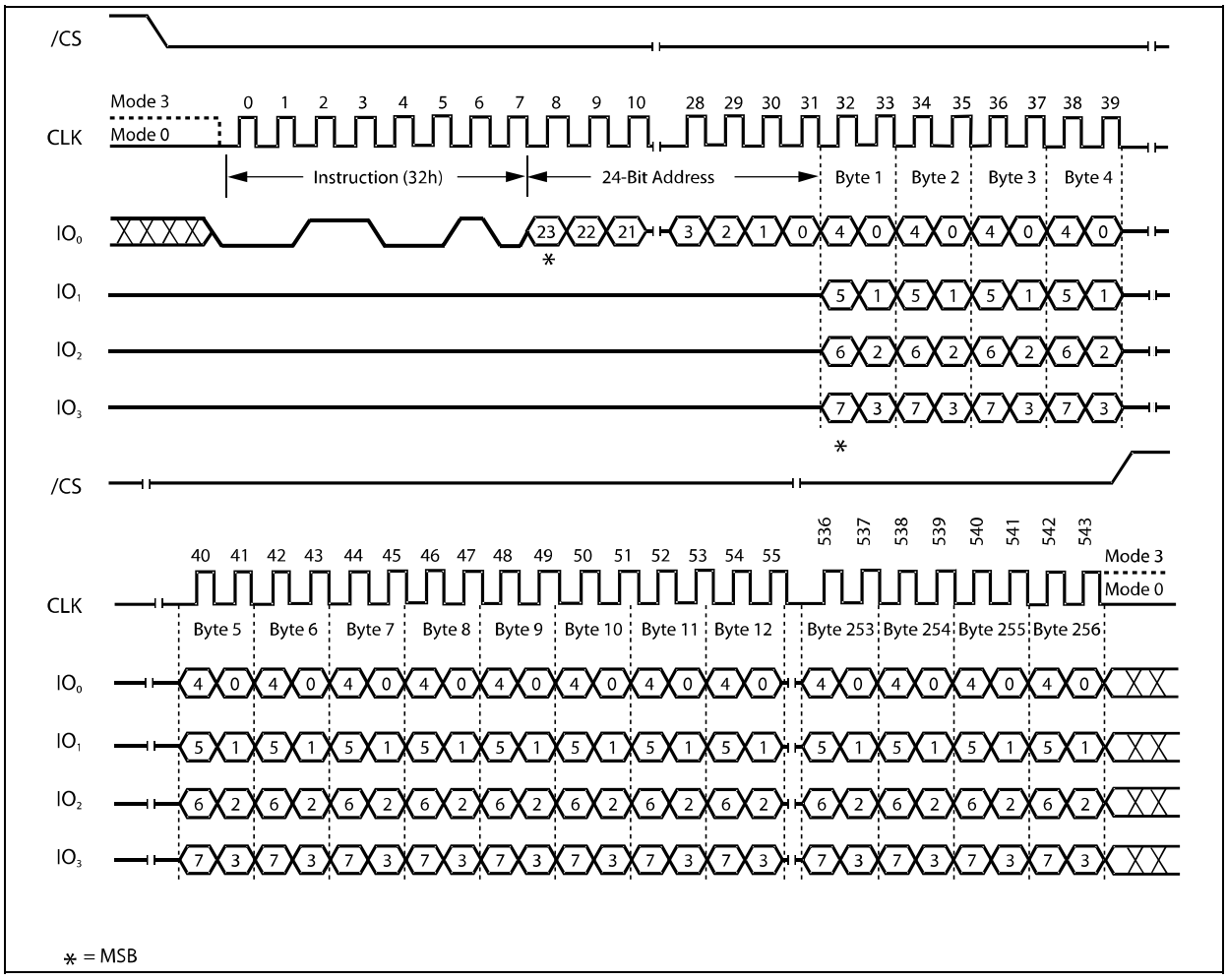


Figure 15. Quad Input Page Program Instruction Sequence Diagram

10.2.16 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "20h" followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 16.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

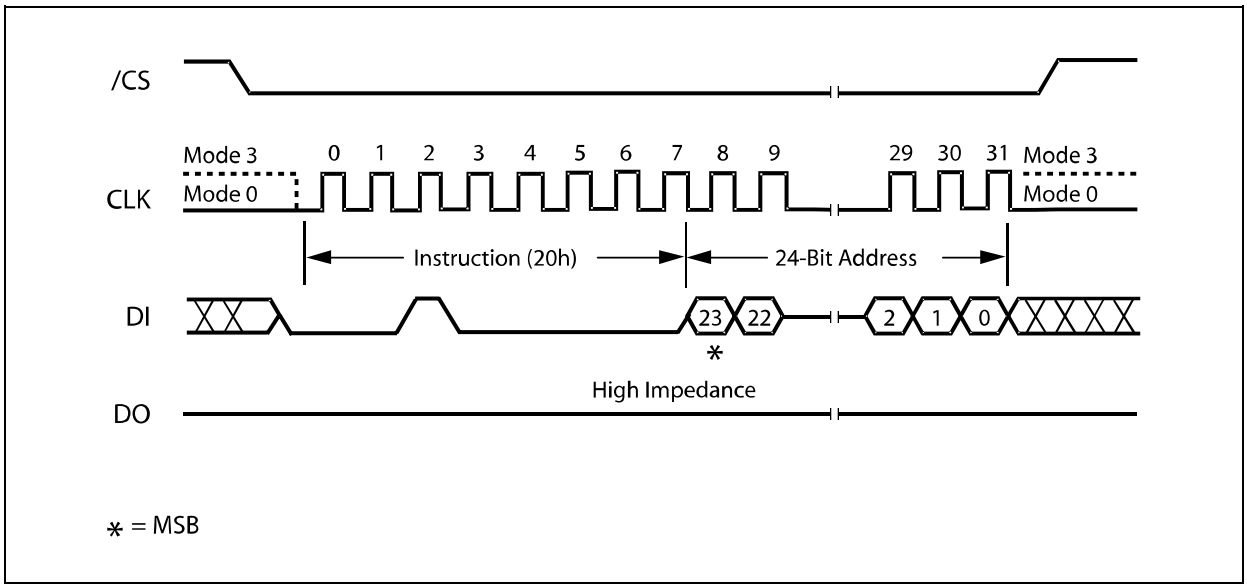


Figure 16. Sector Erase Instruction Sequence Diagram

10.2.17 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "52h" followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 17.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

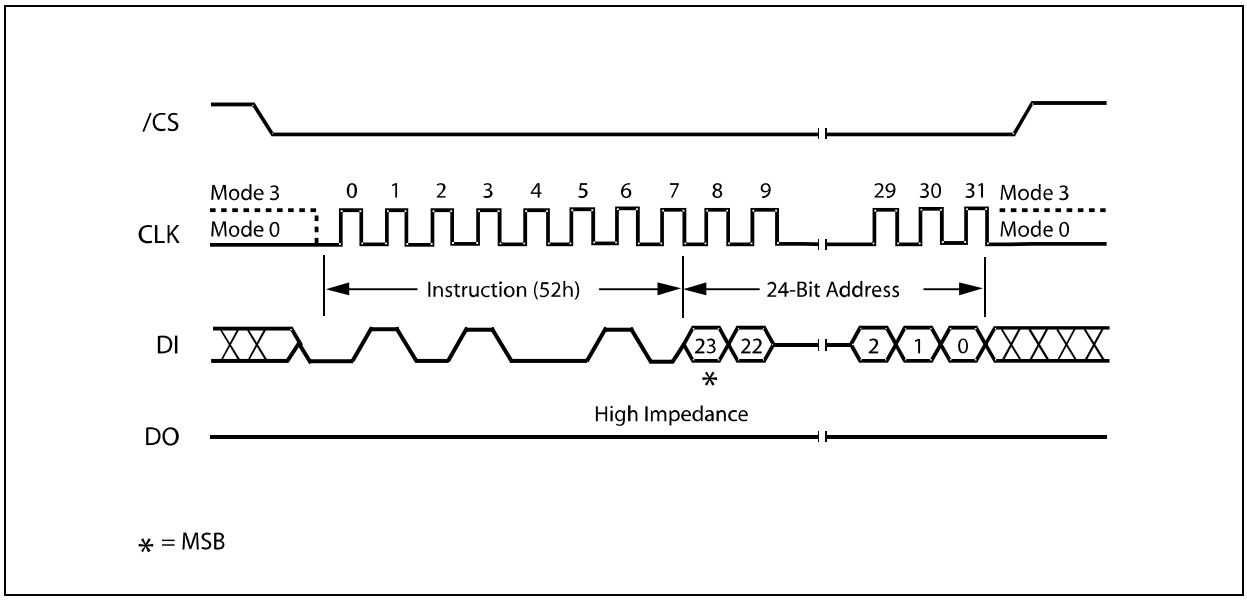


Figure 17. 32KB Block Erase Instruction Sequence Diagram

Note:

For W25Q16, user should not issue 32KB Block Erase (52h) instruction to the top or bottom 32KB block when SEC bit in Status Register is set to "1".

10.2.18 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 18.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

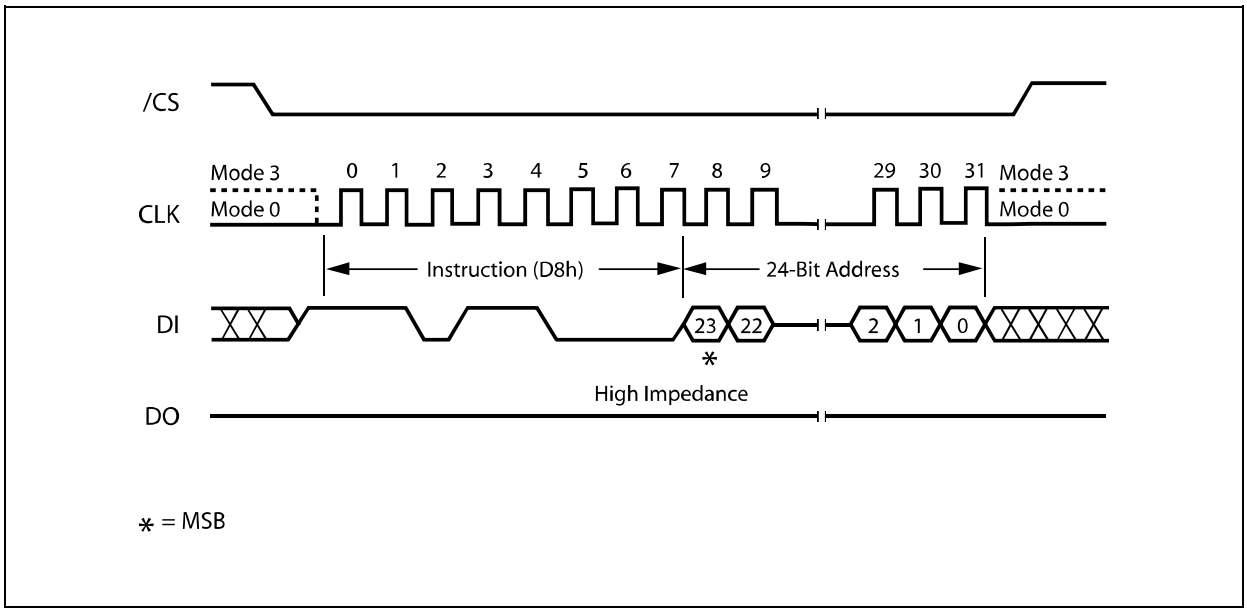


Figure 18. 64KB Block Erase Instruction Sequence Diagram

Note:

For W25Q16, user should not issue 64KB Block Erase (D8h) instruction to the top or bottom 64KB block when SEC bit in Status Register is set to "1".

10.2.19 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 19.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

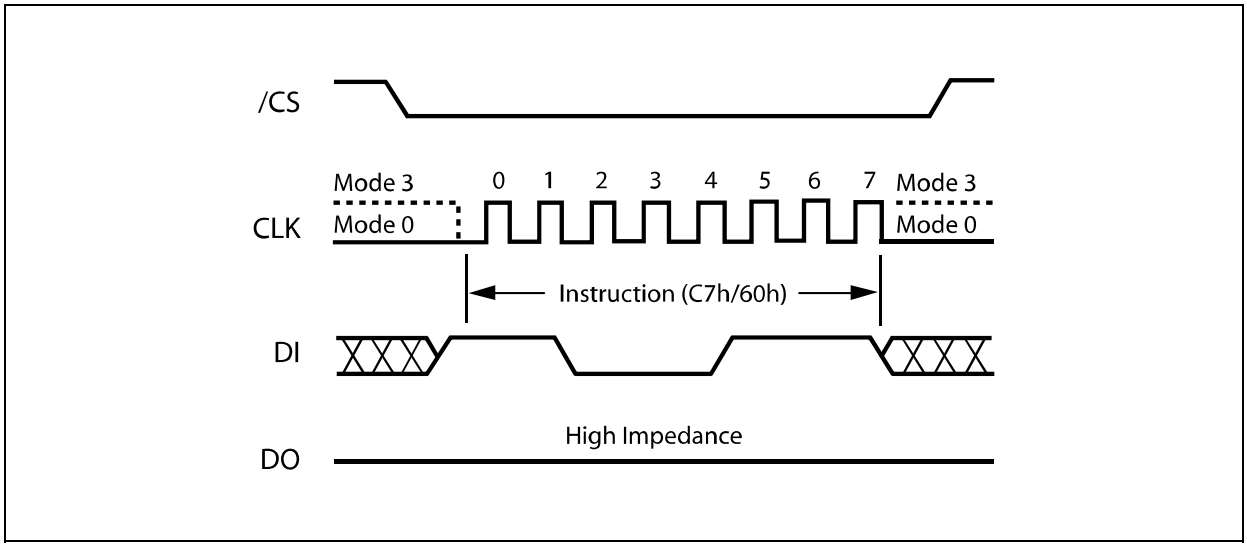


Figure 19. Chip Erase Instruction Sequence Diagram

10.2.20 Erase Suspend (75h)

The Erase Suspend instruction “75h”, allows the system to interrupt a sector or block erase operation and then read from or program data to, any other sector or block. The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8, C7h, 60h) are not allowed during suspend. Erase Suspend is valid only during the sector or block erase operation. If written during the chip erase or program operation, the Erase Suspend instruction is ignored. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the erase operation. The BUSY bit in the Status register will clear to 0 after Erase Suspend.

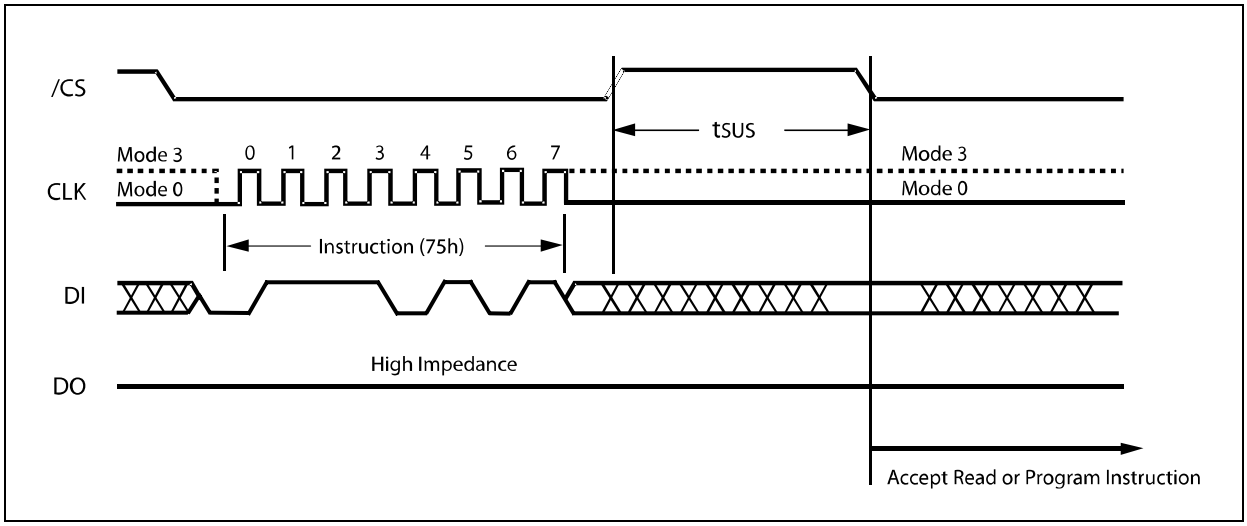


Figure 20. Erase Suspend Instruction Sequence

10.2.21 Erase Resume (7Ah)

The Erase Resume instruction must be written to resume the sector or block erase operation after an Erase Suspend. After issued the BUSY bit in the status register will be set to a 1 and the sector or block will complete the erase operation. Resume instructions will be ignored unless an Erase Suspend operation is active.

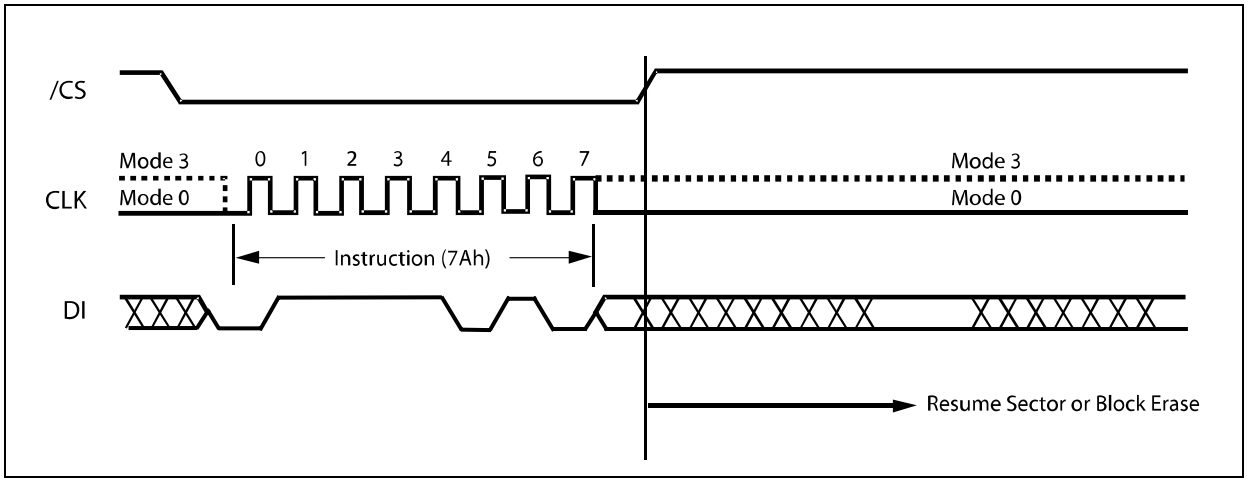


Figure 21. Erase Resume Instruction Sequence

10.2.22 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in figure 22.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

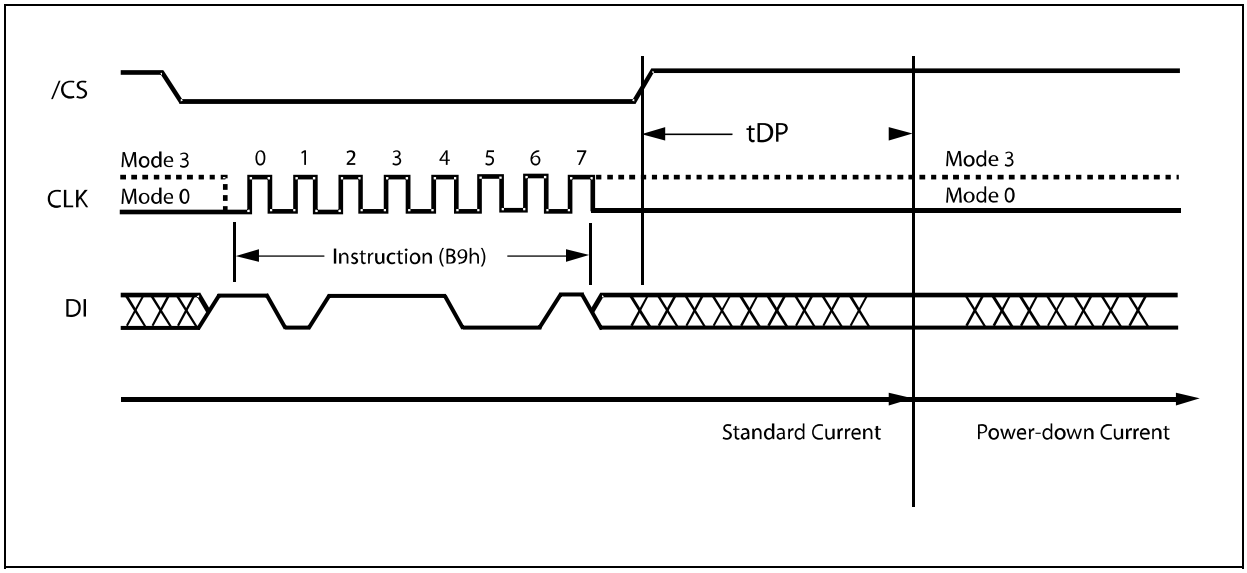


Figure 22. Deep Power-down Instruction Sequence Diagram

10.2.23 High Performance Mode (A3h)

The High Performance Mode (HPM) instruction must be executed prior to Dual or Quad I/O instructions when operating at high frequencies (see FR and FR1 in AC Electrical Characteristics). This instruction allows pre-charging of internal charge pumps so the voltages required for accessing the Flash memory array are readily available. The instruction sequence includes the A3h instruction code followed by three dummy byte clocks shown in Fig. 23. (Contact Winbond for the latest 25Q data sheet with updated HPM diagram). After the HPM instruction is executed, the device will maintain a slightly higher standby current (Icc3) than standard SPI operation. The Release from Power-down or HPM instruction (ABh) can be used to return to standard SPI standby current (Icc1).

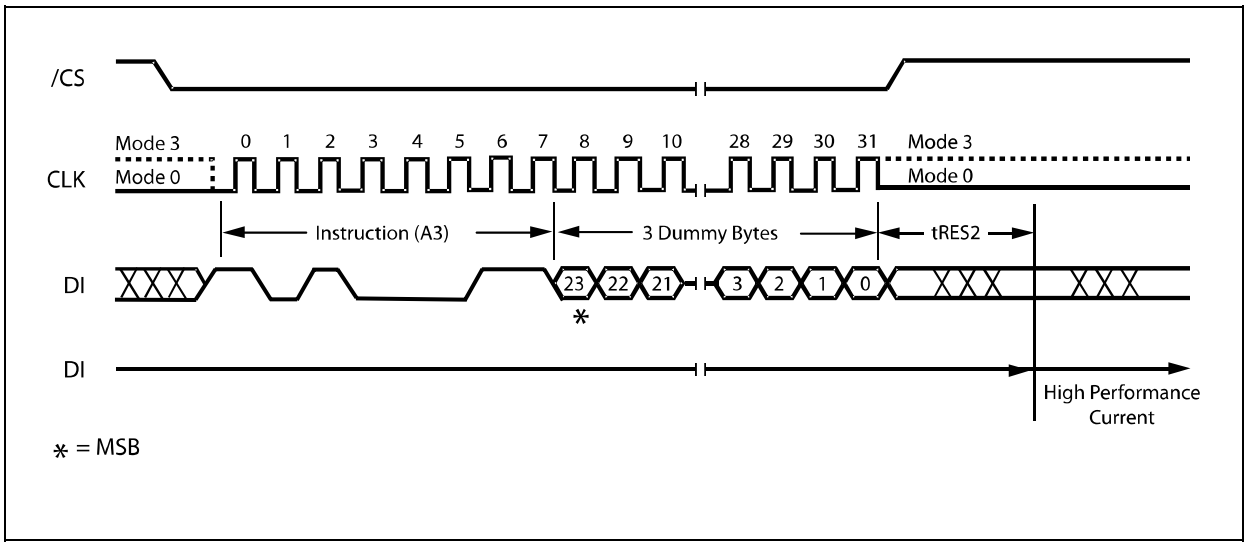


Figure 23. High Performance Mode Instruction Sequence

10.2.24 Release Power-down or High Performance Mode / Device ID (ABh)

The Release from Power-down or High performance Mode / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state or High Performance Mode, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state or High Performance Mode, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in figure 24. Release from power-down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 25. The Device ID values for the W25Q80, W25Q16, and W25Q32 are listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 25, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle

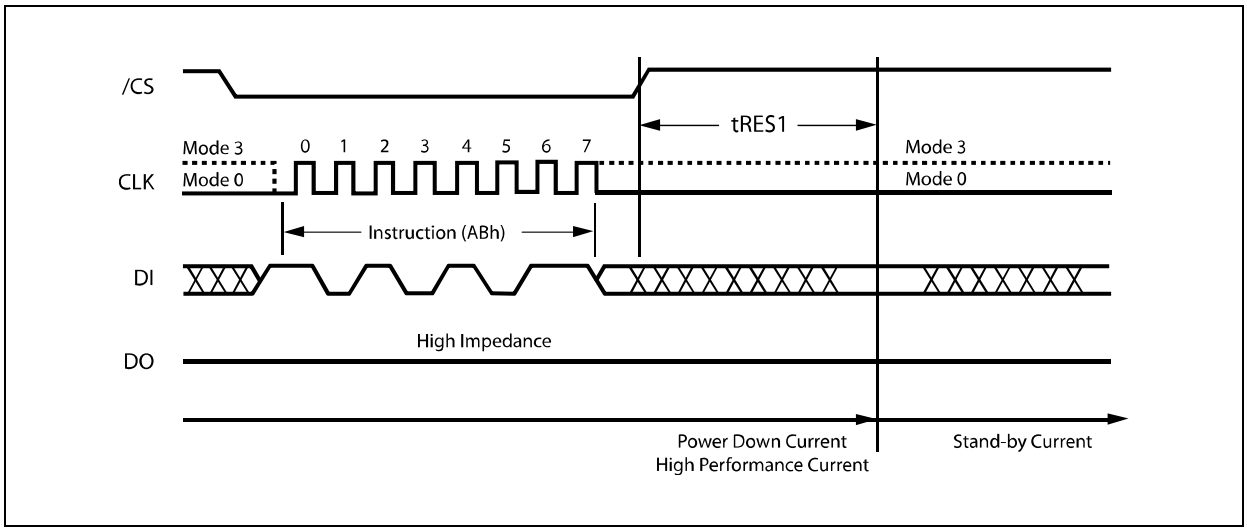


Figure 24. Release Power-down/High Performance Mode Instruction Sequence

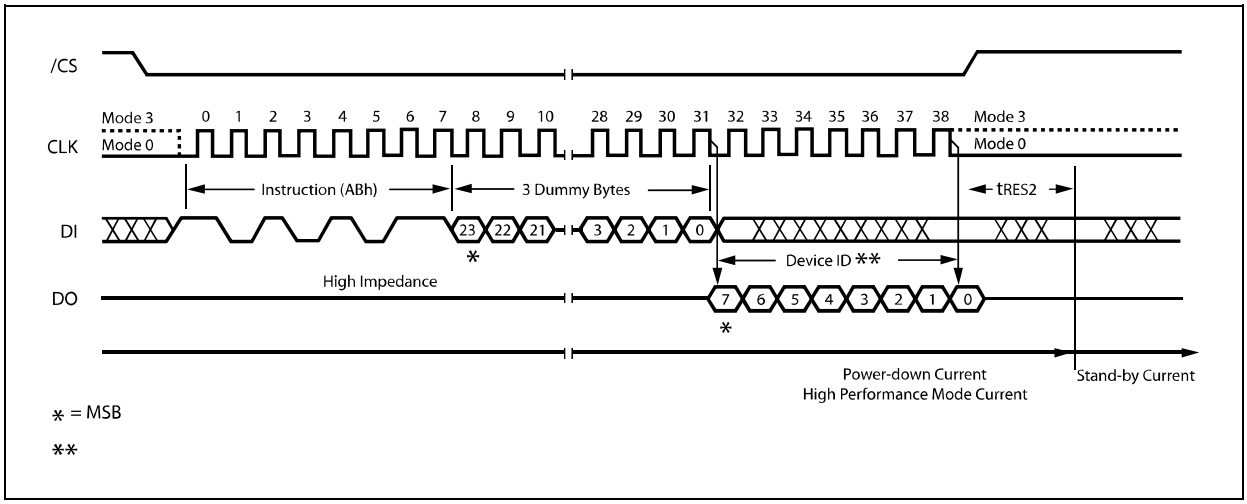


Figure 25. Release Power-down / Device ID Instruction Sequence Diagram

10.2.25 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 26. The Device ID values for the W25Q80, W25Q16, and W25Q32 are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

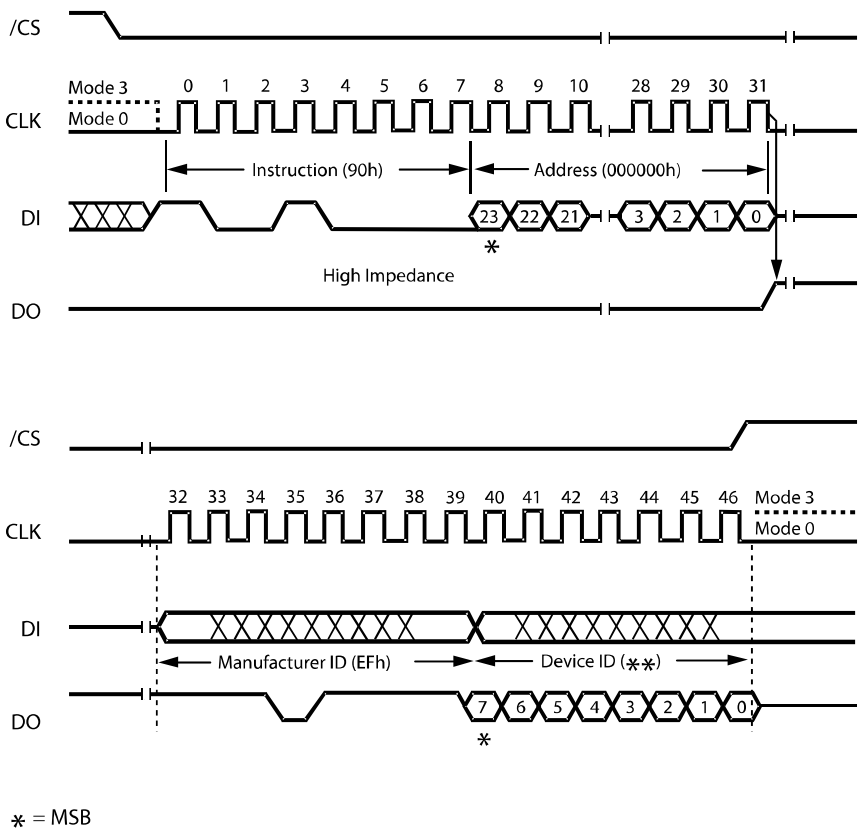


Figure 26. Read Manufacturer / Device ID Diagram

10.2.26 Read Unique ID Number(1)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each W25Q80, W25Q16 or W25Q64 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code "4Bh" followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in figure 27.

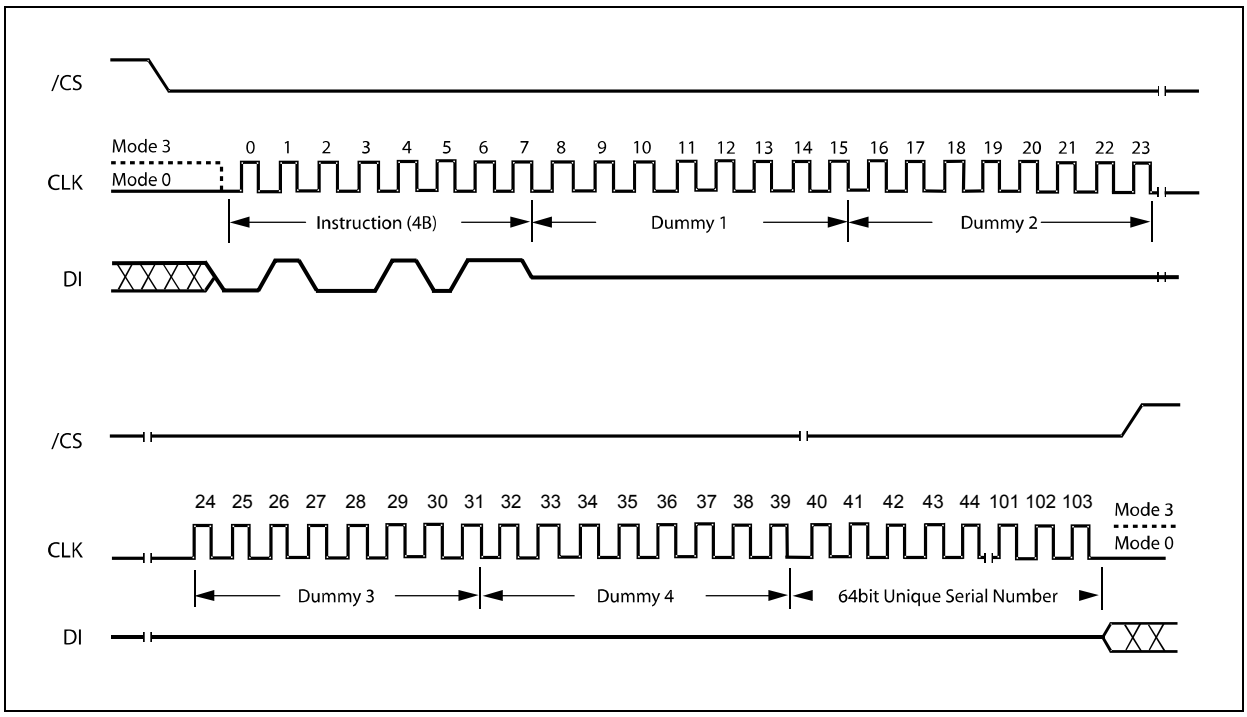


Figure 27. Read Unique ID Number Instruction Sequence

Note:

1. For W25Q16, this feature is available upon special request. Please contact Winbond for details.

10.2.27 JEDEC ID (9Fh)

For compatibility reasons, the W25Q80/16/32 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 28. For memory type and capacity values refer to Manufacturer and Device Identification table.

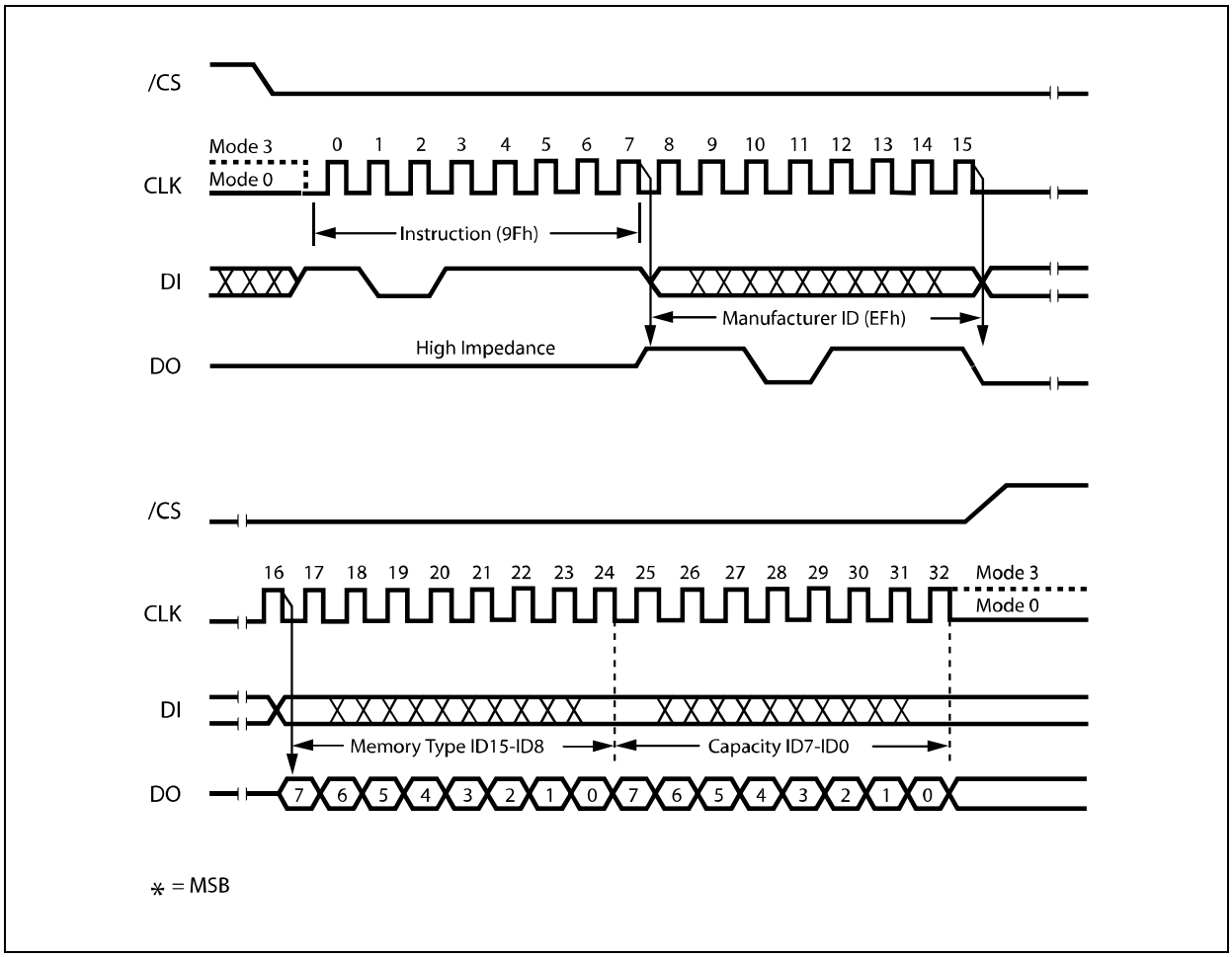


Figure 28. Read JEDEC ID

10.2.28 Mode Bit Reset (FFh or FFFFh)

For Fast Read Dual/Quad I/O operations, Mode Bits (M7-0) are implemented to further reduce instruction overhead. By setting the Mode Bits (M7-0) to "Ax" hex, the next Fast Read Dual/Quad I/O operation does not require the BBh/EBh instruction code (See 10.2.12 Fast Read Dual I/O and 10.2.13 Fast Read Quad I/O for detail descriptions).

If the system controller is Reset during operation it will likely send a standard SPI instruction, such as Read ID (9Fh) or Fast Read (0Bh), to the 25Q16/32/80. However, as with most SPI Serial Flash memories, the 25Q80/16/32 does not have a hardware Reset pin, so if Mode bits are set to "Ax" hex, the 25Q80/16/32 will not recognize any standard SPI instructions. To address this possibility, it is recommended to issue a Mode Bit Reset instruction as the first instruction after a system Reset. Doing so will release the Mode Bits for the "Ax" hex state and allow Standard SPI instructions to be recognized. The Mode Bits Reset instruction is shown in figure 29.

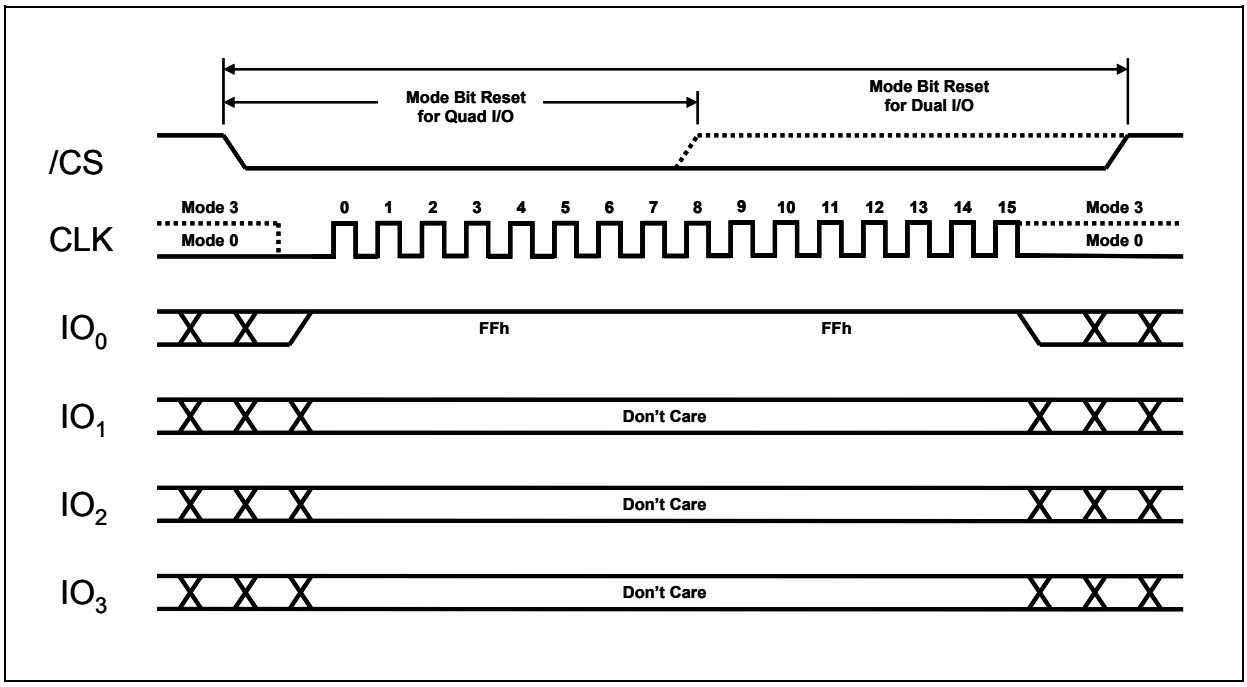


Figure 29. Mode Bit Reset for Fast Read Dual/Quad I/O

To reset Mode Bit during Quad I/O operation, only eight clocks are needed. The instruction is "FFh". To reset Mode Bit during Dual I/O operation, sixteen clocks are needed to shift in instruction "FFFFh".

11. ELECTRICAL CHARACTERISTICS (PRELIMINARY) (4)

11.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.0	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).
4. See preliminary designation at the end of this datasheet.

11.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	F_R = 80MHz, f_R = 50MHz	2.7	3.6	V
Ambient Temperature, Operating	TA	Commercial	0	+70	°C
		Industrial	–40	+85	

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

11.3 Endurance and Data Retention

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Erase/Program Cycles	4KB sector, 32/64KB block or full chip.	100,000		cycles
Data Retention	55°C		20	years

11.4 Power-up Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}(1)	10		µs
Time Delay Before Write Instruction	t_{PUW}(1)	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1	2	V

Note:

1. These parameters are characterized only.

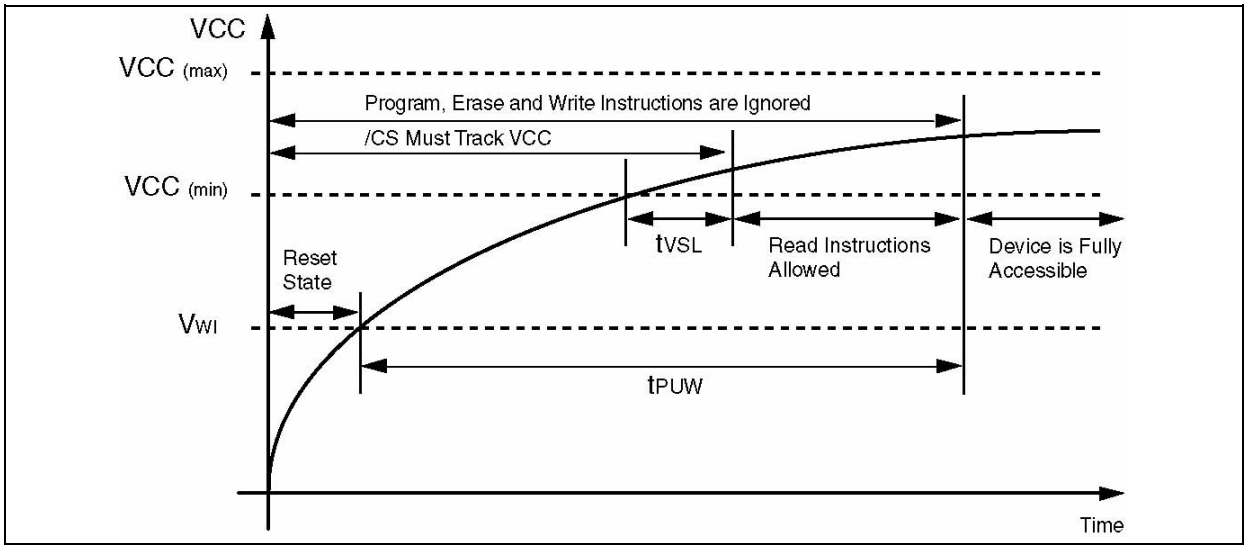


Figure 30. Power-up Timing and Voltage Levels

11.5 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(2)			6	pF
Output Capacitance	Cout(1)	V_{OUT} = 0V(2)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		25	50	µA
Power-down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		1	5	µA
High performance current	I_{CC3}	After enable High Performance mode		50	100	µA
Current Read Data / Dual /Quad 1MHz(2)	I_{CC4}	C = 0.1 VCC / 0.9 VCC DO = Open		4/5/6	6/7.5/9	mA
Current Read Data / Dual /Quad 33MHz(2)	I_{CC4}	C = 0.1 VCC / 0.9 VCC DO = Open		6/7/8	9/10.5/12	mA
Current Read Data / Dual /Quad 50MHz(2)	I_{CC4}	C = 0.1 VCC / 0.9 VCC DO = Open		7/8/9	10/12/13.5	mA
Current Read Data / Dual Output Read/Quad Output Read 80MHz(2)	I_{CC4}	C = 0.1 VCC / 0.9 VCC DO = Open		10/11/12	15/16.5/18	mA
Current Write Status Register	I_{CC6}	/CS = VCC		8	12	mA
Current Page Program	I_{CC7}	/CS = VCC		20	25	mA
Current Sector/Block Erase	I_{CC8}	/CS = VCC		20	25	mA
Current Chip Erase	I_{CC9}	/CS = VCC		20	25	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA=25° C, VCC 3V.
2. Checker Board Pattern.

11.6 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 VCC to 0.8 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

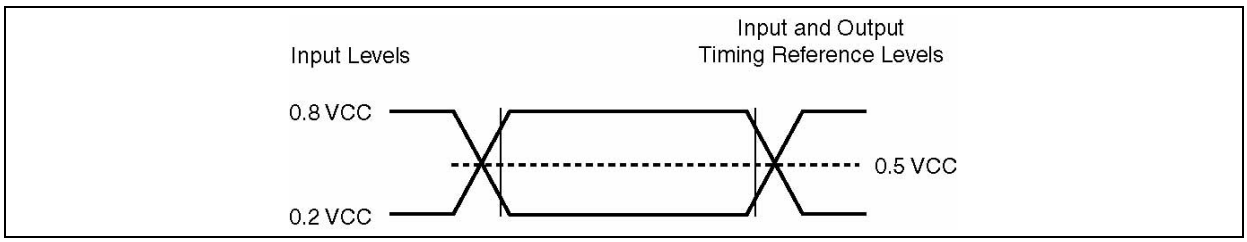


Figure 31. AC Measurement I/O Waveform

11.7 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for all instructions, except Read Data (03h) 2.7V-3.6V VCC & Industrial Temperature	F_R	f_C	D.C.		80	MHz
Clock freq. Read Data instruction (03h)	f_R		D.C.		50	MHz
Clock High, Low Time except Read Data (03h)	t_{CLH}, t_{CLL}(1)		6/7			ns
Clock High, Low Time for Read Data (03h) instruction	t_{CRLH}, t_{CRLL}(1)		8			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	5			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		5			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		5			ns
/CS Deselect Time (for Array Read → Array Read / Erase or Program → Read Status Registers)	t_{SHSL}	t_{CSH}	10/50			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			7	ns
Clock Low to Output Valid 2.7V-3.6V / 3.0V-3.6V	t_{CLQV1}	t_{V1}			7 / 6	ns
Clock Low to Output Valid (for Read ID instructions) 2.7V-3.6V / 3.0V-3.6V	t_{CLQV2}	t_{V2}			8.5 / 7.5	ns
Output Hold Time	t_{CLQX}	t_{HO}	0			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns

Continued – next page

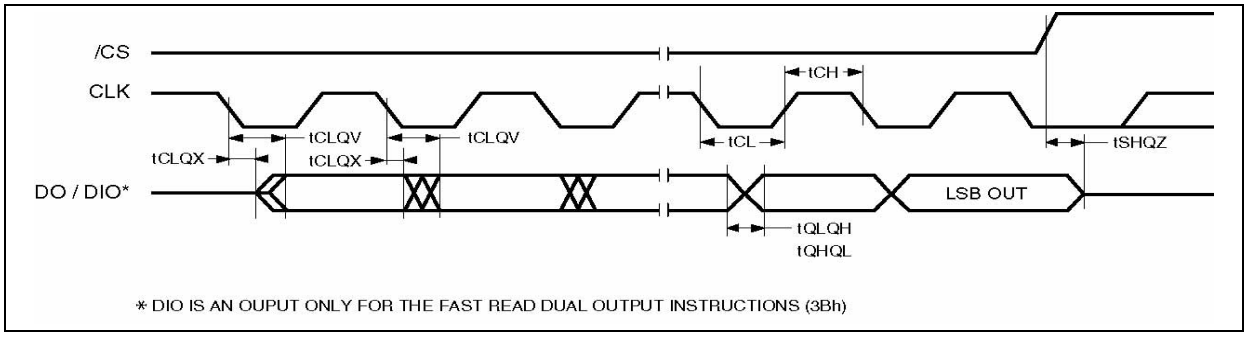
11.8 AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			7	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without Electronic Signature Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with Electronic Signature Read	t_{RES2}(2)				1.8	µs
/CS High to next Instruction after Suspend	t_{SUS}(2)				20	µs
Write Status Register Time	t_W			10	15	ms
Byte Program Time (First Byte) (5)	t_{BP1}			30	50	µs
Additional Byte Program Time (After First Byte) (5)	t_{BP2}			6	12	µs
Page Program Time	t_{PP}			1.5	3	ms
Sector Erase Time (4KB)	t_{SE}			120	200	ms
Block Erase Time (32KB)	t_{BE_1}			0.5	1	s
Block Erase Time (64KB)	t_{BE_2}			0.75	1.5	s
Chip Erase Time W25Q80 Chip Erase Time W25Q16 Chip Erase Time W25Q32	t_{CE}			12 25 50	25 40 80	s s s

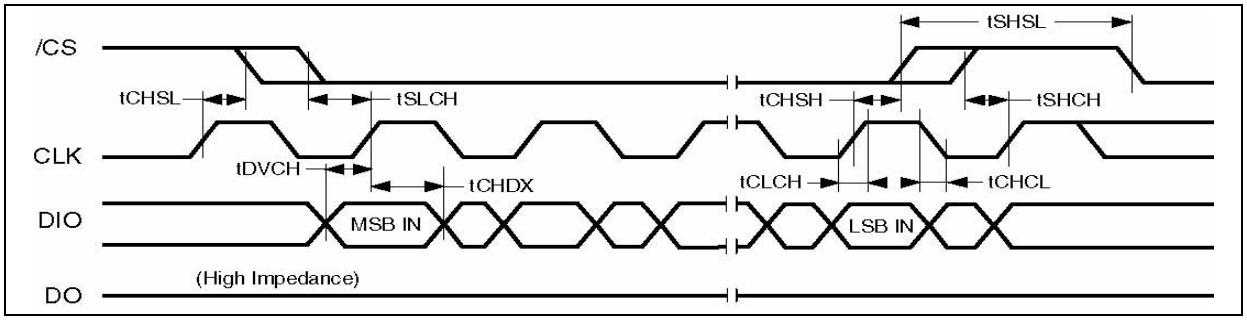
Notes:

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.
4. Commercial temperature only applies to Fast Read (F_{R0} & F_{R1}). Industrial temperature applies to all other parameters.
5. For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.

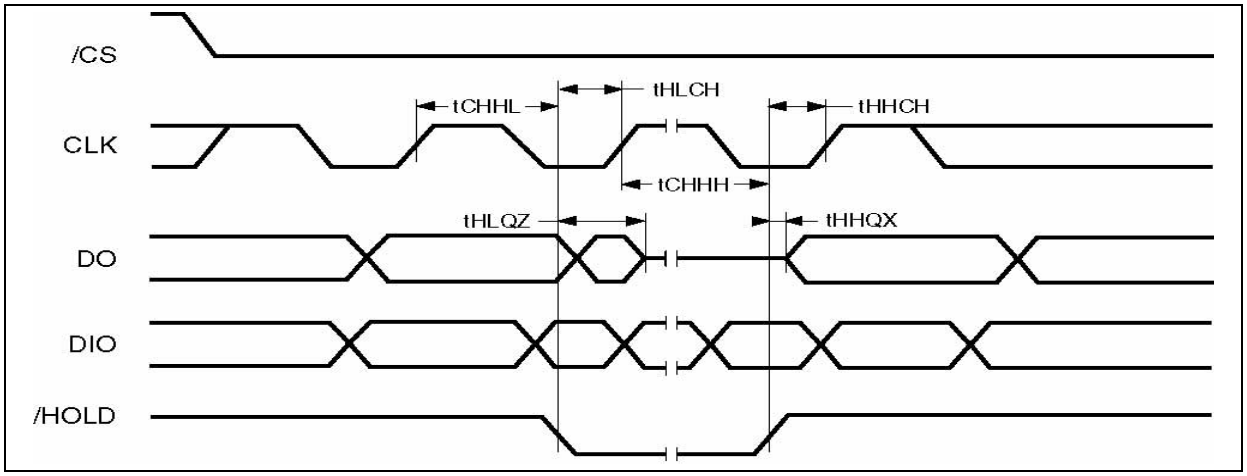
11.9 Serial Output Timing



11.10 Input Timing

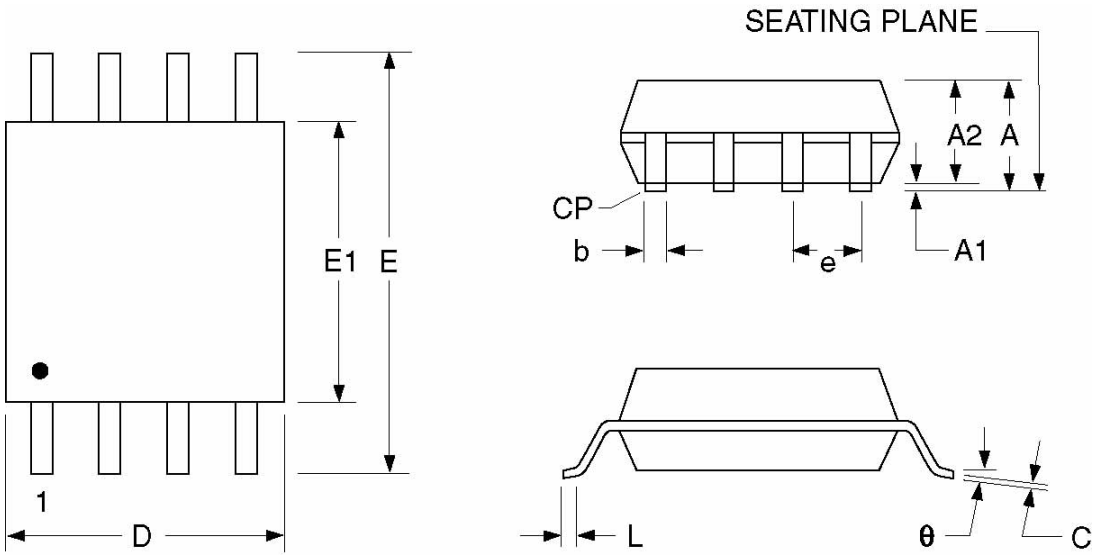


11.11 Hold Timing



12. PACKAGE SPECIFICATION

12.1 8-Pin SOIC 208-mil (Package Code SS)

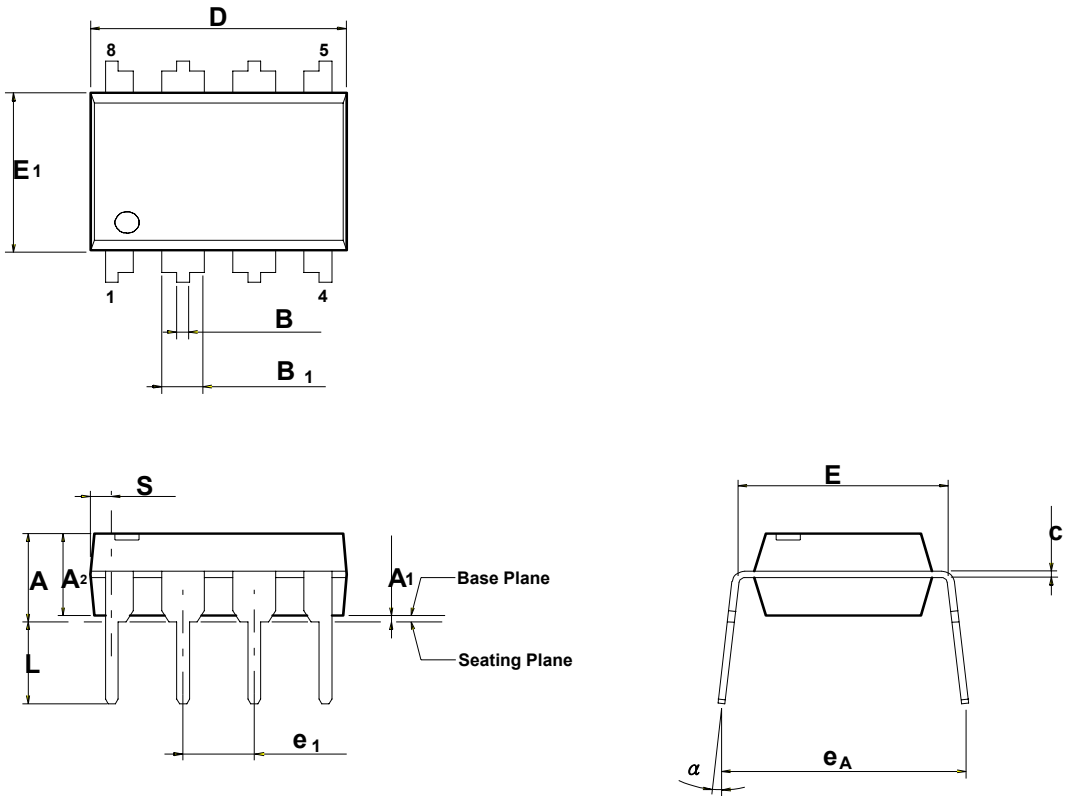


SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.75	2.16	0.069	0.085
A1	0.05	0.25	0.002	0.010
A2	1.70	1.91	0.067	0.075
b	0.35	0.48	0.014	0.019
C	0.19	0.25	0.007	0.010
D	5.18	5.38	0.204	0.212
E	7.70	8.10	0.303	0.319
E1	5.18	5.38	0.204	0.212
e	1.27 BSC		0.050 BSC	
L	0.50	0.80	0.020	0.031
θ	0°	8°	0°	8°
y	---	0.10	---	0.004

Notes:

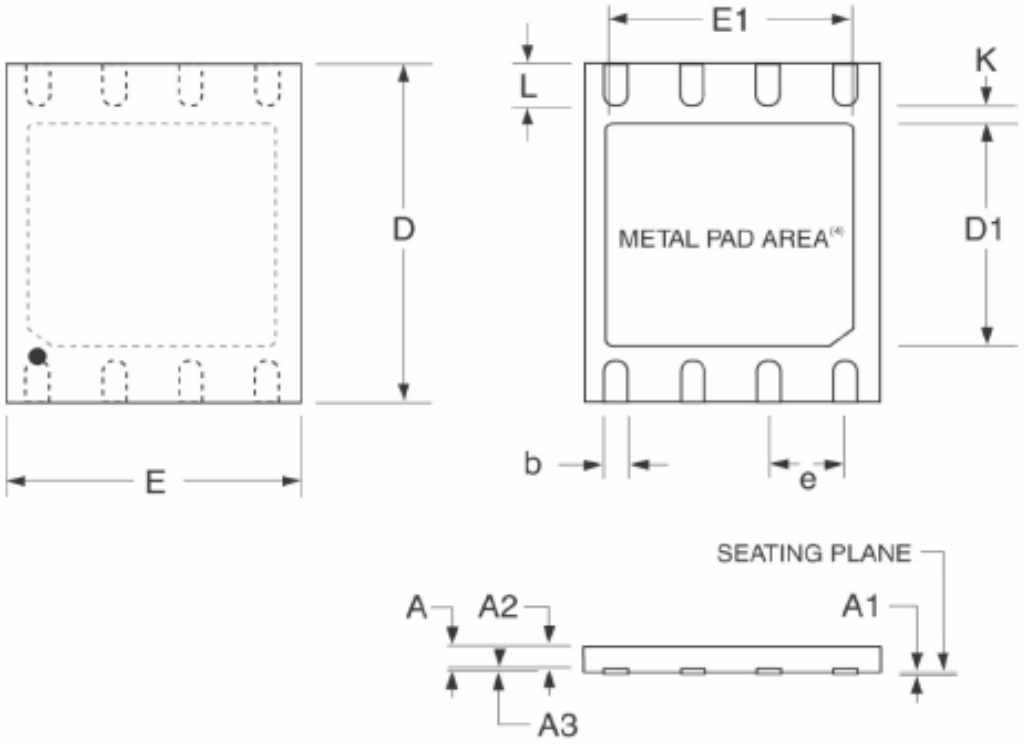
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within .0004 inches at the seating plane.

12.2 8-Pin PDIP 300-mil (Package Code DA)



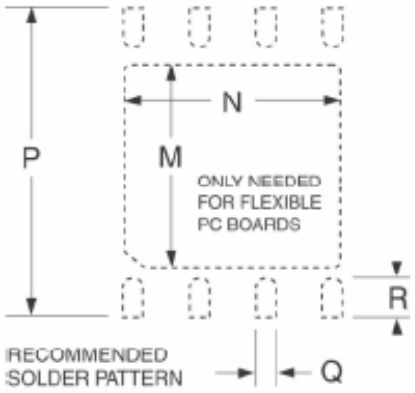
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.360	0.380	—	9.14	9.65
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.045	—	—	1.14

12.3 8-contact 6x5 WSON (Package Code ZP)



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	0.02	0.05	0.0000	0.0008	0.0019
A2		0.55			0.0126	
A3	0.19	.0.20	0.25	0.0075	0.0080	0.0098
b	0.36	0.40	0.48	0.0138	0.0157	0.0190
D(3)	5.90	6.00	6.10	0.2320	0.2360	0.2400
D1	3.30	3.40	3.50	0.1299	0.1338	0.1377
E	4.90	5.00	5.10	0.1930	0.1970	0.2010
E1(3)	4.20	4.30	4.40	0.1653	0.1692	0.1732
e(2)	1.27 BSC			0.0500 BSC		
K	0.20			0.0080		
L	0.50	0.60	0.75	0.0197	0.0236	0.0295

12.4 8-contact 6x5 WSON Cont'd.

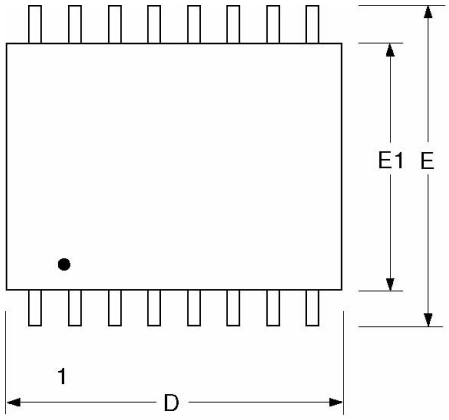


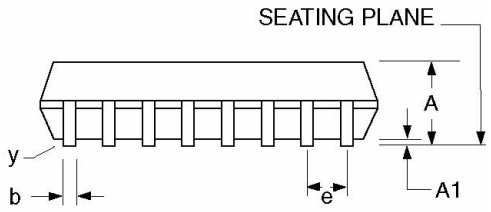
SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
SOLDER PATTERN						
M		3.40			0.1338	
N		4.30			0.1692	
P		6.00			0.2360	
Q		0.50			0.0196	
R		0.75			0.0255	

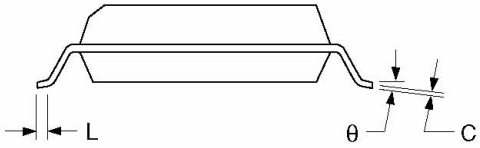
Notes:

1. Advanced Packaging Information; please contact Winbond for the latest minimum and maximum specifications.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. The metal pad area on the bottom center of the package is connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

12.5 16-Pin SOIC 300-mil (Package Code SF)





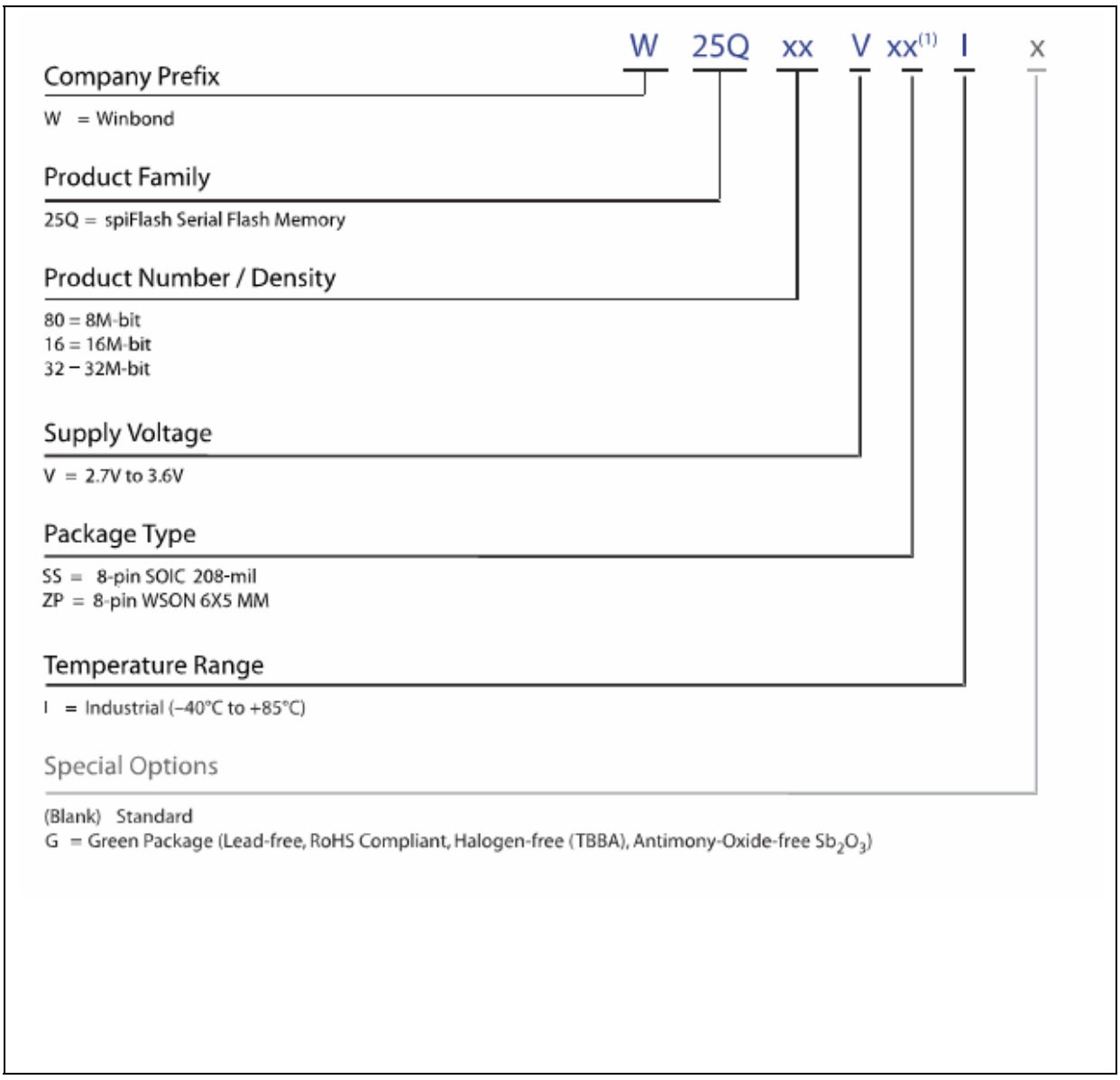


SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.36	2.64	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
C	0.18	0.28	0.007	0.011
D(3)	10.08	10.49	0.397	0.413
E	10.01	10.64	0.394	0.419
E1(3)	7.39	7.59	0.291	0.299
e(2)	1.27 BSC		0.050 BSC	
L	0.39	1.27	0.015	0.050
θ	0°	8°	0°	8°
y	---	0.076	---	0.003

Notes:

1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.

13. ORDERING INFORMATION [1]



Notes:

1a. Only the 2nd letter is used for the part marking.

1b. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T), when placing orders.

1c. The "W" prefix is not included on the part marking.

13.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the 25Q80/16/32 SpiFlash Memories. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use an 11-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages use an abbreviated 9-digit number.

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SS SOIC-8 208mil	8M-bit	W25Q80VSSIG	25Q80VSIG
	16M-bit	W25Q16VSSIG	25Q16VSIG
	32M-bit	W25Q32VSSIG	25Q32VSIG
SF SOIC-16 300mil	16M-bit	W25Q16VSFIG	25Q16VFIG
	32M-bit	W25Q32VSFIG	25Q32VFIG
ZP WSON-8 6x5mm	8M-bit	W25Q80VZPIG	25Q80VPIG
	16M-bit	W25Q16VZPIG	25Q16VPIG

14. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	10/20/06		New Create Advanced
A1	11/9/06	Various	Figures 2, 3A-B, 13A–14C, 16, 24, 25 Table 10.2.2: Write Status Reg 1 and 2 Erase Suspend 10.2.21 tCHSH, tSHCH = 5nS
A2	11/15/06	49	tSHSL = 10ns for Read & 50ns for Write, Erase and Program instructions
A3	2/22/07	20, 45, 49 & 57	Removed Burst Read Quad I/O Instruction. Updated ordering Information. Added transient voltage specification.
A4	4/20/07	19, 28, 30 & 45	Added Mode Bit Reset instruction and description.
A5	6/20/07	13, 15-17 & 23	Added note for SRP1,0 status during Power Lock-Down protection. Updated Status Register memory protection tables.
B	9/26/07	5, 11, 13, 15-17, 19, 35, 36, 43, 45-47, 50 & 59	Updated Instruction Diagrams. Updated Status Register memory protection tables. Added note for Power Lock-Down, OTP functions. Added note for 64 Bit unique ID. Added note for 32KB/64KB block erase command. Updated Mode Bit Reset command description. Updated data retention temperature. Updated tSHSL description, added tCLQV2. Updated tBP1.

Preliminary Designation

The “Preliminary” designation on a Winbond SpiFlash memory datasheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. Winbond or an authorized sales representative should be consulted for current information before using this product.

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