9338,DM9338

9338/DM9338 8-Bit Multiple Port Register

Literature Number: SNOS383A

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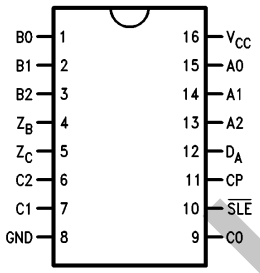
9338/DM9338 8-Bit Multiple Port Register

General Description

The DM9338 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously.

Connection Diagrams

Dual-In-Line Package



TL/F/9794–1

Order Number 9338DMQB, 9338FMQB or DM9338N
See NS Package Number J16A, N16E or W16A

Pin Names	Description
A0–A2	Write Address Inputs
D_A	Data Input
B0–B2	B Read Address Inputs
C0–C2	C Read Address Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SLE}$	Slave Enable Input (Active LOW)
Z_B	B Output
Z_C	C Output

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_A to CP	20 12			20 12			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_A to CP	0 −8.0			0 −8.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to CP	10 10			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to CP	0 0			0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	23 13			23 13			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				27	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−10		−70	mA
			COM	−10		−70	
I_{CC}	Supply Current	V_{CC} = Max				135	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

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Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF				Units
		9338 (MIL)		DM9338 (COM)		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay		40	13	40	ns
t_{PHL}	B_n or C_n to Z_n		35	18	35	
t_{PLH}	Propagation Delay		45	25	45	ns
t_{PHL}	D_A to Z_n		50	25	50	
t_{PLH}	Propagation Delay		35	18	35	ns
t_{PHL}	CP to Z_n		30	13	30	

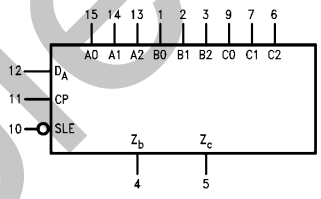
Functional Description

The 9338 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A0–A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B0–B2 and C0–C2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ($\overline{SLE}$), the slave latches are continuously enabled. The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

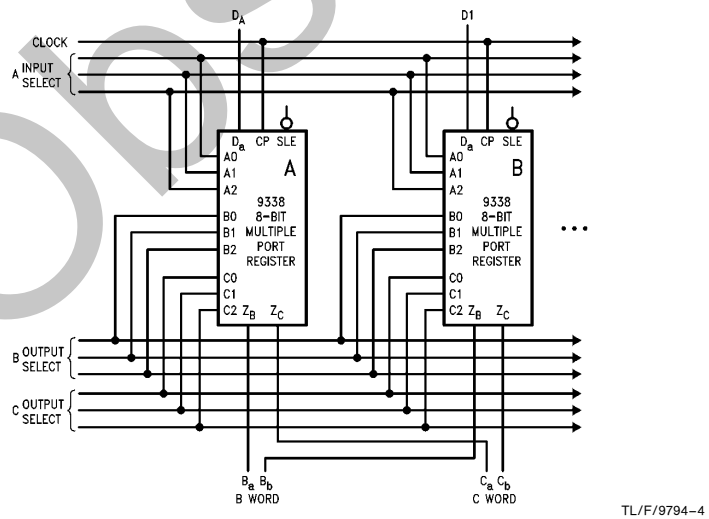
The method of parallel expansion is shown in *Figure a*. One 9338 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

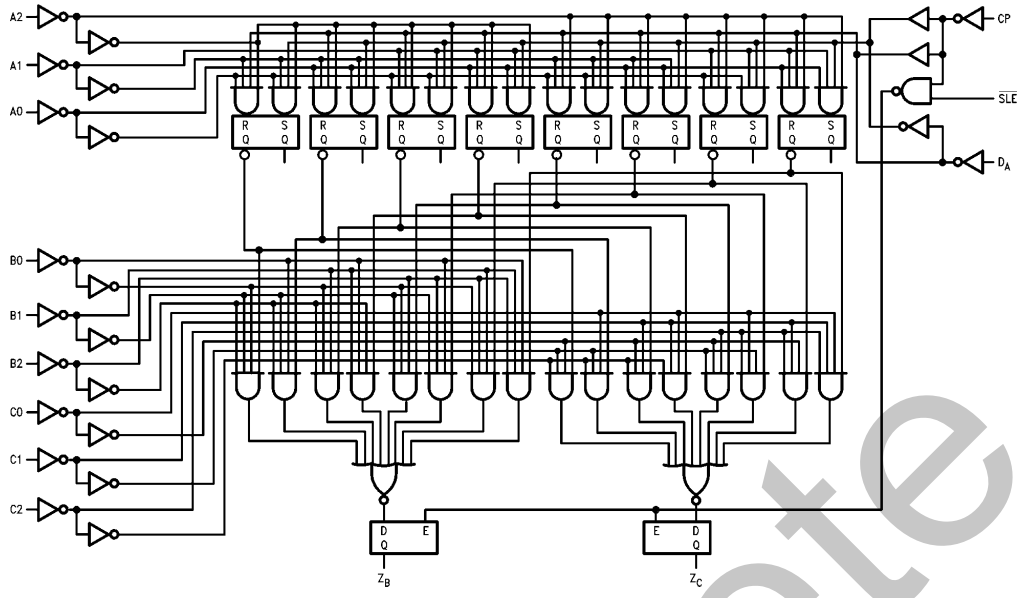


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FIGURE a. Parallel Expansion

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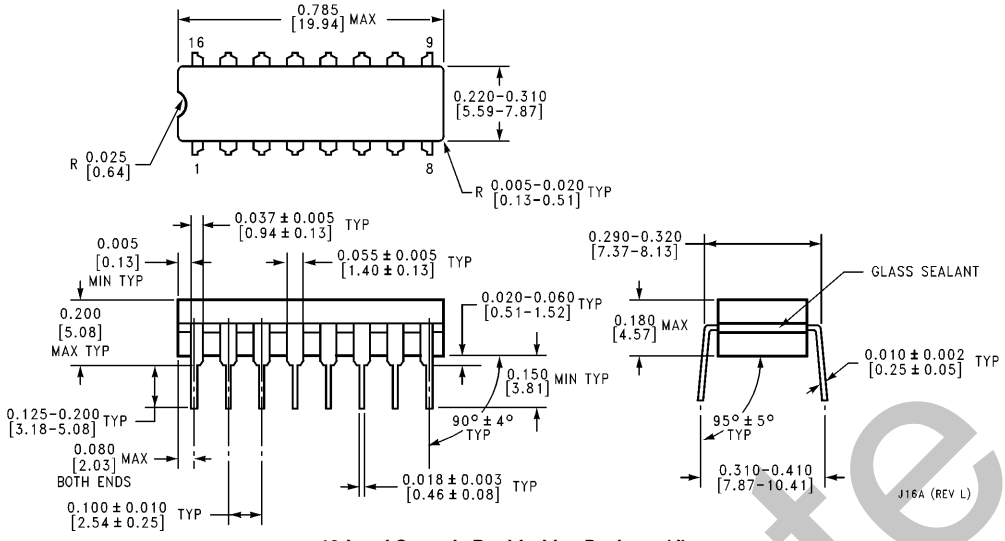
Logic Diagram



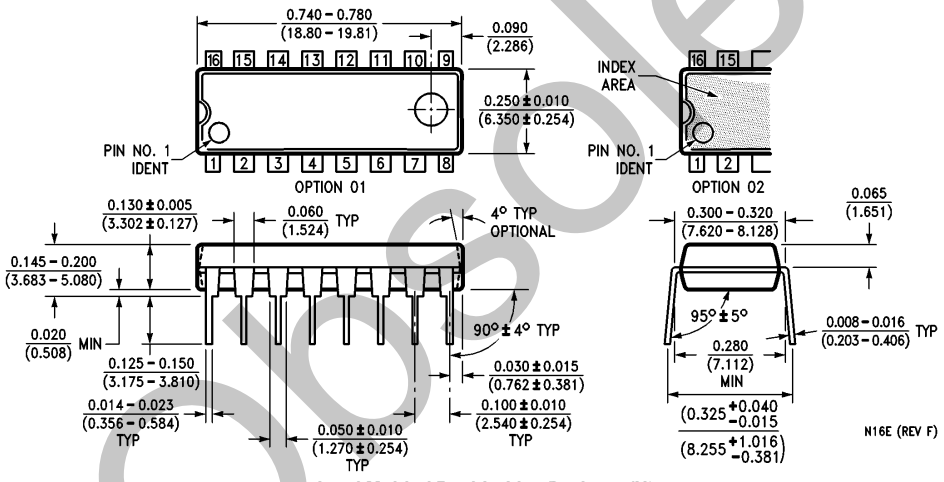
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Physical Dimensions inches (millimeters)



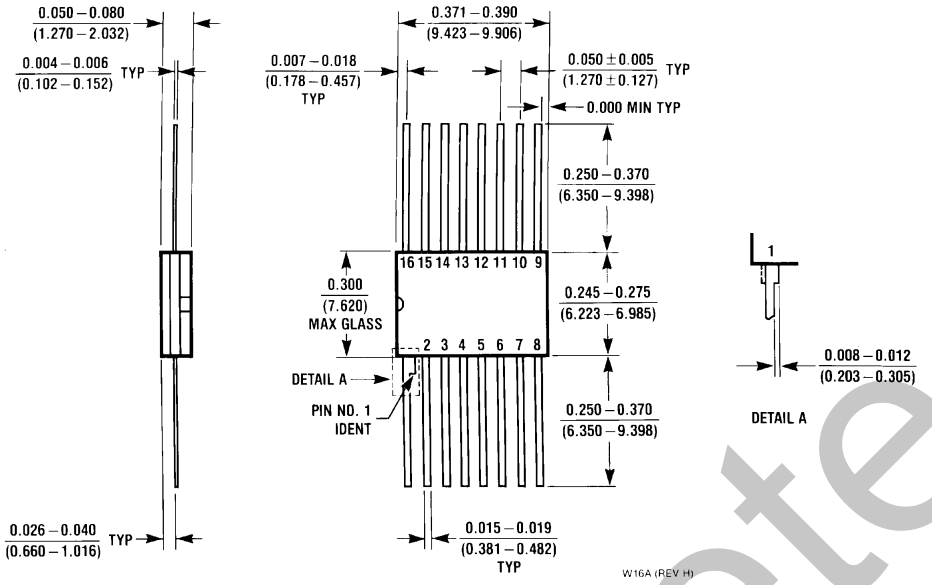
16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9338DMQB
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9338N
NS Package Number N16E

Obsolete

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9338FMQB
NS Package Number W16A

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