W163

Spread Aware™, Zero Delay Buffer

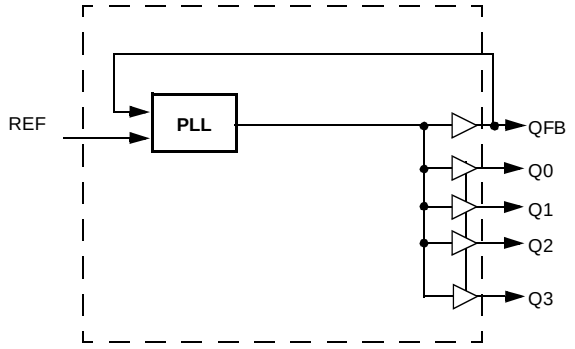
Features

- **Spread Aware™—designed to work with SSFTG reference signals**
- **Outputs may be three-stated**
- **Available in 8-pin SOIC package**
- **Extra strength output drive available (-15 version)**
- **Internal feedback maximized the number of outputs available in 8-pin package**

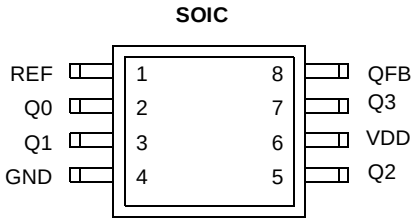
Key Specifications

Operating Voltage: .....3.3V±10%
Operating Range: ..... $10 < f_{OUT} < 133$ MHz
Cycle-to-Cycle Jitter: .....200 ps
Output-to-Output Skew: .....250 ps
Device-to-Device Skew:.....700 ps
Propagation Delay:.....350 ps

Block Diagram



Pin Configuration



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Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
REF	1	I	***Reference Input:*** The output signals Q0:3 will be synchronized to this signal unless the device is programmed to bypass the PLL.
Q0:3	2, 3, 5, 7	O	***Outputs:*** These signals will be synchronous and of equal frequency to the signal input at pin 1.
QFB	8	O	***Feedback Output:*** This output signal does not vary from signals Q0:3 in function, but is noted as the signal used to establish the propagation delay of nearly 0.
VDD	6	P	***Power Connections:*** Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	4	P	***Ground Connections:*** Connect all grounds to the common system ground plane.

Overview

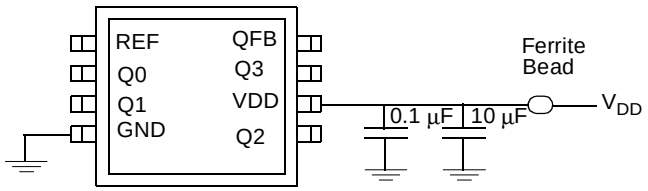
The W163 products are five-output zero delay buffers. A Phase-Locked Loop (PLL) is used to take a time-varying signal and provide five copies of that same signal out. The internal feedback to the PLL provides outputs in phase with the reference inputs.

Spread Aware

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress Application note titled, “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs.”

Schematic



Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: T_A =0°C to 70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current	Unloaded, 100 MHz			40	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA (-15) I_{OL} = 8 mA (-5)			0.4	V
V_{OH}	Output High Voltage	I_{OL} = 12 mA (-15) I_{OL} = 8 mA (-5)	2.4			V
I_{IL}	Input Low Current	V_{IN} = 0V			50	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			100	µA

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency		10		133	MHz
f_{OUT}	Output Frequency	15-pF load[5]	10		133	MHz
t_R	Output Rise Time (-05)[1]	2.0 to 0.8V, 15-pF load			2.5	ns
	Output Rise Time (-15)[1]	2.0 to 0.8V, 20-pF load			1.5	ns
t_F	Output Fall Time (-05)[1]	2.0 to 0.8V, 15-pF load			2.5	ns
	Output Rise Time (-15)[1]	2.0 to 0.8V, 20-pF load			1.5	ns
t_{ICLKR}	Input Clock Rise Time[1]				?	ns
t_{ICLKF}	Input Clock Fall Time[1]				?	ns
t_{PD}	FBIN to REF Skew[2, 3]	Measured at V_{DD}/2	–350	0	350	ps
t_{SK}	Output to Output Skew	All outputs loaded equally	–250	0	250	ps
t_{SKDD}	Device to Device Skew	Measured at FBIN pins, V_{DD}/2	–700	0	700	ps
t_D	Duty Cycle	15-pF load[4]	45	50	55	%
t_{LOCK}	PLL Lock Time	Power supply stable and			1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle				200	ps

Notes:

1. Longer input rise and fall time will degrade skew and jitter performance.
2. All AC specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Skew is measured at 1.4V on rising edges.
4. Duty cycle is measured at 1.4V.
5. For the higher drive -15, the load is 20 pF.

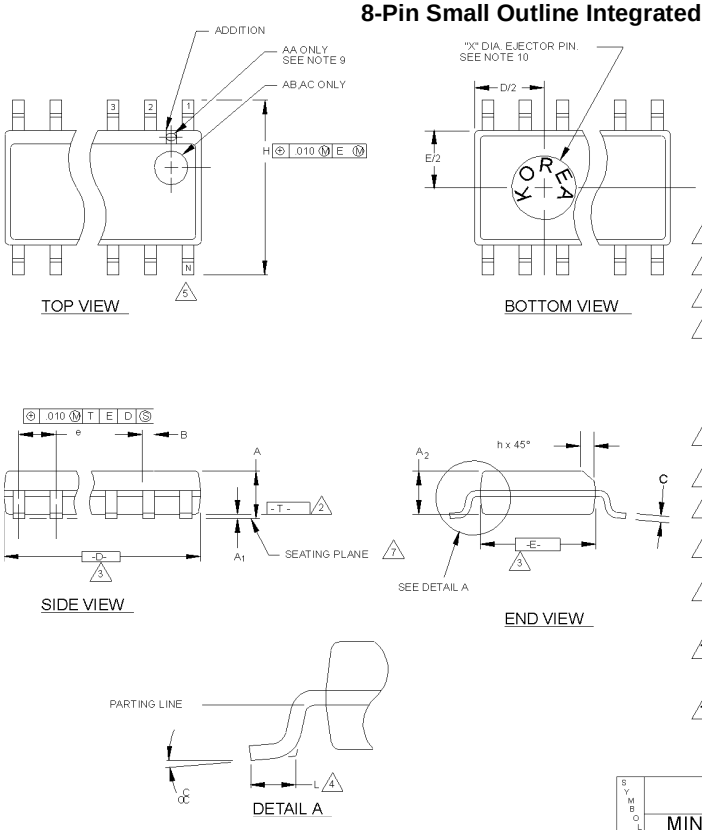
Ordering Information

Ordering Code	Option	Package Name	Package Type
W163	-05, -15	G	8-pin Plastic SOIC (150-mil)

Document #: 38-00787-*A

Package Diagram

8-Pin Small Outline Integrated Circuit (SOIC, 150-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

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