Vivado Design Suite User Guide

Release Notes, Installation, and Licensing

UG973 (v2015.4) November 18, 2015

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/18/2015	2015.4	2015.4 What's New Featuring the latest: • New Device Support. • New Vivado High-Level Design Edition Tools. • New Vivado High-Level System Edition Tools.
09/30/2015	2015.3	2015.3 What's New Featuring the latest: • New Device Support. • New Vivado High-Level Design Edition Tools. • New Vivado High-Level System Edition Tools. Latest support content in the Architecture Support and Requirements section.
06/24/2015	2015.2	2015.2 What's New, Download and Installation and Obtaining and Managing a License new content.
04/01/2015	2015.1	Featuring What's New, Download and Installation and Obtaining and Managing a License new content.

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Release Notes 2015.4

What's New

Beginning with this Vivado® Design Suite 2015.4 release, the high level synthesis tool, Vivado HLS becomes free of charge and gets included in all Vivado software editions. To denote this change, Xilinx introduces Vivado Design Suite HLx Editions. These new HLx Editions include HL System Edition, HL Design Edition and HL WebPACK™ Edition. These editions enable a new approach for designing All Programmable FPGAs, SoCs and reuseable platforms with ultra high productivity. All HLx editions include Vivado HLS high level synthesis, Vivado IP Integrator, LogicCore IP-subsystems, and the full Vivado implementation tool suite to enable mainstream users to readily adopt the most productive and advanced C and IP based design flows.

Users can realize a ten to fifteen times productivity gain over traditional approaches after adopting all or a subset of the following:

1. C based design and optimized reuse
2. Reuse of IP sub-systems
3. Integration automation
4. Accelerated design closure, as explained in the new *UltraFast™ High-Level Productivity Design Methodology Guide* (UG1197) [Ref 1].

Device Support

The following new devices are enabled for this release.

Table 1-1: **Vivado 2015.4 Device Support**

Production Level	Vivado 2015.4 Device Support
New Devices	The following UltraScale+™ devices are introduced in this release: • Zynq® UltraScale+ MPSoC devices: ◦ XCZU9EG • Kintex® UltraScale+ devices: ◦ XCKU9P
General Access	The following devices are production ready (in -1 and -2 speedgrades): • Virtex® UltraScale™ devices: ◦ XCVU125, XCVU160, XCVU190, XCVU440 The following devices are production ready (in -3 and -1L speedgrades): • Kintex® UltraScale devices: ◦ XCKU060, XCKU085, XCKU115 The following devices are production ready (in -3 speedgrades): • Virtex® UltraScale devices: ◦ XCVU160, XCVU190
Bitstream Generation	• Bitstream generation is enabled for all UltraScale devices.

Installation

Beginning with the Vivado 2015.1 release, the install program on Linux no longer requires root or sudo privileges. In the past, these privileges were required to enable cable driver installation. Now, cable drivers must be installed manually by running a separate script while in a root/sudo command shell. For more information on Linux cable driver installation, see the Installing Cable Drivers section of this document.

Vivado High-Level Design Edition Tools

Vivado HLS

The tool is now part of all the newly introduced Vivado HLx Editions, including HL WebPACK™.

This is the last release of Vivado HLS that allows targeting devices only supported by the ISE tool.



IMPORTANT: *This means that you will need to archive this current release in order to target devices such as Spartan-6 or Virtex-6 as future releases of Vivado HLS will only support devices supported by the main Vivado IDE.*

RTL Synthesis

- New RTL strategies and directives (Four new strategies, five new directives).
- Inference of the pattern detect circuitry of the DSP block to support convergent symmetric rounding.
- Automatic inference of shifters onto RAM blocks through new directive `AreaMapLargeShiftRegToBRAM`.
- Inference of the new UltraScale RAMs (UltraRAM).
- Pipelining for cascaded RAMB36E2 and UltraRAM, allowing fast performance while saving multiplexing logic and reduce power.
- New RTL attribute to control the number of RAM block cascaded with `CASCADE_HEIGHT`.

Partial Reconfiguration

- Expanded support for UltraScale devices.
    - Partial bit file generation is now enabled for production silicon for all supported devices, bringing the total number of devices enabled for bitstreams up to twelve.
        - Bitstream generation is disabled by default for all ES silicon.
- For more information, see this link in the *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909) [Ref 5].

Tandem Configuration

- Expanded support for UltraScale devices.
    - Partial bit file generation is now enabled for production silicon for all supported devices save for the KU440, bringing the total number of devices enabled for bitstreams to twelve.
        - Bitstream generation is disabled by default for all ES silicon and production silicon that has not completed verification testing.
- IP generation for Tandem with Field Updates is enabled for all devices that support Tandem Configuration, but place and route is gated, as the flow is still in a beta phase. Contact Xilinx Support to request access.
- For more information on Tandem Configuration, see the *UltraScale Architecture Gen3 Integrated Block for PCI Express Product Guide* (PG156) v4.1.

Vivado Physical Implementation and Power Tools

- The `report_design_analysis` command now has a GUI in the Vivado IDE that supports timing, complexity, and congestion analysis with cross-probing to other

design views such as the device view and schematics. The GUI can be launched either from the **Tools > Report** menu or by using the `-name` option.

- The `report_design_analysis` command can report a list of paths that are critical at both the current design stage and prior stage. This provides a way to check on which critical paths the tools focus at each stage. The `config_design_analysis` command enables this new feature.
- A new command `report_pipeline_analysis` evaluates potential design performance improvements by hypothetically adding latency (pipeline stages) to the design and reporting the new resulting Fmax. The analysis includes loop detection, per-clock analysis, and in-context module analysis.
- The `phys_opt_design` optimizations in a design run can be saved and executed earlier in the design flow to improve the overall design performance.
  - Each optimization such as a fanout optimization or BRAM register optimization is expressed using the new `iphys_opt_design` Tcl command.
  - Writing and reading optimizations are handled using new Tcl commands `write_iphys_opt_tcl` and `read_iphys_opt_tcl` respectively.
- There are new place and route directives for UltraScale designs that experience congestion, available by Tcl only.

  Note: Please note UG904 incorrectly describes the degrees of spreading for each directive. That will be corrected in the next release.

  - `place_design` directives provide low, medium, and high degrees of logic spreading:
    - `AltSpreadLogic_low`
    - `AltSpreadLogic_medium`
    - `AltSpreadLogic_high`
  - `route_design` has a single directive: AlternateCLBRouting
- The `CLOCK_DELAY_GROUP` is a new net property that can be assigned to related clocks that have the same MMCM or PLL source to reduce clock skew on timing paths between the clocks.
- The `CLOCK_ROOT` net property has been replaced by the `USER_CLOCK_ROOT` property:
  - `USER_CLOCK_ROOT` is a writable and readable property for assigning a clock root to a clock region. Assigning `CLOCK_ROOT` will automatically assign `USER_CLOCK_ROOT` instead but also result in a warning that assigning `CLOCK_ROOT`.
  - `CLOCK_ROOT` is now a read-only net property that reflects the clock root of a clock net.
- When targeting UltraScale devices, some block RAM power optimization is enabled by default in `opt_design` with further optimization available in `power_opt_design`.

- UltraScale XPE now provides three selections for Power Optimization on the Summary sheet:
  - None: No power optimization.
  - Default: BRAM power estimation matches the default set of optimizations in `opt_design`.
  - Power Optimization: BRAM power estimation matches the full set of optimizations of opt_design followed by `power_opt_design`.
- The `report_synchronizer_mtbf` command now includes MTBF of FIFO primitives.

PS Power Reports

- Signal Power Accuracy:
  - Vivado `report_power` includes significant improvements in signal power accuracy, resulting in much better correlation between `report_power` and XPE.
  - Signal power is tracked on the XPE Logic sheet using a new column **Routing Complexity** which indicates the average routing resources per logic cell. The default value is 8 and high complexity is 10. A value of 12 is very high, typically used for designs that experience routing congestion. When importing results from `report_power`, Routing Complexity is also imported based on the design's routing.
- Regarding overall PS power reported, there is a discrepancy (in static power only) of a few percent between the values from the Processor Configuration Wizard and the values reported by the power tools: XPE and Vivado Report Power.
- Use the power tools (XPE and Vivado Report Power) to calculate the most accurate power estimation of the PS. This issue will be addressed in the 2016.1 Vivado release.

Vivado IP Integrator - PCIe Designer Assistance

- Support for XDMA with KCU105 hardware.
- Requires XDMA license.

Vivado IP Integrator

- Easy access to IP Example designs from IP Integrator added to right-click menu.
- Enhanced configurable example design including option to configure MicroBlaze.

Vivado Simulator

- Up to 3 times elaboration runtime performance improvement.
- Enhanced waveform debug experience.

- Improved simulator relaunch feature.
  - Retains GUI, breakpoint, signal settings, and markers.

Vivado Simulation Flow

- IP simulation made easy:
  - IP generation creates simulation scripts for all simulators.
  - Clear separation of files reused by IP (Static Files).Vivado Debug
- Enumerated type support for ILA probe values.
- Data or trigger (or both) support for ILA probe type.
- Instance names preservation.
- Robustness of HW connections.
- Enhanced margin analysis support for DDR4/DDR3.

Vivado Programmer

- Ability to generate SVF (Serial Vector Format) files.
- Capability to verify checksum of configuration memory devices.
- Improved robustness of HW connections.

Vivado High-Level System Edition Tools

Vivado System Generator for DSP

- Support for MATLAB 2015B includes tighter integration allowing HDL Coder to automate the generation of a combined model containing high level RTL and target optimized IP.
- Simplified IPs enable up-conversion, down-conversion, and standard digital signal processing designs to deliver high quality of results and performance while minimizing the interfaces and number of parameters required to configure the IP. New IPs include Digital FIR Filter, Sine Wave generator, Product, and Requantize block.
- JTAG co-simulation support for Virtex-7, Kintex-7, Artix-7, and Zynq-7000 families are enhanced and can utilize burst mode to improve performance by 45x.
- Improved launch times and better cross-probing support for the Waveform Viewer and Timing Analyzer aid in the debugging of logic and visualizing timing critical paths.

Important Information

Updates to Existing IP

The following table lists current updates to existing IP for the 2015.4 release.

Table 1-2: **Existing IP Updates**

Existing IP	Existing IP Updates
10G/25G Ethernet Subsystem	• Supports UltraScale+™ • Updated to revision 1.6 of 25G and 50G Consortium Specification
PCI Express®	• AXI-MM support for Gen3 PCI Express hard block (Virtex7 XT/HT). • Package Migration section in User Guide for UltraScale FPGA devices. • Tandem PCIe/PROM support (Beta) for UltraScale FPGA devices. • Upgraded GT Wizard • GUI options update to select PLL and Core Clocks • Additional devices/packages supported for Tandem PCIe®
Aurora	• Additional UltraScale FPGA device support. • Simulation support with Labtools enabled. • AXI4-Lite to DRP interface compliance (Aurora 64B/66B). • Extending line rate to 16.375G support • Grouping of flow control interface and making AXI4-ST compliant • Enable lane location selection though GUI
IBERT for UltraScale	• An issue that may cause the under-reporting of errors has been fixed in all UltraScale IBERT cores. • It is necessary for users who are performing very long tests or deep scans to re-generate the IP. • Upgrade is highly recommended for all other cases (see details in Answer Record 63768).

Device Support

The following devices have been removed from this release of Vivado to align with the silicon availability plan:

- Virtex UltraScale: The VU095 ES1 parts are not supported in this release and beyond.

VIPP

- New core for Video Test pattern generator (Version 7).
  - Resolutions up to 4K60.
  - Version 6 replacement.

- Pre production release of Video processing subsystem.
  - New IP subsystem to do video format conversion. It will replace VIPP cores eventually.
  - Capable handling standard definition video to 4k60 video processing.
  - Functions include deinterlacing, scaling, color space conversion, and correction, chroma re sampling and frame rate conversion.
- Video in and Video out bridges.
  - Improved timing to support 4K60 in 2 –pixel wide mode.

DisplayPort LogiCore V6.1

- Addition of DP159 control to Displayport.

Physical Implementation and Power Tools - Known Issues

- When using `report_design_analysis` at the Tcl console or in the IDE to analyze congestion, router congestion data is lost when saving and reopening a design, or when saving and opening a checkpoint. The result is that router congestion is missing from the report. To work around this issue, you must run `report_design_analysis` in the same session as `route_design` so that the router congestion data is stored in memory. This will be addressed in a future release.
- The `report_pipeline_analysis` may recommend adding pipeline stages within Xilinx IP boundaries, which are not typically accessible. To workaround this issue, use the `top_level_cell` or clocks options to limit the scope of pipeline analysis. This will be addressed in a future release.

Vivado Design Suite Documentation Update

In the 2015.4 Vivado Design Suite Documentation release not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2015.4 documentation suite.

Licensing

Activation licensing is not supported for USB dongles, on floating servers running SOLARIS OS, or on triple-redundant server configurations.

IP Known Issues and Change List

For Xilinx IP known issues, see the *IP Release Notes Guide* (XTP025) [Ref 9].

32-bit OS Support Removal

Beginning with Vivado 2015.1, 32-bit Operating System and application support has been removed for all design entry and implementation flows. The 32-bit support on Windows 7 and Red Hat Enterprise Linux 6 will remain for Vivado 2015.1 Lab Edition. Lab Edition is a free suite of tools for programming and debug.

Known Issues

Vivado® Design Suite Tools Known Issues can be found at Answer Record 63538.

Architecture Support and Requirements

Operating Systems

Xilinx only supports the following operating systems on x86 and x86-64 processor architectures.

Microsoft Windows Support

- Windows 7 and 7 SP1 Professional (64-bit), English/Japanese.
- Windows 8.1 Professional (64-bit), English/Japanese.
- Vivado® Lab Edition is the only Xilinx toolset that supports Windows 7 SP1 Professional, 32-bit Operating System. Lab Edition also supports the 64-bit systems.

Linux Support

- Red Hat Enterprise Workstation 7.0 (64-bit)
- Red Hat Enterprise Workstation 6.5-6.6 (64-bit)
- Red Hat Enterprise Workstation 5.10 (64-bit)
- SUSE Linux Enterprise 11.3 and 12.0 (64-bit)
- Cent OS 6.6 and 7.0 (64-bit)
- Ubuntu Linux 14.04.2 LTS (64-bit)
- Vivado Lab Edition is the only Xilinx toolset that supports the Red Hat Enterprise Workstation 6.5-6.6, 32-bit Operating Systems. Lab Edition also supports the 64-bit systems.

Architectures

The following table lists architecture support for commercial products in the Vivado® Design Suite WebPACK™ tool versus all other Vivado Design Suite editions. For non-commercial support:

- All Xilinx® Automotive devices are supported in the Vivado Design Suite WebPACK tool.
- Xilinx Defense-Grade FPGA devices are supported where their equivalent commercial part sizes are supported.

Table 2-1: **Architecture Support**

	Vivado WebPACK Tool	Vivado Design Suite (All Other Editions)
Zynq® Device	Zynq®-7000 AP SoC Device • XC7Z010, XC7Z015, XC7Z020, XC7Z030	Zynq-7000 AP Soc Device • All
Virtex® FPGA	Virtex-7 FPGA • None Virtex UltraScale FPGA • None	Virtex-7 FPGA • All Virtex UltraScale FPGA • All
Kintex® FPGA	Kintex-7 FPGA • XC7K70T, XC7K160T Kintex UltraScale FPGA • None	Kintex-7 FPGA • All Kintex UltraScale FPGA • All
Artix® FPGA	Artix-7 FPGA • XC7A15T, XC7A35T, XC7A50T, XC7A75T, XC7A100T, XC7A200T	Artix-7 FPGA • All

Compatible Third-Party Tools

Table 2-2: **Compatible Third-Party Tools**

Third-Party Tool	Red Hat Linux	Red Hat Linux-64	SUSE Linux	Windows-7 32-bit	Windows-7 64-bit	Ubuntu
Simulation						
Mentor Graphic ModelSim SE/DE/PE (10.4b)	Yes	Yes	Yes	Yes	Yes	N/A
Mentor Graphics Questa Advanced Simulator(10.4b)	Yes	Yes	Yes	Yes	Yes	N/A
Cadence Incisive Enterprise Simulator (IES) (14.20.006)	Yes	Yes	Yes	N/A	N/A	N/A

Table 2-2: **Compatible Third-Party Tools**

Third-Party Tool	Red Hat Linux	Red Hat Linux-64	SUSE Linux	Windows-7 32-bit	Windows-7 64-bit	Ubuntu
Synopsys VCS and VCS MX (J-2014.12-SP2)	Yes	Yes	Yes	N/A	N/A	N/A
The MathWorks MATLAB® and Simulink® with Fixed-Point Toolbox (2014a, 2014b, 2015a, and 2015b)	Yes	Yes	N/A	Yes	Yes	Yes
Aldec Active-HDL (10.2SP2)[a]	N/A	N/A	N/A	Yes	Yes	N/A
Aldec Riviera-PRO (2015.06)	Yes	Yes	Yes	Yes	Yes	N/A
Synthesis[b]						
Synopsys Synplify/Synplify Pro (K-2015.09-1)[c]	Yes	Yes	Yes	Yes	Yes	N/A
Mentor Graphics Precision RTL/Plus (2015.1)	Yes	Yes	Yes	Yes	Yes	N/A
Equivalence Checking						
Cadence Encounter Conformal (9.1)[d]	Yes	Yes	Yes	N/A	N/A	N/A
OneSpin 360 (2014_12)	Yes	Yes	Yes	N/A	N/A	N/A

a. Support for Aldec simulators is offered by Aldec.

b. Most Vivado IPs can only be synthesized by Vivado synthesis, because the RTL source can include encrypted files. To use these IPs in a third party synthesis flow, the synthesized netlist can be exported from the Vivado tool in a suitable format for use in the third-party synthesis project.

c. Contact Synopsys for availability of Synplify Overlay or Service Pack.

d. Cadence Encounter Conformal Support is for RTL2Gate using Synopsys Synplify only.

System Generator support is restricted to operating systems that are compatible with The MathWorks MATLAB and Simulink tools.

System Requirements

This section provides information on system memory requirements, cable installation, and other requirements and recommendations.

The lab exercises require the installation of MATLAB 2014a (or later) and Vivado Design Suite 2014.2 (or later).

System Memory Recommendations

For memory recommendations for the Vivado Design Suite tools, see: http://www.xilinx.com/design-tools/vivado/memory.htm.

Operating Systems and Available Memory

The Microsoft Windows and Linux operating system (OS) architectures have limitations on the maximum memory available to a Xilinx program. Users targeting the largest devices and most complex designs might encounter this limitation. The Vivado Design Suite has optimized memory and enabled support for applications to increase RAM memory available to Xilinx tools.

Linux

For 32-bit Red Hat Enterprise Linux systems, the operating system can use the hugemem kernel to allocate 4 GB to each process. More information can be found on the Red Hat support site at http://www.redhat.com/docs/manuals/enterprise/.

Cable Installation Requirements

Platform Cable USB II is a high-performance cable that enables Xilinx design tools to program and configure target hardware.

Note: The Xilinx Parallel Cable IV is no longer supported for debugging or programming.

RECOMMENDED: *To install Platform Cable USB II, a system must have at least a USB 1.1 port. For maximum performance, Xilinx recommends using Platform Cable USB II with a USB 2.0 port.*

The cable is officially supported on the 32-bit and 64-bit versions of the following operating systems: Windows-7, Red Hat Linux Enterprise, and SUSE Linux Enterprise 12. Additional platform specific notes are as follows:

- Root privileges are required.
- SUSE Linux Enterprise 11: The fxload software package is required to ensure correct Platform Cable USB II operation. The fxload package is not automatically installed on SUSE Linux Enterprise 11 distributions, and must be installed by the user or System Administrator.

For additional information regarding Xilinx cables, refer to the following documents:

- *USB Cable Installation Guide* (UG344) [Ref 10]
- *Platform Cable USB II Data Sheet* (DS593) [Ref 11]

Equipment and Permissions

The following table lists related equipment, permissions, and network connections.

Table 2-3: **Equipment and Permissions Requirements**

Item	Requirement
Directory permissions	Write permissions must exist for all directories containing design files to be edited.
Monitor	16-bit color VGA with a minimum recommended resolution of 1024 by 768 pixels.
Drive	You must have a DVD-ROM for Vivado Design Suite (if you have received a DVD, rather than downloading from the web).
Ports	To program devices, you must have an available parallel or USB port appropriate for your Xilinx programming cable. Specifications for ports are listed in the documentation for your cable. ***Note:*** Installation of the cable driver software requires Windows-7. If you are not using one of these operating systems, the cables might not work properly.

Note: X Servers/ Remote Desktop Servers, such as Exceed, ReflectionX, and XWin32, are not supported.

Network Time Synchronization

When design files are located on a network machine, other than the machine with the installed software, the clock settings of both machines must be set the same. These times must be synchronized on a regular basis for continued proper functioning of the software.

Download and Installation

This guide explains how to download and install the Vivado® Design Suite tools, which includes the Vivado Integrated Design Environment (IDE), High Level Synthesis tool, and System Generator for DSP.

Downloading the Vivado Design Suite Tools

Xilinx® Design Tools users have multiple choices for download and installation.

Beginning in 2015.1, Xilinx introduced **Vivado Lab Edition**, which features a dedicated and streamlined environment for programming and debugging devices in lab settings.



TIP: *No license is required to use Vivado Lab Edition tools.*

For users wishing to install one of the full Vivado Editions, there are two choices.

- **Single File Full Product installer**: You can choose to download either a single file full product installer or a lightweight installer that utilizes the Xilinx website to download just those files that are required.
- **Lightweight installer**: The lightweight web-based installer can often reduce the download size and speed up the download and installation process considerably.

All Editions and download options are available on the Xilinx website:
http://www.xilinx.com/support/download/index.htm

Most files in the Xilinx Download Center are downloaded using the Akamai download manager. For the optimum download experience:

- Allow pop-ups from entitlenow.com.
- Set security settings to allow for secure and non-secure items to be displayed on the same page.
- Allow the Akamai download manager to run Java processes.

To download a full Edition of the Vivado Design Suite:

1. Select the **Vivado Design Tools** tab in the web page.

2. Under the Version heading, click the version of the tools you want to download.
3. Click the link for the installer you want to download.

To download the Vivado Lab Edition tools, go to the Vivado Design Tools tab, select a version of 2015.1 or newer, and download the file associated with the Vivado Lab Edition.

Note: Lab Edition installer can be run on both 32 or 64-bit machines. The Full Edition installers work only on 64-bit machines.

Installing the Vivado Design Suite Tools

This section explains the installation process for all platforms for the Vivado Design Suite.

Installation Preparation

IMPORTANT: *Before starting installation the follow steps must be completed:*

- Check the links in Important Information section in Chapter 1 for any installation issues pertaining to your system or configuration.
- Make sure your system meets the requirements described in Chapter 2, Architecture Support and Requirements.
- Disable anti-virus software to reduce installation time.
- Close all open programs before you begin installation.
- The Vivado Design Suite installer does not set global environment variables, such as XILINX, on Windows.

Lab Edition, Full Product Download, or DVD

If you downloaded the Lab Edition or full product installation, decompress the file and run xsetup (for Linux) or xsetup.exe (for Windows) to launch the installation. If you received a DVD, which only contains the full Edition products, launch xsetup(.exe) directly.

RECOMMENDED: *Xilinx recommends the use of 7-zip or WinZip (v.15.0 or newer) to decompress the downloaded tar.gz file.*

Lightweight Installer Download

If you downloaded the lightweight installer, launch the downloaded file. You are prompted to log in and use your regular Xilinx login credentials to continue with the installation process.

After entering your login credentials, you can select between a traditional web-based installation or a full install image download.

- The **Download and Install Now** choice allows you to select specific tools and device families on following screens, downloads only the files required to install those selections, and then installs them for you.
- The **Download Full Image** requires you to select a download destination and to choose whether you want a Windows only, Linux only, or an install that supports both operating systems. There are no further options to choose with the **Download Full Image** selection, and installation needs to be done separately by running the xsetup application from the download directory.

Note: Lab Edition is not supported through a lightweight installer. You may download the single-file download image for Lab Edition.

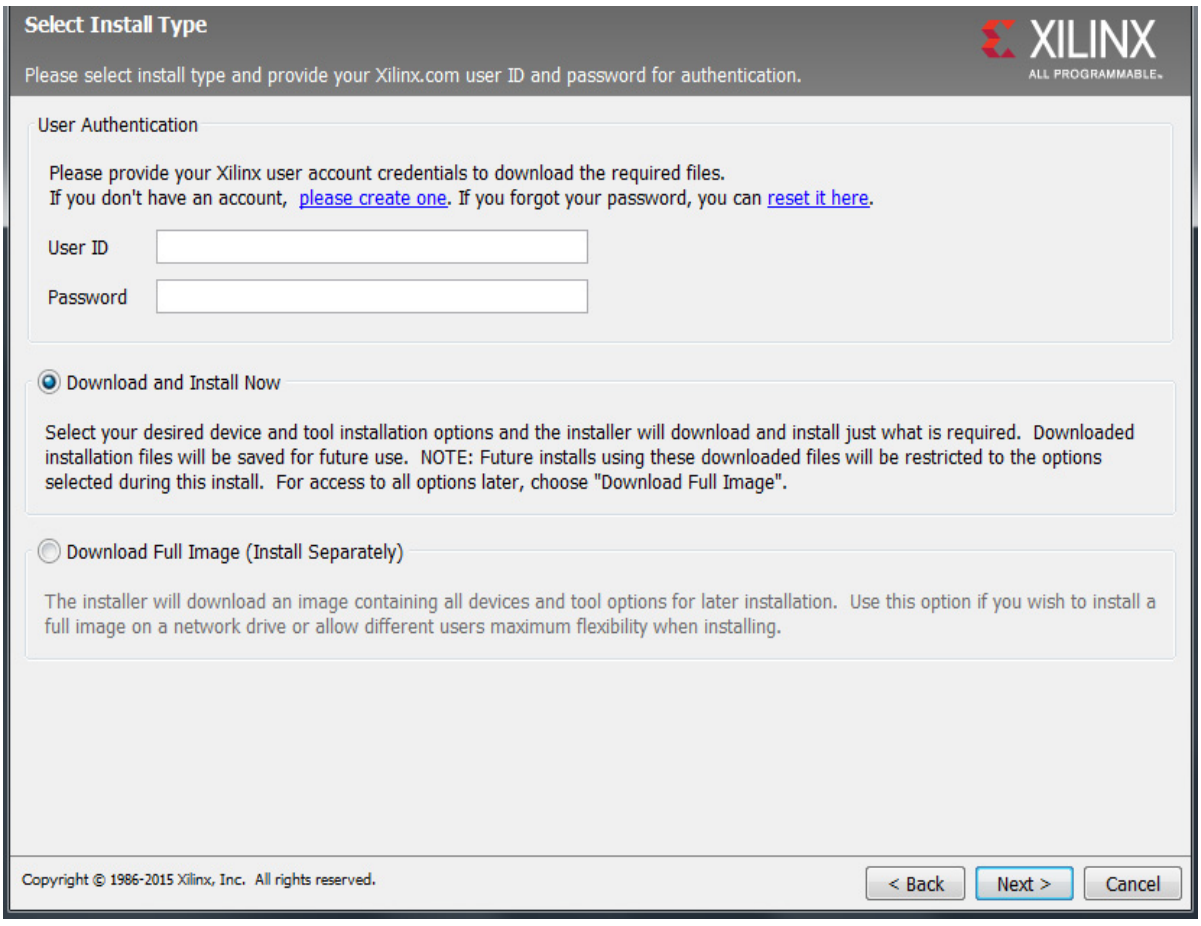


Figure 3-1: **Vivado Design Suite Installation - Select Installation Source**

Connectivity

The installer connects to the internet through the system proxy settings in Windows. These settings can be found under **Control Panel > Network and Internet > Internet Options**. For Linux users, the installer uses Firefox browser proxy settings (when explicitly set) to determine connectivity.

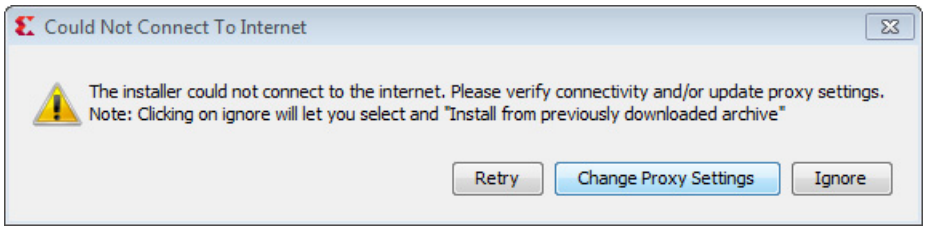


Figure 3-2: **Vivado Design Suite Installation - Connectivity**

If there are connectivity issues, verify the following:

1. If you are using alternate proxy settings to the ones referred to, select the **Manual Proxy Configuration** option to specify the settings.

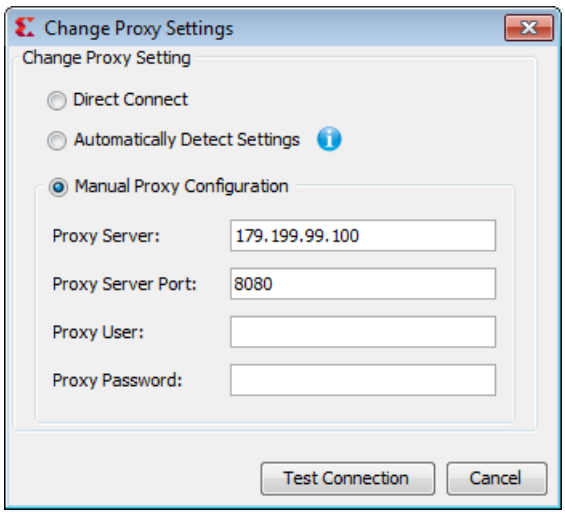


Figure 3-3: **Vivado Design Suite Installation - Change Proxy Settings**

2. Check if your company firewall requires a proxy authentication with a username and password. If so, select the **Manual Proxy Configuration** option in the dialog box above.
3. For Linux users, if either the **Use System settings** or the **Auto detect settings** option is selected in the Firefox browser, you must manually set the proxy in installer.

License Agreements

Carefully read the license agreements before continuing with the installation. If you do not agree to the terms and conditions, cancel the installation and contact Xilinx.

Edition Selection

Select the edition or standalone tool that is required. You can also install Software Development Kit (SDK) as part of the Vivado WebPACK, System and Design editions.

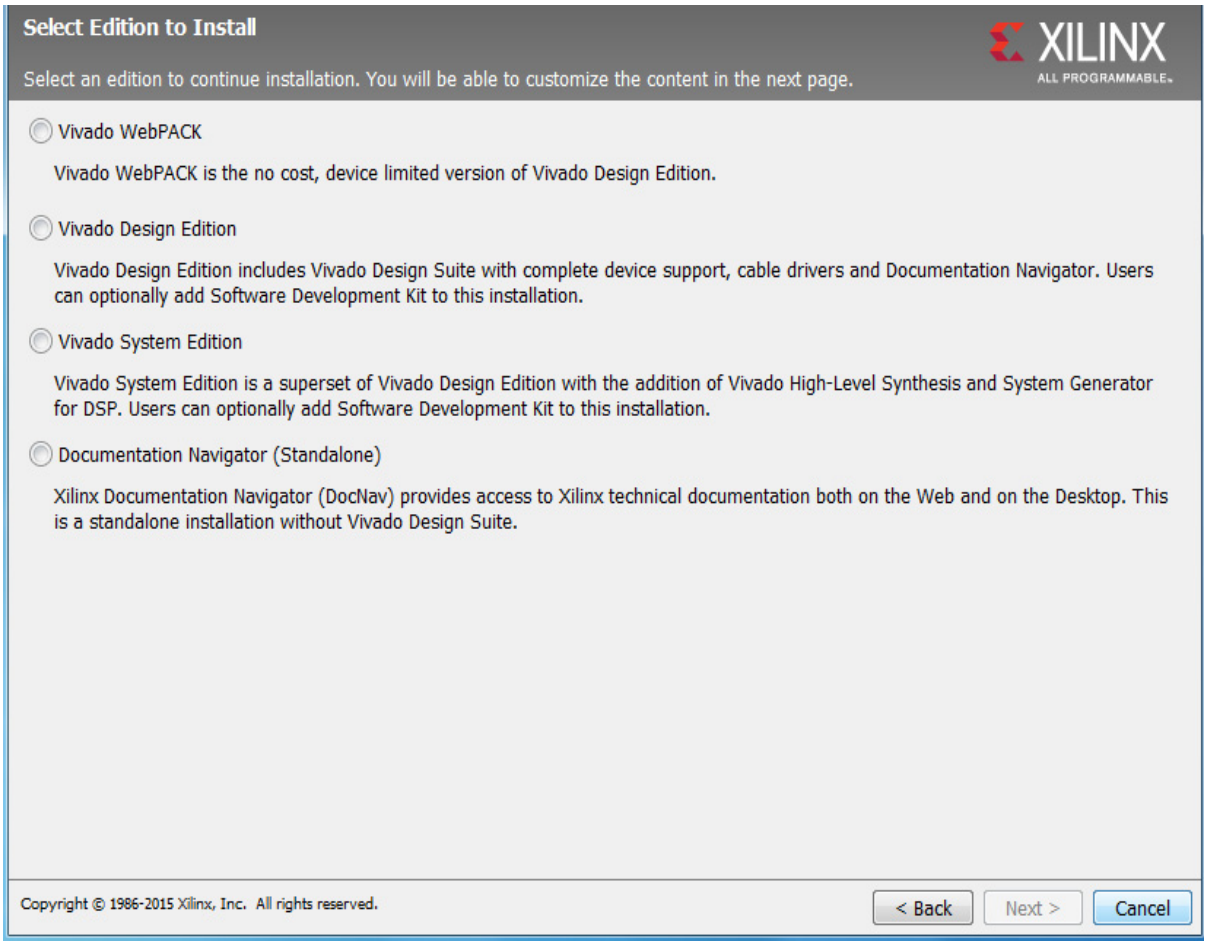


Figure 3-4: **Vivado Design Suite Installation - Select Products**

Vivado WebPACK and Design edition users will also be able to upgrade to a higher edition post installation. See Adding Additional Tools and Devices, page 25 for more details.

Tools, Devices, and Options

Customize the installation by choosing the design tools, device families and installation options. Selecting only what you need helps to minimize the time taken to download and

install the product. You will be able to add to this installation later by clicking **Add Design Tools or Devices** from either the operating system Start Menu or the **Vivado > Help** menu.



Figure 3-5: **Vivado Design Suite Installation - Vivado System Edition**

Shortcuts and File Associations

You can customize the creation of the program group entries (Start Menu) and the creation of desktop shortcuts. Optionally, you can also create file associations to launch Vivado project files directly with this version of Vivado. The shortcut creation and file association options can be applied to the current user or all users.

Installing Cable Drivers

On Windows, **Install Cable Drivers** is an optional selection in the installer.

For Linux, because root or sudo access is required to install drivers, this option has been removed from the Linux installer beginning in Vivado 2015.4. The general Vivado installer

can now be run on Linux without root or sudo privileges. To install cable drivers on Linux, there is now a script that must be run as root or sudo post installation.

Script Location: `<Vivado Install Dir>/data/xicom/cable_drivers/lin64/install_script/install_drivers/`

Script Name: `install_drivers`

Adding Additional Tools and Devices

You can incrementally add additional tools, devices or even upgrade Vivado editions post-install. This is useful for users that have chosen to install a subset of devices and/or tools.

To add new tools or devices:

- **Start Menu > Xilinx Design Tools > Vivado <version> > Add Design Tools** or **Devices**.
- Launch **Vivado > Help > Add Design Tools** or **Devices**.

If you have installed the Vivado WebPACK or Design Edition, you are presented with the option to upgrade the edition.

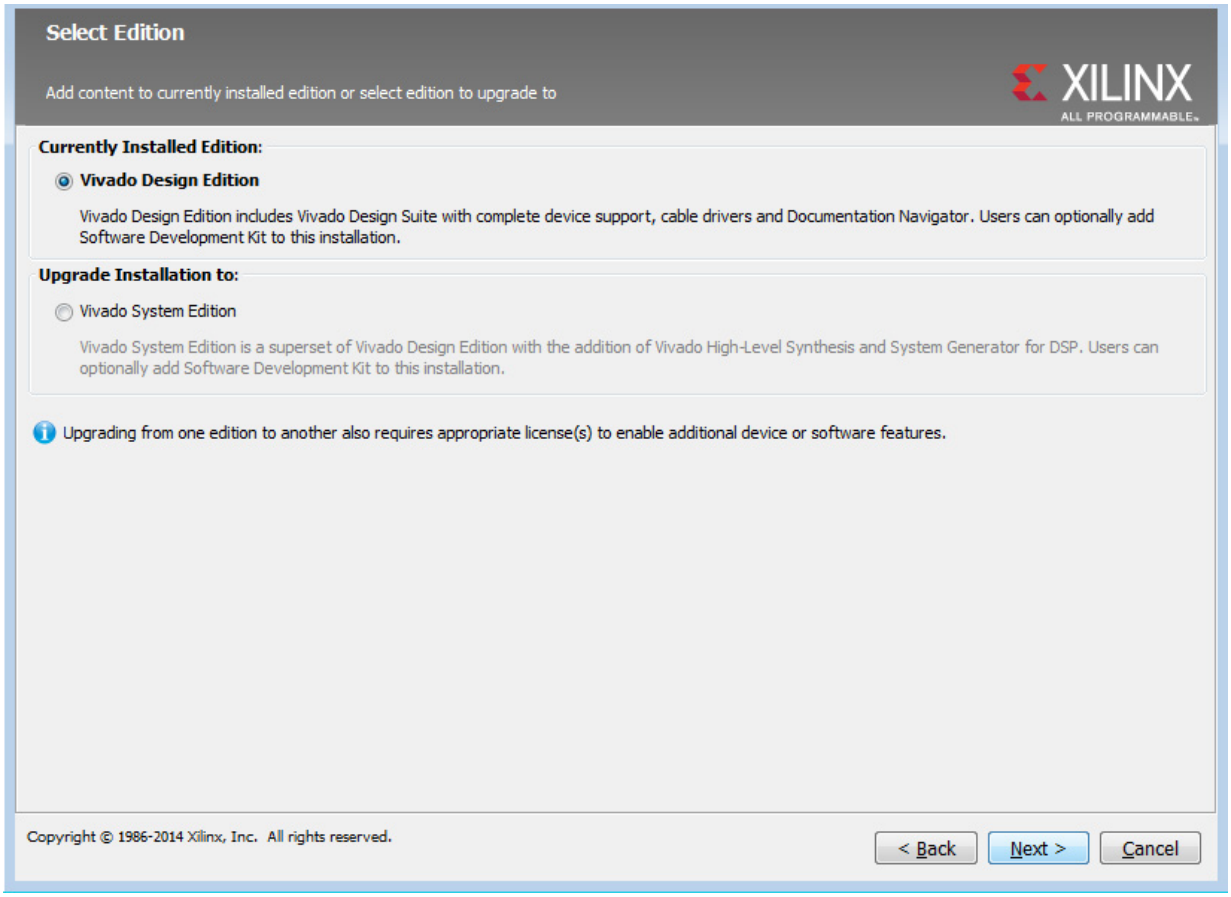


Figure 3-6: **Vivado Design Suite Installation - Select Edition**

Based on the above selection, you are presented with all available tools and devices that can be added to the current installation.

You can also add tools or devices from the Xilinx Information Center (XIC). See the Obtaining Quarterly Releases section for using this flow.

Network Installations

Installing to a network location provides a way for client machines to access the design tools by pointing to it on the network drive. To run the design tools on the network, the client machines must be set up correctly to ensure the environment variables, registry, and program groups all point to the network. The following sections describe the procedure for network setups.

Linux Clients

You must source `settings32.(c)sh` or `settings64.(c)sh` (whichever is appropriate for your operating system) from the area in which the design tools are installed. This sets up the environment to point to this installed location.

To run the design tools from a remotely installed location, run an X Windows display manager, and include a DISPLAY environment variable. Define `DISPLAY` as the name of your display. DISPLAY is typically `unix:0.0`. For example, the following syntax allows you to run the tools on the host named bigben and to display the graphics on the local monitor of the machine called mynode.

```
setenv DISPLAY mynode:0.0
xhost = bigbenPC Clients
```

Microsoft Windows Clients

1. Install design tools to a PC network server. Make sure your users know the location of the design tools and have access to the installation directory, and they have Administrator privileges for the following steps.
2. From the local client machine, browse to the following directory: `network_install_location\.xinstall\Vivado_<version>` and run the program `networkShortcutSetup.exe`.

   Running this program sets up the Windows settings batch files and **Program Group** or **Desktop** shortcuts to run the Xilinx tools from the remote location.
3. From the client machine, launch the Vivado Design Suite tools by clicking the **Program Group** or **Desktop** shortcuts, or by running the applications on the network drive.

Installing to a Mounted Network Drive

Xilinx design tools are designed to be installed in a directory under ROOT (typically `C:\Xilinx`). The installer normally presents this option when installing to a local driver.

To work around this issue, either specify a UNC path (for example, `\\network_loc\Xilinx\`) or define your target installation directory as `\Xilinx` under the network mount point (For example: `N:\Xilinx`).

Windows 7 default security levels do not allow you to select remote mapped drives. To install Xilinx Design Tools on remote mapped drives, you must change your account control settings using the following steps:

1. Open the Windows Control Panel, from the Windows Start menu, and select 'User Accounts'. If your Control Panel Uses 'Category View', click 'User Accounts' on two successive screens
2. Click 'Change User Account Control settings' and allow the program to make changes.

3. Click and slide the slide-bar down to the second to lowest setting (as seen in the following figure).
4. Click **OK**.

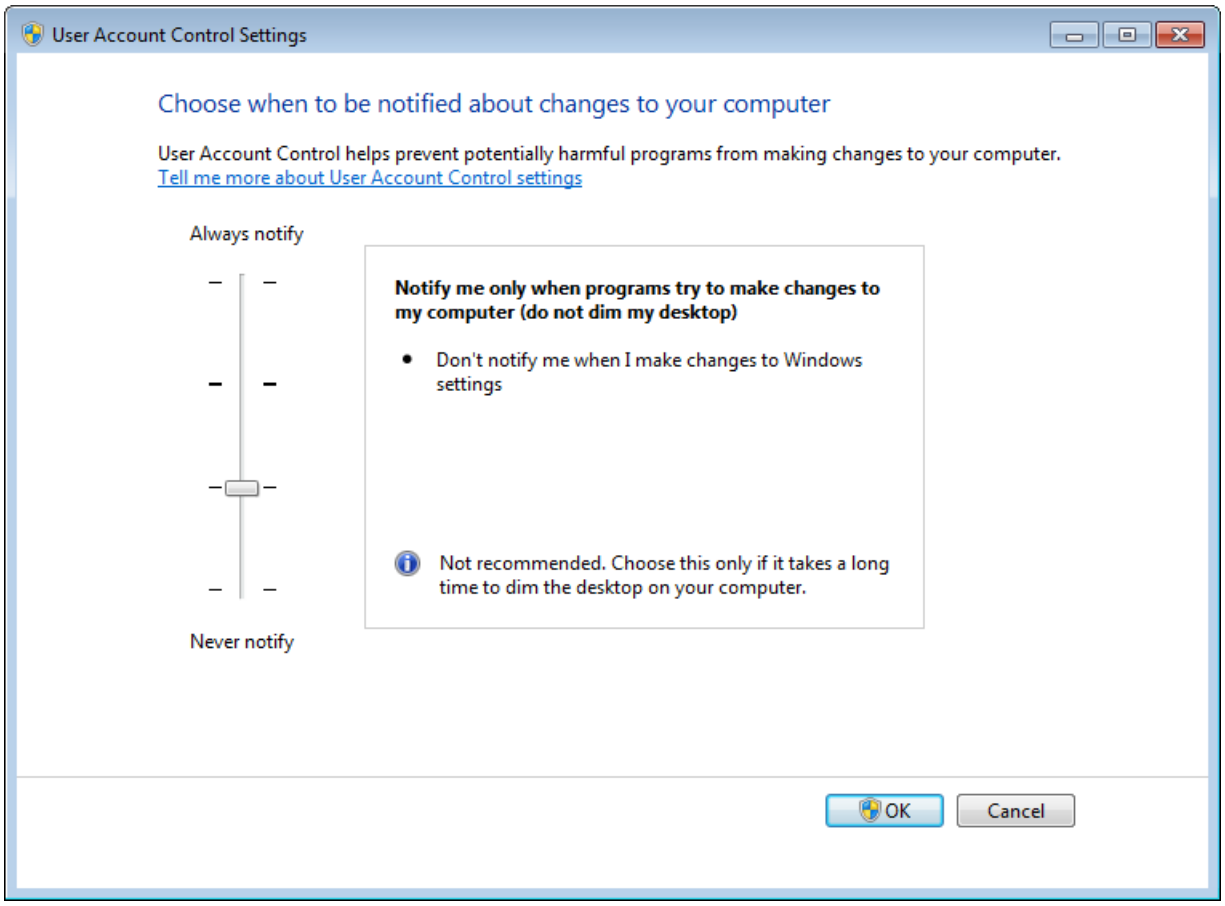


Figure 3-7: **Vivado Design Suite Installation - User Account Control Settings**

RECOMMENDED: *Xilinx recommends that you revisit this procedure to restore your settings to their previous state after installation.*

Note: You are not able to browse to the remote mapped drives using the Xilinx installer. You need to manually type in your installation path which contains a mapped network drive.

Batch Mode Installation Flow

Beginning in Vivado 2015.1, the installer can be run as an unattended batch process. To run unattended, a standard Edition and install location must be specified or a configuration file must be present which tells the installer the install location and which of the tools, devices and options you wish to install. The installer has a mode in which it can generate a reference

option file for you based on common configurations, which you can further edit to customize your installation.



RECOMMENDED: *It is recommended that you generate this reference for each new quarterly release, so that new devices, tools, options or other changes will be accounted for in your options file.*

To begin using batch mode, open a command shell and change to the directory where you have stored your extracted installer.

Note: For Windows, open the command window with administrator privileges and run the xsetup.bat file, found in the \bin directory, and not xsetup.exe with the options below.

Generate Configuration File

Run: `xsetup -b ConfigGen`

This will put you in an interactive mode where you will see the following menu. Choose an edition from the list given below.

1. Vivado WebPACK
2. Vivado Design Edition
3. Vivado System Edition
4. Documentation Navigator (Standalone)

After you select an edition, you will be prompted for a location/filename for your configuration file and the interactive mode will exit.

Below is a sample of a WebPACK configuration file:

```
#### Vivado WebPACK Install Configuration ####
Edition=Vivado WebPACK
Destination=C:\Xilinx
Modules=Vivado:1,Vivado High Level Synthesis:0,Software Development
Kit:0,DocNav:0,Artix-7,Kintex-7,Zynq-7000:1
#### Shortcut creation ####
CreateProgramGroupShortcuts=1
CreateShortcutsForAllUsers=0
ProgramGroupFolder=Xilinx Design Tools
CreateDesktopShortcuts=1
CreateFileAssociation=1
#### Post install tasks ####
## Post install tasks can be configured as shown below.
InstallOptions=Configure WebTalk:1,Install and Initialize Trusted Storage
Licensing:1,Generating installed device list:1,Install VC++ runtime libraries for
64-bit OS:1,Install Cable Drivers:0,Acquire or Manage a License Key:0,run:xic:1
```

Basically, each option in the configuration file matches a corresponding option in the GUI. A value of `1` means that option is selected, a value of `0` means the option is unselected.

Run the Installer

Now that you have edited your configuration file to reflect your installation preferences, you are ready to run the installer. As part of the installer command-line, you will need to indicate your acceptance of the Xilinx and Third Party license agreements, and confirm you understand the WebTalk Terms and Conditions.

Xilinx End-User License Agreement (EULA)

http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_4/end-user-license-agreement.pdf

Third Party End-User License Agreement (EULA)

http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_4/ug763_tplg.pdf

WebTalk Terms and Conditions

> By indicating `I AGREE`, I also confirm that I have read Section 13 of the terms and conditions above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at http://www.xilinx.com/webtalk. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

There is a command-line switch, `-a` or `--agree` for you to indicate your agreement to each of the above. If one of the above is left out of the list, or the agree switch is not specified, the installer will exit with an error and will not install.

Example Command-Lines

This is an example of the command-line for a typical new installation using a configuration file.

```
xsetup --agree XilinxEULA,3rdPartyEULA,WebTalkTerms --batch Install  --config
install_config.txt
```

If you wish to use one of Xilinx's default Edition configurations, you do not have to specify the `--config` option, but since the destination directory is included in the configuration file, you will be required to specify this on the command-line.

```
xsetup --agree 3rdPartyEULA,WebTalkTerms,XilinxEULA --batch Install --edition
"Vivado System Edition" --location "C:\Xilinx"
```

The above command will utilize the default configuration options for the edition specified. To see the default configuration options, use the –b ConfigGen mode as described above.The Vivado installer's batch mode can also perform uninstallation and upgrades (adding additional tools and devices). For the full list of the installer's batch options run `xsetup -h` or `xsetup --help`.

Obtaining Quarterly Releases

Xilinx releases quarterly versions of the Vivado Design Suite tools throughout the year. Each quarterly version contains device support updates, new features and bug fixes. The following sections describe how to obtain updates through the Xilinx Information Center.

Xilinx Information Center

Xilinx Information Center (XIC) is the next generation replacement of XilinxNotify. This functionality resides in the task bar (Windows) and periodically checks for new releases and updates from Xilinx. Users can view and dismiss notifications as well as update installations.

In addition, XIC now includes a cockpit from which you can manage all of your Xilinx tool installations. Update, check licenses or uninstall all from the new Manage Installs tab.

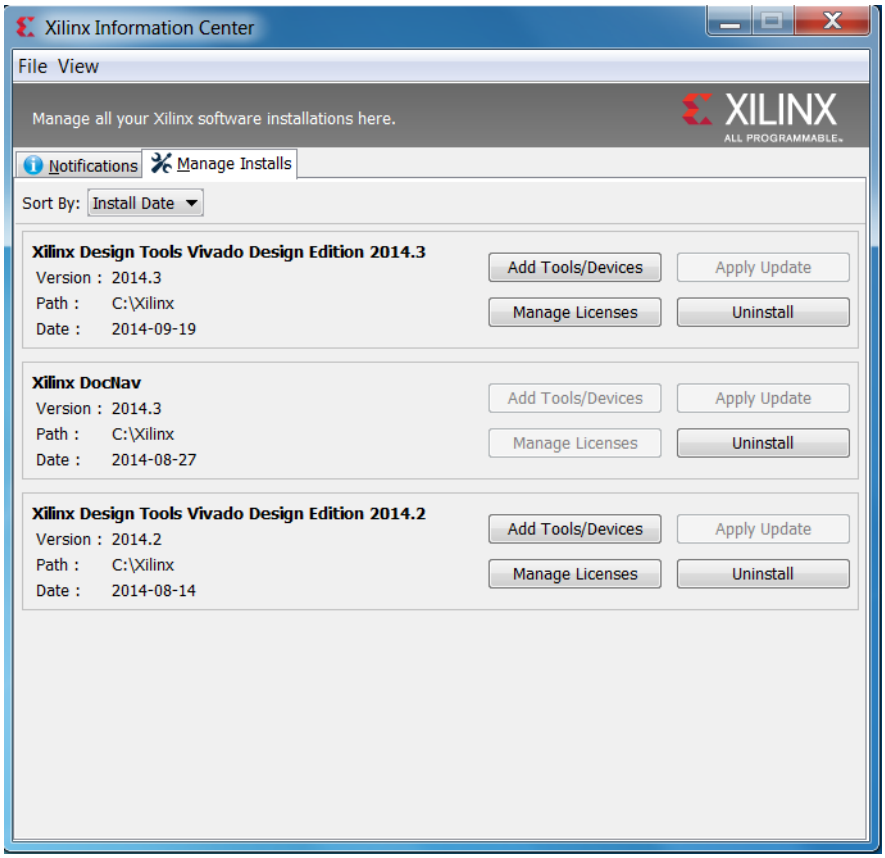


Figure 3-8: **Xilinx Information Center (XIC)**

Uninstalling the Vivado Design Suite Tool

Before uninstalling, make sure to have moved any project files you want to keep outside your Xilinx installation directory structure, or they are deleted.

Note: Xilinx Documentation Navigator is not removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. You need to uninstall it separately if it is no longer required.

Uninstallation

Before uninstalling, make sure to have moved any project files you want to keep outside your Xilinx installation directory structure, or they will be deleted. See below for information on uninstalling Documentation Navigator and Xilinx Information Center.

Uninstalling Documentation Navigator

Xilinx Documentation Navigator will not be removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. If it is no longer required, you will need to uninstall separately either from the Start Menu program group entry 'Uninstall DocNav' or through the corresponding entry in the 'Uninstall or change a program' control panel option (for Windows).

Uninstalling Xilinx Information Center

Xilinx Information Center will not be removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. If it is no longer required, you will need to uninstall separately through the corresponding entry in the 'Uninstall or change a program' control panel option (for Windows).

Uninstalling on Microsoft Windows

To uninstall the Vivado Design Suite tool product, launch the uninstaller from the launcher menu: select **Applications > Xilinx Design Tools > Vivado 2015.4 > Uninstall**.

Uninstalling on Linux

To uninstall any Xilinx product, select the Uninstall item from that product's Start Menu folder. For instance, to uninstall Vivado Design Suite: Edition, select **Start > All Programs > Xilinx Design Tools > Vivado 2015.4 > Uninstall**.

If you do not have a program group entry, use the command line option to uninstall:

```
<install_path>\.xinstall\Vivado_2015.4\ xsetup.exe –Uninstall
```

Alternatively, use the corresponding entry in the Uninstall or change a program control panel option (for Windows).

WebTalk

The WebTalk feature helps Xilinx understand how you use Xilinx® FPGA devices, software, and intellectual property (IP). The information collected and transmitted by WebTalk allows Xilinx to improve the features most important to you as part of our ongoing effort to provide products that meet your current and future needs. When enabled, WebTalk provides information on your use of the Vivado® Design Suite tools.

WebTalk Participation

Your participation in WebTalk is voluntary except in the following cases:

- You are using a WebPack™ license.
- You are using pre-release software or devices.

In these cases, WebTalk data collection and transmission always occurs, regardless of your preference settings. For all other cases, data is not transmitted if you disable WebTalk.

The following table summarizes WebTalk behavior for data transmission to Xilinx from your post-route design, based on your Xilinx license, WebTalk install preference, and user preference settings.

Table 4-1: **WebTalk Behavior for Bitstream Generation or Route Design Flow**

Early Access Devices	License	WebTalk Install Preference Selected as "Enabled"	WebTalk User Preference Selected as "Enabled"	Send WebTalk Data to Xilinx
Yes	X	X	X	Yes
No	WebPACK™	X	X	Yes
No	Edition License	No	X	No
No	Edition License	Yes	No	No
No	Edition License	Yes	Yes	Yes

Note: If the device is a WebPACK device, the Tools first look for a WebPACK license.

Setting WebTalk Install Preference

You can enable or disable WebTalk globally during or after installation as described below. During installation you can enable or disable WebTalk installation options by checking or unchecking the **Enable WebTalk to send software, IP and device usage statistics to Xilinx (Always enabled for WebPACK license)** checkbox.

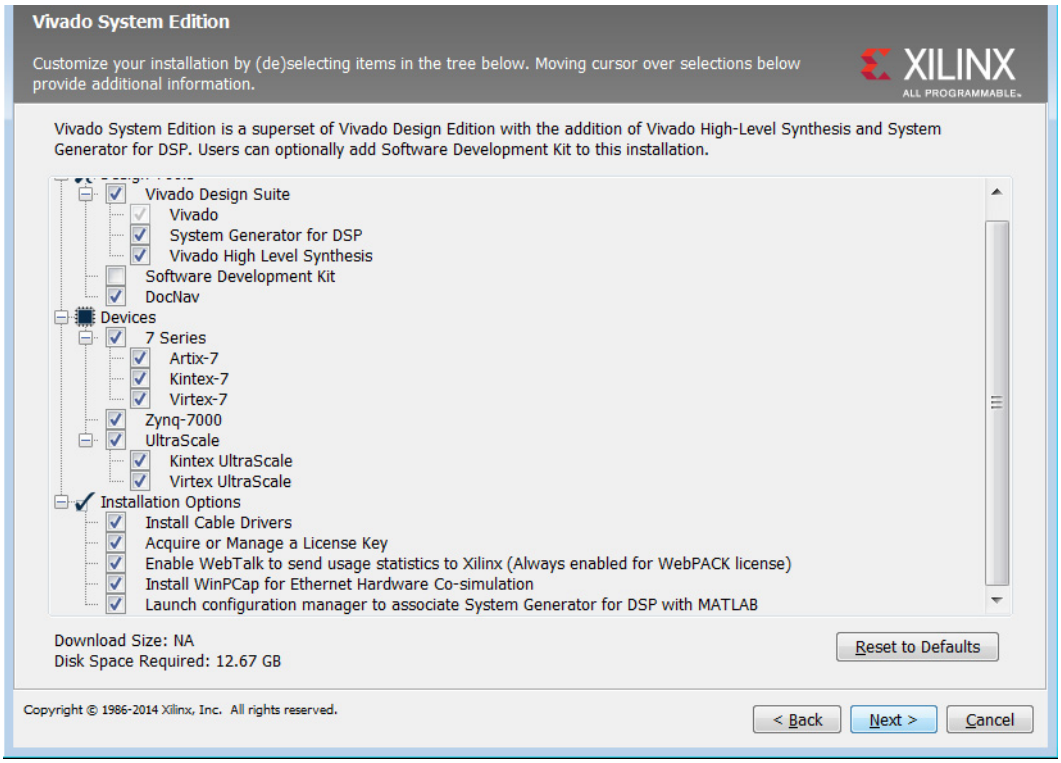


Figure 4-1: **WebTalk Install Options**

You can enable or disable WebTalk installation options using the Tcl command `config_webtalk`:

```
config_webtalk -install on|off
```

- `on` turns WebTalk on for the installation.
- `off` turns WebTalk off for the installation.

Install settings are saved in the following location:

- **Windows 7**: `<install dir>/vivado/data/webtalk/webtalksettings`
- **Linux**: `<install dir>/vivado/data/webtalk/webtalksettings`

Note: You need administrator privileges to write to the install location.

Setting WebTalk User Preferences

You can enable or disable WebTalk user options by selecting **Tools > Options > General** as shown below.

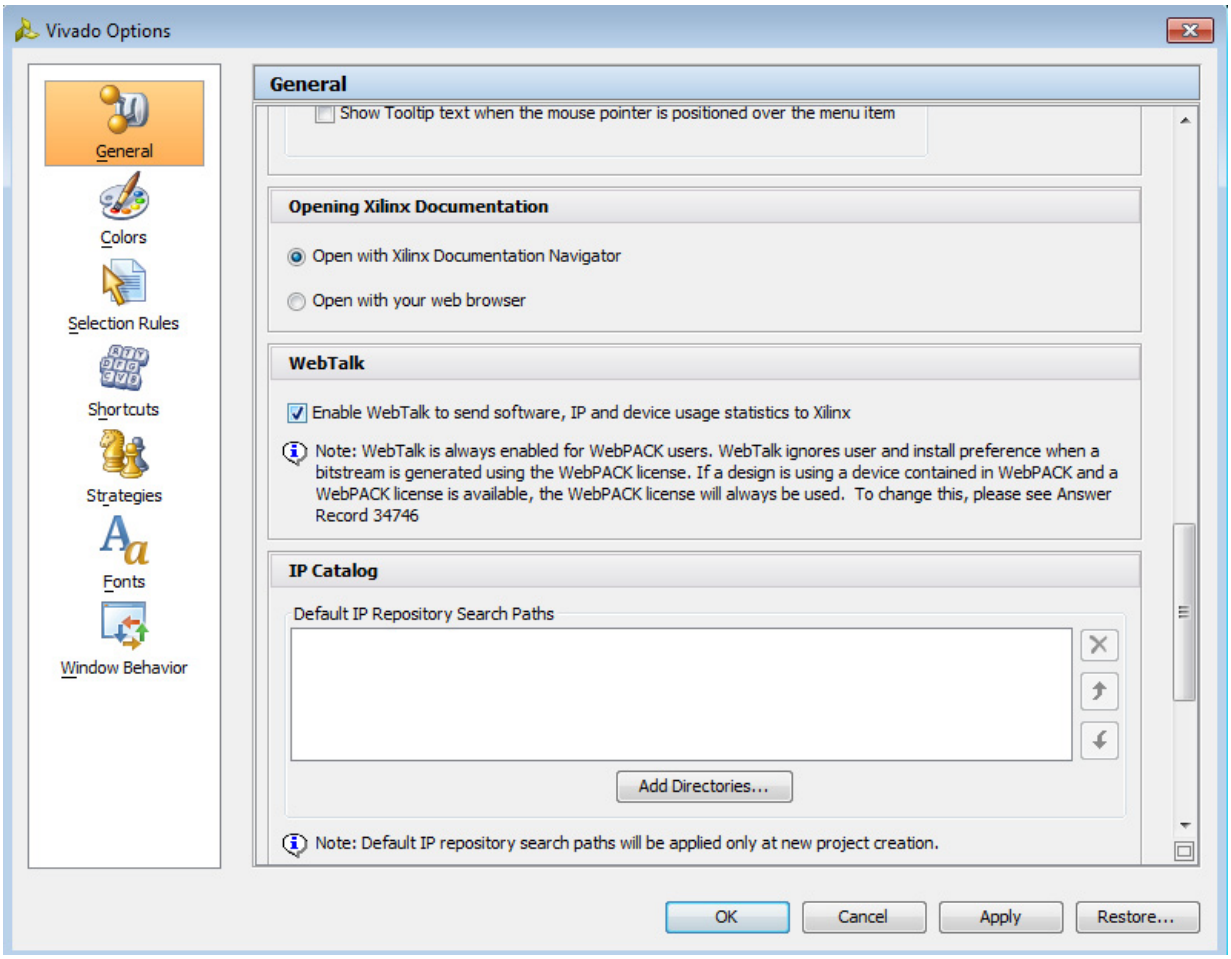


Figure 4-2: **WebTalk User Preferences**

After installation, you can enable or disable WebTalk user options using the `config_webtalk` Tcl command:

```
config_webtalk -user on|off
```

- `on` turns WebTalk on for the current user.
- `off` turns WebTalk off for the current user.

User settings are saved in the following location:

- **Windows 7**:

  `%APPDATA%\Xilinx\Common\<version>\webtalk`

  where:

  `%APPDATA%` is:

  `C:\Users\<user>\AppData\Roaming`

- **Linux**:

  `%APPDATA%/.Xilinx/Common/<version>/webtalk`

  where:

  `%APPDATA%` is:

  `/home/<user>`

Checking WebTalk Install and User Preferences

You can also use the `config_webtalk` Tcl command to check the current status of WebTalk settings. The command line option `-info` reports the values for the install setting and the user setting:

```
config_webtalk -info
```

Types of Data Collected

WebTalk does not collect your design netlist or any other proprietary information that can be used to reverse engineer your design. The data Xilinx collects through WebTalk includes:

- Software version
- Platform information (for example, operating system, speed and number of processors, and main memory)
- Unique project ID
- Authorization code
- Date of generation
- Targeted device and family information

For more information on the type of data that is collected, see the Xilinx Design Tools WebTalk web page [Ref 14]. To see the specific WebTalk data collected for your design, open the `usage_statistics_webtalk.xml` file in the project directory. You can also open the `usage_statistics_webtalk.xml` file for easy viewing of the data transmitted to Xilinx.

Transmission of Data

WebTalk is invoked after bitstream or route design compilation. WebTalk bundles the collected data in an `usage_statistics_webtalk.xml` file and sends this file to Xilinx by https (hypertext transfer protocol secure) post. Every new compilation for a given design overwrites the previous `usage_statistics_webtalk.xml` file. WebTalk also writes an HTML file equivalent `usage_statistics_webtalk.html` file for easy viewing of the data transmitted to Xilinx. WebTalk also writes to the `vivado.log` (or `runme.log`) file that contains additional information about whether the file was successfully transmitted to Xilinx.

Chapter 5

Obtaining and Managing a License

The Xilinx® Product Licensing site is an online service for licensing and administering evaluation and full copies of Xilinx design tools and intellectual property (IP) products. This chapter describes the FLEXnet license generation functionality of the Product Licensing Site.

Licensing Overview

Two Product Licensing Methodologies

There are now two ways in which Xilinx enforces the Xilinx End-User License Agreement at run time in the Xilinx design tools.

- **Certificate-Based Licenses**: This is the license enforcement method Xilinx introduced for the ISE® Design Suite in the ISE 11.1 release. A certificate, commonly referred to as a "license file (`.lic`)" is issued from the Xilinx Product Licensing Site. The certificate is matched to a given machine, server or licensing dongle using your entering host-id which uniquely identifies the machine. This license certificate must remain present on the machine and in the license search path, because the Vivado tools need access to this file to check for a valid license feature during run time.
- **Activation Licenses**: Instead of requiring a file to be present to authorize a machine, Activation uses a trusted area on the client or servers hard-drive to store the authorization credentials. Most new Vivado tools licenses purchased after April, 2014 utilize a licensing technology referred to as Activation-based licensing. This trusted storage area should be automatically installed and initialized on Windows operating systems if Vivado was installed with Administrative privileges. If not, or if using Linux, then the trusted storage area must be installed//initialized prior to any other Activation licensing activities. See either Certificate-Based Node Locked License or Activation-Based Floating License.

  When the Vivado tools look for a license feature, they are allowed to run if this trusted storage area contains the proper authorization. Because activation-based licenses do not use a license file, they will not work with USB license dongles.

Certificate Licensing Terminology

- **Host ID**: An identifier, placed within certificate licenses, which binds the license to the computer using this identifier. Typical identifiers are: Hard-drive volume ID, Ethernet port MAC address, or USB Dongle ID.
- **Node-Locked License**: A node-locked license allows for the use of a single seat of a product entitlement on a specific machine.
- **Floating License**: A floating license resides on a network server and enables applications to check out a license when they are invoked. At any one time, the number of licenses for simultaneous users is restricted to the number of license seats purchased.
- **License Rehosting**: The act of changing the host ID of a generated license due to machine hardware changes, hard-drive failure or the moving of a license from one machine to another.
- **License Deletion**: The act of removing a license from a machine, and having the entitlement placed back into the Xilinx Product Licensing Account.
- **Affidavit of Destruction**: A click through agreement by which you certify that the license file (.lic) for a rehosted or deleted license will be destroyed and no longer used.

Activation Licensing Terminology

- **Client License**: A client license allows for the use of a single seat of a product entitlement on a specific machine. This is the activation-based equivalent of a certificate-based node-locked license.
- **Server License**: A server license is the activation-based equivalent of a certificate-based floating license. A server license resides on a network server and enables applications to check out a license when they are invoked. At any one time, the number of licenses for simultaneous users is restricted to the number of license seats purchased.
- **Trusted Storage**: The area where activation license host information and authorizations are stored.
- **Request Creation**: Activation licensing is based upon a request/fulfillment system. A request for a new license must first be recorded into trusted storage. This is done automatically by the Vivado License Manager whenever you use the **Connect Now** or **Save Link As Button in Obtain License** screen or by using similar command-line arguments for the `xlicsrvrmgr` tool, required for setting up a floating Activation license. After a request identifier is created, it is sent to the Xilinx Product Licensing Site along with the host information. When a license is generated on the Licensing Site, a fulfillment XML file is created with this same request identifier. When the activation fulfillment XML file is loaded into trusted storage, activation will be successful only if the request identifier on the fulfillment matches the one stored in trusted storage.

After the license is activated, the request becomes inactive and a new request can be made for additional licenses.

- **Return License**: With activation, license rehosting, license deletion and affidavits of destruction are no longer necessary. Activation features a methodology by which you can initiate a return of a license to Xilinx from the client or server machine. When the return request is made, the license is disabled on the local machine, and a return request is sent to the Xilinx Product Licensing Site. After processed, the return request causes an entitlement to be placed back in your Product Licensing Account, and a message is sent to trusted storage to remove the returned license from the machine.

License Compatibility

The Vivado 2014.1 and later releases recognize both certificate and activation-based licenses. If the license versions and dates are valid for the tool version being used, it does not matter whether the license is certificate or activation-based.

Differences with Activation Licenses

To authorize the trusted storage area, activation records need to be sent from the Xilinx Product Licensing Site to the client or server machine. Currently, this is done by using XML files with encrypted authorizations. When you generate an Activation license, you receive an XML file by email, much like you might have received a certificate file (`.lic`) in the past. The difference is that certificate .lic files need to be continually accessed by the Xilinx software, and so must be retained and in a valid license search path. The XML activation record is used to load the authorization into the trusted storage area. After the authorization has been loaded, the XML activation record is no longer needed.

To generate licenses based on activation entitlements, a request for a license must first be made into the client or server computer's trusted storage area. For client (node-locked) activation license requests, Vivado License Manager or the command-line utility `xlicclientmgr` must be used. For server (floating) license requests, the command-line `utility xlicsrvrmgr` must be used. For more information on the `xlicclientmgr` or `xlicsrvrmgr` utilities, see the Xlicclientmgr Command-Line Utility or Xlicsrvrmgr Command-Line Utility section.

After this request is processed, a URL to the Xilinx Product Licensing Site will be generated and will contain the id of the request along with specific machine identification information of the Xilinx Product Licensing Site. This URL should be placed into a web browser, and if activation entitlements exist, they are accessible in the Activation-Based Licenses section of the Create New Licenses tab of the Xilinx Product Licensing Site.

If you enter the Xilinx Product Licensing Site directly or through older Xilinx license managers, the machine identification necessary to generate an activation-based license will not be present. In this case, the Activation-Based Licenses section of the website will be inactive, and only certificate licenses will be available for generation.

Generating/Installing/Managing Activation-Based Licenses

Activation-Based Node-Locked License

Getting Started

Activation Exceptions

If you meet any of the following conditions, you are not a candidate to use Activation for your licensing solution. Please contact Xilinx Development System Customer Service for an alternate licensing solution.

- License dongles are not supported by Xilinx's activation licensing. If you wish to utilize your existing dongles, only certificate-based licenses should be used.
- If you are creating a license for a secured area where files are not allowed to be exported, certificate-based licenses which support the legacy host ID structure are a better fit.

Initializing Trusted Storage

Windows: If you are using Windows and installed with Administrative rights, the trusted storage area should have been installed and initialized automatically. If trusted Storage has not been initialized, perform the following steps:

1. Open a command window in Administrative mode by typing `cmd` in the Windows Start Menu search box, right clicking on the `cmd.exe` icon and choosing **Run as administrator**.
2. Run `<Vivado Tools Directory>\Vivado\2015.4\bin\unwrapped\win64.o\installanchorservice.exe`.

Linux: Trusted storage must be manually installed and initialized on Linux by performing the following steps:

1. With root or sudo access, open a command-line shell.
2. Run `<Vivado Tools Directory>/Vivado/2015.4/bin/unwrapped/lin64.o/install_fnp.sh`

Requesting a Node-Locked License From Your Machine

In order to generate node-locked (client) activation-based licenses, you must use either the Vivado License Manager GUI, or the `xlicclientmgr` command-line executable to access

the Xilinx License Management site. Failure to use one of these tools, and going to the Xilinx License Manage website directly in a browser will result in all activation-based licenses being non-selectable. The following instructions are for using the Vivado License Manager GUI to access the Xilinx License Management website.

1. Launch Vivado License Manager
   a. For Windows 7 or earlier: Select **Start > All Programs > Xilinx Design Tools > Vivado 2015.4 > Manage Xilinx Licenses**.
   b. For Windows 8.1: Run the Manage Xilinx Licenses app from the full listing of Apps on your Start screen.
   c. For Linux: Type `vlm` in a command-line shell.
2. In the left window frame select **Obtain License** which is located under the **Get License** section.
3. In the main window frame, select either Get Free Licenses, Start 30-Day Evaluation or Get My Purchased Licenses (not Start now) and click the **Connect Now** button (Figure 5-1).
4. Your default web browser should now open with a Xilinx login screen.

Note: If your machine is not currently connected to the internet or is having proxy issues, please click the Save Link As button. This will allow you to save the required information into an HTML file. This HTML file can be opened by a web browser on any machine that is connected to the internet.

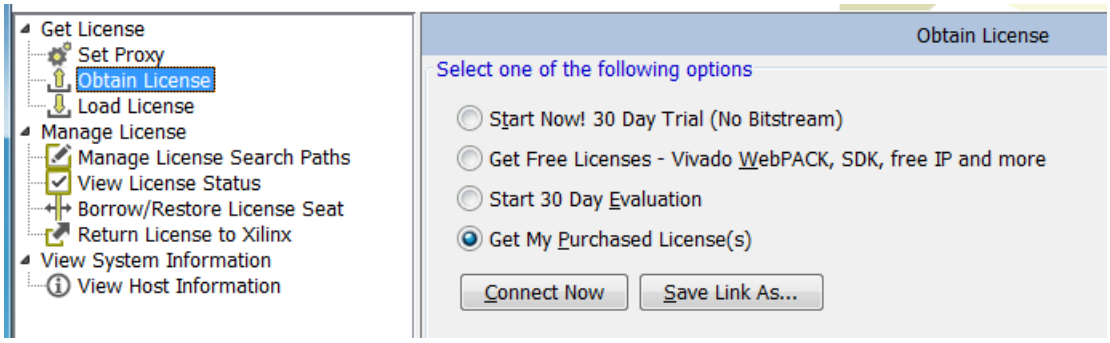


Figure 5-1: **Obtain License**

Generating a Node-Locked Activation License on the Xilinx License Management Website

Whether Vivado License Manager launched your web browser, or you manually launched a browser with the HTML file provided by the **Save Link As** command, you should now be at the **Sign In To The Xilinx Licensing Site** screen.

1. Use your Xilinx.com username and password to sign in and confirm your address information.
2. Select the licensing account which contains your licenses from the **Account** drop-down menu, if necessary.

3. Scroll down, if necessary, to the **Activation Based Licenses** section of the webpage (Figure 5-2).
4. Select the Activation licenses of your choice.

Note: Once you check an entitlement in either the "Activation Based Licenses" area or the "Certificate Based Licenses" area, the other area will automatically become inactive. Activation and Certificate licenses must be generated separately, although multiple licenses of the same license type may be selected. To reactivate both areas, uncheck all licenses in that area.

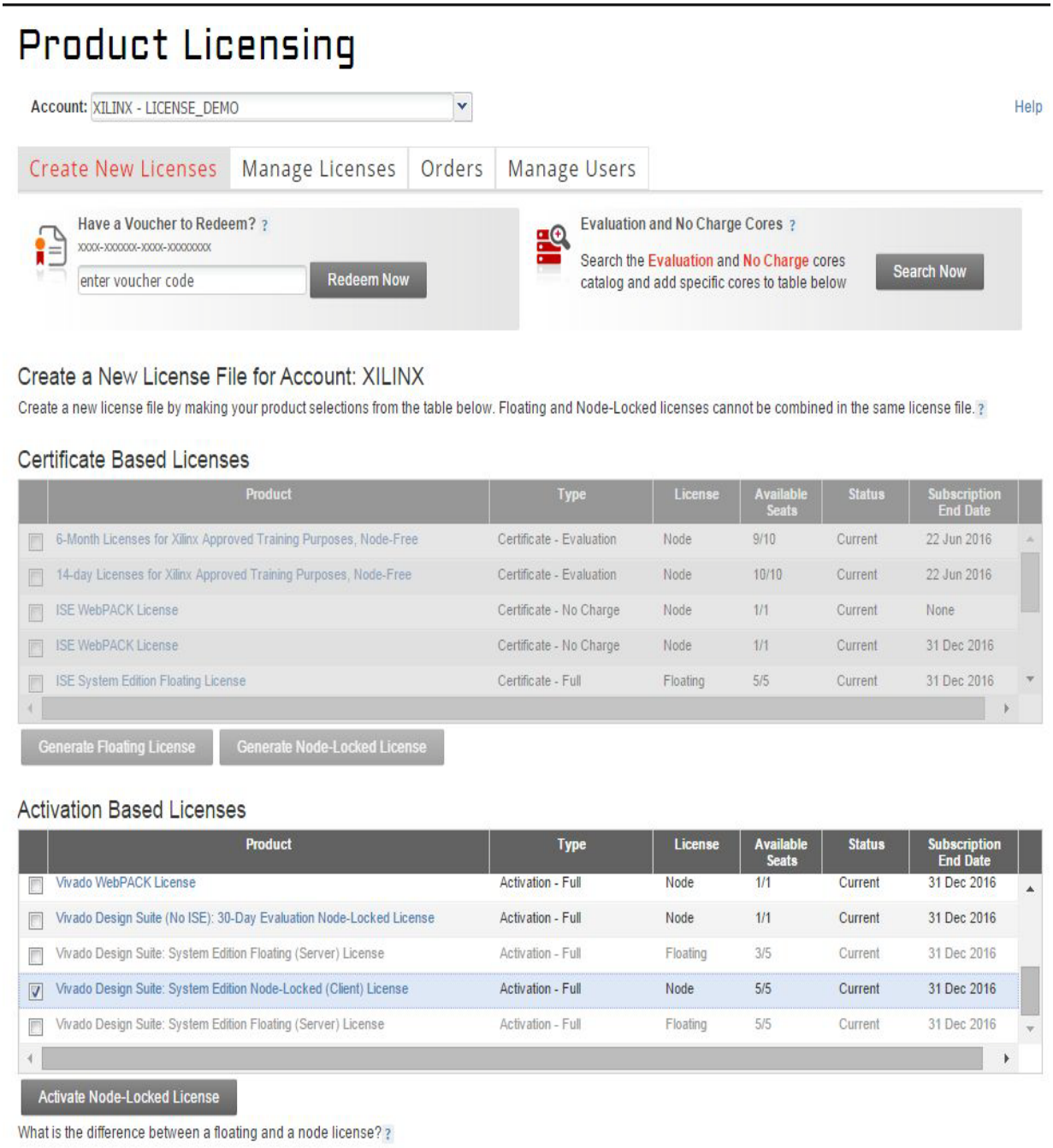


Figure 5-2: **Create New Node-Locked (Client) Activation License**

5. Select the **Activate Node-Locked License** button.
6. On the pop-up dialogs confirm each page of information is correct by pressing the **Next** buttons until the license generation begins.

Installing a Node-Locked Activation License On Your Machine

One-Step Activation Method

Beginning in Vivado 2014.3, pressing the **Connect Now** button in the Vivado License Manager causes the VLM to go into polling mode. After a two-minute delay, VLM shows the following dialog box (Figure 5-3).

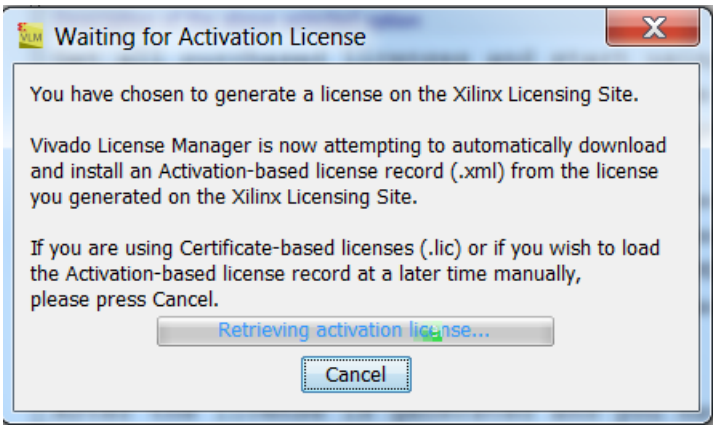


Figure 5-3: **Waiting for Activation License Dialog**

If your internet and proxy connects are correct, Vivado License Manager detects the existence of your Xilinx_License.xml file soon after you press the final **Next** button on the license generation dialogs in step 3. VLM will then automatically download and install the .xml file for you, immediately activating your license and presenting you with a **Success** dialog. You may view your installed license in the **View License Status** page under the **Manage License** heading in the left most window frame.

Your Xilinx_License.xml file will be e-mailed to you for your records, but no further action with this file is required.

Manual Method

The One-Step Activation polling stops after about 15 minutes. If it has taken you longer than this to generate your license file, if you manually cancelled the polling, or if you accessed the Xilinx License Management Website on a different machine because yours was not connected to the internet, you will need to utilize the manual method for loading your license onto your machine.

1. Save the activation fulfillment file (.xml) attached to thee-mail to a temporary directory on your local system.
2. Run the **Vivado License Manage**r.
3. On the left hand frame of VLM, choose **Load License** under the **Get License** section
4. Click the **Activate License** button.

5. Browse to your activation fulfillment file (Xilinx_License.xml) and click **Open**.
6. This loads your activation fulfillment into trusted storage, where it is verified and the machine authorized for the corresponding tools.

Activation-Based Floating License

Getting Started

Activation Exceptions

If you meet any of the following conditions, you are not a candidate to use Activation for your floating license server. Contact Xilinx Development System Customer Service for an alternate licensing solution.

- Triad (triple-redundant) floating license server configurations are not supported by Xilinx's activation licensing. Certificate-based licenses must be used with triple-redundant floating servers.
- SUN-OS based activation floating license servers are not supported by Xilinx. Certificate-based licenses do still support the SUN-OS.
- If you are creating a license for a secured area where files are not allowed to be exported, certificate-based licenses which support the legacy host ID structure are a better fit.

Initializing Trusted Storage

Trusted storage must be manually installed and initialized on your floating license server. All the files required to install, initialize and serve floating licenses are available in the platform specific ZIP files located on the Xilinx Download Center in the License Management Tools section of the current Vivado release.

Windows:

1. Extract the License Management Tools archive onto your disk. A permanent location is suggested as you will need the `lmgrd` and `xilinxd` files in this archive to actually serve your licenses.
2. Open a command window in Administrative mode by typing `cmd` in the Windows Start Menu search box, right clicking on the `cmd.exe` button and choosing Run as administrator.
3. Run `< Server Tools Directory>\<Tools Version>\win64.o\installanchorservice.exe`.

Linux:

Trusted storage must be manually installed and initialized on Linux by performing the following steps.

1. Extract the License Management Tools archive onto your disk. A permanent location is suggested as you will need the `lmgrd` and `xilinxd` files in this archive to actually serve your licenses.
2. With root or sudo access, open a command-line shell.
3. Run `<Server Tool Directory>/<Tools Version>/lnx64.o/install_fnp.sh`.

Requesting a Floating License From Your License Server Machine

To generate floating (server) activation-based licenses, you must use the `xlicsrvrmgr` command-line executable run from your server machine to access the Xilinx License Management site. Failure to use this tool and going to the Xilinx License Manage website directly in a browser results in all activation-based licenses being non-selectable. To generate a floating license from an entitlement in your Xilinx License Management Account, do the following.

1. From your sever tools directory (above), run `xlicsrvrmgr -cr <outputdir>/server_req.xml`.

   This creates a license request into the trusted storage area which causes XML and HTML files to be output containing your server's Host ID information.

2. Open the `server_req.html` file in the browser of your choice.

   This.html file effectively contains a URL with the Host ID information that activation requires to lock a floating license to your server.

3. Your web browser should now open with a Xilinx login screen.

   Note: If your machine is not currently connected to the internet or is having proxy issues you may take this HTML to a web browser on any machine that is connected to the internet.

Generating a Floating Activation License on the Xilinx License Management Website

1. From the **Xilinx Licensing Site** login screen, enter your Xilinx.com username and password to sign in and confirm your address information.
2. Select the licensing account which contains your licenses from the **Account** drop-down menu, if necessary.
3. Scroll down, if necessary, to the Activation Based Licenses section of the webpage (Figure 5-4.).

   Note: After you check an entitlement in either the "Activation Based Licenses" area or the "Certificate Based Licenses" area, the other area will automatically become inactive. Activation and Certificate licenses must be generated separately, although multiple licenses of the same license type may be selected. To reactivate both areas, uncheck all licenses in that area.

4. Select the Activation licenses of your choice and click the **Activate Floating License** button..

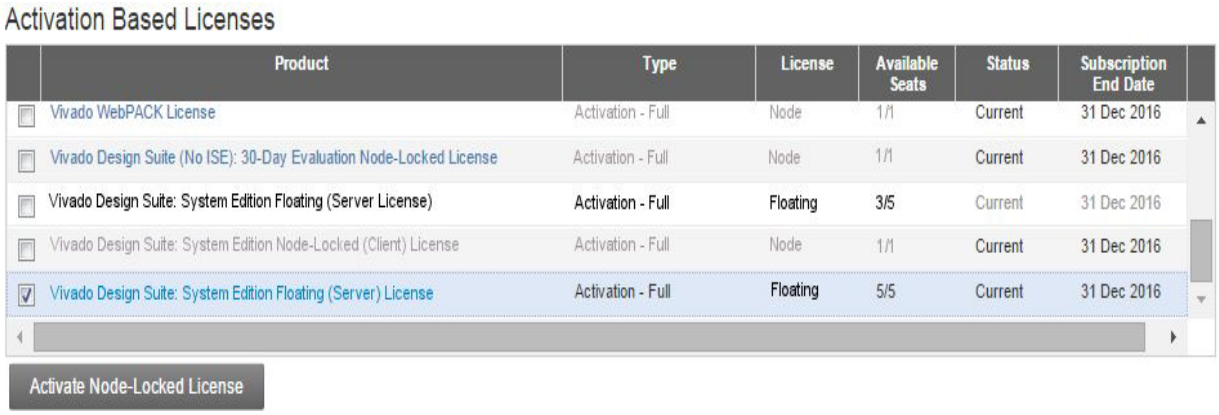


Figure 5-4: **Create New Floating (Server) Activation License**

5. A dialog will open where you can specify the number of license seats from your entitlement that you wish to assign to this server in the **Requested Seats** field. The default is 0, but a non-zero number is required to continue.

   Note: If your Vivado subscription was purchased or renewed after the launch of Vivado 2015.4, a borrow feature is enabled on your floating license. For more information on the borrow feature, see Borrowing Licenses below.

6. If the borrow feature is enabled on your licenses, you will see an additional field to the right called **Borrowed Seats** (Figure 5-5). Here you will specify the number of requested seats that are eligible to be borrowed. The default is 0, which means no seats will be available for a user to borrow and you may enter any number up to the number of requested seats in the previous column

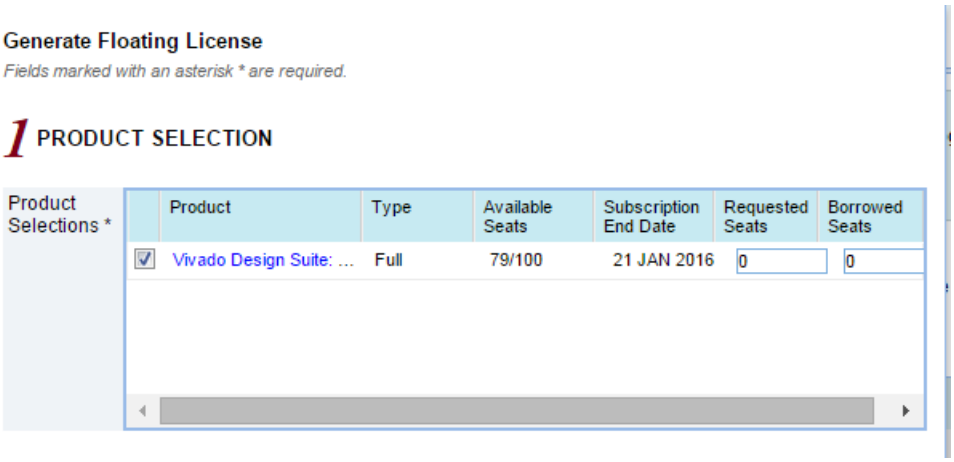


Figure 5-5: **Specifying Floating and Borrowable Seats**

7. After inputting the requested and borrowed seats, press the **Next** buttons until the license generation begins.

8. Your `Xilinx_License.xml` file will be e-mailed to you. You will need this file to finish installing and serving your license

Installing and Serving a Floating Activation License File On Your Machine

After you receive your `Xilinx_License.xml` file, please save it off to a local directory. The following steps instructs you on how to install the license, and how to serve it on your floating server.

1. From your sever tools directory (above), run `xlicsrvrmgr -p <response filename i.e.(xilinx_license)>.xml`.
2. This will store the license information into your trusted storage area.
3. Verify that the license is installed by viewing your trusted storage area: xlicsrvrmgr –v "format=long".

License File Requirements

Before completing the following steps, there are some things that need to be understood about Flexera's lmgrd license server utility. LMGRD and other familiar FLEX server utilities are still used for serving and managing activation-based floating licenses. While licenses in trusted storage are automatically found and served by lmgrd, lmgrd requires that a license file (.lic) be specified. For activation-based floating licenses, the license file is just needed to specify certain network basics.

```
SERVER <host_name> <host_id> <port>  (Xilinx's default port=2100)
USE_SERVER
VENDOR xilinxd
```

If you already going to serve an existing Xilinx license file, like for Xilinx IP or ISE Design Suite, there is nothing further needed. If you are only going to be serving the activation-based licenses on the server, then you will need to create a basic license file (.lic) with the information listed above.

4. Ensure that a license file .(lic) meeting the minimum criteria above is present.
5. Run lmgrd to serve your licenses.

Windows:

<Server Tool directory>\win64.o\lmgrd -c <path_to_license>\<license filename>.lic –l <path_to_license>\<log filename>.log

Linux:

Note: For Linux users - lmgrd command requires library paths to be set. Xilinx provides a shell script to set this for you, lmgrd.sh. If you use the lmgrd command-line tool alone, you are likely to see an error

```
<Server Tool directory>/lnx64.o/lmgrd.sh -c
<path_to_license>/<license file>.lic -l <path_to_license>/<log
filename>1.log
```

IMPORTANT: *If you are using a Windows 8.1 machine as your floating server or if you wish to support borrowing from your server, you must use the 11.13.0 version of `lmgrd` and `xilinxd` found in the Vivado 2015.x Server Tools download. Re-initialization of trusted storage will be required when moving from the previous 11.11.0 `lmgrd` and `xilinxd` to 11.13.0. If you do not wish to enable borrow and are not using a Windows 8.1 machine, you may continue to use your existing 11.11.0 `lmgrd` and `xilinxd`.*

Borrowing Licenses

Beginning with Vivado 2015.1, Xilinx introduces the ability to borrow activation-based licenses from a compatible server to the trusted storage of your local machine. This means that, for a period of time specified during the borrow request process, the license seat count on the server is decremented by 1, and the license is activated in the local trusted storage of the borrow client. This allows the borrow client to then have an effective node-locked Activation license, which can be taken off network, etc. At the end of the borrow time period, the license will automatically deactivate on the client's machine, and will be restored to the floating server. Vivado also gives you the ability to restore a license to the floating server early, if the borrowed seat is no longer needed.

Is The Server License Borrowable?

Existing Vivado floating activation-based licenses issued prior to April, 2015 cannot be borrowed. When your Vivado subscription comes up for renewal after April, 2015, new floating activation-based entitlements from that renewal will be borrowable. However, the decision to allow borrow or not, or how many seats of a total entitlement are borrowable rests with administrator generating the license and is made during the license generation process.

From a client, it is straightforward to determine if a license is borrowable using Vivado License Manager, and this is discussed in the Borrowing Licenses section.

Borrowing a License

At this time, it is only possible to borrow from an activation-based floating server to a node-locked client. The following steps cover how to borrow a license using Vivado License Manager.

1. Open VLM and select **Borrow/Restore License Seat** which is located under the **Manage License** section in the left-hand window pane.

2. In the main area, all floating servers on your network will be queried to see if they contain borrowable activation-based licenses (Figure 5-6).

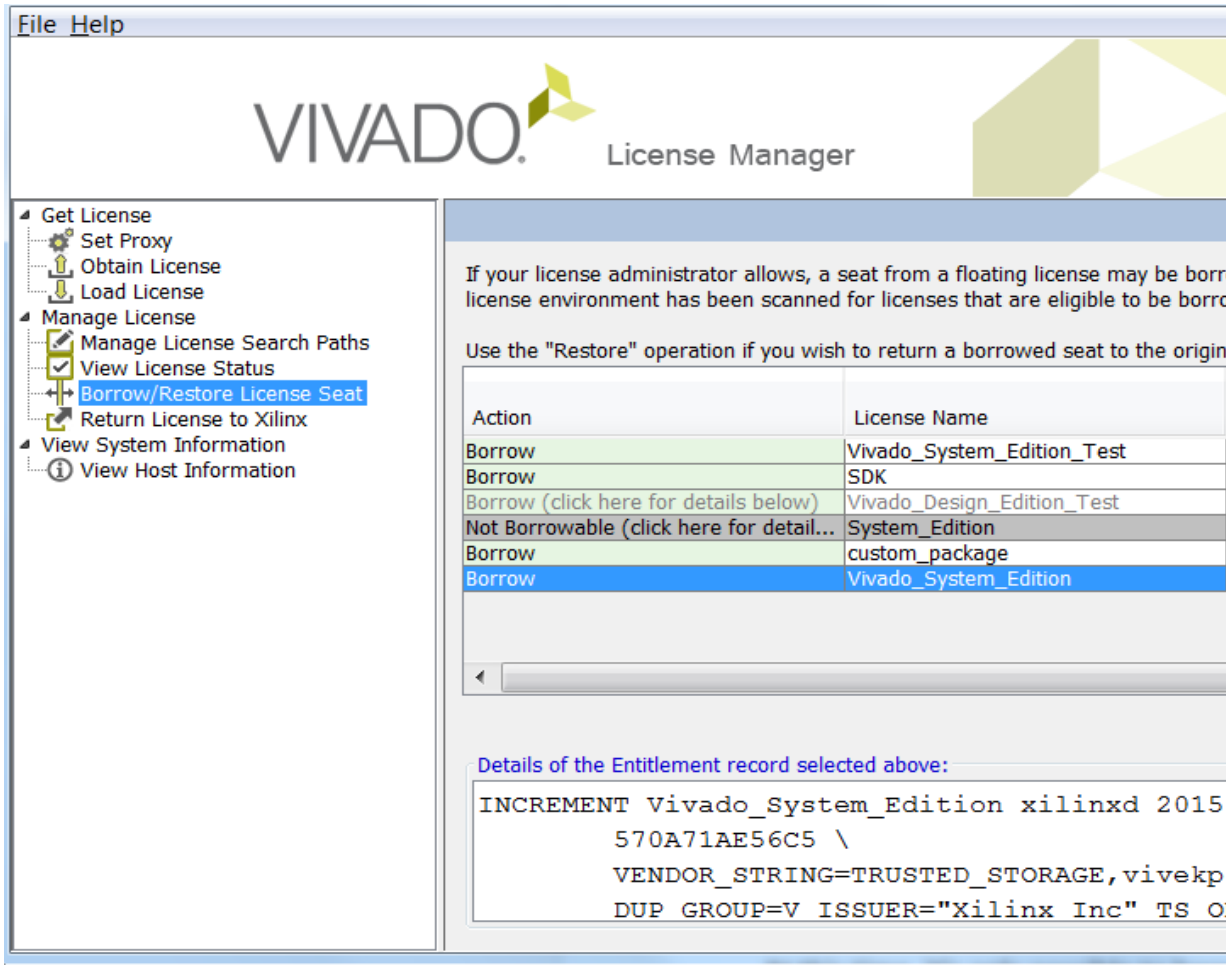


Figure 5-6: **Borrow/Restore License Seat**

3. Select the license you wish to borrow and click the **Borrow/Restore** button.

   In Figure 5-6, there is a license row where the text is gray, but the background is the normal coloration. This indicates that this license is allowed to be borrowed, but cannot be borrowed at the moment. In this case, it is because all borrowable seats have already been borrowed. If the background of a row is gray, as in the Figure, this is an indication that the license cannot ever be borrowed. Common causes for this are older server Flex software (11.11.0 or 11.6.0 – 11.13.0 is required), or the license itself is not setup for borrow (Example: A 2014.x era floating license.)

4. A Borrow Confirmation screen will appear, this is where you will need to specify how long you wish to borrow the license. This is done in the **Set Borrow Expiration Date** dialog box highlighted in Yellow (Figure 5-7).

The default borrow date is set 30-days from the current date, or at the expiration date of the server license, whichever comes first. You will not be allowed to enter a borrow end-date that is greater than the license expiration date.

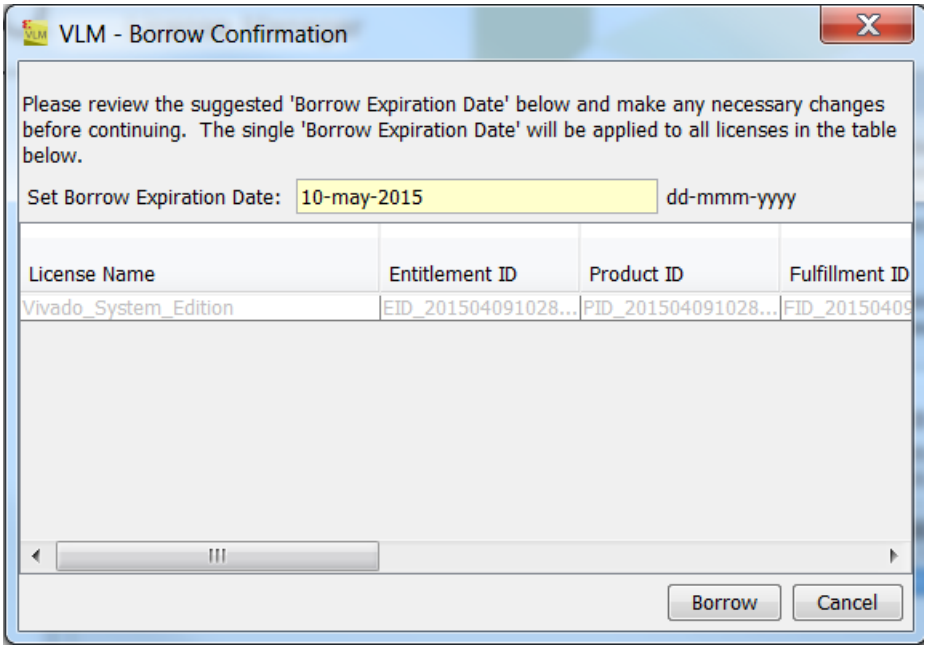


Figure 5-7: **Set Borrow Time-Limit**

5. Click the **Borrow** button on the confirmation screen and the license will be decremented from the server and added to the client's local trusted storage.

   The screen will refresh, and you will see that a license seat has now been added to the list with a value of **Restore** in the first column.

Restoring a Borrowed License

If you do not wish to keep the borrowed license for the entire time you specified, you may restore it to your local license server.

1. Open VLM and select **Borrow/Restore License Seat** which is located under the **Manage License** section in the left-hand window pane.
2. Select the license you wish to restore. Eligible licenses will have **Restore** listed next to them in the Action column (Figure 5-8).
3. Click the **Borrow/Restore** button and the confirmation dialog box appears.
4. Specify the Port that the floating license server is using.

   Unfortunately, Vivado License Manager cannot detect which port the license server is using. VLM prepopulates the default Xilinx license server port, but if your server is using something different, it needs to be specified. Specifying an incorrect port will disable

the license on the local client machine, but the seat will not be available to others until the original borrow time period expires.

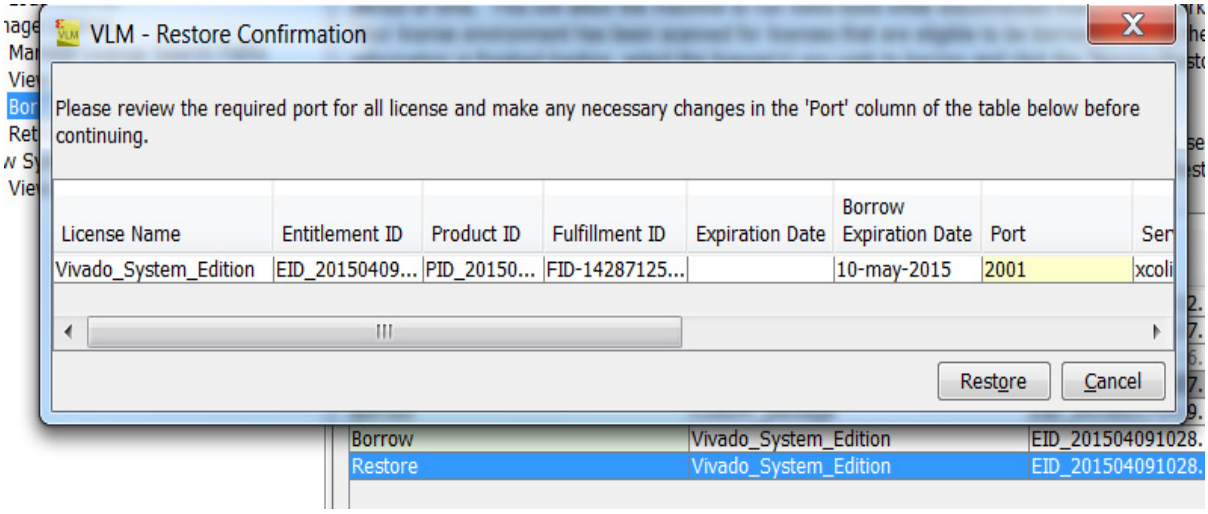


Figure 5-8: **Set Restore Port**

5. Click the **Restore** button and the license will be rendered inactive on the client machine, and the license count on the server will be incremented by one.

Returning Licenses

For information on returning certificate-based licenses from your machine to Xilinx, please see Modifying Licenses. Activation-based licenses can returned to Xilinx through either Vivado License Manager (Node-Locked) or the `xlicsrvmrgr` command line utility (Floating).

Returning Node-Locked (Client) Licenses

1. Open the Vivado License Manager.
2. In the left-hand window pane click **Return License to Xilinx** which is located under the Manage License section.
3. In the main area of the screen, a list of the node-locked licenses currently in your trusted storage area will appear.

   If **No** appears in the Disabled column, this means that license is an active license and is eligible to be returned. If **Yes** appears in the Disabled column, this usually means a return has already been attempted, but not completed (your account has not been credited).

4. Select the license you wish to return and verify the contents of the license by looking in the **Details** section at the bottom of the main area.
5. Click **Return**.

6. An important confirmation dialog appears (Figure 5-9).

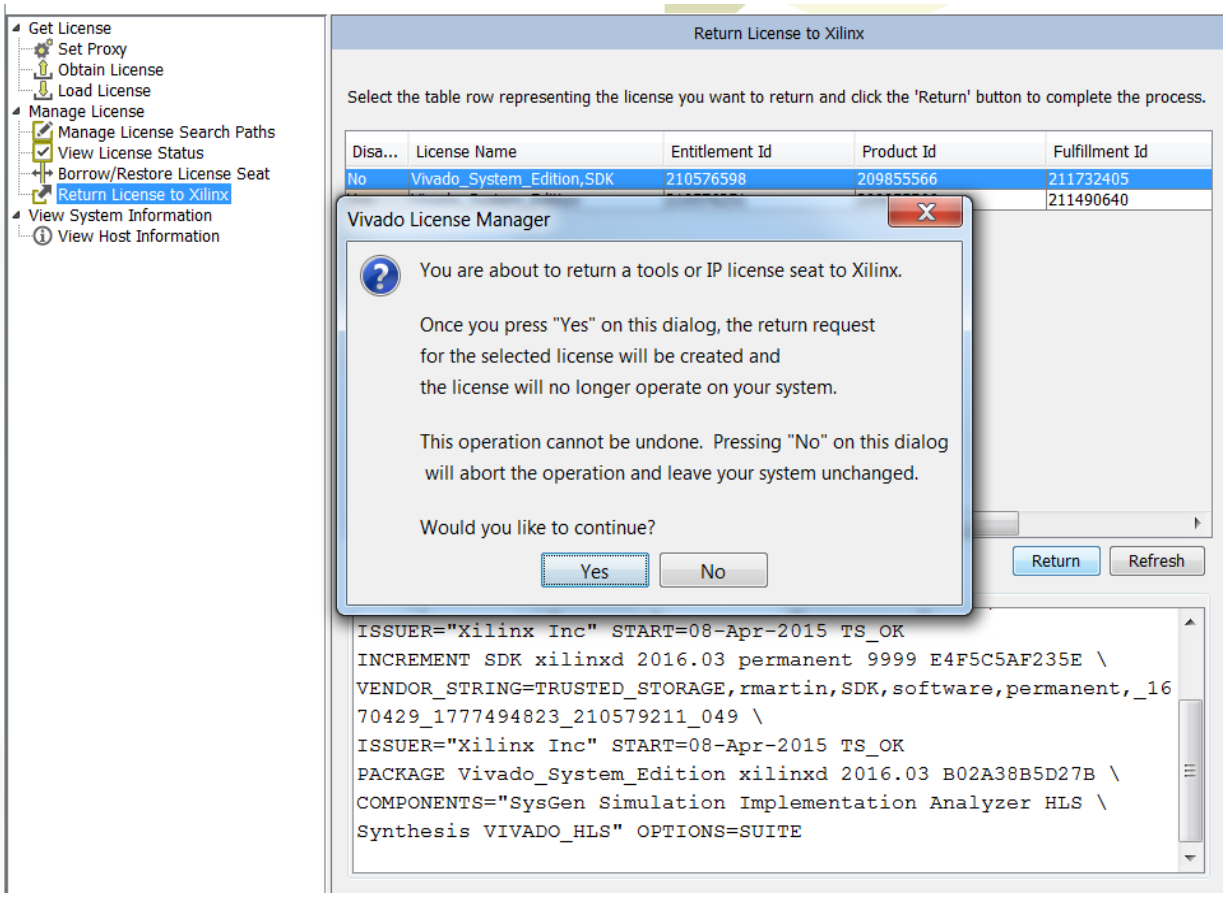


Figure 5-9: **Return License to Xilinx**

When you attempt to return an Activation license, it is first marked disabled in your trusted storage area, which means it can no longer be used on your machine, before VLM attempts to contact the Xilinx License Management website and place the entitlement back in your account. Since this cannot be undone, it is recommended that you ensure a connection to the internet.

7. Vivado License Manager will contact the Xilinx License Management website and will automatically credit your account with the license return.

Returning Floating (Server) Licenses

To return a license from a floating license server to Xilinx, you must do so from that server using the xlicsrvrmgr utility

1. Create the return request.

   xlicsrvrmgr –cr <return request.xml> -r <fulfillment ID>

Notice how both the –cr (create request) flag AND –r (return request) flag are used. Fulfillment ID can be obtained by running the xlicsrvrmgr –v "format=long" command

2. Send the return request to Xilinx.

   xlicsrvrmgr –returnTransaction "request=<return request.xml>" "response=<response filename.xml>" "proxy=<proxy:port>"

   This command sends the return request .xml to Xilinx, where the return is made and your account is credited with the returned seat. A response XML is generated which you will use for Step 3.

3. Process the return response .xml file which removes the deactivated license from the local server's trusted storage.

   xlicsrvmgr –p <response filename.xml>

Generating/Installing Certificate-Based Licenses

For certificate-based licenses, as long as you know the Flexera Host ID (Ethernet MAC ID, Drive Serial Number or Dongle ID) you wish to lock your license to, you do not need to enter the Xilinx License Management site from one of our utilities. Instead, you may go directly to www.xilinx.com/getlicense. After logging in and selecting your account, you may select products as described in the Product Selection section.

After one or more licenses are selected on the Create New Licenses page, click the **Generate License** button corresponding to the type of license file you are generating (client/node-locked or server/floating).

The step-by-step instructions below are for generating a floating certificate-based license as this process contains a superset of all other certificate-based license generation flows.

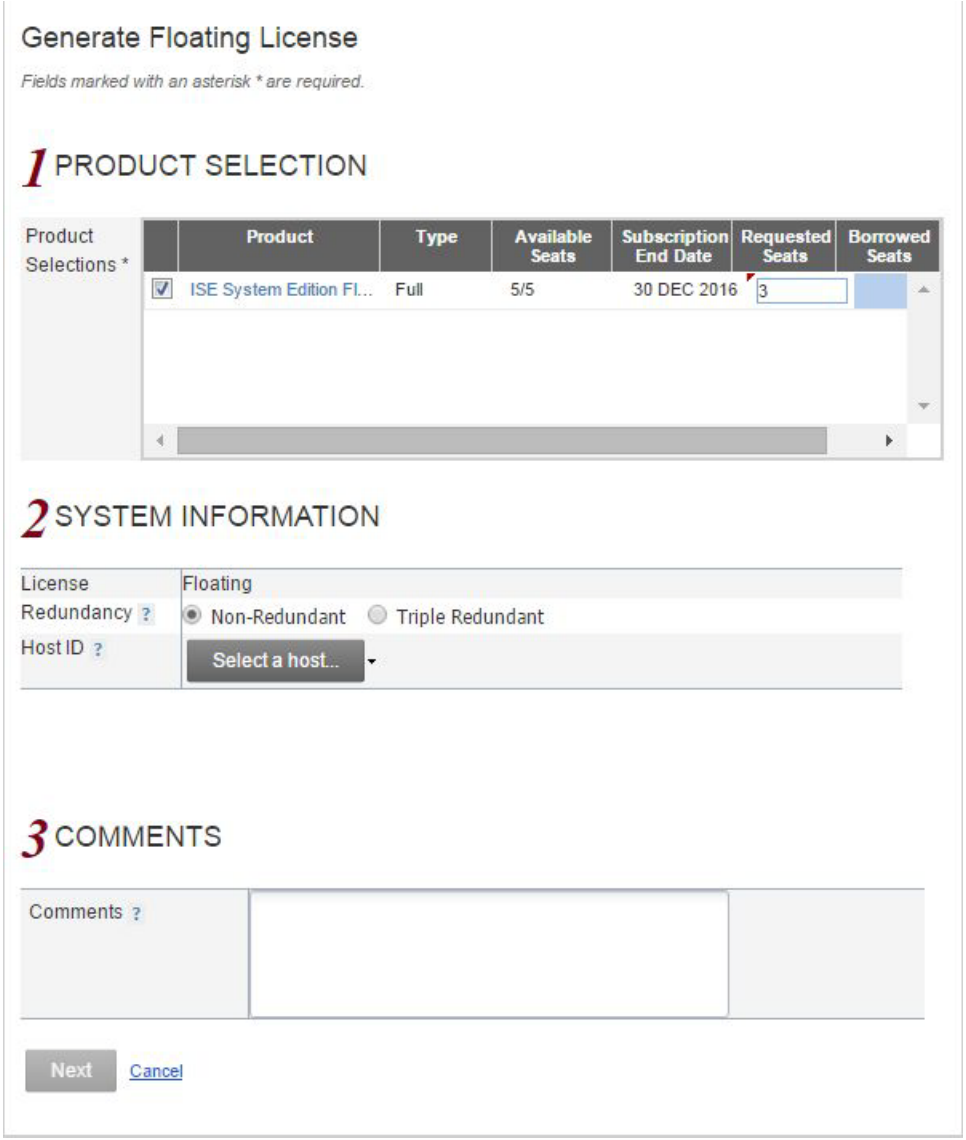


Figure 5-10: **Generate Certificate-Based Floating License**

Certificate-Based Node Locked License

After generating a license file, you will receive an email from 'xilinx.notification@entitlenow.com'.

1. Save the license file (`.lic`) attached to the e-mail to a temporary director y on your local system.
2. Run the Vivado License Manager:
   - For Windows 7 or earlier: **Select Start > All Programs > Xilinx Design Tools > Vivado 2015.4 > Manage Xilinx Licenses**.

- For Windows 8.1: Run the **Manage Xilinx Licenses** app from the full listing of Apps on your Start screen.
- For Linux: Type vlm in a command-line shell.

3. On the left hand pane of Vivado License Manager, expand **Getting a License** and choose **Load License**.
4. If you received a certificate license (`.lic`) file, click the **Copy License** button on the Load License screen.
5. Browse to your license file (`Xilinx.lic`) and click **Open**.
6. This action copies the license file to the `<Homedrive (typically C)>:\.Xilinx (Windows)` or `<Home>/.Xilinx` directory of your computer where it will be automatically found by the Xilinx tools.

Certificate-Based Floating License

1. Select the number of seats required for each product license.

   This is for floating licenses only. All node-locked licenses are for one seat. The number of seats available for a product entitlement is automatically maintained by the system. The Requested Seats field is populated, by default, with zero, although you are allowed to enter any number up to the full number of seats remaining on the product entitlement. A product is removed from the product entitlement table once all seats have been generated.

2. Enter system information.

   For floating certificate-based licenses, the first field is redundancy. A triple-redundant server configuration, also known as a triad, provides a fail over for the license manager software. As long as two of the three servers are running, the license manager can continue to run. This does not apply to node-locked licenses.

   The system information is pre-populated in the Host ID drop-down menu if you arrived at the Product Licensing Site from a link within the Vivado License Manager. If you do not have pre-populated system information, or if you want to add a different host, select the **Add a host** option.

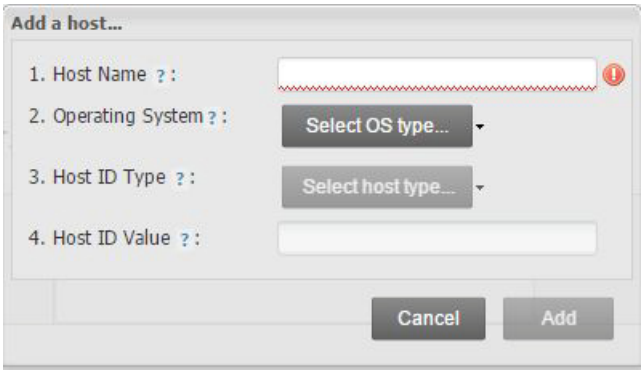


Figure 5-11: **Add a Host**

The Host ID value uniquely identifies the machine to which your design tools or IP is licensed. You can choose a Host ID Type to be a MAC address, a hard drive serial number or a dongle ID.

For activation-based licenses, all required system information is passed from the Vivado License Manager, or the command-line tools, through the web-browser's URL. There is no need to manually enter host information for either client or server-based activation licenses.

Note: Not all host ID types are supported for all operating systems. The easiest way to obtain your host ID is to run Vivado License Manager on the machine that serves as the license host.

3. Add a comment.

   Adding a comment to the license key file makes it easier for an administrator to track the allocation of design tools and IP product entitlements among users.

4. Click **Next**.

   The Review License Request form opens.

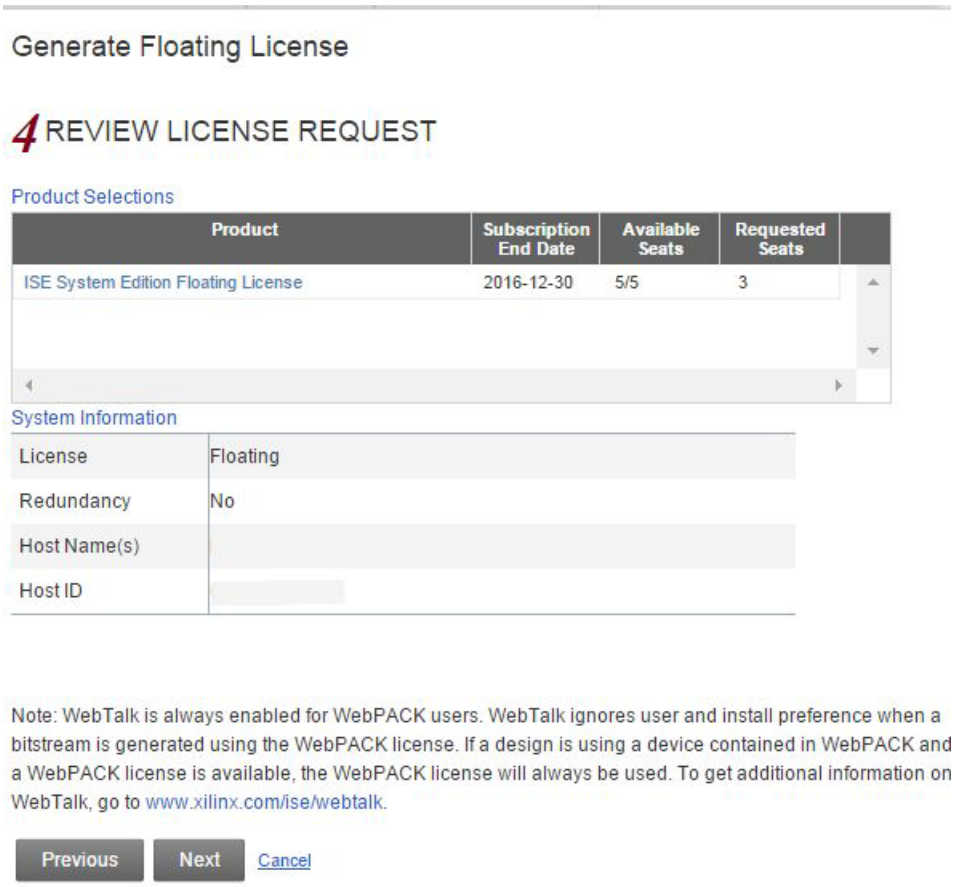


Figure 5-12: **Review License Request**

5. Review your selections.
6. If you are satisfied with your selections, click **Next**.

End-User License Agreements

Xilinx Design Tools and No Charge IP product End User License Agreements (EULAs) are agreed to during the product installation process. A complete copy of this license agreement is located at: `<install directory>/.xinstall/Vivado_2015.4/data/unified_xilinx_eulas.txt`

If you license IP products, you must accept the terms of the associated IP product EULAs before the license file can be generated.

Third-Party Licenses

A complete copy of the third-party licenses is located at: `<install_directory>/.xinstall/Vivado_2015.4/data/unified_3rd_party_eula.txt`

License Generation Confirmation

When you finish generating the licenses, you will receive a confirmation message summarizing your licensing activity.

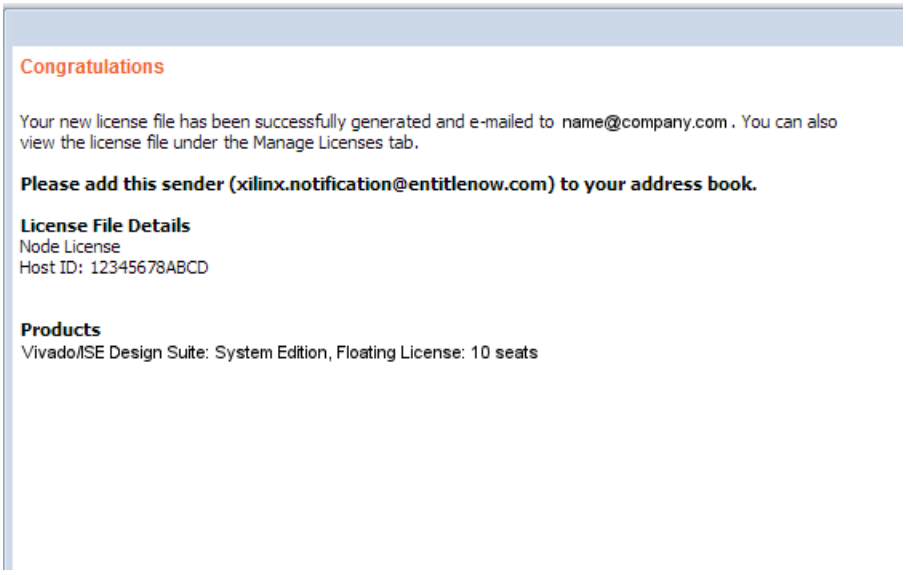


Figure 5-13: **License Generation Confirmation**

You will also receive a license generation confirmation email. This message contains the generated license key file as an attachment. Add xilinx.notification@entitlenow.com as a trusted sender in your email address book.

If you do not receive your license by email, you can download it directly from the Xilinx Licensing Site. See the Managing Licenses on the Xilinx Product Licensing Site section for details

Serving Certificate-Based Floating Licenses

For existing FLEXnet license servers serving certificate-based licenses, a common practice is to copy the contents of the license file, mailed from `xilinx.notification@entitlenow.com`, into the existing license file on your FLEXnet server.

For existing FLEXnet license servers serving activation-based licenses, load the license into trusted storage using the command: `xlicsrvrmgr -p <responseFIleName>`

Note: Restart the floating license server to ensure the new Xilinx licenses are enabled.

For New License Servers

1. Download the appropriate Xilinx FLEXnet license utilities for your server's operating system from the Xilinx Download Center at http://www.xilinx.com/download/index.htm.
2. Unzip these utilities into a destination directory. Xilinx recommends you place this directory into your application search path.
3. After the FLEXnet utilities are installed, run the following commands to start the floating license server:
   - Linux
     - `<Server Tool directory>/lnx64.o/lmgrd.sh -c <path_to_license>/<license file>.lic -l <path_to_license>/<log filename>1.log`
   - Windows
     - `<Server Tool directory>\win64.o\lmgrd -c <path_to_license>\<license filename>.lic -l <path_to_license>\<log filename>.log`

Client Machines Pointing to a Floating License

1. Run the Vivado License Manager (VLM).
2. Click the Manage Xilinx Licenses tab.
3. On the Manage Xilinx Licenses tab, enter the network path to the license server in the port@server format into the `XILINXD_LICENSE_FILE` field.
4. Click **Set**. The default Xilinx port number is 2100.

For Linux operating systems, licensing environment variables cannot be set using the Vivado License Manager (VLM). The environment variable fields are read only, so they are grayed out and there are no **Set** buttons. The environment variable must be set using the appropriate OS shell and commands.

Managing Licenses On Your Machine

Vivado License Manager

The Vivado® License Manager (VLM) is intended to assist with license generation for Node-Locked (Client) Activation and Certificate-based licenses only. For license servers using activation-based licensing, see the section entitled Xlicsrvrmgr Command-Line Utility.

Vivado License Manager is installed with Vivado Edition and many standalone tool installations.

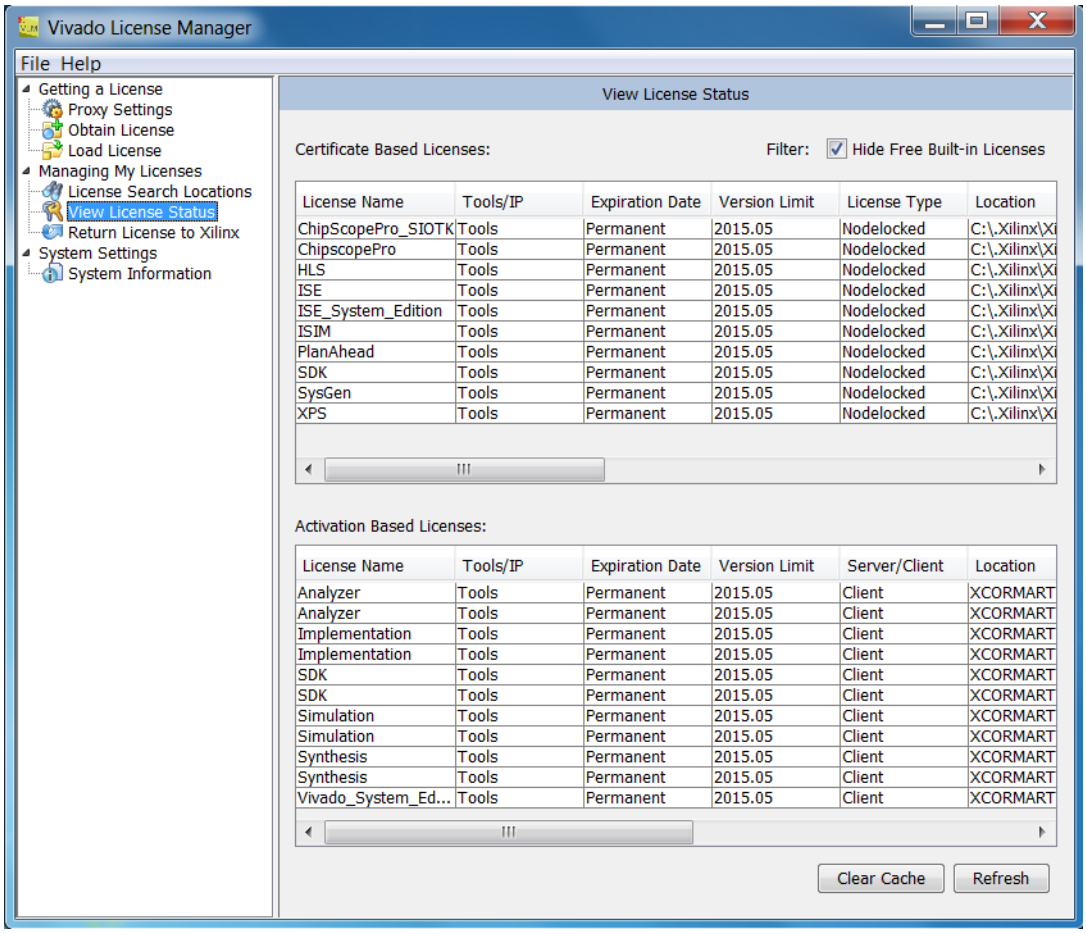


Figure 5-14: **Vivado License Manager**

To Open the Vivado License Manager:

- On Linux, type `VLM` from a command-line shell that has the Xilinx environment loaded. On Windows 7 or earlier, you can run this from the Start menu at **Start > Xilinx Design Tools > Vivado 2015.4 > Manage Xilinx licenses**.
- On Windows 8.1, run the **Manage Xilinx Licenses** app from the full listing of Apps on your Start screen. You can also run Vivado License Manager from the Help menu of Vivado: **Help > Obtain A License Key** or **Help > Manage License**.

The typical tasks that Vivado License Manager is used for are:

- **Obtaining A License**: Choose from several license options and go to the Xilinx Product Licensing Site to complete the license generation process. To generate a license for an activation-based entitlement, Vivado License Manager should be used to access the Xilinx Product Licensing Site. This can be done on the **Obtain a License** screen by

pressing **Connect Now**, if an internet connection is present, or by pressing **Save Link As** if one is not. **Save Link As**, saves the information that Vivado License Manager normally passes to the Xilinx Product Licensing Site through parameters on the URL, into an HTML file for later use.

- **Viewing License Status**: See which licenses are visible to the local machine. This is a useful view for debugging licensing issues.
- **Loading Licenses Onto a Local Machine**: After a certificate license (`.lic`) or Activation fulfillment (`.xml`) file has been received, they can be placed into the appropriate location on the machine. For step-by-step instructions, see the Installing Your License key section for your license type below.
- **Returning a License to Xilinx**: (Activation-based licenses only) If a license is no longer needed on a local machine, it can be returned to Xilinx and the entitlement credited back to the licensing account.
- **Viewing and Setting (Windows) License Search Locations**: Vivado tools will look in several default locations to try to find authorization to run. If your license is located elsewhere on the machine or on a floating license server, a path to that license must be specified.



RECOMMENDED: *It is recommended that the `XILINXD_LICENSE_FILE` environment variable be used to specify Xilinx license file locations. `LM_LICENSE_FILE` can also be used, but is mainly intended for non-Xilinx or legacy license path use.*

Xlicclientmgr Command-Line Utility

Xlicclientmgr is a command-line utility for creating Activation license requests and otherwise managing a client (node-lock) computer's trusted storage area. See the details on the Xlicsrvrmgr utility below for creating and interacting with a server (floating) computer's trusted storage area.

Xlicclientmgr can do many of the same functions the graphical Vivado License Manager utility can do, but is limited to servicing activation licenses. `Xlicclientmgr` is located in the `<Install Directory>\Vivado\2015.4\bin` directory of a Xilinx tool installation.

Key Xlicclientmgr Command-Line Flags

- `-help all`: Prints usage information for xlicclientmgr.
- `-v or -v "format=long"`: Displays a list or detailed list of the contents of the machine's trusted storage area.
- `-cr <XML RequestFileName> [-r fulfillmentID]`: Creates a request in trusted storage. This is the command used to request an activation license from Xilinx. It will create an activation request in XML format, as well as an HTML file containing a URL with information for use with the Xilinx Product Licensing Site. If `-r` is used, it will create a request to return the license with the specified fulfillment ID to Xilinx.
- `-p <responseFIleName>`: Process XML file into trusted storage. This is essentially the same command run by the **Activate License** button on Vivado License Manager's Load License screen.
- `-returnTransaction "request=<requestFileName>" "response=<responseFileName>" "proxy=<host:port> [<proxy userId> <proxy passwd>]"`: Transmits a return request from local machine to the Xilinx Product Licensing Site.

  Note: A return request must already exist in the form of an XML file. This return request must have already been created by a previous run of `xlicclientmgr` using `-cr` and `-r` options together.

Xlicsrvrmgr Command-Line Utility

The Xlicsvrmgr is a command-line utility for creating Activation license requests and otherwise managing a floating license server computer's trusted storage area.For floating license generation on activation-based entitlements, the OMS website must be accessed by first running the Xlicsvrmgr utility. Vivado License Manager supports client (node-lock) activation transactions only, but floating server license requests require xlicsrvrmgr.

The Xlicsrvrmgr is contained in the License Management Tools download located at: http://www.xilinx.com/download/index.htm. The utility is also located in the `<Install Directory>\Vivado\2015.4\bin` directory of a Xilinx tool installation.

Before Running Xlicsrvrmgr The First Time

If this is the first time `xlicsrvrmgr` is to be run on a floating license server, then you will need to ensure that the computer's trusted-storage area, where activation authorizations are stored, is first installed and initialized. In the License Management Tools download, you will find an initialization utility that varies by OS. Run the commands as specified below from the `<OS><bitwidth>.o` directory where the License Manage Tools were unzipped. (For Example: `c:\servertools\win64.o\`):

- Windows:installanchorservice.exe xilinxd Xilinx-Design-Suite-Software
- Linux: `install_fnp.sh`

Key Xlicsrvrmgr Command-Line Flags

- `-help all`: Prints usage information for xlicsrvrmgr.
- `-v or -v "format=long"`: Displays a list or detailed list of the contents of the machine's trusted storage.
- `-cr <XML RequestFileName> [-r fulfillmentID]`: Creates a request in trusted storage.

  This is the command used to request an activation license from Xilinx. It will create an activation request in XML format, as well as an HTML file containing a URL with information for use with the Xilinx Product Licensing Site. If –r is used, it creates a request to return the license with the specified fulfillment ID to Xilinx.

  Note: If you wish to create a new activation license for a floating license server, this -cr command must be run and the URL in the resulting HTML file must be used to access the Xilinx Product Licensing Site. If you enter the product licensing site directly or through links, the Activation section of the website will be inactive.
- `-p <responseFIleName>`: Process XML file into trusted storage.
- `-returnTransaction "request=<requestFileName>" "response=<responseFileName>" "proxy=<host:port> [<proxy userId> <proxy passwd>]"`: Transmits a return request from local machine to the Xilinx Product Licensing Site.

Note: A return request must already exist in the form of an XML file. This return request must have already been created by a previous run of xlicclientmgr using `–cr` and `–r` options together.

Using the Xilinx Product Licensing Site

The Xilinx Product Licensing site is where both certificate and activation-based licenses are generated, where certificate-based licenses are modified and where information about license orders reside. As mentioned earlier, creation of activation-based licenses requires

you to access the Xilinx Product Licensing Site from the Vivado License Manager or appropriate command-line utility.

You can access the Xilinx Product Licensing Site in various ways depending upon the type of license being generated.

- If you purchased products which use certificate-based licenses, follow the link included in your order confirmation email. It provides direct access to an account containing your product entitlements.
- If you purchased products which use activation-based licenses, use Vivado License Manager, xlicclientmgr or xlicsrvrmgr to generate your license request. The license request information is then sent from the Vivado License Manager or command-line tools through a URL to access the account containing your product entitlements.
- To evaluate the Vivado® Design Suite products, go to http://www.xilinx.com/products/design_tools/vivado/vivado-webpack.htm.
- To evaluate IP products, go to http://www.xilinx.com/ipcenter and follow the Evaluate link on the IP product page of interest.
- To access the Product Licensing Site directly, go to http://www.xilinx.com/getlicense. By accessing the site this way, you will not be able to create activation-based licenses, but you will be able to create certificate-based licenses as well as perform license account management functions.

  When entering the Xilinx Product Licensing Site, you must first register or enter your registration information.

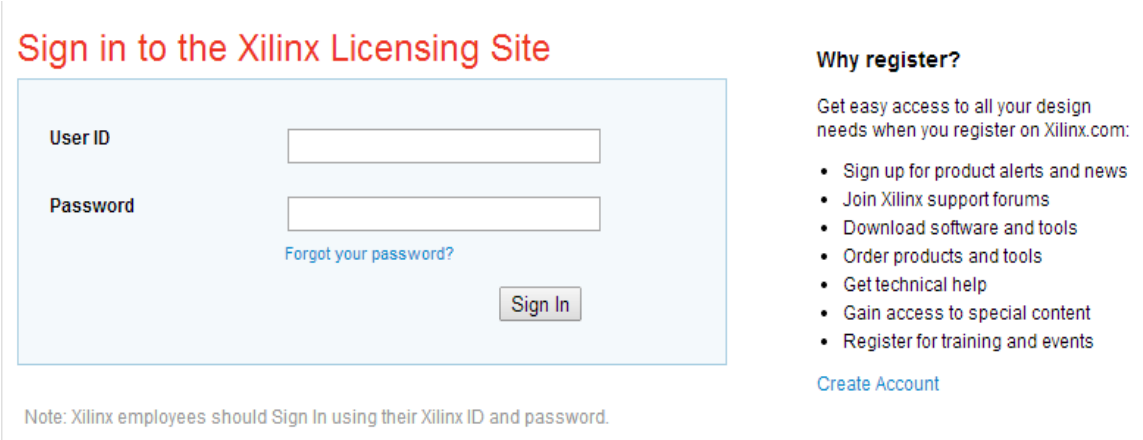


Figure 5-15: **Xilinx Product Licensing Site - Sign In Page**

5. You must first sign in. If you already have a Xilinx user account, enter your user ID and password, and then confirm your contact information is current. If you do not have an account, click the **Create Account** button.

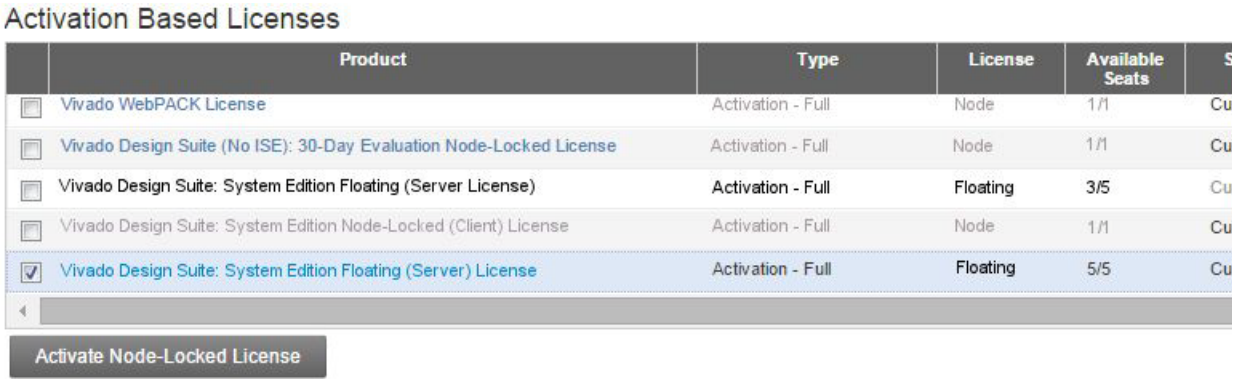


Figure 5-16: **Create New License**

Product Selection

To begin the license generation process for products you have purchased or want to evaluate:

1. Select a product licensing account from the Account drop-down list.

   Note: This selection is not available if you are entitled to evaluation or free products only.

2. Enter product voucher codes for design tools or IP product licenses purchased with kits or for tools purchased from the Xilinx online store (optional).
3. Add evaluation or no-charge IP product entitlements to the product entitlement table (optional).
4. Make your product selections from the product entitlement table.

Entitlements are grouped into two broad categories: certificate-based or activation-based licensing. The type of product entitlements available are Full (purchased), No Charge, or Evaluation. Full and No Charge licenses have a subscription period of one year. Design tool evaluation is for 30 days and IP evaluations are for 120 days.

Floating/server and node-locked/client licenses cannot be combined in the same license file. Selecting an entitlement that contains only one license type causes the **Generate** button for the other license type to become inactive. Likewise certificate-based and activation-based entitlements cannot be generated at the same time. Selecting an entitlement in one license area causes the other license area to become inactive for the remainder of the license generation session.

For design tools, available seats represents the number of seats available for licensing over the total number of seats purchased. For IP, seats are managed according to the terms of the site wide license agreement.

Products with a status of Current are within their warranty period. Products with a status of Expired have a warranty period end date that has passed. If seats are available, licenses can be generated for either Current or Expired product entitlements.

The Vivado Design Suite: 30-Day System Edition evaluation product entitlement provides access to all the capabilities in the Vivado Design Tools. This product entitlement is automatically included in your product licensing account.

Product vouchers for design tools and IP product licenses can be shipped with a Xilinx or partner development board or design kit. If you have a product voucher card, you can enter the voucher code on the card into the associated text field and click Redeem Now. This places the corresponding design tools or IP product entitlement in the product entitlement table which you can use to generate a license key.

To add Evaluation and No Charge IP to the list of product entitlements, click the **Search Now** button in the Add Evaluation and No Charge IP Cores section of the page. This opens an IP product finder tool.

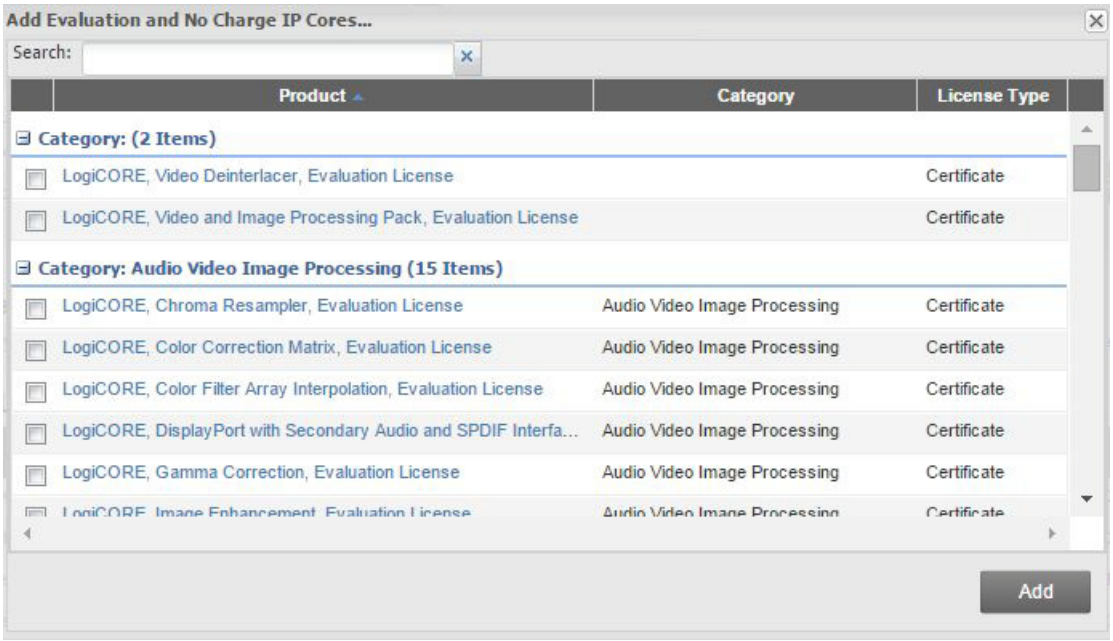


Figure 5-17: **IP Product Selector**

Managing Licenses on the Xilinx Product Licensing Site

The Xilinx Product Licensing Site tracks the licenses that you have generated. Select the Manage Licenses tab to see all licenses generated in your product licensing account.

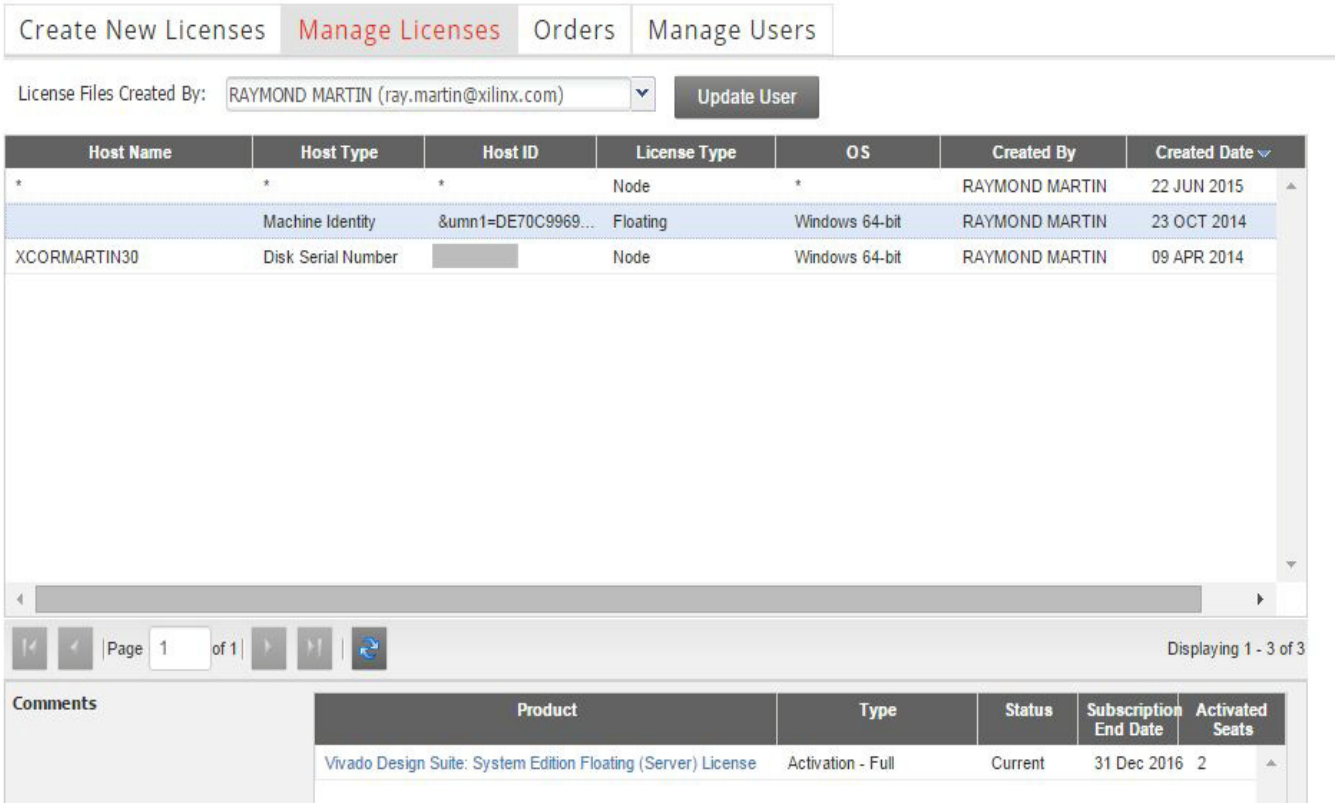


Figure 5-18: **Manage Licenses**

Use the Manage Licenses page to perform the actions described below.

Exploring and Retrieving Your Existing Licenses

Information regarding the licenses in your product licensing account are displayed in a split-section view. Click a row in the master view in the top table, to see detailed information about the licenses in the detail view in the bottom table. The detail view table displays:

- A list of product entitlements enabled by file.
- Comments associated with the file.

The detail view table gives you the ability to:

- Download - If your license or activation fulfillment file does not arrive through email you can download it here.
- Email - Have the license or activation fulfillment file emailed to you or another user.
- View - Gives you the ability to view the actual license file.

- Delete (Certificate-based Licenses only) - Delete the license file. After a file is deleted the entitlement will then become available on the Create New License page and can be regenerated for another host ID.
- View the end user license agreement (IP only).

Modifying Licenses

Activation-based licenses cannot be modified on the Xilinx Product Licensing Site. To modify an activation-based license, first use the Return License to Xilinx page in the Vivado License Manager or create a return request in the appropriate command-line license manager. After you return an activation-based license, you will see that the entitlement count on the Xilinx Product Licensing Site's Create New Licenses tab has been incremented by the number of seats you have returned. A new activation-based license can now be generated for a different machine, for the same machine with more seats, different features, or other changes.

To modify an existing certificated-based license, select the license file in the master view. You can modify a certificated-based license as follows:

Delete Entire License File and Place Entitlement Back into Your Account

1. From the Manage Licenses Tab (see Figure 5-18, page 70), select the license file you wish to delete.
2. Click the **Delete** button located below and to the left of the license file details.
3. Click the **Accept** button to accept the Affidavit of Destruction.

Note: This will delete all license seats in the entire license file and return the entitlements to your account.

Rehost: Change the Node-Locked or License Server Host ID for a License File

1. From the Manage Licenses Tab (see Figure 5-18), select the license file you wish to rehost.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **System Information**.
4. Change or add new Host ID and/or Host Name by using the drop-down list and text entry boxes respectively.
5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Add Additional Seats to an Existing Licensed Product Entitlement

1. From the Manage Licenses Tab (see Figure 5-18), select the license file to which you wish to add seats.

2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. For floating licenses, you will be able to change the Requested Seats field and add seats up to the total number of seats available in your entitlement.
5. Click **Next** twice. No Affidavit of Destruction is required for adding seats.

Remove Seats From an Existing Licensed Product Entitlement

1. From the Manage Licenses Tab (see Figure 5-18), select the license file from which you wish to remove seats.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. For floating licenses, you will be able to change the Requested Seats field and reduce the number of seats that will be authorized by this license file.
5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Add Additional Product Entitlements to a License Key File

1. From the Manage Licenses Tab (see Figure 5-18), select the license file to which you wish to add features/entitlements.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. Check boxes of any new entitlements you wish to add to this license file.
5. Click **Next** twice. No Affidavit of Destruction is required for adding features.

Delete Product Entitlements From a License Key File

1. From the Manage Licenses Tab (see Figure 5-18), select the license file to which you wish to delete features/entitlements.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. Check boxes of any entitlements you wish to remove from this license file.
5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Modifying a key file uses the same input form as when the license key file was created, except that additional product entitlements of the same license type (floating or node-locked) are made available for adding to the license file.

If, during any of the modification steps, you receive a message that you have exceeded your number of rehost attempts, email cs_1@xilinx.com to request additional rehost options.

Reclaiming Deleted License Components

A product entitlement is deleted when one of the following occurs:

- Changing the license server host for a license key file.
- Removing seats from an existing licensed product entitlement.
- Deleting product entitlements from a license key file.

When you delete seats or remove products from your certificate-based license files, the entitlement is essentially "put back" or reallocated into your licensing account. You will find that the number of entitled seats in the Create New Licenses tab of your account is incremented by the same number of seats you deleted previously from existing license files.

Before the reallocation of entitlement occurs, you must first agree to an Affidavit of Destruction. This legal agreement is required to ensure the deactivated product entitlements are no longer being used.

The number of allocation operations is recorded for each user. Administrators are allowed to reallocate product entitlements five times per major release. End users are allowed to reallocate product entitlements three times per major release.

What Happens to Your License Key File

Each time a license is generated for a product entitlement, a FLEXnet increment line and corresponding package line is added to the license key file. When a license key file is modified to add seats for an existing or new product entitlement, additional increment or package lines are added to the license key file.

When a license key file is rehosted or is modified to delete seats or product entitlements, the corresponding increment lines are regenerated or removed from the modified license key file.

Legacy Licensing

If you wish to obtain a license for Releases 10.1 or earlier, click the **Legacy Licensing** tab.



Figure 5-19: **Legacy Licensing**

Then complete the following steps for the respective versions:

10.1 and Prior Versions

1. Select the version you desire. You will be prompted to verify your contact information.
2. Fill out the requested form with the required information to receive your registration IDs. Your registration ID will be displayed on the screen and emailed for your records.
3. Go to the Xilinx download center, click the **Archive** link under the **Version** column on the left side of the page to select the product you desire.
4. During the download process you are prompted to insert your registration ID to complete the download process.

Your Licensing Account

Product Licensing Accounts

When you purchase a design tool edition or IP product from Xilinx, you are purchasing a license to use and receive updates for that product for one year. The license to use Xilinx deign tools and IP products is managed through the use of product entitlements. A product entitlement is the determination of:

- Which product was purchased
- The number of seats purchased
- The license type (certificate or activation-based, floating or node-locked)
- The product subscription period (product updates are provided throughout the year)

In addition to managing the product entitlements for your purchased design tools and IP, you can also access product entitlements for No Charge or Evaluation products. Full and No

Charge licenses have a subscription period of one year. Design tools evaluations are for 30 days, and IP evaluations are for 120 days.

Generating a license from a product entitlement results in one or more license keys being generated by the website. When installed, the license keys enable the use of the design tools and IP that were purchased or are being evaluated. Your product entitlements and resulting license key f iles are managed in a product licensing account on the Xilinx website.

Product licensing accounts are specific to the individual listed on the Xilinx Software Purchase Order, who is either the end user or administrator of the design tools. All purchases made can be managed in the same product licensing account if a single administrator is named. A company site can have multiple accounts managed by different administrators. The latter is helpful if a site has multiple design teams working on differing projects with different budget pools.

Note: A license can be generated for a product entitlement that has expired; however, it only enables product releases up to the subscription end date. Applying a product update made available after the subscription end date of your license will result in a licensing error the next time the tool is used.

LogiCORE IP License Generation in the Xilinx Design Tools

Any LogiCORE™ IP and design tools entitlements you have purchased appear in your list of entitled products when you log into the Product Licensing Site. Currently, all IP entitlements will generate certificate-based licenses. Licenses for Evaluation and No Charge IP are available on the site in a separate area. Licenses for all your certificate-based design tools and IP can now be generated in one pass. They are emailed to you in a single license file.

User Types and Actions

There are three user types for the Product Licensing Site: customer account administrator, end user, and no-charge user.

Customer Account Administrator

An example of a typical customer account administrator is a CAD tools manager. Every product licensing account must have at least one customer account administrator. A customer account administrator can manage more than one product licensing account.

The responsibilities as the customer account administrator include:

- Generating node-locked or floating licenses for Xilinx design tools and IP products.
- Adding and removing users from the product licensing account.
- Assigning administrative privileges to other users.
- Ordering product DVDs (if desired).

The original customer account administrator is the Ship To contact identified during the product ordering process. That person receives an email with instructions on how to download and license each purchased product. The customer account administrator must follow the link in the email, to ensure access to the purchased products.

End User

Adding end users to a product licensing account allows an engineer or design team member the flexibility to manage and generate license keys on their own. The end user can generate license keys for node-locked products entitlements within the account as well as evaluation and "no charge" license keys for design tools and IP products. A customer account administrator can also configure the end user account to allow an end user to generate floating licenses. An end user cannot:

- View or generate floating license keys by default. This privilege can be assigned to them by the customer account administrator.
- View the license keys generated by other users.
- Add or remove other users to or from the product licensing account.

No-Charge User

No-Charge users can:

- Generate a 30-day free evaluation license key that enables Vivado System Edition.
- Generate a 30-day free evaluation license that enables Vivado HLS.
- Generate license keys for evaluation and no charge IP products.
- Generate a WebPACK™ tool license that enables WebPACK features in both ISE and Vivado.
- Request a Xilinx Design Tools DVD package with one of the following shipping options:
  - Free Shipping (2-4 Weeks)
  - Standard (2-3 Days)
  - Overnight

All user types can download products electronically and request a Xilinx Design Tools DVD.

Note: A customer who is already licensed for a full version of a Xilinx Design Tools product edition can evaluate other Xilinx Design Tools product editions or IP. These product entitlements are made available in the same product licensing account.

Changing Xilinx User Account Information

IMPORTANT: *It is important to keep your Xilinx User Account up to date. As you change companies, addresses or emails might change.*

Modifying Your Corporate Email Address

1. Go to www.xilinx.com.
2. Click **Sign In**.
3. Expand **Personal Information**.
4. Enter your new corporate email address in the **Enter new Corporate email address** box.
5. Click **Save Profile** button for changes to take effect.

Understanding Your Tool and IP Orders

The Orders tab will display information regarding the purchasing orders that created the entitlements you see in this account.

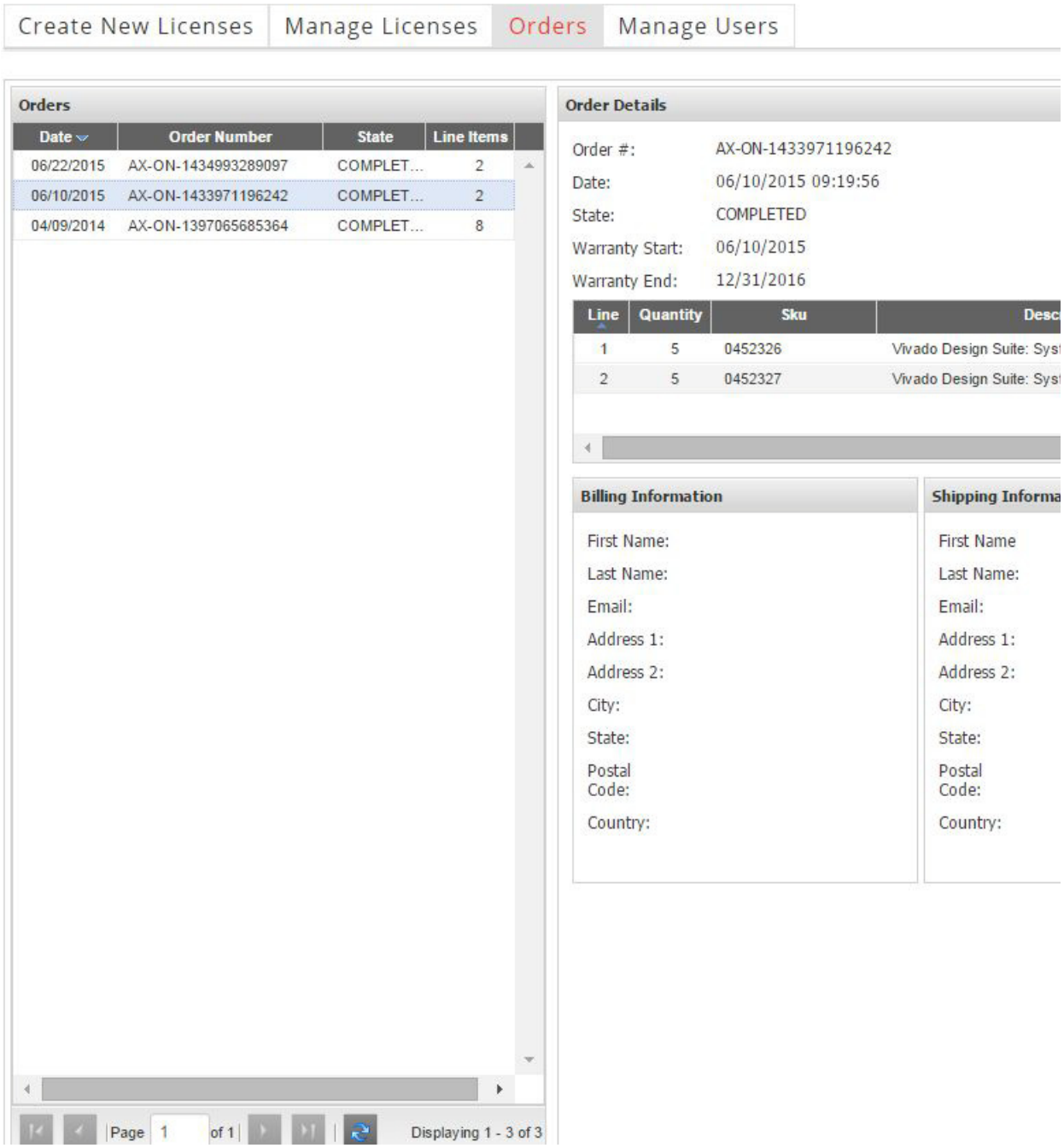


Figure 5-20: **Orders**

- Xilinx order numbers are listed on the left panel of the screen.
- Order details populate on the right panel of the screen when you highlight specific order.
- You might only select one order at a time.

- The order's shipping address information is visible even when product is delivered electronically.

Managing User Access to Product Licensing Account

The responsibility of administering a product licensing account can be transferred or shared with another user. The ability to add or remove users from a product licensing account is managed under the Manage Users tab.

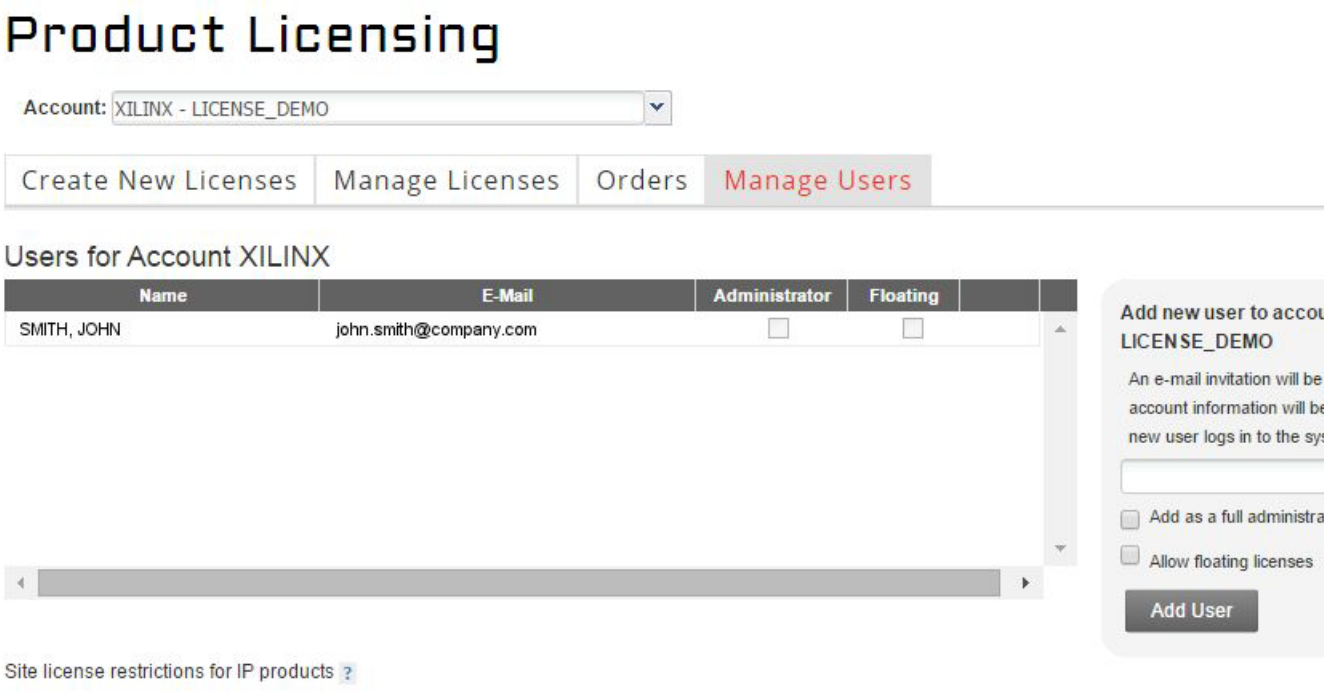


Figure 5-21: **Manage Users**

Adding Users

To add a user to your product licensing account:

- Type in the corporate email address of the new user.
- Check **Add as a full administrator**, to grant the new user customer account administrative privileges. Check **Allow Floating Licenses**, to grant the new user the ability to generate Floating Licenses, but not have full administrative privileges.

Note: The email address you provide must be the same email address the user supplied or supplies when creating their Xilinx account. If not, you might not be properly recognized when logging in.

If added users have already logged into the Product Licensing Site, their name appears in the user list. If they have never been to the site, the words Not Yet Registered appears in the space for their name. After they registered, their name is filled in.

In some instances, a customer account administrator might wish to have design team members administer license key files for their own use. By leaving both Add as full administrator and Allow Floating Licenses check boxes unchecked, you grant the user the following restricted privileges:

- User can generate node-locked license keys only.
- User can view and modify only those license key files they generated for themselves.
- User cannot manage users.

If you check Allow Floating Licenses only, the restriction on node-locked keys is lifted, but the others remain. You cannot check both boxes because it is not allowed. Full administrators already have floating license generation capaility.

Removing Users

To remove administrative or floating license generation privileges from a user, uncheck the **Administrator** or **Floating** check box for that user.

To remove a user from a product licensing account, click the **Delete** button for that user.

Older Release Notes

Vivado 2015.3

What's New

Vivado® Design Suite 2015.3 introduces new market tailored plug-and-play IP subsystems. The new subsystems, in combination with enhancements to Vivado IP Integrator (IPI) and High-Level Synthesis (HLS) for C/C++ and SystemC based design, significantly decrease design creation and integration efforts by abstracting time consuming RTL development.

Device Support

The following new devices are enabled for this release.

Table 6-1: **Vivado 2015.3 Device Support**

Production Level	Vivado 2015.3 Device Support
New Devices	The following UltraScale devices are introduced in this release: • Kintex® UltraScale devices: ◦ XCKU095, XCKU025, XCKU085

Table 6-1: **Vivado 2015.3 Device Support**

Production Level	Vivado 2015.3 Device Support
General Access	The following devices are production ready (in -1 and -2 speedgrades): • Kintex® UltraScale devices: ◦ XCKU095, XCKU025, XCKU085 • Virtex UltraScale devices: ◦ XCVU095, XCVU080
Bitstream Generation	• Bitstream generation for UltraScale devices are limited to: • Virtex UltraScale: ◦ XCVU095 ES2 ◦ XCVU095 ◦ XCVU065 ES2 ◦ XCVU080 ◦ XCVU125 ES2 ◦ XCVU160 ES2 ◦ XCVU190 ES2 ◦ XCVU440 ◦ XCVU440 ES2 • Kintex UltraScale: ◦ All Parts in ES2 and Production

Installation

Beginning with the Vivado 2015.1 release, the install program on Linux no longer requires root or sudo privileges. In the past, these privileges were required to enable cable driver installation. Now, cable drivers must be installed manually by running a separate script while in a root/sudo command shell. For more information on Linux cable driver installation, see the Installing Cable Drivers section of this document.

Vivado Design Edition Tools

RTL Synthesis

- New RTL strategies and directives (Four new strategies, five new directives).
- Inference of the pattern detect circuitry of the DSP block to support convergent symmetric rounding.
- Automatic inference of shifters onto RAM blocks through new directive `AreaMapLargeShiftRegToBRAM`.
- Inference of the new UltraScale RAMs (UltraRAM).
- Pipelining for cascaded RAMB36E2 and UltraRAM, allowing fast performance while saving multiplexing logic and reduce power.
- New RTL attribute to control the number of RAM block cascaded with `CASCADE_HEIGHT`.

Partial Reconfiguration

- Expanded support for UltraScale devices.
  - Place and route support for the KU085, KU095, VU065, and VU080 has been added, bringing the total number of UltraScale devices supported up to twelve.
  - Partial bit file generation is now enabled for KU060, KU095, KU115, and VU095 production silicon, bringing the total number of devices enabled for bitstreams up to six.
    - Bitstream generation is disabled by default for all ES silicon and production silicon that has not completed verification testing.
  - The per-frame CRC checking feature has been enabled in bitstream generation for UltraScale devices.
- A new IP, the Partial Reconfiguration Decoupler, has been released. This IP allows users to easily isolate Reconfigurable Partitions from the static design during reconfiguration.
  - See its IP page for more details: http://www.xilinx.com/products/intellectual-property/pr-decoupler.html
- For more information, see this link in the *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909) [Ref 4].

Tandem Configuration

- Expanded support for UltraScale devices.
  - Place and route support for the KU085, KU095, VU065 and VU080 has been added, bringing the total number of UltraScale devices supported up to 13.
  - Partial bit file generation is now enabled for KU060, KU095, KU115 and VU095 production silicon, bringing the total number of devices enabled for bitstreams to 6.
    - Bitstream generation is disabled by default for all ES silicon and production silicon that has not completed verification testing.
- IP generation for Tandem with Field Updates is enabled for all devices that support Tandem Configuration, but place and route is gated, as the flow is still in a beta phase. Contact Xilinx Support to request access.
- For more information on Tandem Configuration, see the *UltraScale Architecture Gen3 Integrated Block for PCI Express Product Guide* (PG156) v4.1.

Vivado Physical Implementation and Power Tools

- The `report_design_analysis` command now has a GUI in the Vivado IDE that supports timing, complexity, and congestion analysis with cross-probing to other

design views such as the device view and schematics. The GUI can be launched either from the **Tools > Report** menu or by using the `-name` option.

- The `report_design_analysis` command can report a list of paths that are critical at both the current design stage and prior stage. This provides a way to check on which critical paths the tools focus at each stage. The `config_design_analysis` command enables this new feature.
- A new command `report_pipeline_analysis` evaluates potential design performance improvements by hypothetically adding latency (pipeline stages) to the design and reporting the new resulting Fmax. The analysis includes loop detection, per-clock analysis, and in-context module analysis.
- The `phys_opt_design` optimizations in a design run can be saved and executed earlier in the design flow to improve the overall design performance.
  - Each optimization such as a fanout optimization or BRAM register optimization is expressed using the new `iphys_opt_design` Tcl command.
  - Writing and reading optimizations are handled using new Tcl commands `write_iphys_opt_tcl` and `read_iphys_opt_tcl` respectively.
- There are new place and route directives for UltraScale designs that experience congestion, available by Tcl only.
  - `place_design` directives provide low, medium, and high degrees of logic spreading:
    - `AltSpreadLogic_low`
    - `AltSpreadLogic_medium`
    - `AltSpreadLogic_high`
  - `route_design` has a single directive: AlternateCLBRouting
- The `CLOCK_DELAY_GROUP` is a new net property that can be assigned to related clocks that have the same MMCM or PLL source to reduce clock skew on timing paths between the clocks.
- The `CLOCK_ROOT` net property has been replaced by the `USER_CLOCK_ROOT` property:
  - `USER_CLOCK_ROOT` is a writable and readable property for assigning a clock root to a clock region. Assigning `CLOCK_ROOT` will automatically assign `USER_CLOCK_ROOT` instead but also result in a warning that assigning `CLOCK_ROOT`.
  - `CLOCK_ROOT` is now a read-only net property that reflects the clock root of a clock net.
- When targeting UltraScale devices, some block RAM power optimization is enabled by default in `opt_design` with further optimization available in `power_opt_design`.
- UltraScale XPE now provides three selections for Power Optimization on the Summary sheet:

  - None: No power optimization.
  - Default: BRAM power estimation matches the default set of optimizations in `opt_design`.
  - Power Optimization: BRAM power estimation matches the full set of optimizations of opt_design followed by `power_opt_design`.
- The `report_synchronizer_mtbf` command now includes MTBF of FIFO primitives.

PS Power Reports

- Regarding overall PS power reported, there is a discrepancy (in static power only) of a few percent between the values from the Processor Configuration Wizard and the values reported by the power tools: XPE and Vivado Report Power.
- Use the power tools (XPE and Vivado Report Power) to calculate the most accurate power estimation of the PS. This issue will be addressed in the 2016.1 Vivado release.

Vivado IP Integrator - PCIe Designer Assistance

- Support for XDMA with KCU105 hardware.
- Requires XDMA license.

Vivado IP Integrator

- Easy access to IP Example designs from IP Integrator added to right-click menu.
- Enhanced configurable example design including option to configure MicroBlaze.

Vivado Simulator

- Up to 3 times elaboration runtime performance improvement.
- Enhanced waveform debug experience.
  - Improved simulator relaunch feature.
    - Retains GUI, breakpoint, signal settings, and markers.

Vivado Simulation Flow

- IP simulation made easy:
  - IP generation creates simulation scripts for all simulators.
  - Clear separation of files reused by IP (Static Files).Vivado Debug
- Enumerated type support for ILA probe values.
- Data or trigger (or both) support for ILA probe type.

- Instance names preservation.
- Robustness of HW connections.
- Enhanced margin analysis support for DDR4/DDR3.

Vivado Programmer

- Ability to generate SVF (Serial Vector Format) files.
- Capability to verify checksum of configuration memory devices.
- Improved robustness of HW connections.

Vivado System Edition Tools

Vivado System Generator for DSP

- Support for MATLAB 2015B includes tighter integration allowing HDL Coder to automate the generation of a combined model containing high level RTL and target optimized IP.
- Simplified IPs enable up-conversion, down-conversion, and standard digital signal processing designs to deliver high quality of results and performance while minimizing the interfaces and number of parameters required to configure the IP. New IPs include Digital FIR Filter, Sine Wave generator, Product, and Requantize block.
- JTAG co-simulation support for Virtex-7, Kintex-7, Artix-7, and Zynq-7000 families are enhanced and can utilize burst mode to improve performance by 45x.
- Improved launch times and better cross-probing support for the Waveform Viewer and Timing Analyzer aid in the debugging of logic and visualizing timing critical paths.

Vivado HLS

- Vivado HLS can launch the Vivado waveform viewer, after running a C/RTL co-simulation it is now possible to visualize the simulation waveforms by clicking on an **Open Wave Viewer** toolbar button.
- Support for half-precision floating point through a new `hls_half.h` header file. This allows for smaller and faster designs while in many cases retaining sufficient numerical precision.
- The `DATAFLOW` pragma can be enabled for elements processed in a loop for shorter latency and/or better throughput.
- Automatic burst inference for AXI4 master (`m_axi`) type argument accessed in loops.
- New `-register` option for AXI-Stream (axis) through `config_interface`.
- AXI-Lite (s_axilite) interfaces can now be implemented with a dedicated separate clock.

- New resource core option `Mul_LUT` to force a multiplier to be exclusively mapped onto the fabric rather than using a DSP block.
- See the *Vivado Design Suite User Guide: High-Level Synthesis* (UG902) [Ref 3] for more details.

Important Information

Updates to Existing IP

The following table lists current updates to existing IP for the 2015.3 release.

Table 6-2: **Existing IP Updates**

Existing IP	Existing IP Updates
Integrated 100G Ethernet for UltraScale(CMAC)	• Added optional fee based soft 100G RS-FEC.
10G Ethernet Subsystem	• Supports Virtex® UltraScale • Supports 10G/25G Ethernet MAC, 10G/25G BASE-R/KR, or 10G/25G BASE-R/KR standalone • 10GBASE-R and 25GBASE-R available at no charge • Separate fee based licenses required for EMAC and KR variants
AXI 10G Ethernet MAC	• Added Artix-7 support for 2.5G EMAC
10G Ethernet PCS/PMA	• 64-bit IP latency and size reduction.
XAUI	• Added UltraScale GTY support.
RXAUI	• Added UltraScale GTY support.
10G BASE-R	• New optional 32-bit low latency and size reduced IP • Added Zynq-7000 AP Soc and 7 series defense grade devices
100G IEEE 802.3bj Reed-Solomon Forward Error Correction IP	• Supports Virtex UltraScale. • Connects to integrated 100G Ethernet MAC or soft 100G Ethernet MAC. • Enables optical solutions such as SR4, CWDM4, PSM4 or ER4f.
AXI 1G/2.5G Ethernet Subsystem	• Added 2.5G support for Kintex-7, Virtex-7, Zynq and UltraScale families • Supports 2500BASE-X or 2.5G SGMII single rate • Tri-Mode Ethernet Media Access Controller (TEMAC) • Added 2.5G support for Kintex-7, Virtex-7, Zynq and UltraScale devices • 1G/2.5G Ethernet PCS/PMA or SGMII • Added 2500BASE-X support for Kintex-7, Virtex-7, Zynq, and UltraScale families • Added 2.5G SGMII single rate support for Kintex-7, Virtex-7, Zynq, and UltraScale families

Table 6-2: **Existing IP Updates**

Existing IP	Existing IP Updates
PCI Express®	• AXI-MM support for Gen3 PCI Express hard block (Virtex7 XT/HT). • Package Migration section in User Guide for UltraScale FPGA devices. • Tandem PCIe/PROM support (Beta) for UltraScale FPGA devices. • Upgraded GT Wizard • GUI options update to select PLL and Core Clocks • Additional devices/packages supported for Tandem PCIe®
Aurora	• Additional UltraScale FPGA device support. • Simulation support with Labtools enabled. • AXI4-Lite to DRP interface compliance (Aurora 64B/66B). • Extending line rate to 16.375G support • Grouping of flow control interface and making AXI4-ST compliant • Enable lane location selection though GUI
IBERT for UltraScale	• An issue that may cause the under-reporting of errors has been fixed in all UltraScale IBERT cores. • It is necessary for users who are performing very long tests or deep scans to re-generate the IP. • Upgrade is highly recommended for all other cases (see details in Answer Record 63768).

Device Support

The following devices have been removed from this release of Vivado to align with the silicon availability plan:

- Virtex UltraScale: The VU095 ES1 parts are not supported in this release and beyond.

VIPP

- New core for Video Test pattern generator (Version 7).
  - Resolutions up to 4K60.
  - Version 6 replacement.
- Pre production release of Video processing subsystem.
  - New IP subsystem to do video format conversion. It will replace VIPP cores eventually.
  - Capable handling standard definition video to 4k60 video processing.
  - Functions include deinterlacing, scaling, color space conversion, and correction, chroma re sampling and frame rate conversion.
- Video in and Video out bridges.
  - Improved timing to support 4K60 in 2 –pixel wide mode.

DisplayPort LogiCore V6.1

- Addition of DP159 control to Displayport.

Physical Implementation and Power Tools - Known Issues

- When using `report_design_analysis` at the Tcl console or in the IDE to analyze congestion, router congestion data is lost when saving and reopening a design, or when saving and opening a checkpoint. The result is that router congestion is missing from the report. To work around this issue, you must run `report_design_analysis` in the same session as `route_design` so that the router congestion data is stored in memory. This will be addressed in a future release.
- The `report_pipeline_analysis` may recommend adding pipeline stages within Xilinx IP boundaries, which are not typically accessible. To workaround this issue, use the `top_level_cell` or clocks options to limit the scope of pipeline analysis. This will be addressed in a future release.

Vivado Design Suite Documentation Update

In the 2015.3 Vivado Design Suite Documentation release not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2015.3 documentation suite.

Licensing

Activation licensing is not supported for USB dongles, on floating servers running SOLARIS OS, or on triple-redundant server configurations.

IP Known Issues and Change List

For Xilinx IP known issues, see the *IP Release Notes Guide* (XTP025) [Ref 8].

32-bit OS Support Removal

Beginning with Vivado 2015.1, 32-bit Operating System and application support has been removed for all design entry and implementation flows. The 32-bit support on Windows 7 and Red Hat Enterprise Linux 6 will remain for Vivado 2015.1 Lab Edition. Lab Edition is a free suite of tools for programming and debug.

Known Issues

Vivado® Design Suite Tools Known Issues can be found at Answer Record 63538.

Vivado 2015.2

What's New

Vivado® Design Suite 2015.2 features support for the following devices:

- Virtex® 7 XQ7VX690T High-Reliability
- Zynq® 7000 XQ7Z045 and XQ7Z100 High-Reliability
- Kintex® UltraScale KU060 Production Support

There have also been improvements in Partial Reconfiguration, Tandem Configuration, and the Vivado implementation tools.

Device Support

The following new devices are enabled for this release.

Table 6-3: **Vivado 2015.2 Device Support**

Production Level	Vivado 2015.2 Device Support
New Devices	The following UltraScale devices are introduced in this release: • Virtex® UltraScale devices: ◦ XCVU160 The following New 7 series devices are introduced in this release: • XQ7VX690T RF1158 • XQ7Z045 RFG676
General Access	The following devices are production ready: • Kintex® UltraScale devices: ◦ XCKU035, XCKU060, XCKU115 • Virtex UltraScale devices: ◦ XCVU065
Bitstream Generation	• Bitstream generation for UltraScale devices are limited to: • Virtex UltraScale: ◦ XCVU095 ES1 ◦ XCVU065 ◦ XCVU125 ◦ XCVU160 ◦ XCVU190 ◦ XCVU440 • Kintex UltraScale: ◦ XCKU040 ◦ XCKU060 ES2 ◦ XCKU115 ES2

Installation

Beginning with the Vivado 2015.1 release, the install program on Linux no longer requires root or sudo privileges. In the past, these privileges were required to enable cable driver installation. Now, cable drivers must be installed manually by running a separate script while in a root/sudo command shell. For more information on Linux cable driver installation, see the Installing Cable Drivers section of this document.

Vivado Design Edition Tools

Partial Reconfiguration

- Expanded support for UltraScale devices.
  - Support for the KU035 and VU160 have been added, bringing the total number of UltraScale devices supported up to 8.
- Partial bit file generation enabled for KU035 and KU040 production silicon.
  - In general, bitstream generation is disabled until ES2 silicon (Virtex UltraScale except the VU440) or production silicon (Kintex UltraScale plus the VU440) is available and verified.
- For more information, see this link in the *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909) [Ref 5].

Tandem Configuration

- Expanded support for UltraScale devices.
  - Support for the KU035, VU160, and VU440 have been added, bringing the total number of UltraScale devices supported up to 9.
- Partial bit file generation enabled for KU035 and KU040 production silicon.
  - In general, bitstream generation is disabled until ES2 silicon (Virtex UltraScale except the VU440) or production silicon (Kintex UltraScale plus the VU440) is available and verified.
- Encryption support is fully enabled for Tandem PROM and Tandem PCIe for both 7 series and UltraScale architectures.
- For more information, see the *UltraScale Architecture Gen3 Integrated Block for PCI Express Product Guide* (PG156) v3.1.
- Report CDC: Vivado Integrated Design Environment (IDE) support has been added in this release. Report CDC now identifies 16 CDC topologies with support for 4 new topologies added in this release. The GUI report has summary by clock pair and summary by rule type and allows cross probing to schematic and RTL.

Vivado System Edition Tools

Vivado System Generator for DSP

- Advanced Hardware Co-Simulation Burst Mode support accelerates simulation to increase performance by 100x.
- Improved timing analysis allows cross probing to quickly identify failing paths.
- New capability parses an SoC platform design from Vivado IP Integrator to tailor a complementary set of gateways for easy and accurate IP development.
- Enhanced support for multiple AXI4-Lite interfaces enables independent register alignment to clock domains.
- Support for MATLAB 2015A.

Important Information

Device Support

The following devices have been removed from this release of Vivado to align with the silicon availability plan:

- Kintex UltraScale: KU075 and KU100
- Virtex UltraScale: The -1LV variants will not be offered for this family and Vivado has been updated to remove the parts that are no longer supported.

Vivado Design Suite Documentation Update

In the 2015.2 Vivado Design Suite Documentation release not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2015.2 documentation suite.

Licensing

Activation licensing is not supported for USB dongles, on floating servers running SOLARIS OS, or on triple-redundant server configurations.

IP Known Issues and Change List

For Xilinx IP known issues, see the *IP Release Notes Guide* (XTP025) [Ref 9].

32-bit OS Support Removal

Beginning with Vivado 2015.1, 32-bit Operating System and application support has been removed for all design entry and implementation flows. The 32-bit support on Windows 7 and Red Hat Enterprise Linux 6 will remain for Vivado 2015.1 Lab Edition. Lab Edition is a free suite of tools for programming and debug.

Known Issues

Vivado® Design Suite Tools Known Issues can be found at Answer Record 63538.

Vivado 2015.1

What's New

Vivado® Design Suite 2015.1 features acceleration of system verification and major productivity advances for the development and deployment of All Programmable FPGAs and SoCs. This release introduces the Vivado Lab Edition, accelerated Vivado Simulator and third party simulation flows, interactive clock domain crossing (CDC) analysis, and advanced system performance analysis with the Xilinx® Software Development Kit (SDK). Several new devices have also been introduced in Vivado 2015.1 including the XCVU440 FPGA.

Device Support

The following new devices are enabled for this release.

Table 6-4: **Vivado 2015.1 Device Support**

Production Level	Vivado 2015.1 Device Support
New Devices	The following UltraScale devices are introduced in this release: • Virtex® UltraScale devices: ◦ XCVU125, XCVU190, XCVU440 The following New 7 series packages are introduced in this release to support the EU RoHS (Restriction of Hazardous Substances) directive: • FBV, FFV, SBV
General Access	The following devices are production ready: • Kintex® UltraScale devices: ◦ XCKU035, XCKU060, XCKU115 • Virtex UltraScale devices: ◦ XCVU065

Table 6-4: **Vivado 2015.1 Device Support**

Production Level	Vivado 2015.1 Device Support
Early Access	• Virtex UltraScale devices: ◦ XCVU160 • Contact Xilinx Field Application Engineer for access to these devices.
Bitstream Generation	• Bitstream generation for UltraScale devices are limited to: • Virtex UltraScale: ◦ XCVU095 ES1 • Kintex UltraScale: ◦ XCKU040, XCKU060 ES2, XCKU115 ES2

Installation

Beginning with the Vivado 2015.1 release, the install program on Linux no longer requires root or sudo privileges. In the past, these privileges were required to enable cable driver installation. Now, cable drivers must be installed manually by running a separate script while in a root/sudo command shell. For more information on Linux cable driver installation, see the Installing Cable Drivers section of this document.

Licensing

Borrowing Vivado Licenses

- After you renew your Vivado subscription license after Vivado 2015.1, you will be able to generate borrowable floating licenses. This is for Activation licenses only.
- The license administrator can determine how many, if any, license seats will be borrowable when the licenses are generated.
- Next a network license client can borrow 1 floating seat and lock it to their machine for non-network use for a period of time.
- When the borrow time expires, the license is automatically re-enabled on the floating license server. For more details on borrow, see the Chapter 5, Obtaining and Managing a License.

Software Development Kit (SDK)

Advanced In-system Performance Analysis and Validation

To accelerate the development of the Zynq®-7000 All Programmable SoC, Xilinx has extended its system performance and analysis toolbox for bare metal and Linux applications. The Xilinx SDK now provides embedded software developers the ability to analyze the performance and the bandwidth of their SoC design, including key performance metrics for the processor subsystem (PS) as well as bandwidth analysis between the PS, the Programmable Logic (PL) and external memories. System modeling designs using AXI traffic

generators are provided for the Zynq® All Programmable SoC ZC702 and ZC706 evaluation boards.

Vivado Design Edition Tools

Partial Reconfiguration

- The Partial Reconfiguration Controller IP is now available for any user of Partial Reconfiguration (PR) in 7 series, Zynq® or UltraScale devices.
  - This IP is the heart of a PR system, fetching from memory and delivering to the configuration port partial bitstreams when hardware or software trigger events occur.
  - The IP supports AXI-Stream and AXI-Lite interfaces and is dynamically customizeable.
  - For more information on the PR Controller IP, see (PG193).
- Expanded support for UltraScale devices
  - Supports implementation only for KU115, VU125, and VU190 devices, also the previously supported KU040, KU060, and VU095 devices.
  - Bitstream generation disabled until ES2 silicon (Virtex UltraScale except the VU440) or production silicon (Kintex UltraScale plus the VU440) is available and verified.
- For more information, see this link in the *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909) [Ref 4].

Tandem Configuration

- Tandem PROM and Tandem PCIe® is available for the same UltraScale devices as supported for Partial Reconfiguration: KU115, VU125, and VU190.
- Just as for Partial Reconfiguration, bitstream generation disabled until ES2 silicon (Virtex UltraScale except the VU440) or production silicon (Kintex UltraScale plus the VU440) is available and verified.
- For more information, see the *UltraScale Architecture Gen3 Integrated Block for PCI Express Product Guide* (PG156) v3.1.

RTL Synthesis

- New multicore support for Windows (Linux already supports multicore).
- Improved hierarchical cell pins naming for default synthesis settings (for flatten_hierarchy set to **rebuilt**).
- General inference improvements for integrated DSP block with in particular inference for the squarer mode (specific to UltraScale DSP block).

- New finite state machine (FSM) reporting included into the synthesis log file.

Simulation Flow

- Integration of Aldec Active-HDL and Riviera-PRO.
- Separate Modelsim and QuestaSim integration to support Modelsim PE and DE users.
- Enhanced algorithm of simulation scripts to speedup compile time by 2.5 times.

Simulation Performance

- New UltraScale Memory (memory IP) BFM model, delivering up to 4 times the simulation speed.
- Accelerated UltraScale PCIe® simulation performance.
- Updated MMCM and PLL models for faster simulation.

Vivado Simulator

- UltraScale Memory simulation support.
- Debug EOU features:
  - Debug operations enabled in text editor and waveform.
    - Report driver
    - Force dialogue
  - Cross probe between text editor and waveform.
  - Locate signals in wave, object and source code through context menu.
- Other Vivado simulator performance improvements:
  - 25% faster PCIe simulation.
  - 10X average reduction in disk foot-print.

Vivado Physical Implementation and Power Tools

- Improved support of Laguna flip-flops in the UltraScale 3D IC interconnect resources.
  - Automatic opportunistic use: register placed in Laguna site if it improves timing.
  - Soft mapping to Laguna site ranges using Pblocks.
  - Manual mapping to specific Laguna sites using LOC assignments and drag-and-drop in the IDE.
- Improved design performance using post-route Physical Optimization (post-route `phys_opt_design`). All directive values are now enabled for all supported devices.

- For UltraScale devices, registers without reset (set/reset/preset/clear) can be packed in the same CLB where resets are used. The reset is ignored by the non-reset registers.
- Report Design Analysis: The `report_design_analysis` command has a new option -congestion to report congestion metrics of the top-level design. The most information is available when `report_design_analysis` is run in the same session after `place_design` and `route_design`.
- When using the IDE to report power, the switching activity settings persist between reporting runs.
- Report CDC: Vivado Integrated Design Environment (IDE) support has been added in this release. Report CDC now identifies 16 CDC topologies with support for 4 new topologies added in this release. The GUI report has summary by clock pair and summary by rule type and allows cross probing to schematic and RTL.

Vivado IP Integrator

- Bottom up synthesis flow option for faster design iterations. Each IP is synthesized by itself and only changed IP need to be synthesized again.
- A new layout optimized for IP integrator is available.
- Up to 50% reduction in project flow time including design generation and validation.
- Revision control ease of use improvements:
  - write_bd_tcl support for remote sources per the recommended methodology.
  - With the same version of Vivado, design regeneration is possible from only the .bd file (the block locations / comments are not stored in the .bd file).
- Support for saving a design in the validated state so validation does not need to be rerun during generation.
- The search in the "Add IP..." window has been enhanced and there is now quick access to IP details.

Vivado IP Packager

- Packaging a Block Design is now supported.
- Packaged IP can now be added to custom categories in the IP Catalog.
- Additional dependency options are available for IP customization GUIs.

Vivado IP Flows

Option to enable IP synthesis caching to eliminate synthesis time when iterating on a design.

Vivado IP Catalog

The Northwest Logic DMA Back-End IP is now listed in the Vivado IP Catalog under **Alliance Partners**.

Vivado Debug

- **Vivado Lab Edition** is now available supporting all 7-series, Zynq, and UltraScale devices. This is a new, compact, and standalone product targeted for use in the lab environments:
  - Small download (1GB) and footprint size.
  - No license required.
  - Support for 64- and 32-bit OS platforms.
  - Provides all features for programming and logic/serial IO debug
- MARK_DEBUG Improvements:
  - Better name retaining in HDL flow:
- Ease of Use for Hardware Manger Window Management:
  - Fully customized dashboard layout.
    - A configurable docking manager to update dashboards.
    - Desired user setup to view multiple VIO, or VIO and ILA cores.
  - Layout and content persistent in project.

Power Analysis

Report Power in the IDE and `report_power` (Tcl) now support all UltraScale devices including UltraScale SSI devices.

Vivado System Edition Tools

Vivado HLS

- New synthesizable C++ library functions with a special focus on software defined radio applications: numerically controlled oscillator (nco), QAM modulator, and demodulator. See the *Vivado Design Suite User Guide: High-Level Synthesis* (UG902) [Ref 3] for more details.
- Support for the LogiCore DDS (Direct Digital Synthesizer) IP.
- OpenCL kernel compilation.
- 64-bit addressing for AXI Master.

- General QoR improvements.

Vivado System Generator for DSP

- Advanced Hardware Co-Simulation Burst Mode support accelerates simulation to increase performance by 100x.
- Improved timing analysis allows cross probing to quickly identify failing paths.
- New capability parses an SoC platform design from Vivado IP Integrator to tailor a complementary set of gateways for easy and accurate IP development.
- Enhanced support for multiple AXI4-Lite interfaces enables independent register alignment to clock domains.
- Support for MATLAB 2015A.

Important Information

Updates to Existing IP

The following table lists current updates to existing IP for the 2015.1 release.

Table 6-5: **Existing IP Updates**

Existing IP	Existing IP Updates
Integrated 100G Ethernet for UltraScale(CMAC)	• Added simplex Tx and Rx support.
10G Ethernet Subsystem	• Added low latency 32-bit Ethernet MAC/PCS support. • Added 1588 hardware timestamping for UltraScale devices. • Added stacked VLAN support. • 64-bit IP latency reduction.
AXI 10G Ethernet MAC	• 10G Ethernet MAC and 10GBASE-KR or 10GBASE-R • Available in IP Integrator and IP Catalog • Added UltraScale Kintex® device support • Added Zynq-7000 AP Soc and 7 series defense grade devices
10G Ethernet PCS/PMA	• 64-bit IP latency and size reduction.
XAUI	• Added UltraScale GTY support.
RXAUI	• Added UltraScale GTY support.
10G BASE-R	• New optional 32-bit low latency and size reduced IP • Added Zynq-7000 AP Soc and 7 series defense grade devices
100G IEEE 802.3bj Reed-Solomon Forward Error Correction IP	• Supports Virtex UltraScale. • Connects to integrated 100G Ethernet MAC or soft 100G Ethernet MAC. • Enables optical solutions such as SR4, CWDM4, PSM4 or ER4f.

Table 6-5: **Existing IP Updates**

Existing IP	Existing IP Updates
AXI 1G/2.5G Ethernet Subsystem	• Added 2.5G support for Kintex-7, Virtex-7, Zynq and UltraScale families • Supports 2500BASE-X or 2.5G SGMII single rate • Tri-Mode Ethernet Media Access Controller (TEMAC) • Added 2.5G support for Kintex-7, Virtex-7, Zynq and UltraScale devices • 1G/2.5G Ethernet PCS/PMA or SGMII • Added 2500BASE-X support for Kintex-7, Virtex-7, Zynq, and UltraScale families • Added 2.5G SGMII single rate support for Kintex-7, Virtex-7, Zynq, and UltraScale families
PCI Express®	• AXI-MM support for Gen3 PCI Express hard block (Virtex7 XT/HT). • Package Migration section in User Guide for UltraScale FPGA devices. • Tandem PCIe/PROM support (Beta) for UltraScale FPGA devices. • Upgraded GT Wizard • GUI options update to select PLL and Core Clocks • Additional devices/packages supported for Tandem PCIe®
Aurora	• Additional UltraScale FPGA device support. • Simulation support with Labtools enabled. • AXI4-Lite to DRP interface compliance (Aurora 64B/66B). • Extending line rate to 16.375G support • Grouping of flow control interface and making AXI4-ST compliant • Enable lane location selection though GUI
IBERT for UltraScale	• An issue that may cause the under-reporting of errors has been fixed in all UltraScale IBERT cores. • It is necessary for users who are performing very long tests or deep scans to re-generate the IP. • Upgrade is highly recommended for all other cases (see details in Answer Record 63768).

Note: Part names aligned to silicon availability: XCKU040 ES1 is no longer supported and Multiple ES1 parts changed to ES2.

Documentation Navigator

- Integrated **Web Search Results** tab that searches for documents on Xilinx Support.
- Support for Design Hubs in the main Catalog View.
  - Guided learning curve with recommended key concepts and FAQs.
- New **Send Feedback** link added to each Design Hub.

Vivado Design Suite Documentation Update

In the 2015.1 Vivado Design Suite Documentation release not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2015.1 documentation suite.

Licensing

Activation licensing is not supported for USB dongles, on floating servers running SOLARIS OS, or on triple-redundant server configurations.

IP Known Issues and Change List

For Xilinx IP known issues, see the *IP Release Notes Guide* (XTP025) [Ref 8].

32-bit OS Support Removal

Beginning with Vivado 2015.1, 32-bit Operating System and application support has been removed for all design entry and implementation flows. The 32-bit support on Windows 7 and Red Hat Enterprise Linux 6 will remain for Vivado 2015.1 Lab Edition. Lab Edition is a free suite of tools for programming and debug

Known Issues

Vivado® Design Suite Tools Known Issues can be found at Answer Record 63538.

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Xilinx Documentation Navigator

You can view Xilinx tool and hardware documentation in the Xilinx Documentation Navigator or on the Xilinx website. The Documentation Navigator is integrated with the Vivado® Design Suite and it provides a catalog of Xilinx documentation and videos.

For more information about the Documentation Navigator, see the *Vivado Design Suite User Guide: Getting Started* (UG910).

Licenses and End User License Agreements

The third-party licenses govern the use of certain third-party technology included in and/or distributed in connection with the Xilinx design tools. Each license applies only to the applicable technology expressly governed by such license and not to any other technology. You must accept the terms of the End User License Agreements (EULAs) for Xilinx design tools and third-party products before license files can be generated.

To view the third-party license details and EULA, see End User License Agreement.

To view the Xilinx design tools license details and EULA, see http://www.xilinx.com/cgi-bin/docs/rdoc?v=2015.4;d=end-user-license-agreement.pdf.

References

1. *UltraFast™ High-Level Productivity Design Methodology Guide* (UG1197)
2. *UltraFast Embedded Design Methodology Guide* (UG1046)
3. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
4. *Vivado® Design Suite User Guide: High-Level Synthesis* (UG902)
5. *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909)
6. *Vivado Design Suite Tutorial: Partial Reconfiguration* (UG947)
7. *Vivado Design Suite User Guide: Hierarchical Design* (UG905)
8. *Vivado Design Suite Tutorial: Hierarchical Design* (UG946)
9. *IP Release Notes Guide* (XTP025)
10. *USB Cable Installation Guide* (UG344)
11. *Platform Cable USB II Data Sheet* (DS593)
12. *Parallel Cable IV Data Sheet* (DS097)
13. Xilinx Download Center (http://www.xilinx.com/support/download/index.htm)
14. Xilinx Design Tools WebTalk page (http://www.xilinx.com/webtalk/index.htm)
15. *Vivado Design Suite Video Tutorials* (www.xilinx.com/training/vivado/index.htm)
16. *Vivado Design Suite Documentation* (www.xilinx.com/support/documentation/dt_vivado2015-4.htm)

Training Resources

Xilinx provides a variety of training courses and QuickTake videos to help you learn more about the concepts presented in this document. Use these links to explore related training resources:

1. Vivado Design Suite Hands-on Introductory Workshop
2. Vivado Design Suite Tool Flow
3. Essentials of FPGA Design

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