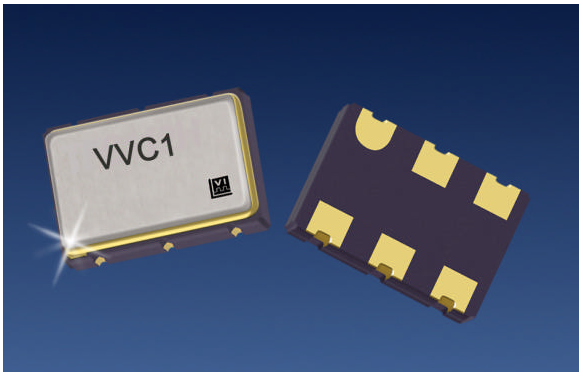
VVC1/VVC2

Voltage Controlled Crystal Oscillator



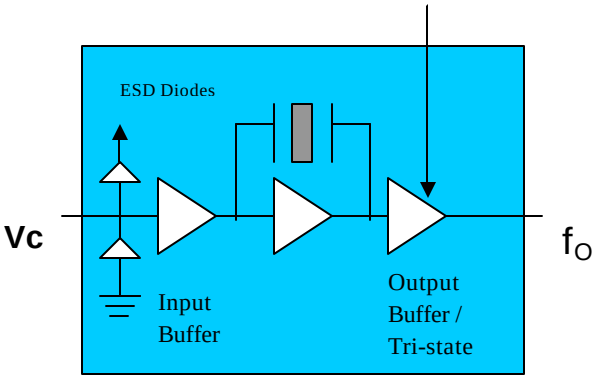
The VVC1 Voltage Controlled Crystal Oscillator

Features

- VCXO with a CMOS output
- Small 5.0 X 7.0 X 1.8 mm package
- Output frequencies to 66 MHz
- 5.0 or 3.3 V operation
- Low Jitter < 6 pS rms, f_o>12MHz
- Tri-State Output for test and board debug
- 0/70 or –40/85 °C operating temperature
- Hermetically sealed ceramic SMD package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- SONET/SDH/DWDM
- Ethernet, Gigabit Ethernet
- xDSL/PCMCIA cards
- Digital Video
- Broadband Access



Description

Vectron's VVC1 Voltage Controlled Crystal Oscillator (VCXO) is a quartz stabilized square wave generator with a CMOS output and is tested at CMOS and TTL (5.0 volt operation) logic levels.

The VVC1 uses fundamental crystals resulting in low jitter performance and a monolithic IC which improves reliability and reduces cost.

Performance Characteristics

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	f_O	1.544		65.536	MHz
Supply Voltage [1] (+5.0 V) (+3.3 V)	V_{DD}	4.750 3.135	5.0 3.3	5.250 3.465	V
Supply Current (+5.0 V) (+3.3 V)	I_{DD}			55 40	mA
Output Logic Levels Output Logic High[2] Output Logic Low[2]	 V_{OH} V_{OL}	 0.9*V_{DD}		 0.1V_{DD}	 V V
Transition Times Rise Time[2] Fall Time[2]	 t_R t_F			 5 5	 ns ns
Symmetry or Duty Cycle[3]	SYM	45	50	55	%
Operating temperature (*ordering option*)		0/70 or –40/85			°C
Total Pull Range (*ordering option)* *Or* Absolute Pull Range		±50, ±100 or ±150 ±50, ±80 or ±100			ppm
Test Conditions for APR (+5V option)	V_C	0.5		4.5	V
Test Conditions for APR (+3.3V option)	V_C	0.3		3.0	V
Gain Transfer (See Figure 3)		Positive			ppm/V
Control Voltage Leakage Current	I_{VCXO}			±1	uA
Control Voltage Bandwidth (-3dB)	BW	10			kHz
Package Size		5.0 x 7.0 x 1.8			mm

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the equivalent five gate TTL load and operating conditions under which these parameters are tested and specified.
3. Symmetry is defined as (ON TIME/PERIOD with Vs= 1.4 V for TTL and Vs=2.5 V for CMOS, 5 volt operation, and Vs=1.65V for 3.3 Volt operation.

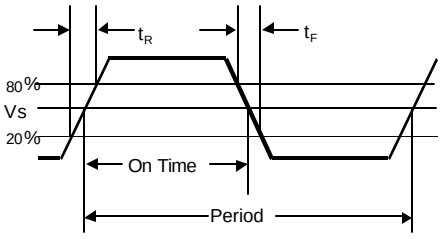


Figure 1. Output Waveform

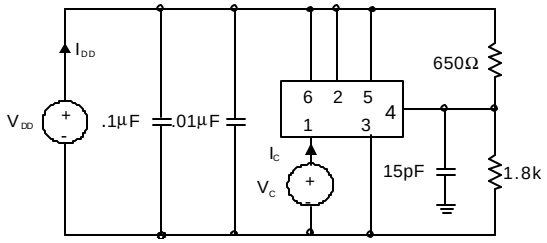
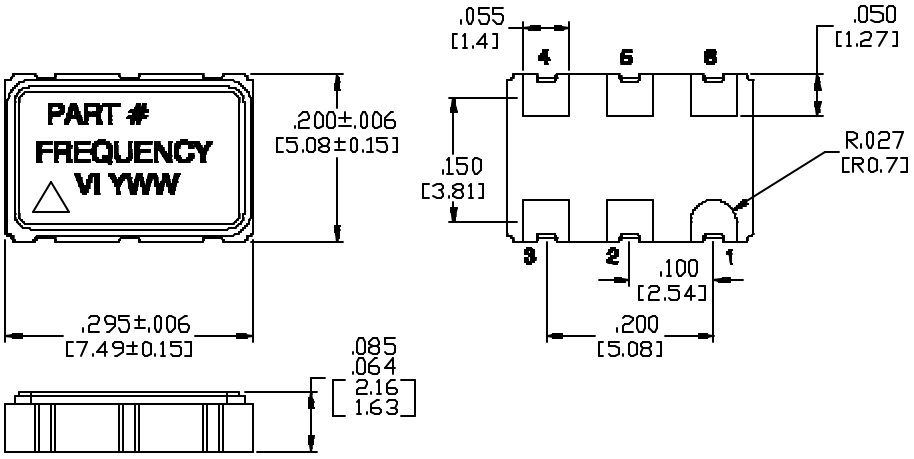


Figure 2. Typical Output Test Conditions (25±5°C)

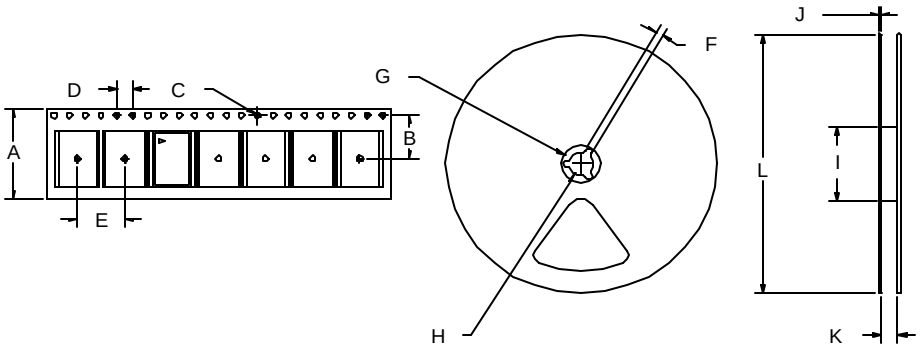
Outline Diagram, Pad Layout and Pin Out



Inch/[mm]

Pin #	Symbol	Function
1	V_C	Control Voltage
2	NC or Tri-state	No Connect or Tri-state
3	GND	Ground
4	f_O	Output Frequency
5	Tri-state or NC	Logic low disables output Logic high or no connection enables output waveform
6	V_{DD}	Supply Voltage

Tape and Reel



Tape and Reel Dimensions (mm)													
Tape Dimensions						Reel Dimensions							# Per
Product	A	B	C	D	E	F	G	H	I	J	K	L	Reel
VVC1	12	5.5	1.5	4	8	1.78	20.6	13	55	6	12.4	178	500

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	6	Vdc
Storage Temperature	Tstorage	-55/125	°C
Voltage Control Range	V_C	Gnd to V_{DD}	V

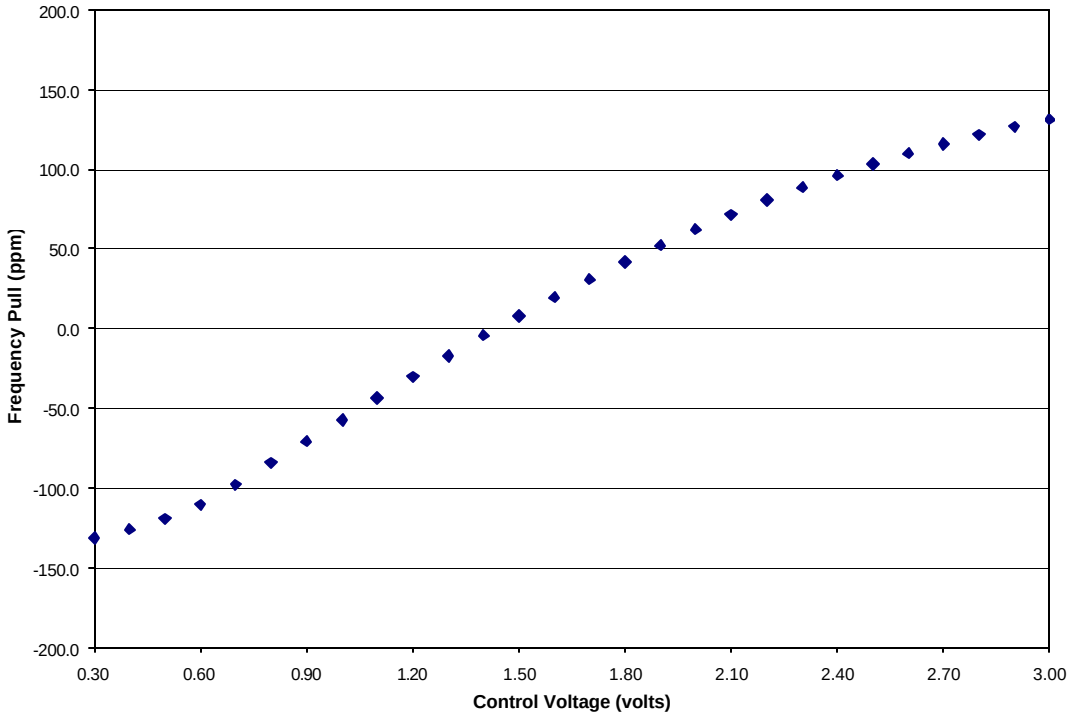


Figure 3. Typical Frequency Pull versus Control Voltage, 35.328MHz Output, 3.3 Volt Supply

Reliability

The VVC1 is capable of meeting the following qualification tests.

Table 3. Environnemental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Solderability	MIL-STD-883 Method 2003
Gross and Fine Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the the VVC1, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

Table 4. ESD Ratings

Model	Minimum	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Suggested IR profile

Devices are built using lead free epoxy and can also be subjected to standard lead free IR reflow conditions.

VVC1 Voltage Controlled Crystal Oscillator

Standard Frequencies (MHz)

1.544	2.048	4.096	8.192	10.000
12.000	12.288	12.352	13.000	14.318
15.440	16.000	16.384	18.432	19.440
20.000	20.480	24.576	24.704	27.000
30.000	32.000	32.768	34.368	35.328
38.880	40.000	40.960	44.736	51.840
52.000	62.208	65.536		

Other frequencies may be available upon request. Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

Ordering Information

VVC1-BGE – xxMxxx

Product Family

VC=VCXO

Package

5x7x2

TriState

1=Pin 5

2=Pin 2

Power Supply, Linearity

A: 5.0V , 20% Linearity

B: 3.3V, 20% Linearity

C: 5.0V, 10% Linearity

F: 3.3V, 10% Linearity

Frequency

example: 44M736= 44.736MHz

Temperature Range/Stability(for TPR)

B: 0/70 C, ±50 ppm

D: -40/85 C, ±50 ppm

E: 0/70 C, ±25 ppm

F: -40/85C, ±25 ppm

Absolute Pull Range

G: ±50 ppm APR

N: ±80 ppm APR

H: ±100 ppm APR

or Total Pull Range

1: ±50 ppm

2: ±100 ppm

3: ±150 ppm

NOTE: *Not all combinations of options are available. Higher frequencies have less pull capability, especially at +3.3 volts supply, and higher pull can result in 20% linearity instead of 10%. Consult factory or your local sales representative with application requirements.*

For Additional Information, Please Contact:

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