

Data Sheet

VT6212 / VT6212L

PCI USB 2.0 Controller

Revision 1.06
December 7, 2005

VIA TECHNOLOGIES, INC.

Copyright Notice:

Copyright © 2002-2005 VIA Technologies Incorporated. Printed in the United States. ALL RIGHTS RESERVED.
No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual or otherwise without the prior written permission of VIA Technologies Incorporated.

Trademark Notices:

 is a registered trademark of VIA Technologies, Incorporated.
VT6202, VT6212 and VT6212L may only be used to identify products of VIA Technologies, Incorporated.
Windows XP™, Windows 2000™, Windows ME™ and Windows 98SE™ are registered trademarks of Microsoft Corporation.
PCI™ is a registered trademark of the PCI Special Interest Group.
All trademarks are the properties of their respective owners.

Disclaimer Notice:

No license is granted, implied or otherwise, under any patent or patent rights of VIA Technologies. VIA Technologies makes no warranties, implied or otherwise, in regard to this document and to the products described in this document. The information provided by this document is believed to be accurate and reliable as of the publication date of this document. However, VIA Technologies assumes no responsibility for any errors in this document. Furthermore, VIA Technologies assumes no responsibility for the use or misuse of the information in this document and for any patent infringements that may arise from the use of this document. The information and product specifications within this document are subject to change at any time, without notice and without obligation to notify any person of such change.

Offices:

USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 -or- (510) 687-4654
Web: http://www.viatech.com

Taipei Office:
1st Floor, No. 531
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453
Web: http://www.via.com.tw

REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	6/5/03	Initial external release	EY
1.01	2/27/04	Updated cover page Updated copyright page Changed pins 104, 103, 57, 58, 59, 97 to NC Updated pin-out diagram Updated pin list Updated pin descriptions	JW
1.02	10/21/04	Added figure 4, lead-free mechanical specification diagram	JW
1.03	12/21/04	Specified PCI 2.2 bus support	JW
1.04	4/19/05	Registers updated f0rx41[4], f0rx42[1-0], f0rx48[5], f0rx4B[0], f2rx41[4], f2rx48[5], f2rx49[7-5], f2rx4A, f2rx4B[5, 3-0], f2rx51	JW
1.05	11/16/05	Modified legal page Changed pins 60, 63, 64 and 102 to NC Updated pin-out diagram Updated pin list Updated pin descriptions	SV
1.06	12/7/05	Updated pin information	SV

TABLE OF CONTENTS

REVISION HISTORY I
TABLE OF CONTENTS II
LIST OF FIGURES III
LIST OF TABLES IV
PRODUCT FEATURES 1
OVERVIEW 2
PINOUTS 3
PIN DIAGRAM 3
PIN LIST 4
PIN DESCRIPTIONS 5
REGISTERS 8
REGISTER OVERVIEW 8
REGISTER SUMMARY TABLES 8
Function 0-1 UHCI Universal Host Controller Interface 8
Function 0-1 UHCI PCI Configuration Header 8
Function 0-1 UHCI Device Specific Registers 8
Function 0-1 USB UHCI I/O Registers 8
Function 2 EHCI Enhanced Host Controller Interface 9
Function 2 EHCI PCI Configuration Header 9
Function 2 EHCI Device Specific Registers 9
Function 2 USB EHCI Memory-Mapped I/O Registers 10
EHCI Memory Mapped I/O Capability Registers 10
EHCI Memory Mapped I/O Operational Registers 10
REGISTER DESCRIPTIONS 11
Function 0-1 UHCI Universal Host Controller Interface 11
Function 0-1 Configuration Space Header 11
Function 0-1 Device Specific Registers 12
Function 2 EHCI Enhanced Host Controller Interface 14
Function 2 Configuration Space Header 14
Function 2 Device-Specific Registers 15
Function 2 EHCI Compliant USB Memory-Mapped I/O Registers 16
EHCI Capability Registers 16
EHCI Operational Registers 16
ELECTRICAL SPECIFICATIONS 17
PACKAGE MECHANICAL SPECIFICATIONS 19

LIST OF FIGURES

FIGURE 1. VT6212 / VT6212L CHIP BLOCK DIAGRAM 2
FIGURE 2. VT6212 (PQFP) / VT6212L (LQFP) PIN DIAGRAM (TOP VIEW) 3
FIGURE 3. MECHANICAL SPECIFICATIONS – 128 PIN PQFP (VT6212) / LQFP (VT6212L) PACKAGE 19
FIGURE 4. LEAD-FREE MECHANICAL SPECIFICATIONS – 128 PIN PQFP (VT6212) / LQFP (VT6212L) PACKAGE 20

LIST OF TABLES

TABLE 1. VT6212 / VT6212L PIN LIST (ALPHABETICAL ORDER) 4
TABLE 2. VT6212 / VT6212L PIN DESCRIPTIONS 5
TABLE 3. ABSOLUTE MAXIMUM RATINGS 17
TABLE 4. DC CHARACTERISTICS 17
TABLE 5. POWER SPECIFICATIONS 18

VT6212 / VT6212L

PCI USB 2.0
4-Port Host Controller

USB 2.0 UHCI / EHCI Host Controller for the PCI 2.2 Bus

PRODUCT FEATURES

- **USB 2.0**
  - Compliant with Universal Serial Bus Specification Revision 2.0
  - Compliant with Enhanced Host Controller Interface Specification Revision 1.0
  - Compliant with Universal Host Controller Interface Specification Revision 1.1
  - PCI multi-function device consists of two UHCI Host Controllers for full/low-speed signaling and one EHCI Host Controller core for high-speed signaling
  - 4 downstream facing ports in the root hub with integrated physical layer transceivers shared by UHCI and EHCI Host Controllers
  - Supports PCI-Bus Power Management Interface Specification release 1.1
  - Legacy support for all downstream facing ports
  - 4 DMA engines with pipelined control for USB data transfer bandwidth improvement
  - Dynamic clock stop control for power consumption reduction
- **Serial EEPROM Support for Boot Register Update**
- **Cardbus Mode Support**
- **2.5V Power Supply with 5V Tolerant Inputs**
- **0.22µm, Low Power CMOS Process**
- **128-Pin PQFP (VT6212) and 128-Pin LQFP (VT6212L) Packages Available**
- **Schematics and PCB Reference Designs Available**
- **System Clock Using 24 MHz Crystal**
- **Support for PCI Mobile Design Guide**

OVERVIEW

The VT6212 / VT6212L USB 2.0 UHCI and EHCI Host Controller for the PCI 2.2 Bus provides higher bandwidth (480 Mbps) and is backward compatible with USB 1.1. It implements Universal Serial Bus Specification Revision 2.0 and is compliant with UHCI 1.1 and EHCI 1.0 with a 32-bit PCI host bus interface. The VT6212 / VT6212L adopts 4 DMA engines with pipelined control for USB data transfer bandwidth improvement and dynamic clock stop control for power consumption reduction.

The VT6212 / VT6212L supports 4 downstream facing ports with 1.5 (low-speed), 12 (full-speed) and 480 (high-speed) Mbps transaction capability. The Root Hub is integrated with physical-layer transceivers shared by UHCI (for full/low-speed) and EHCI (for high-speed) Host Controllers. The VT6212 / VT6212L also supports PCI-Bus Power Management Interface Specification 1.1 and has legacy support for all downstream facing ports.

The VT6212 / VT6212L is ready to provide a PCI 4-port USB2.0 peripheral-interface to satisfy the needs of desktops, mobile systems, and other host platforms. Support for the VT6212 / VT6212L is built into Microsoft Windows XP and Windows 2000. Win98SE and WinME drivers are provided by VIA.

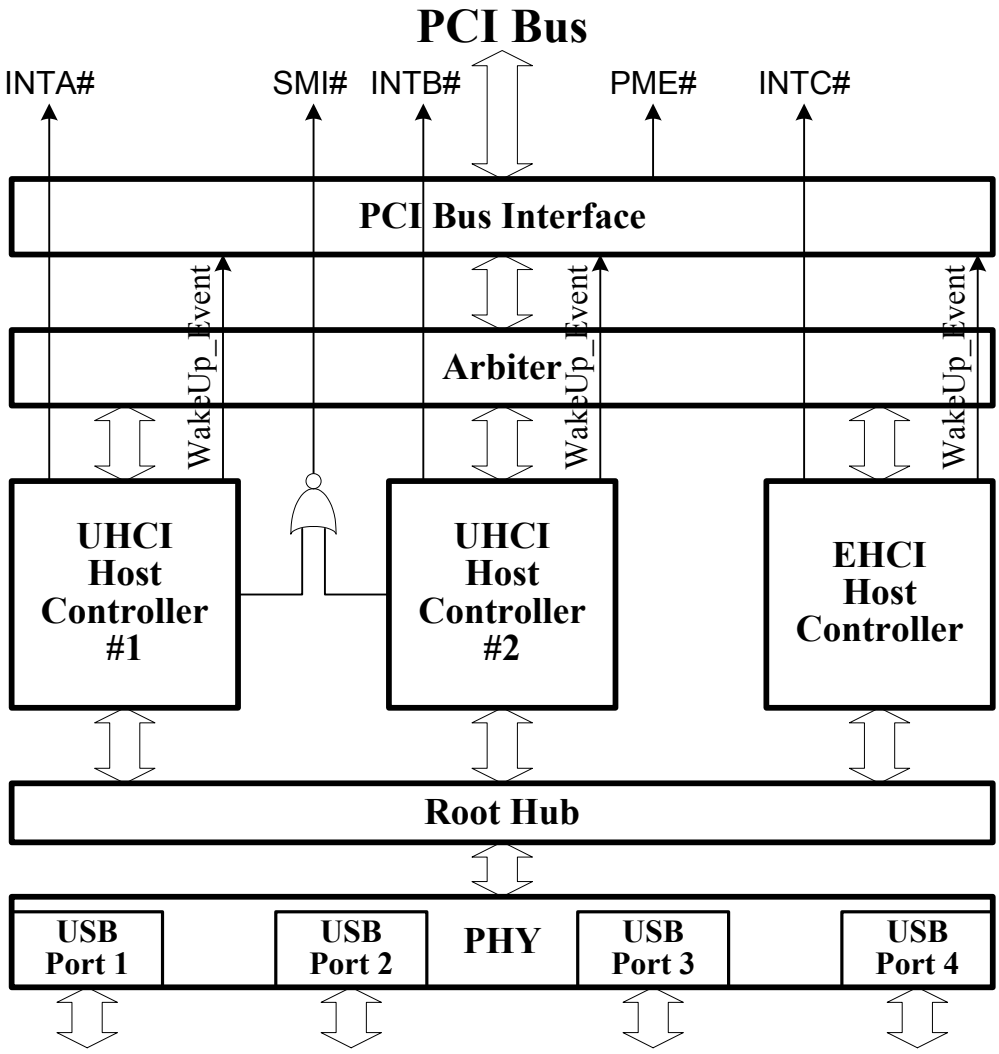


Figure 1. VT6212 / VT6212L Chip Block Diagram

PINOUTS

Pin Diagram

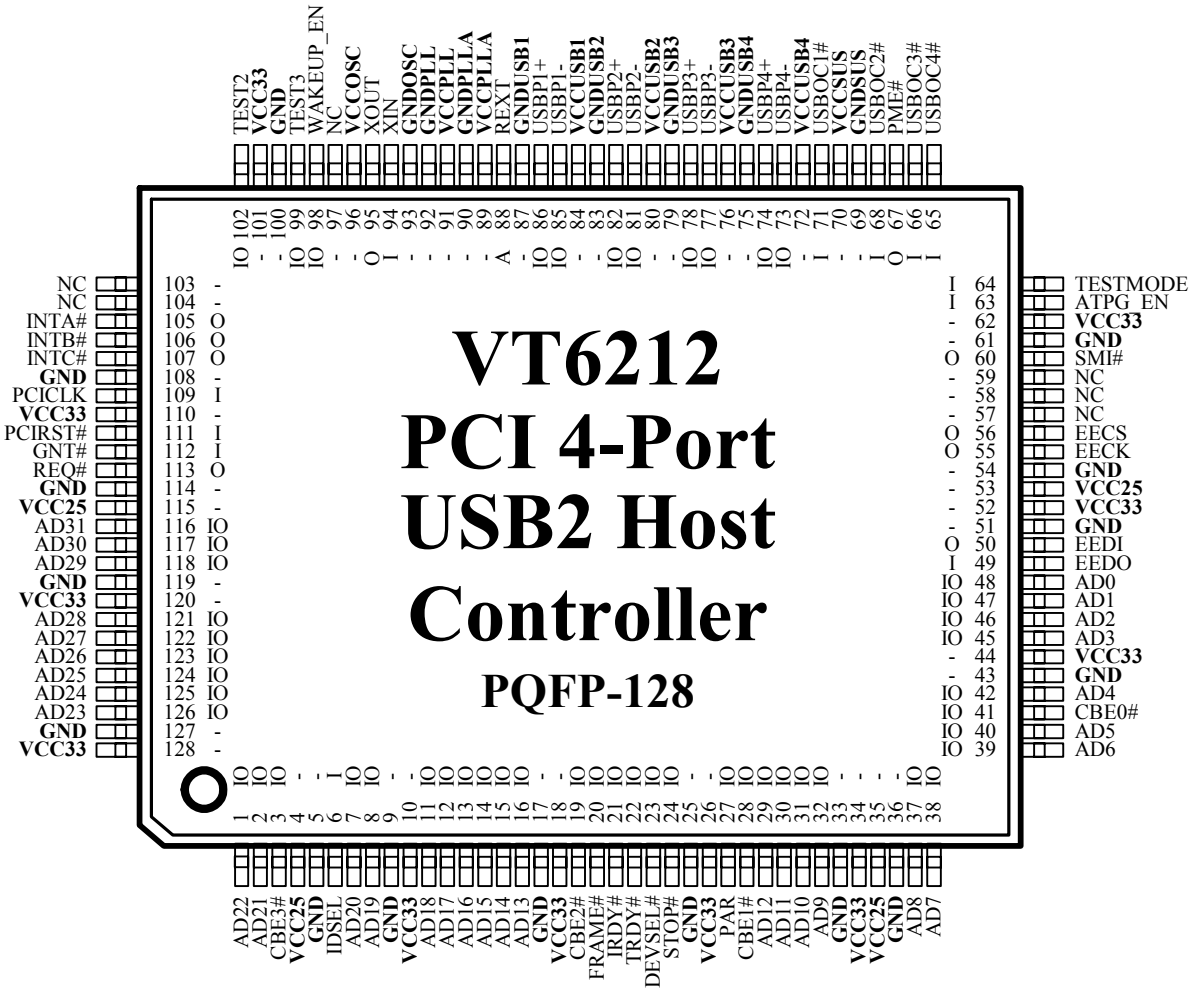


Figure 2. VT6212 (PQFP) / VT6212L (LQFP) Pin Diagram (Top View)

Pin List

Table 1. VT6212 / VT6212L Pin List (Alphabetical Order)

Pin	Typ	PU	Pin Name	Pin	Typ	PU	Pin Name	Pin	Typ	PU	Pin Name	Pin	Typ	PU	Pin Name
48	IO		AD0	63	I	PD	ATPG_EN	**93**	**P**		**GNDOSC**	86	IO		USBP1+
47	IO		AD1	41	IO		CBE0#	**92**	**P**		**GNDPLL**	81	IO		USBP2–
46	IO		AD2	28	IO		CBE1#	**90**	**P**		**GNDPLLA**	82	IO		USBP2+
45	IO		AD3	19	IO		CBE2#	**69**	**P**		**GNDSUS**	77	IO		USBP3–
42	IO		AD4	3	IO		CBE3#	**87**	**P**		**GNDUSB1**	78	IO		USBP3+
40	IO		AD5	23	IO		DEVSEL#	**83**	**P**		**GNDUSB2**	73	IO		USBP4–
39	IO		AD6	55	O	PD	EECK	**79**	**P**		**GNDUSB3**	74	IO		USBP4+
38	IO		AD7	56	O		EECS	**75**	**P**		**GNDUSB4**	**4**	**P**		**VCC25**
37	IO		AD8	50	O		EEDI	112	I		GNT#	**35**	**P**		**VCC25**
32	IO		AD9	49	I	PU	EEDO	6	I		IDSEL	**53**	**P**		**VCC25**
31	IO		AD10	104	-		NC	105	O		INTA#	**115**	**P**		**VCC25**
30	IO		AD11	103	-		NC	106	O		INTB#	**10**	**P**		**VCC33**
29	IO		AD12	58	-		NC	107	O		INTC#	**18**	**P**		**VCC33**
16	IO		AD13	97	-		NC	21	IO		IRDY#	**26**	**P**		**VCC33**
15	IO		AD14	57	-		NC	27	IO		PAR	**34**	**P**		**VCC33**
14	IO		AD15	59	-		NC	109	P		PCICLK	**44**	**P**		**VCC33**
13	IO		AD16	20	IO		FRAME#	111	I		PCIRST#	**52**	**P**		**VCC33**
12	IO		AD17	**5**	**P**		**GND**	67	O		PME#	**62**	**P**		**VCC33**
11	IO		AD18	**9**	**P**		**GND**	113	O		REQ#	**101**	**P**		**VCC33**
8	IO		AD19	**17**	**P**		**GND**	88	A		REXT	**110**	**P**		**VCC33**
7	IO		AD20	**25**	**P**		**GND**	60	O		SMI#	**120**	**P**		**VCC33**
2	IO		AD21	**33**	**P**		**GND**	24	IO		STOP#	**128**	**P**		**VCC33**
1	IO		AD22	**36**	**P**		**GND**	102	IO		TEST2	**96**	**P**		**VCCOSC**
126	IO		AD23	**43**	**P**		**GND**	99	IO		TEST3	**91**	**P**		**VCCPLL**
125	IO		AD24	**51**	**P**		**GND**	98	IO		WAKEUP_EN	**89**	**P**		**VCCPLLA**
124	IO		AD25	**54**	**P**		**GND**	64	I	PD	TESTMODE	**70**	**P**		**VCCSUS**
123	IO		AD26	**61**	**P**		**GND**	22	IO		TRDY#	**84**	**P**		**VCCUSB1**
122	IO		AD27	**100**	**P**		**GND**	71	I	PU	USBOC1#	**80**	**P**		**VCCUSB2**
121	IO		AD28	**108**	**P**		**GND**	68	I	PU	USBOC2#	**76**	**P**		**VCCUSB3**
118	IO		AD29	**114**	**P**		**GND**	66	I	PU	USBOC3#	**72**	**P**		**VCCUSB4**
117	IO		AD30	**119**	**P**		**GND**	65	I	PU	USBOC4#	94	I		XIN
116	IO		AD31	**127**	**P**		**GND**	85	IO		USBP1–	95	O		XOUT

Pin Descriptions

Table 2. VT6212 / VT6212L Pin Descriptions

PCI Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
AD[31:0]	(see pin list)	IO	**VCC33**	**Address and Data.** Addresses are passed during the first clock cycle. Data is passed in subsequent cycles.
CBE[3 :0]#	3, 19, 28, 41	IO	**VCC33**	**Command / Byte Enables.** The command for the current cycle is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are then driven on following clocks.
PAR	27	IO	**VCC33**	**Parity.** A single parity bit is provided over AD[31:0] and CBE[3:0]# to check that the data has been transferred accurately..
IDSEL	6	I	**VCC33**	**Initialization Device Select.** Used as a chip select during configuration read and write cycles.
DEVSEL#	23	IO	**VCC33**	**Device Select.** As an output, this signal is asserted to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT6212-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	20	IO	**VCC33**	**Cycle Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
STOP#	24	IO	**VCC33**	**PCI Stop.** Asserted by the target (the VT6212 / VT6212L chip) to request the master (PCI device) to stop the current transaction.
IRDY#	21	IO	**VCC33**	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	22	IO	**VCC33**	**Target Ready.** Asserted when the target is ready for data transfer.
PCIRST#	111	I	**VCC33**	**PCI Reset.** When detected low, an internal hardware reset is performed. PCIRST# assertion or deassertion may be asynchronous to PCICLK, however, it is recommended that deassertion be synchronous to guarantee a clean and bounce free edge.
PCICLK	109	I	**VCC33**	**PCI Clock.** 33 MHz. Used to clock all PCI bus transactions.
INTA#	105	O	**VCC33**	**PCI Interrupt A.** Asynchronous signal used to request an interrupt.
INTB#	106	O	**VCC33**	**PCI Interrupt B.** Asynchronous signal used to request an interrupt.
INTC#	107	O	**VCC33**	**PCI Interrupt C.** Asynchronous signal used to request an interrupt.
REQ#	113	O	**VCC33**	**PCI Bus Request.** Asserted by the VT6212 / VT6212L to request bus use.
GNT#	112	I	**VCC33**	**PCI Bus Grant.** Asserted by the bus arbiter to grant permission to the VT6212 / VT6212L for access to the PCI bus for bus master operations.

Serial EEPROM Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
EECS	56	O	**VCC33**	**EEPROM Chip Select.** Connect to EEPROM EECS pin.
EECK	55	O	**VCC33**	**EEPROM Clock.** Connect to EEPROM EECK pin.
EEDI	50	O	**VCC33**	**EEPROM Data In.** Connect to EEPROM EEDI pin.
EEDO	49	I	**VCC33**	**EEPROM Data Output.** Connect to EEPROM EEDO pin.

Chipset South Bridge Interface				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
SMI#	60	O	**VCC33**	**System Management Interrupt.**
PME#	67	O	**VCCSUS**	**Power Management Event Interrupt.**

No Connection				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
NC	57-59, 97, 103-104	-		**No connection.**

USB Ports				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
USBP1+	86	IO	**VCCUSB1**	**USB Port 1 Differential Data Plus.** Asserted high (> 2.8V) †
USBP1–	85	IO	**VCCUSB1**	**USB Port 1 Differential Data Minus.** Asserted low (< 0.3V) †
USBP2+	82	IO	**VCCUSB2**	**USB Port 2 Differential Data Plus.** Asserted high (> 2.8V) †
USBP2–	81	IO	**VCCUSB2**	**USB Port 2 Differential Data Minus.** Asserted low (< 0.3V) †
USBP3+	78	IO	**VCCUSB3**	**USB Port 3 Differential Data Plus.** Asserted high (> 2.8V) †
USBP3–	77	IO	**VCCUSB3**	**USB Port 3 Differential Data Minus.** Asserted low (< 0.3V) †
USBP4+	74	IO	**VCCUSB4**	**USB Port 4 Differential Data Plus.** Asserted high (> 2.8V) †
USBP4–	73	IO	**VCCUSB4**	**USB Port 4 Differential Data Minus.** Asserted low (< 0.3V) †
USBOC1#	71	I	**VCCSUS**	**USB Over-Current Input Port 1.** When the supplied current exceeds 500 mA on a USB port, USBOC# should be asserted. If this input is asserted low, the host controller will disable USB port 1. The port will remain disabled as long as the condition persists. See Design Guide and evaluation board schematics for overcurrent detection scheme.
USBOC2#	68	I	**VCCSUS**	**USB Over-Current Input Port 2.** Same as above but for port 2.
USBOC3#	66	I	**VCCSUS**	**USB Over-Current Input Port 3.** Same as above but for port 2.
USBOC4#	65	I	**VCCSUS**	**USB Over-Current Input Port 4.** Same as above but for port 2.
XIN	94	I	**VCCOSC**	**Crystal Input.** May be connected to a 24 MHz parallel resonant fundamental mode crystal (see Design Guide for specific connection details).
XOUT	95	O	**VCCOSC**	**Crystal Output.** Must be connected to a 24 MHz parallel resonant fundamental mode crystal (see Design Guide for specific connection details).
REXT	88	A	**VCCPLL**	**External Resistor.** Typical 6.12kΩ 1% pull down to analog ground (see Design Guide for specific connection details).

† Data encoding is NRZI (Non Return to Zero Inverted) so at times the reverse may be true (i.e., the plus pin may be asserted low and the minus pin asserted high.)

Test Pins and Reserved Pins				
Signal Name	**Pin #**	**I/O**	**Power**	**Signal Description**
ATPG_EN	63	I	**VCC25**	**Automatic Test Program Generator Enable.** Do not connect for normal operation. Internal pulldown.
TESTMODE	64	I	**VCC25**	**Test Mode Enable.** Do not connect for normal operation. Internal pulldown.
TEST2	102	IO	**VCC25**	**Test Signal 2.** Leave unconnected for normal operation.
TEST3	99	IO	**VCC25**	**Test Signal 3.** Pull down 4.7K-ohm for normal operation.
WAKEUP_EN	98	IO	**VCC25**	**WAKEUP_EN.** Enable wakeup function

Power and Ground			
Signal Name	**Pin #**	**Power**	**Signal Description**
VCC33	10, 18, 26, 34, 44, 52, 62, 101, 110, 120, 128	**Digital I/O**	**Digital I/O Power.** 3.3V ±100mV
VCC25	4, 35, 53, 115	**Internal**	**Internal Logic Power.** 2.5V ±5%
GND	5, 9, 17, 25, 33, 36, 43, 51, 54, 61, 100, 108, 114, 119, 127	**Ground**	**Ground.** Connect to primary PCB ground plane.
VCCSUS	70	**Suspend**	**Suspend I/O Power.** Connect to system 3.3V ±5% suspend power for support of wakeup on USB incoming port activity.
GNDSUS	69	**Suspend**	**Suspend I/O Ground.** Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.
VCCUSB[4-1]	72, 76, 80, 84	**USB Ports**	**USB Port Power.** Connect to system 3.3V ±5% suspend power for support of wakeup on USB incoming port activity.
GNDUSB[4-1]	75, 79, 83, 87	**USB Ports**	**USB Port 1-4 Analog Ground**. Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.
VCCPLL	91	**PLL**	**PLL Digital Power.** Connect to quiet 2.5V ±5% power source.
GNDPLL	92	**PLL**	**PLL Digital Ground.** Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.
VCCPLLA	89	**PLL**	**PLL Analog Power.** Connect to quiet 2.5V ±5% power source.
GNDPLLA	90	**PLL**	**PLL Analog Ground.** Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.
VCCOSC	96	**OSC**	**Oscillator Power.** Connect to quiet 2.5V ±5% power source.
GNDOSC	93	**OSC**	**Oscillator Analog Ground.** Connect to analog ground plane (connected to primary PCB ground plane through ferrite beads for isolation from digital switching noise). See Design Guide for details.

REGISTERS

Register Overview

Register settings are located in different sections of this document corresponding to "functions". Each section is indicated by the function number and is dedicated to a specific controller function. These are summarized as follows:

Function 0: Universal Host Controller Interface #1 (UHCI)
Function 1: Universal Host Controller Interface #2 (UHCI)
Function 2: Enhanced Host Controller Interface (EHCI)

The tables in this section describe the register settings for the UHCI Host Controllers and the EHCI Host Controller. The registers are listed according to their offset values. The tables show the Access Type (Read/Only, Read/Write, and Read/Write/Clear) and power-on default values ("Default). All offset values are shown in hexadecimal unless otherwise indicated. Default values for each register are also indicated in hexadecimal notation.

Note: Registers indicated as RW may have some read-only bits that always read back a fixed value (usually 0 if unused); registers assigned as RWC or WC may have some read-only or read-write bits (see individual register descriptions for details).

Register Summary Tables

Function 0-1 UHCI Universal Host Controller Interface

Function 0-1 UHCI PCI Configuration Header

Offset	UHCI PCI Configuration Header	Default	Acc
1-0	Vendor ID	**1106**	**RO**
3-2	Device ID	**3038**	**RO**
5-4	Command	0000	RW
7-6	Status	**0210**	**WC**
8	Revision ID	**60**	**RO**
B-9	Class Code	**0C 03 00**	**RO**
C	Cache Line Size	00	RW
D	Latency Timer	**16**	RW
E	Header Type	00	**RO**
F	BIST	00	RW
10-13	-reserved-	00	–
17-14	CIS Base Addr (Cardbus Mode Only)	0000 0000	RW
18-1F	-reserved-	00	–
23-20	UHCI-Compliant I/O Base Address	**0000 0001**	RW
24-27	-reserved-	00	–
2B-28	Cardbus CIS Pointer	**0000 0053**	**RO**
2F-2C	Subsystem ID / Subsystem Vendor ID	**3038 1106**	**RO**
30-33	-reserved-	00	–
34	Power Management Capability	**80**	RW
35-3B	-reserved-	00	–
3C	Interrupt Line	00	RW
3D	Interrupt Pin PCI:	**01, 02**	RW
	Cardbus:	**01**	
3E-3F	-reserved-	00	–

Function 0-1 UHCI Device Specific Registers

Offset	UHCI Device Specific Registers	Default	Acc
40	Miscellaneous Control 1	**40**	RW
41	Miscellaneous Control 2	**10**	RW
42	Miscellaneous Control 3	03	RW
43	-reserved-	00	–
44-47	Reserved (Do Not Program)	–	–
48	Miscellaneous Control 5	00	RW
49	Miscellaneous Control 6	**0B**	RW
4A	-reserved-	00	–
4B	Miscellaneous Control 8	00	RW
4C-5F	-reserved-	00	–
60	Serial Bus Release Number	**10**	RW
61-7F	-reserved-	00	–
83-80	Power Management Capabilities Rx49[0]=0: / Rx49[0]=1:	**7E0A 0001** / **FFC2 0001**	**RO**
84	Power Management Capability Status	00, **03**	RW
85-BF	-reserved-	00	–
C1-C0	Legacy Support	**2000**	RW
C2-FF	-reserved-	00	–

Function 0-1 USB UHCI I/O Registers

Offset	UHCI I/O Registers	Default	Acc
1-0	USB Command		
3-2	USB Status		
5-4	USB Interrupt Enable		
7-6	Frame Number		
B-8	Frame List Base Address		
C	Start of Frame Modify		
D-F	-reserved-		
11-10	Port 1 Status / Control		
13-12	Port 2 Status / Control		
14-FF	-reserved-		

Function 2 EHCI Enhanced Host Controller Interface

Function 2 EHCI PCI Configuration Header

Offset	EHCI PCI Configuration Header	Default	Acc
1-0	Vendor ID	**1106**	**RO**
3-2	Device ID	**3104**	**RO**
5-4	Command	0000	RW
7-6	Status	**0210**	RW
8	Revision ID	**60**	**RO**
B-9	Class Code	**0C 03 20**	**RO**
C	Cache Line Size	00	RW
D	Latency Timer	**16**	RW
E	Header Type	00	**RO**
F	BIST	00	**RO**
13-10	Memory Mapped IO Base Address	0000 0000	RW
17-14	CIS Base Addr (Cardbus Mode Only)	0000 0000	RW
18-2A	-reserved-	00	–
2B-28	Cardbus CIS Pointer	**0000 00AA**	**RO**
2F-2C	Sub-system and Sub-sys Vendor ID	**3104 1106**	**RO**
30-33	-reserved-	00	–
34	Power Management Capability	**80**	RW
35-3B	-reserved-	00	–
3C	Interrupt Line	00	**RO**
3D	Interrupt Pin	**03**	**RO**
3E-3F	-reserved-	00h	–

Function 2 EHCI Device Specific Registers

Offset	EHCI Device Specific Registers	Default	Acc
40	Miscellaneous Control 1	00	RW
41	Miscellaneous Control 2	00	RW
42	Miscellaneous Control 3	00	RW
43	-reserved-	00	–
44-47	Reserved (Do Not Program)	–	–
48	Miscellaneous Control 4	A0	RW
49	Miscellaneous Control 5	20	RW
4A	MAC Inter-transaction Delay Parameter	00	RO
4B	MAC Turn-around Time Parameter	09	RW
50	Reserved (Do Not Program)	–	–
51	USB 2.0 Timeout RX Parameter	5A	RW
52-59	Reserved (Do Not Program)	–	–
5B-5A	Hi-Speed Port Pad Termination Resistor Fine Tune	**4444**	RW
5C	Reserved (Do Not Program)	–	–
5D-5F	-reserved-	00	–
60	Serial Bus Release Number		**RO**
61	Frame Length Adjust		RW
63-62	Port Wake Capability		RW
64-67	-reserved-	00	–
6B-68	USB Legacy Support Extd Capability	**0000 0001**	RW
6F-6C	USB Legacy Support Control / Status	0000 0000	RW
71-70	SRAM Direct Access Address	0000	RW
72	-reserved-	00	–
73	SRAM Direct Access Control	00	RW
77-74	SRAM Direct Access Data	0000 0000	RW
78-7F	-reserved-	00	–
83-80	Power Management Capabilities Rx49[1]=0: / Rx49[1]=1:	**7E0A 0001** / **FFC2 0001**	**RO**
84	Power Management Capability Status		RW
85-FF	-reserved-	00	–

Function 2 USB EHCI Memory-Mapped I/O Registers

EHCI Memory Mapped I/O Capability Registers

Offset	EHCI Capability Registers	Default	Acc
0	Capability Register Length	**10**	RW
1	-reserved-	00	–
3-2	Interface Version Number	**0100**	RW
7-4	Structure Parameters	**0000 2204**	RW
B-8	Capability Parameters	**0000 6872**	RW
C-F	-reserved-	00	–

EHCI Memory Mapped I/O Operational Registers

Offset	EHCI Operational Registers	Default	Acc
13-10	USB Command		
17-14	USB Status		
1B-18	USB Interrupt Enable		
1F-1C	USB Frame Index		
23-20	4G Segment Selector		
27-24	Frame List Base Address		
2B-28	Next Asynchronous List Address		
2C-4F	Reserved		
53-50	Configured Flag		
57-54	Port 1 Status / Control		
5B-58	Port 2 Status / Control		
5F-5C	Port 3 Status / Control		
63-60	Port 4 Status / Control		
64-FF	-reserved-		

Register Descriptions

Function 0-1 UHCI Universal Host Controller Interface

The VT6212 / VT6212L contains two USB host controllers, which are controlled by functions 0 and 1 respectively. Register definitions for both controllers are identical, except where noted. Function 0 and function 1 registers conform to the UHCI (Universal Host Controller Interface) Specification.

There are two sets of registers: PCI configuration space registers (located in functions 0 and 1) and USB I/O registers (located in system I/O space at offsets from the address stored in the Base Address Register).

Function 0-1 Configuration Space Header

Offset 1-0 - Vendor ID (1106h) ..... **RO**

15-0 Vendor ID ..... 1106h = VIA Technologies

Offset 3-2 - Device ID (3038h) ..... **RO**

15-0 Device ID ..... reads 3038h to identify the VT6212

Offset 5-4 – Command Register (0000h) ..... **RW**

15-8 Reserved ..... always reads 0

7 Address Stepping
- 0 Disable ..... default
- 1 Enable

6-5 Reserved ..... always reads 0

4 Memory Write and Invalidate
- 0 Disable ..... default
- 1 Enable

3 Special Cycle ..... fixed at 0

2 Bus Master
- 0 Disable ..... default
- 1 Enable

1 Memory Space
- 0 Disable ..... default
- 1 Enable

0 I/O Space
- 0 Disable ..... default
- 1 Enable

Offset 7-6 – Status Register (0210h) ..... **RW**

15 Reserved ..... always reads 0

14 Signaled System Error ..... always reads 0

13 Received Master Abort ..... **RWC**
Set by the VT6212 interface logic if it generates a master abort while acting as a master ..... default = 0

12 Received Target Abort ..... **RWC**
Set by the VT6212 interface logic if it receives a target abort while acting as a master ..... default = 0

11 Signaled Target Abort

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... fixed
- 10 Slow
- 11 Reserved

8-5 Reserved ..... always reads 0

4 Power Management Interrupt ..... **always reads 1**

3-0 Reserved ..... always reads 0

Offset 8 - Revision ID (60h) ..... **RO**

Offset B-9 - Class Code (0C 03 00h) ..... **RO**

23-0 Class Code fixed value indicates USB 1.1 Controller

Offset C - Cache Line Size (00h) ..... **RW**

Offset D - Latency Timer (16h) ..... **RW**

Offset E - Header Type (00h) ..... **RO**

Offset F - BIST (00h) ..... **RO**

Offset 17-14 - CIS Base Addr – Cardbus Mode Only ... RW

31-8 Correspond to AD [31:8] ..... default = 0

7-0 Reserved ..... always reads 0

Offset 23-20 – Base Address for UHCI 1.1 Compliant USB I/O ..... **RW**

31-16 Reserved ..... always reads 0

15-5 Port Base Address for USB IO Registers Corresponding to AD[15:5] .....

4-0 Fixed ..... always reads 00001b

Offset 2B-28 – Cardbus CIS Pointer ..... **RO**

31-8 Reserved ..... always reads 0

7-3 Cardbus CIS Pointer ..... fixed at 50h

2-0 Second Base Address ..... fixed at 3'b010

Offset 2F-2C – Subsystem ID / Subsystem Vendor ID .. **RO**

24-0 Subsystem ID / Subsystem Vendor ID
Rx42[4] = 0 ..... fixed at 30381106h

Offset 34 - Power Management Capability (80h) ..... **RO**

Offset 3C - Interrupt Line (00h) ..... **RO**

Offset 3D - Interrupt Pin (01h, 02h) ..... **RO**

Function 0-1 Device Specific Registers

Offset 40 - Miscellaneous Control 1 (40h).....**RW**

7 PCI Memory Command Option
- 0 Support "Memory Read Line", "Memory Read Multiple", and "Memory Write and Invalidate" commands.....default
- 1 Support only "Memory Read" and "Memory Write" commands

6 Babble Option
- 0 Auto-disable babbled port on EOF
- 1 Keep babbled port enabled.....default

5 PCI Parity Check
- 0 Disable .....default
- 1 Enable

4 Reserved (Do Not Program) ..... default = 0

3 USB Data Length Option
- 0 Support transmit data length up to 1280 .....def
- 1 Support transmit data length up to 1023

2 Improve FIFO Latency for packets less than 64B
- 0 Enable .....default
- 1 Disable

1 DMA Options
- 0 8DW burst access with better FIFO latency def
- 1 16DW burst access (original performance level)

0 PCI Wait State
- 0 Zero Wait States.....default
- 1 One Wait State

Offset 41 - Miscellaneous Control 2 (10h).....**RW**

7-5 Reserved (Do Not Program) ..... default = 0

4 Hold PCI REQ_ for successive access
- 0 Disable
- 1 Enable

3 Reserved (Do Not Program) ..... default = 0

2 Trap Option
- 0 Set trap 60/64 status bits without checking enable bits .....default
- 1 Set trap 60/64 status bits only when trap 60/64 enable bits are set

1 A20Gate Pass Through Option
- 0 Pass through A20Gate command sequence .def
- 1 Do not pass through write I/O port 64

0 Reserved (Do Not Program) ..... default = 0

Offset 42 - Miscellaneous Control 3 (03h) ..... **RW**

7-2 Reserved (Do Not Program)..... default = 0

1-0 Release continuous REQ_ after N PCICLKs (feature controlled by Function 0's register)
- 00 Do not release
- 01~11 Number X 32 PCICLKs

Offset 48 - Miscellaneous Control 5 (00h) ..... **RW**

7-6 Reserved (Do Not Program)..... default = 0

5 Enable enhanced PCI read command generation in reading descriptors
- 0 Enable..... def
- 1 Disable

4-0 Reserved (Do Not Program)..... default = 0

Offset 49 - Miscellaneous Control 6 (0Bh)..... **RW**

7-2 Reserved (Do Not Program)..... default = 0

1 EHCI Supports PME# Assertion in D3cold State
- 0 Not support
- 1 Supported ..... default

0 UHCI Supports PME# Assertion in D3cold State
- 0 No Support
- 1 Supported ..... default

Offset 4B - Miscellaneous Control 8 (00h)..... **RW**

7-1 Reserved .....default = 0

0 Cardbus mode select (strapped via EESK)
- 0 PCI mode
- 1 Cardbus mode

Offset 60 - Serial Bus Release Number (10h) ..... **RO**

Offset 83-80 - Power Management Capabilities ..... **RO**

24-0 Power Management Capabilities

Rx49[0] = 0 ..... fixed at 00 02 00 01h

Rx49[0] = 1 .....fixed at C9 C2 00 01h

Offset 84 - Power Mgmt Capability Status (00h or 03h) **RW**

Offset C1-C0 - UHCI 1.1 Legacy Support (2000h)..... **RW**

Function 0-1 UHCI Compliant USB I/O Registers

The USB I/O registers are compliant with the UHCI v1.1 standard. For more details of the register configurations, refer to the relevant documentation for the UHCI V1.1 standard.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start of Frame Modify

I/O Offset 11-10 - Port 1 Status / Control

I/O Offset 13-12 - Port 2 Status / Control

Function 2 EHCI Enhanced Host Controller Interface

In addition to the UHCI host controllers at functions 0 and 1, the VT6212 / VT6212L also contains another USB host controller, which conforms to the EHCI (Enhanced Host Controller Interface) Specification.

There are two sets of registers: PCI configuration space registers (located in function 2) and USB Memory Mapped I/O registers, (located in system memory at offsets from the address stored in the Base Address Register).

Function 2 Configuration Space Header

Offset 1-0 - Vendor ID (1106h) ..... **RO**

7-0 Vendor ID .....1106h = VIA Technologies

Offset 3-2 - Device ID (3104h).....**RO**

7-0 Device ID .....3104h = EHCI controller

Offset 5-4 – Command (0000h).....**RW**

15-8 Reserved ..... always reads 0

7 Address Stepping
- 0 Disable .....default
- 1 Enable

6-5 Reserved .....fixed at 0 (disabled)

4 Memory Write and Invalidate
- 0 Disable .....default
- 1 Enable

3 Special Cycle .....fixed at 0

2 Bus Master
- 0 Disable .....default
- 1 Enable

1 Memory Space
- 0 Disable .....default
- 1 Enable

0 I/O Space
- 0 Disable .....default
- 1 Enable

Offset 7-6 – Status (0210h)..... **RW**

15 Reserved .....always reads 0

14 Signaled System Error..... default = 0

13 Received Master Abort..... default = 0

12 Received Target Abort..... default = 0

11 Signaled Target Abort ..... default = 0

10-9 DEVS EL# Timing
- 00 Fast
- 01 Medium ..... fixed
- 10 Slow
- 11 Reserved

8-5 Reserved .....always reads 0

4 Power Management Interrupt ..... always reads 1

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (60h) ..... **RO**

Offset B-9 - Class Code (0C0320=EHCI Host Controller) **RO**

23-0 Fixed value of class code indicates USB2.0 EHCI Host Controller

Offset C - Cache Line Size (00h) ..... **RW**

Offset D - Latency Timer: (16h)..... **RW**

Offset E - Header Type (00h)..... **RO**

Offset F - BIST (00h)..... **RO**

Offset 13-10 – EHCI 0.95 Memory Mapped I/O Base .. RW

31-8 I/O Base Address for EHCI 0.95 USB Memory Mapped I/O Registers..... default = 0
(these bits correspond to AD[31:8])

7-3 Reserved.....always reads 0

2-1 Fixed .....fixed at 00h (32-bit addressing only)

0 Reserved.....always reads 0

Offset 17-14 - CIS Base Addr – Cardbus Mode Only ... RW

31-8 Correspond to AD [31:8] ..... default = 0

7-0 Reserved .....always reads 0

Offset 2B-28 – Cardbus CIS Pointer (AAh)..... **RO**

31-8 Reserved .....always reads 0

7-3 Cardbus CIS Pointer ..... fixed at A8h

2-0 Second Base Address ..... fixed at 3'b010

Offset 34 – Power Management Capability (80h)..... **RO**

Offset 3C - Interrupt Line (00h)..... **RO**

Offset 3D - Interrupt Pin (03h)..... **RO**

Function 2 Device-Specific Registers

Offset 40 - Miscellaneous Control 1 (00h).....RW

7 PCI Memory Command Option
- 0 Support "Memory Read Line", "Memory Read Multiple", and "Memory Write and Invalidate" commands.....default
- 1 Only supports "Memory Read" and "Memory Write" commands

6 Babble Option
- 0 Auto-disable babbled port when EOF ...default
- 1 Keep babbled port enabled

5 PCI Parity Check
- 0 Disable .....default
- 1 Enable

4 Reserved (Do Not Program) ..... default = 0

3-2 Reserved ..... always reads 0

1 DMA Options
- 0 8DW burst access.....default
- 1 16DW burst access

0 PCI Wait States
- 0 Zero Wait States.....default
- 1 One Wait State

Offset 41 - Miscellaneous Control 2 (00h).....RW

7-5 Reserved ..... always reads 0

4 Hold PCI REQ_ for successive access
- 0 Disable
- 1 Enable

3-0 Reserved ..... always reads 0

Offset 42 - Miscellaneous Control 3 (00h).....RW

7-5 Reserved ..... always reads 0

4 Sub-system and sub-system Vendor ID R/W
- 0 Disable .....default
- 1 Enable

3-0 Reserved ..... always reads 0

Offset 48 - Miscellaneous Control 4 (A0h).....RW

7-6 Reserved ..... always reads 0

5 Disable PCI burst access
- 0 Burst enable .....default
- 1 Burst disable

4-0 Reserved ..... always reads 0

Offset 49 - Miscellaneous Control 5 (20h) ..... RW

7 Enable MAC (provides more delay between transactions)
- 0 Disable..... default
- 1 Enable

6 Enable MAC (provides timeout to device when error is detected)
- 0 Disable..... default
- 1 Enable

5 Clock Auto Stop
- 0 Disable, no stop
- 1 Enable, auto stop ..... default

4-0 Reserved .....always reads 0

Offset 4A - MAC inter-transaction delay parameter (00h)RO

Offset 4B - MAC turn around time parameter (09h).... RW

7-6 Reserved .....always reads 0

5 EHCI sleep time select
- 0 1 µs ..... default
- 1 10 µs

4 Reserved .....always reads 0

3-0 USB 2.0 MAC TX time parameter ..... default = 9

Offset 51 - USB 2.0 Timeout RX Parameter (5Ah) ..... RW

Offset 5B 5A - High-Speed Port Pad Termination Resistor Fine Tune (4444h)..... RW

15-12 Control A[3:0] .....default = 4h

11-8 Control B[3:0].....default = 4h

7-4 Control C[3:0] .....default = 4h

3-0 Control D[3:0] .....default = 4h

Offset 60 - Serial Bus Number (20h = USB 2.0)..... RO

Offset 61- Frame Length Adjust (20h) ..... RW

Offset 63-62 - Port Wake Capability (0001h)..... RW

Offset 83-80 - Power Management Capability..... RO

Function 0 49[1] = 0: .....fixed at C9 C2 00 01h
Function 0 49[1] = 1: ..... fixed at 48 0A 00 01h

Offset 84 - Power Mgmt Capability Status (00h or 03h) RW

Function 2 EHCI Compliant USB Memory-Mapped I/O Registers

The USB Memory Mapped I/O registers are compliant with the EHCI standard. For more details of the register configurations, refer to the relevant documentation for the EHCI standard.

EHCI Capability Registers

Offset 0 - Capability Register Length (10h).....**RW**

Offset 3-2 - Interface Version Number (0100h).....**RW**

Offset 7-4 - Structure Parameters (00002204h).....**RW**

Offset B-8 - Capability Parameters (00006872h) .....**RW**

EHCI Operational Registers

Offset 13-10 - USB Command.....**RW**

Offset 17-14 - USB Status.....**RW**

Offset 1B-18 - USB Interrupt Enable.....**RW**

Offset 1F-1C - USB Frame Index .....**RW**

Offset 23-20 - 4G Segment Select.....**RW**

Offset 27-24 - Frame List Base Address.....**RW**

Offset 2B-28 - Next Asynchronous List Address.....**RW**

Offset 53-50 - Configured Flag .....**RW**

Offset 57-54 - Port 1 Status / Control.....**RW**

Offset 5B-58 - Port 2 Status / Control .....**RW**

Offset 5F-5C - Port 3 Status / Control .....**RW**

Offset 63-60 - Port 4 Status / Control.....**RW**

ELECTRICAL SPECIFICATIONS

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comment
T_{STG}	Storage temperature	-55	125	^{o}C	
T_C	Case operating temperature	0	85	^{o}C	
V_{CC}	Power supply voltages	-0.5	4.0	V	
V_I	Input voltage	-0.5	5.5	V	
V_O	Output voltage at any output	-0.5	V_{CC} + 0.5	V	
V_{ESD}	Electrostatic discharge		2	kV	Human Body Model

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Table 4. DC Characteristics

T_C = 0-55^{o}C, V_{CCPCI} = V_{CCSUS} = V_{CCUSBN} = 3.3V+/-5%, V_{CC25} = V_{CCOSC} = V_{CCPLL} = V_{CCPLLA} =2.5V+/-5%, GND = 0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input Leakage Current	-	+/-10	µA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate Leakage Current	-	+/-20	µA	$0.45<V_{OUT}<V_{CC}$

Table 5. Power Specifications

T_C = 0-55°C, V_{CC33} = V_{CCSUS} = V_{CCUSB} = 3.3V+/-5%, V_{CC25} = V_{CCOSC} = V_{CCPLL} = V_{CCPLLA} =2.5V+/-5%, GND = 0V

Symbol	Parameter	Typ	Max	Unit	Condition
$I_{CC25-PD}$	Power Supply Current – 2.5V	1.1		mA	Power down or suspend
$I_{CC33-PD}$	Power Supply Current – 3.3V	5.4		mA	Power down or suspend
I_{CC25}	Power Supply Current – VCC25 (2.5V)	38		mA	Idle with no port activity
I_{CC33}	Power Supply Current – VCC33 (3.3V)	89		mA	Idle with no port activity
I_{CC25A}	Power Supply Current – Analog (2.5V)†	60		mA	Idle with no port activity
I_{CC0USB}	Power Supply Current – USB (3.3V)‡	47		mA	Idle with no port activity
I_{CC1USB}	Power Supply Current – USB (3.3V)‡	105		mA	One port transmitting
I_{CC2USB}	Power Supply Current – USB (3.3V)‡	160		mA	Two ports transmitting
I_{CC3USB}	Power Supply Current – USB (3.3V)‡	211		mA	Three ports transmitting
I_{CC4USB}	Power Supply Current – USB (3.3V)‡	263		mA	Four ports transmitting
P_{D-PD}	Overall Chip Power Dissipation	18		mW	Power down or suspend
P_{D-IDLE}	Overall Chip Power Dissipation	672		mW	Idle with no port activity
P_{D-4USB}	Overall Chip Power Dissipation	1312		mW	Four ports transmitting

†"Analog 2.5V" power includes VCCPLL, VCCPLLA, and VCCOSC

‡ "USB 3.3V" power includes VCCUSB and VCCSUS

PACKAGE MECHANICAL SPECIFICATIONS

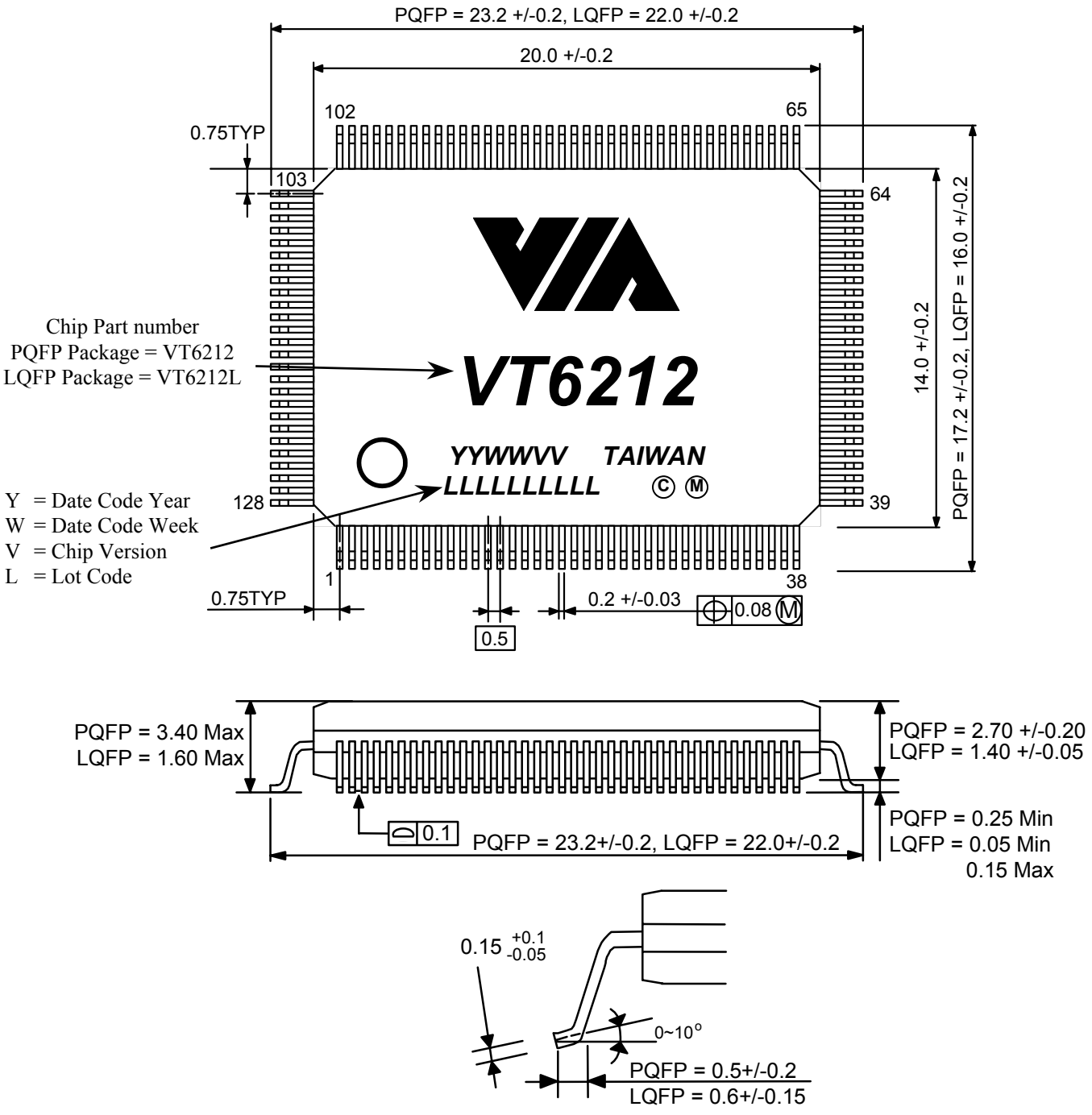


Figure 3. Mechanical Specifications – 128 Pin PQFP (VT6212) / LQFP (VT6212L) Package

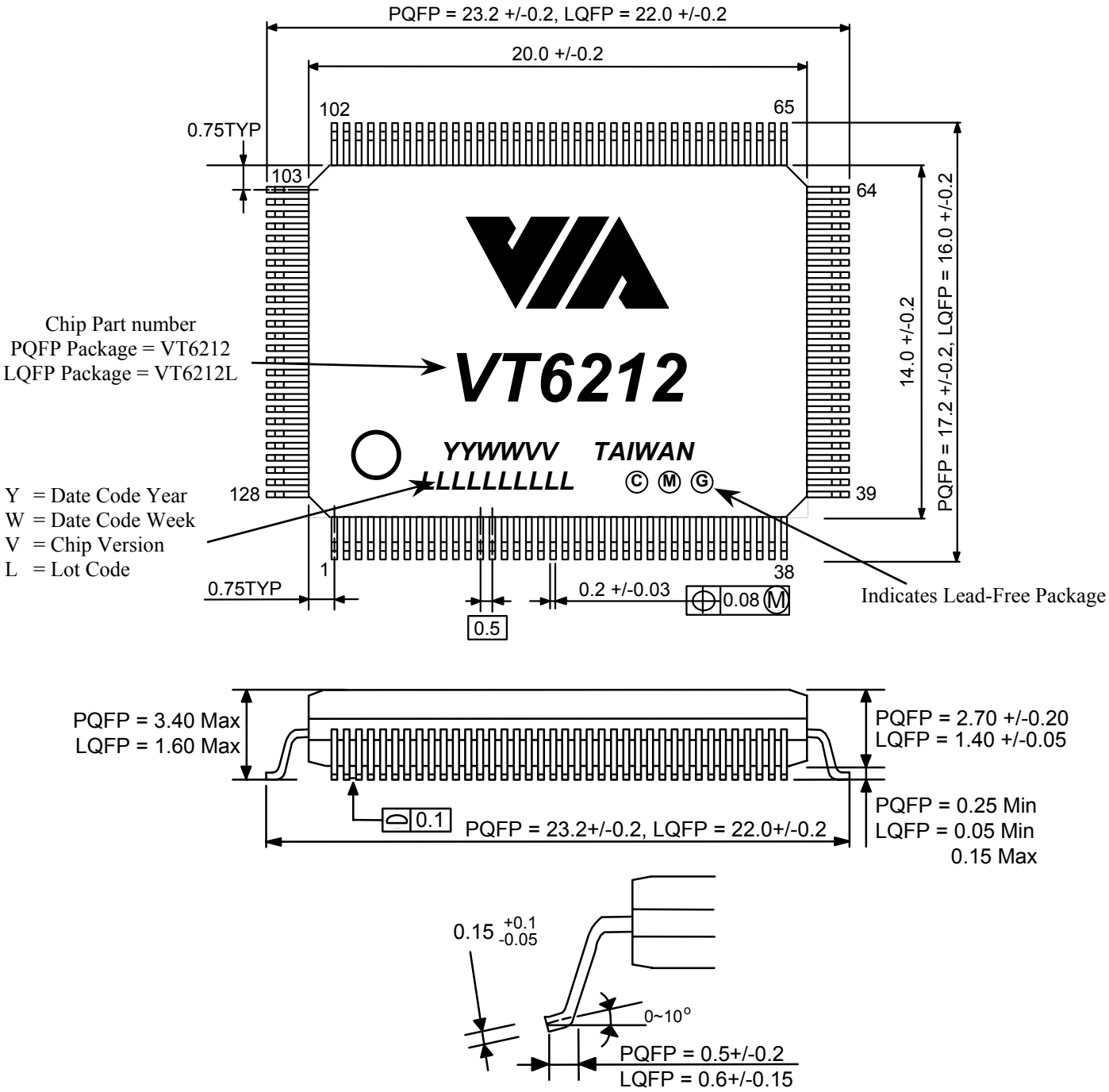


Figure 4. Lead-free Mechanical Specifications – 128 Pin PQFP (VT6212) / LQFP (VT6212L) Package