

Size:
1.91 x 1.09 x 0.37 in
48,6 x 27,7 x 9,5 mm

Applications

- Solid state lighting
- Stadium displays
- Industrial controls
- Avionics
- Underseas
- RF Amplifiers
- Microprocessor and DSP requiring fast response

Features

- 100°C baseplate operation
- 48 V to 2 V Converter
- 80.0 A (120.0 A for 1 ms)
- High density – up to 104 A/in^3
- Small footprint – 1.64 and 2.08 in^2
- Height above board – 0.37 in (9.5 mm)
- Low weight – 1.10 oz (31.3 g)
- ZVS / ZCS isolated sine amplitude converter
- Typical efficiency 91%
- <1 µs transient response
- Isolated output
- No output filtering required
- Lead free wave solder compatible
- Agency approvals

Product Overview

The thermally enhanced VI BRICK VTM current multiplier excels at speed, density and efficiency to meet the demands of advanced power applications. Combined with the VI BRICK PRM regulator they create a DC-DC converter with flexibility to provide isolation and regulation where needed. The PRM can be located with the VTM at the point of load or remotely in the back plane or on a daughter card.

Part Numbering

VT	048	A	020	T	080	F	P
Voltage Transformation Module	Input Voltage Designator	Package Size	Output Voltage Designator (=V_{OUT} x10)		Output Current Designator (=I_{OUT})		

Product Grade Temperatures (°C)

Grade	Operating	Storage
T =	-40 to +100	-40 to +125
M =	-55 to +100	-65 to +125

Baseplate

F = Slotted flange
T = Transverse heat sink[a]

[a] Contact factory

Pin Style

P = Through hole

SPECIFICATIONS

Electrical characteristics apply over the full operating range of input voltage, output load (resistive) and baseplate temperature, unless otherwise specified. All temperatures refer to the operating temperature at the center of the baseplate.

Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60	Vdc	
+In to -In	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
VC to -In	-0.3 to 19.0	Vdc	
+Out to -Out	-0.5 to 4.0	Vdc	
Isolation voltage	2,250	Vdc	Input to output
Output current	80.0	A	Continuous
Peak output current	120.0	A	For 1 ms
Output power	174	W	Continuous
Peak output power	262	W	For 1 ms
Operating temperature	-40 to +100	°C	T-Grade; baseplate
	-55 to +100	°C	M-Grade; baseplate
Storage temperature	-40 to +125	°C	T-Grade
	-65 to +125	°C	M-Grade

Note: Stresses in excess of the maximum ratings can cause permanent damage to the device. Operation of the device is not implied at these or any other conditions in excess of those given in the specification. Exposure to absolute maximum ratings can adversely affect device reliability.

Input Specifications *(Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)*

Parameter	Min	Typ	Max	Unit	Notes
Input voltage range	26.0	48	55	Vdc	Max V_{IN} = 53 V, operating from -55°C to -40°C
Input dV/dt			1	V/µs	
Input overvoltage turn-on	56.0			Vdc	
Input overvoltage turn-off			59.5	Vdc	
Input current			3.8	Adc	
Input reflected ripple current		170		mA p-p	Using test circuit in Figure 10; See Figure 1
No load power dissipation		4.5	6.2	W	
Internal input capacitance		4.0		µF	
Internal input inductance			5	nH	

Output Specifications *(Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)*

Parameter	Min	Typ	Max	Unit	Note
Output voltage	1.09		2.29	Vdc	No load
	0.970		2.18	Vdc	Full load
Rated DC current	0		80.0	Adc	26.0 - 55 V_{IN}
Peak repetitive current			120.0	A	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
Short circuit protection set point	104			Adc	Module will shut down
Current share accuracy		5	10	%	See Parallel Operation on Page 7
Efficiency					
Half load	91.5	91.4		%	See Figure 3
Full load	91.3	91.2		%	See Figure 3
Internal output inductance		0.8		nH	
Internal output capacitance		306		µF	Effective value
Output overvoltage setpoint	2.3			Vdc	Module will shut down
Output ripple voltage					
No external bypass		55	150	mVp-p	See Figures 2 and 5
100 µF bypass capacitor		2		mVp-p	See Figure 6
Effective switching frequency	2.5	2.7	2.8	MHz	Fixed, 1.3 MHz per phase
Line regulation					
K	0.0413	1/24	0.0421		$V_{OUT} = K \bullet V_{IN}$ at no load
Load regulation					
R_{OUT}		1.3	1.5	mΩ	See Figure 13
Transient response					
Voltage overshoot		20		mV	80.0 A load step with 100 µF C_{IN}; See Figures 7 and 8
Response time		200		ns	See Figures 7 and 8
Recovery time		1		µs	See Figures 7 and 8

WAVEFORMS

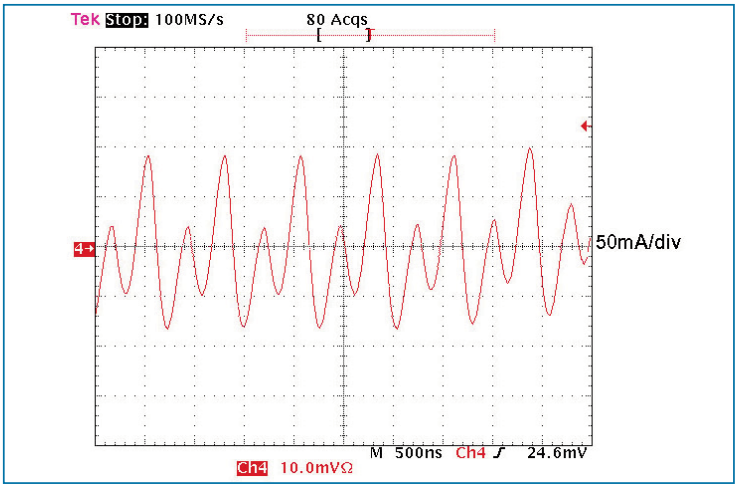


Figure 1 — Input reflected ripple current at full load and 48 Vf.

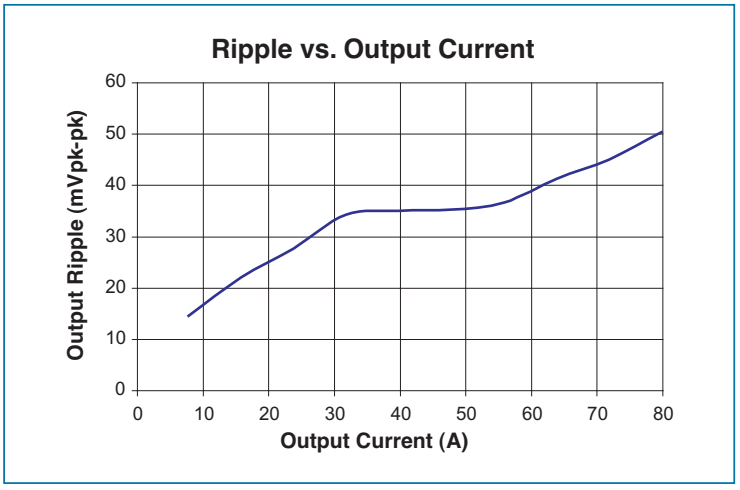


Figure 2 — Output voltage ripple vs. output current at 48 Vf with no POL bypass capacitance.

WAVEFORMS

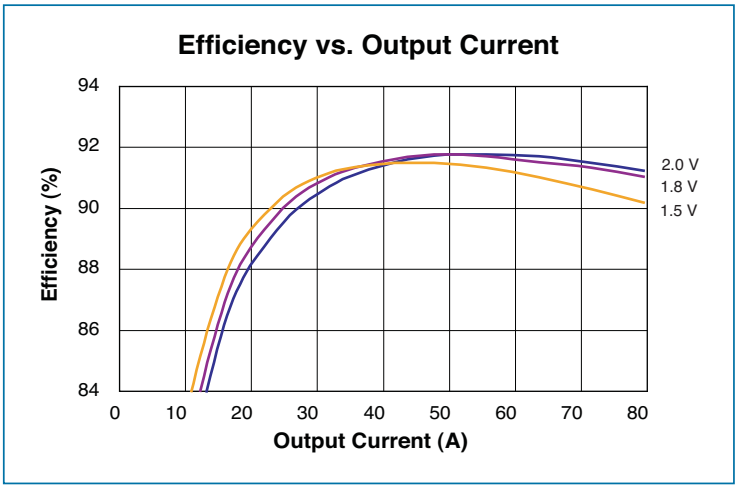


Figure 3 — Efficiency vs. output current.

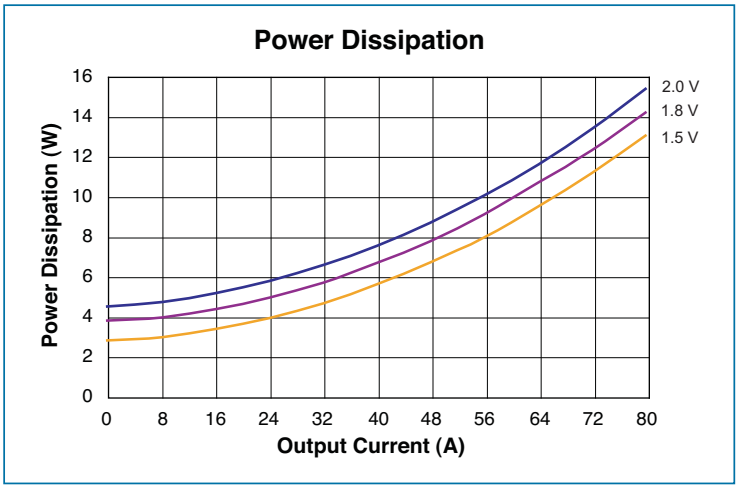


Figure 4 — Power dissipation vs. output current.

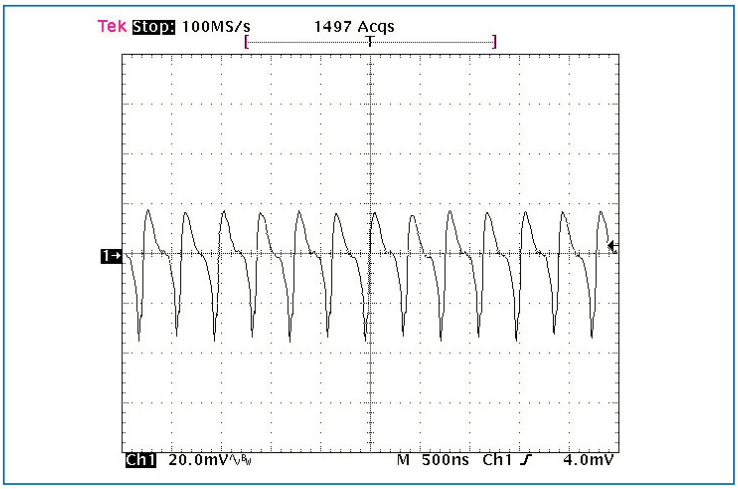


Figure 5 — Output voltage ripple at full load and 48 Vf with no POL bypass capacitance.

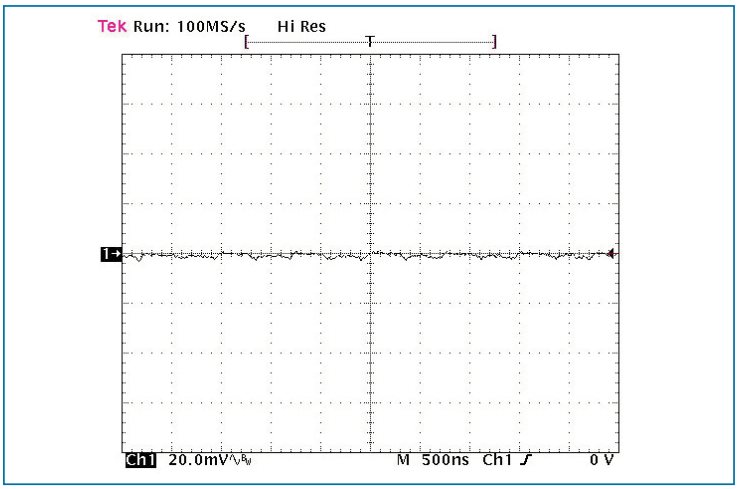


Figure 6 — Output voltage ripple at full load and 48 Vf with 100 µF ceramic POL bypass capacitance and 20 nH distribution inductance.

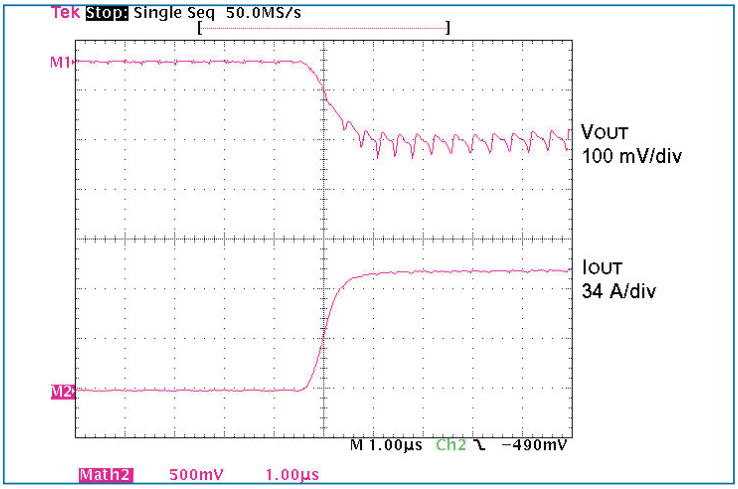


Figure 7 — 0-80.0 A load step with 100 µF input capacitance and no output capacitance.

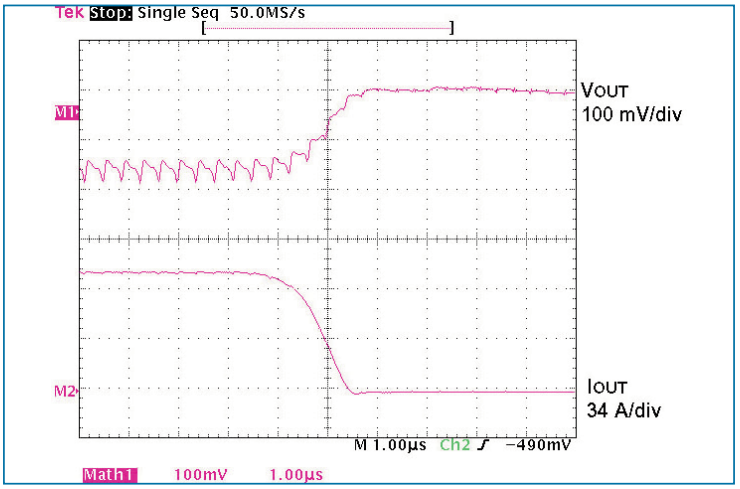


Figure 8 — 80.0-0 A load step with 100 µF input capacitance and no output capacitance.

General Specifications

Parameter	Min	Typ	Max	Unit	Notes
MTBF					
MIL-HDBK-217F		3.5		Mhrs	25°C, GB
Isolation specifications					
Voltage	2,250			Vdc	Input to output
Capacitance		2,500		pF	Input to output
Resistance	10			MΩ	Input to output
Agency approvals		cTÜVus			UL/CSA 60950-1, EN 60950-1
		CE Mark			Low voltage directive
		RoHS			
Mechanical					See Mechanical Drawings, Figures 15, 16
Weight		1.10/31.3		oz/g	
Dimensions					
Length		1.91/48,6		in/mm	Baseplate model
Width		1.09/27,7		in/mm	Baseplate model
Height		0.37/9,5		in/mm	Baseplate model
Thermal					
Over temperature shutdown	125	130	135	°C	Junction temperature
Thermal capacity		23.8		Ws/°C	
Baseplate-to-ambient		7.7		°C/W	
Baseplate-to-ambient; 1000 LFM		2.9		°C/W	
Baseplate-to-sink; flat, greased surface		0.40		°C/W	
Baseplate-to-sink; thermal pad		0.36		°C/W	

Auxiliary Pins

Parameter	Min	Typ	Max	Unit	Notes
Primary Control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	VC voltage must be applied when module is enabled using PC
Current limit	2.4	2.5	2.9	mA	Source only
Disable delay time		10		µs	PC low to Vout low
VTM Control (VC)					
External boost voltage	12	14	19	Vdc	Required for VTM start up without PRM
External boost duration		10		ms	Vin > 26.0 Vdc. VC must be applied continuously if Vin < 26.0 Vdc.

+In / -In DC Voltage Ports

The VTM input should not exceed the maximum specified. Be aware of this limit in applications where the VTM is being driven above its nominal output voltage. If less than 26 Vdc is present at the +In and -In ports, a continuous VC voltage must be applied for the VTM to process power. Otherwise VC voltage need only be applied for 10 ms after the voltage at the +In and -In ports has reached or exceeded 26 Vdc. If the input voltage exceeds the overvoltage turn-off, the VTM will shutdown. The VTM does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

TM – For Factory Use Only

VC – VTM Control

The VC port is multiplexed. It receives the initial V_{CC} voltage from an upstream PRM, synchronizing the output rise of the VTM with the output rise of the PRM. Additionally, the VC port provides feedback to the PRM to compensate for the VTM output resistance. In typical applications using VTMs powered from PRMs, the PRM's VC port should be connected to the VTM VC port.

In applications where a VTM is being used without a PRM, 14 V must be supplied to the VC port for as long as the input voltage is below 26 V and for 10 ms after the input voltage has reached or exceeded 26 V. The VTM is not designed for extended operation below 26 V. The VC port should only be used to provide V_{CC} voltage to the VTM during startup.

PC – Primary Control

The Primary Control (PC) port is a multifunction port for controlling the VTM as follows:

Disable – If PC is left floating, the VTM output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5 Vdc.

+Out / -Out DC Voltage Output Ports

The output and output return are through two sets of contact locations. The respective +Out and –Out groups must be connected in parallel with as low an interconnect resistance as possible. Within the specified input voltage range, the Level 1 DC behavioral model shown in Figure 13 defines the output voltage of the VTM. The current source capability of the VTM is shown in the specification table.

To take full advantage of the VTM, the user should note the low output impedance of the device. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.

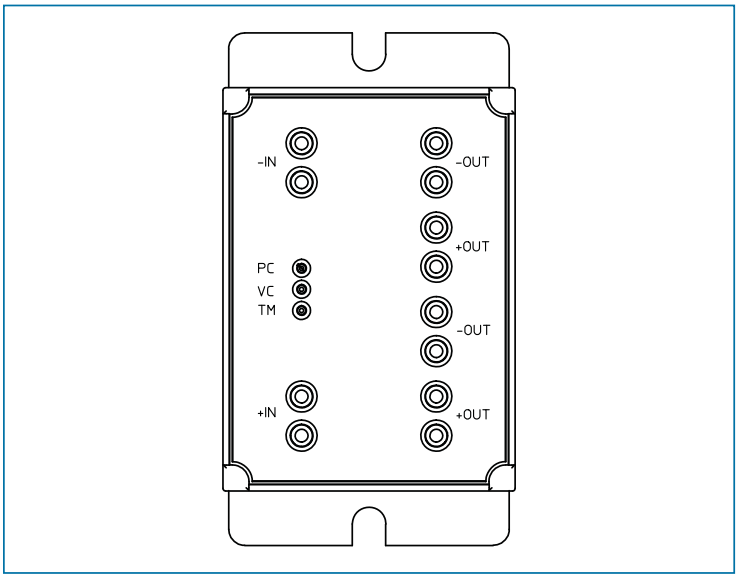


Figure 9 *— VI BRICK VTM pin configuration (viewed from pin side)*

Parallel Operation

In applications requiring higher current or redundancy, VTMs can be operated in parallel without adding control circuitry or signal lines. To maximize current sharing accuracy, it is imperative that the source and load impedance on each VTM in a parallel array be equal. If VTMs are being fed by an upstream PRM, the VC nodes of all VTMs must be connected to the PRM VC.

To achieve matched impedances, dedicated power planes within the PC board should be used for the output and output return paths to the array of paralleled VTMs. This technique is preferable to using traces of varying size and length.

The VTM power train and control architecture allow bi-directional power transfer when the VTM is operating within its specified ranges. Bi-directional power processing improves transient response in the event of an output load dump. The VTM may operate in reverse, returning output power back to the input source. It does so efficiently.

Input Impedance Recommendations

To take full advantage of the VTM's capabilities, the impedance of the source (input source plus the PC board impedance) must be low over a range from DC to 5 MHz. The input of the VTM (factorized bus) should be locally bypassed with a 8 µF low Q aluminum electrolytic capacitor. Additional input capacitance may be added to improve transient performance or compensate for high source impedance. The VTM has extremely wide bandwidth so the source response to transients is usually the limiting factor in overall output response of the VTM.

Anomalies in the response of the source will appear at the output of the VTM, multiplied by its K factor of 1/24. The DC resistance of the source should be kept as low as possible to minimize voltage deviations on the input to the VTM. If the VTM is going to be operating close to the high limit of its input range, make sure input voltage deviations will not trigger the input overvoltage turn-off threshold.

Input Fuse Recommendations

VI BRICKs are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of VI BRICKs must always be incorporated within the power system. A fast acting fuse is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +In port. For agency approvals and fusing conditions, click on the link below:

http://www.vicorpower.com/technical_library/technical_documentation/quality_and_certification/safety_approvals/

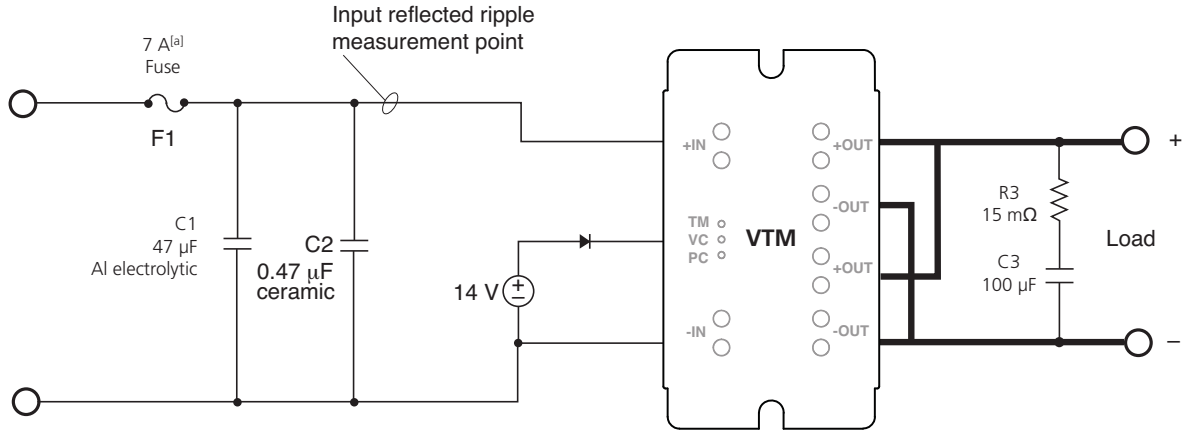
Application Notes

For VTM and VI BRICK application notes on soldering, board layout, and system design please click on the link below:

http://www.vicorpower.com/technical_library/application_information/

Applications Assistance

Please contact Vicor Applications Engineering for assistance, 1-800-927-9474, or email at apps@vicorpower.com.



Notes:
1. C3 should be placed close to the load
2. R3 may be ESR of C3 or a separate damping resistor.

[a] See Input Fuse Recommendations section

Figure 10 — VI BRICK VTM test circuit

In figures below;

K = VTM transformation ratio
R_O = VTM output resistance
V_f = PRM output (Factorized Bus Voltage)
V_O = VTM output
V_L = Desired load voltage

FPA ADAPTIVE LOOP

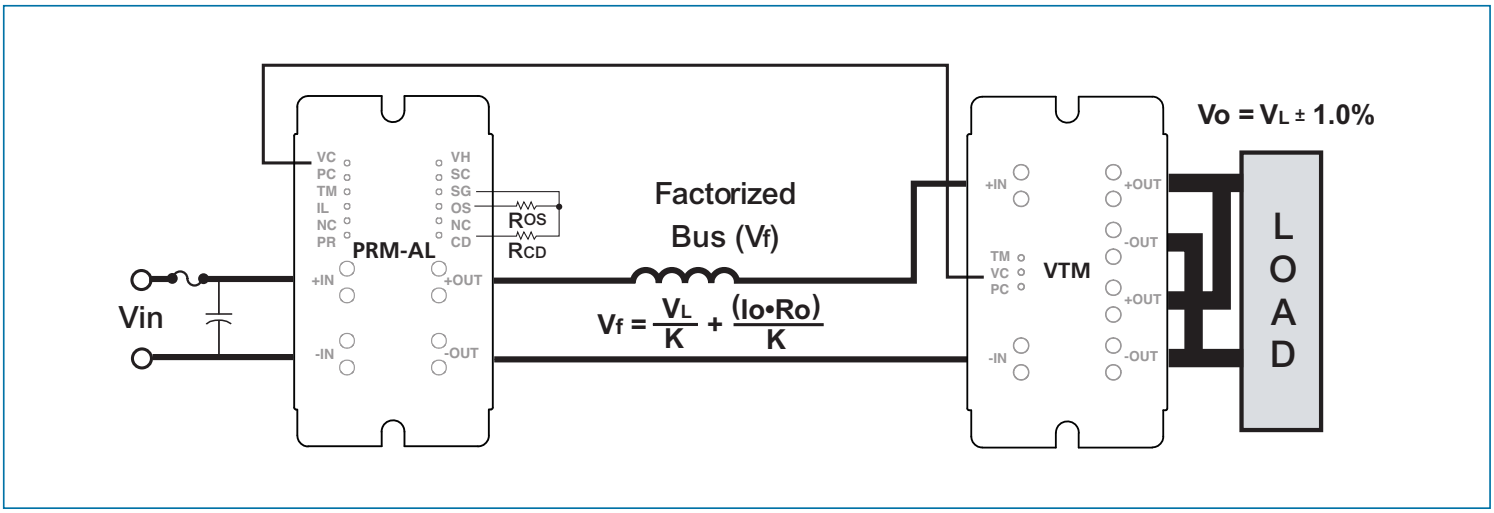


Figure 11 *— The PRM controls the factorized bus voltage, V_f, in proportion to output current to compensate for the output resistance, Ro, of the VTM. The VTM output voltage is typically within 1% of the desired load voltage (V_L) over all line and load conditions.*

FPA NON-ISOLATED REMOTE LOOP

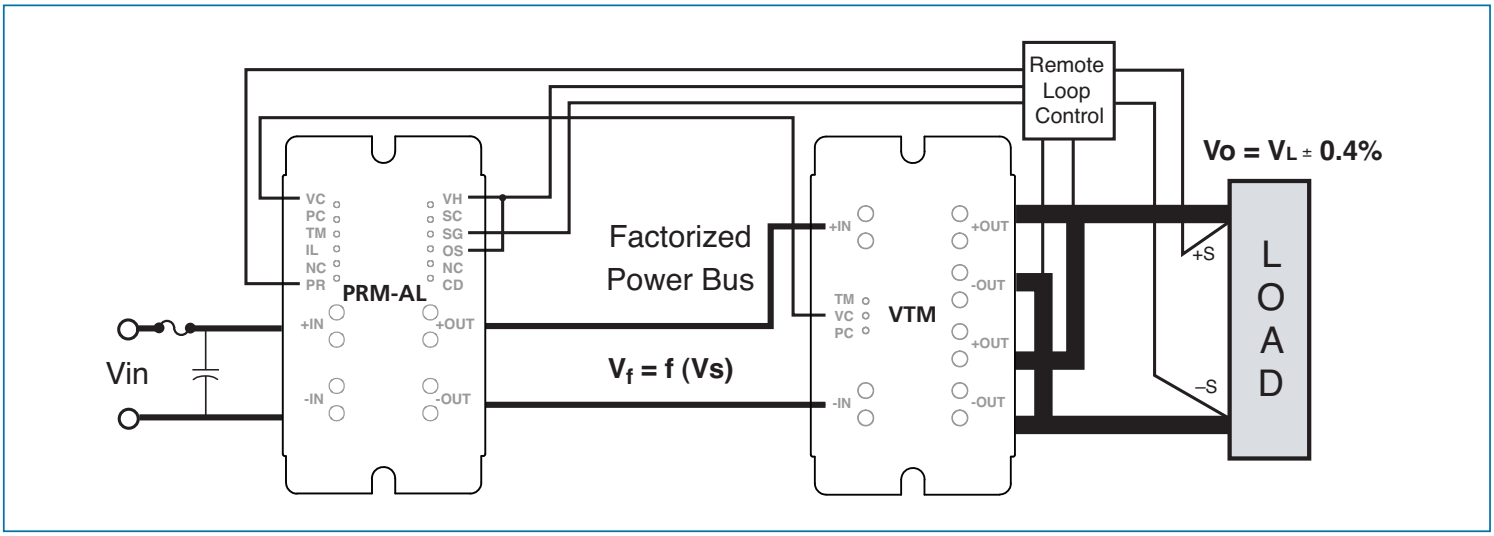


Figure 12 *— An external error amplifier or Point-of-Load IC (POLIC) senses the load voltage and controls the PRM output – the Factorized Bus – as a function of output current, compensating for the output resistance of the VTM and for distribution resistance.*

VI BRICK VTM LEVEL 1 DC BEHAVIORAL MODEL FOR 48 V TO 2 V, 80.0 A

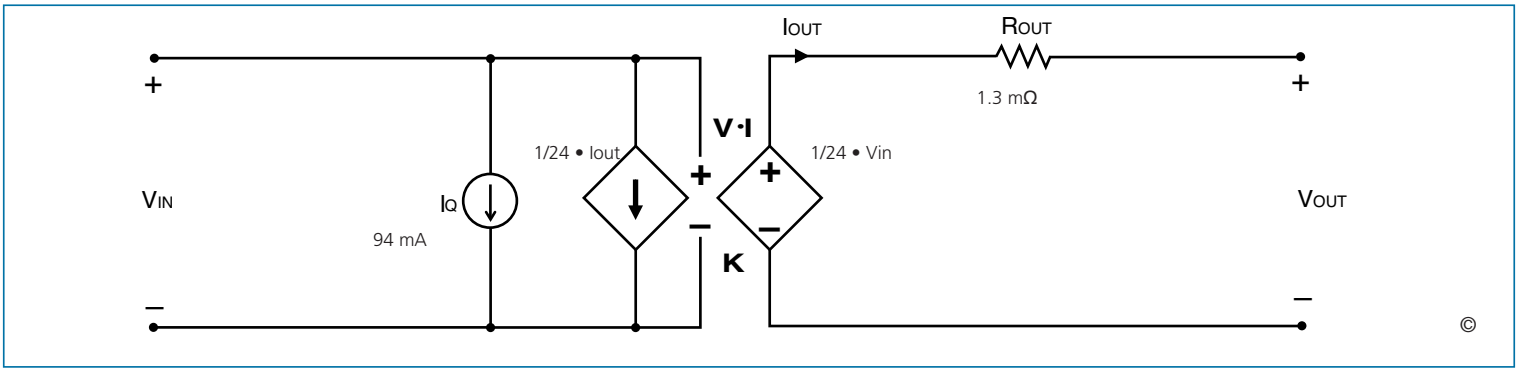


Figure 13 — This model characterizes the DC operation of the VI BRICK VTM, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.

VI BRICK VTM LEVEL 2 TRANSIENT BEHAVIORAL MODEL FOR 48 V TO 2 V, 80.0 A

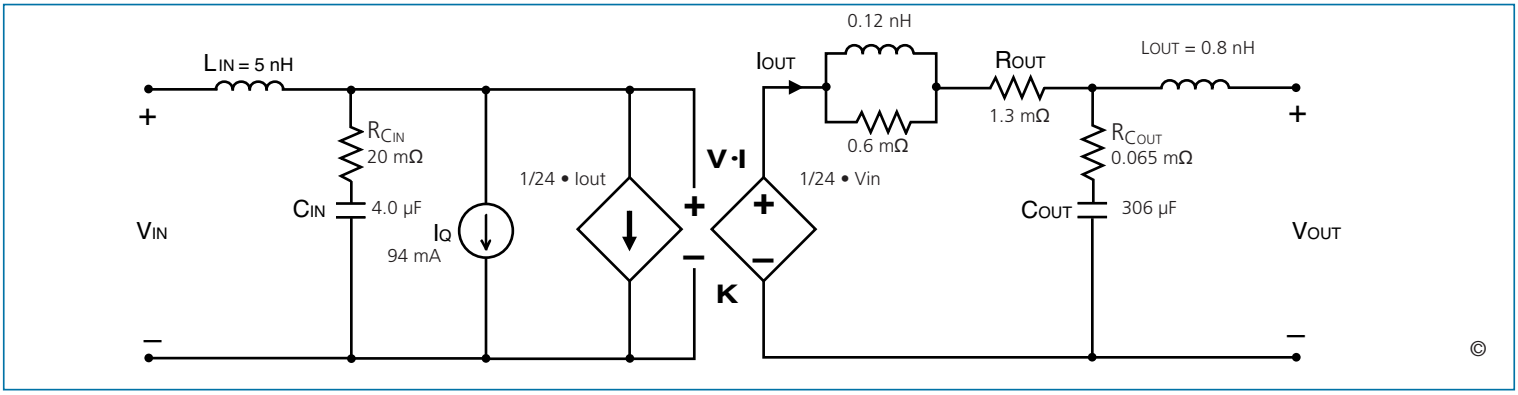
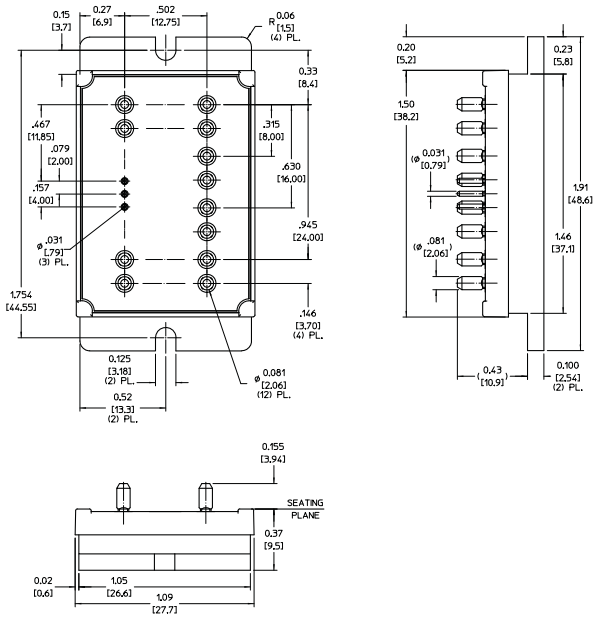
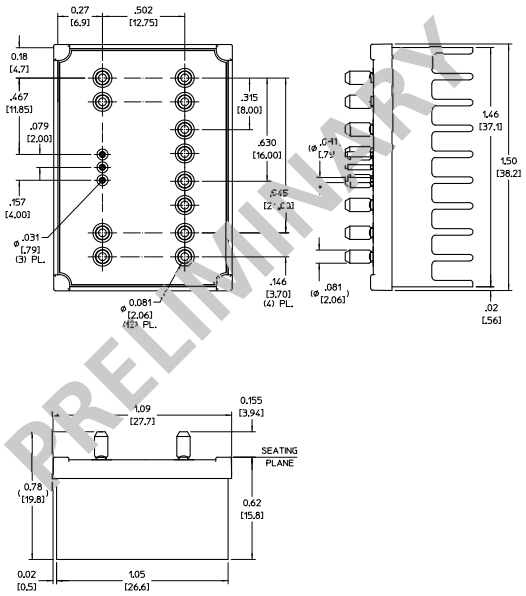


Figure 14 — This model characterizes the AC operation of the VI BRICK VTM including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.

Baseplate - Slotted Flange



Heat Sink (Transverse)



PRELIMINARY

Figure 15 — Module outline

Recommended PCB Pattern
(Component side shown)

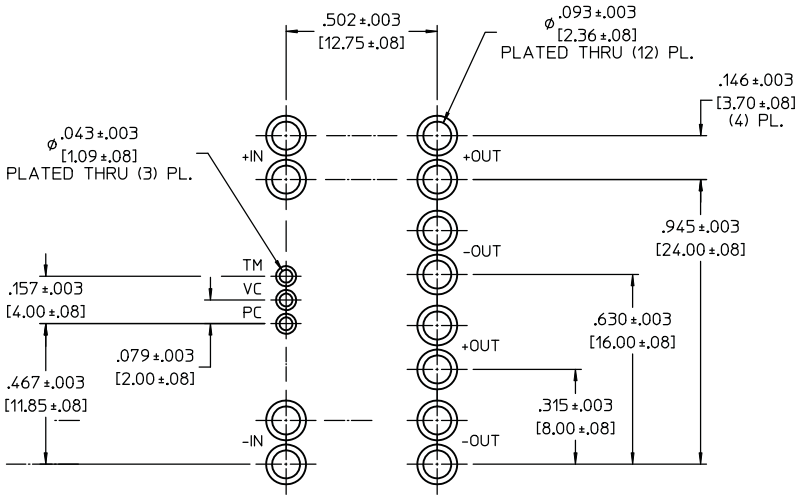


Figure 16 — PCB mounting specifications

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