VSC8256-01 Datasheet
Quad Channel 1G/10GBASE-KR to SFI Multi-Rate Multiprotocol Bi-Directional Repeater/Re-Timer/Conditioner



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1 Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Revision 4.0 was published in February 2018. The following is a summary of the changes in revision 4.0 of this document.

- Host- and line-side 10G receiver input characteristics were updated. For more information, see Table 11, page 23 and Table 12, page 24.
- Host- and line-side 10G transmitter output characteristics were updated. For more information, see Table 15, page 26 and Table 16, page 26.
- 10 Gbps transmitter 10GBASE-KR AC characteristics were updated. For more information, see Table 18, page 27.
- Host- and line-side optical 10G output jitter specifications were updated. For more information, see Table 19, page 28.
- Recommended operating conditions were updated. For more information, see Table 26, page 33.

1.2 Revision 2.1

Revision 2.1 was published in January 2018. The following is a summary of the changes in revision 2.1 of this document.

- The two-wire serial slave interface register address illustrations and 24-bit addressing scheme details were updated.
- DC characteristics for low-speed inputs and outputs were updated.
- Receiver and transmitter AC characteristics were updated.
- Reference clock AC characteristics were updated.
- The SPI interface timing diagram was updated.
- Pin descriptions were updated to correctly reflect device functionality.

1.3 Revision 2.0

Revision 2.0 was published in September 2017. It was the first publication of the document.

2 Overview

The VSC8256-01 device is part of Microsemi's SynchroPHY™ product family. It is a four channel 1G/10G serial-to-serial, protocol-agnostic repeater/retimer that integrates hardware-based host-side only 10GBASE-KR auto-negotiation and training in a small form factor, low-power FCBGA ideal for a wide array of board-level signal integrity applications.

The VSC8256-01 device provides a complete suite of on-chip instrumentation including built-in self-test (BIST) functions, line-side and client-side circuit loopbacks, pattern generation, and error detection. Its highly flexible clocking options support LAN and WAN operation using a single 156.25 MHz reference clock rate.

The VSC8256-01 device delivers excellent jitter attenuation with low power. It is well-suited for SFP+ based optical modules and direct-attach copper cabling as well as challenging backplane interface applications. As a signal conditioner, it supports protocol-agnostic data rates. It also supports 10 GbE LAN, 10 Gb WAN, 40 GbE (4 x 10G), as well as 1 Gb Ethernet.

2.1 Highlights

The following standards are supported by the device, which is programmed to operate as a protocol-agnostic signal conditioner/repeater:

- IEEE Standard 802.3ae-2002, Telecommunications and Information Exchange between Local and Metropolitan Area Networks, 10 Gbps Ethernet over fiber for LAN (10GBASE-SR, -LR, -ER, -LX4) and WAN (10GBASE-SW, -LW, and -EW)
- IEEE Standard 802.3ap-2007, Backplane Ethernet (1 and 10 Gbps over printed circuit boards)
- SFF-INF-8074i MSA for 1GbE SFP, Revision 1.0, 2001
- SFF-INF-8077i MSA for XFP, 2005, Specification for 10 Gbps Small Form Factor 10G Pluggable (XFP) Module supporting SONET OC-192 and G.709 (OTU-2), and 10 Gbps Ethernet
- SFF-8431 MSA Specification for SFP+, 2009, High- and Low-speed electrical and management interface specifications for enhanced Small Form Factor Pluggable modules and hosts

Data rates supported include:

- Ethernet 10.3125 Gbps, Ethernet 9.95328 Gbps, and Ethernet 1.25 Gbps
- OTN OTU2 (10.709 Gbps), OTU1e (11.049 Gbps), and OTU2e (11.095 Gbps)
- Support for SFP+ I/O and auto-negotiation and training for 10GBASE-KR (IEEE 802.3-2012) backplanes

2.2 Interfaces

The VSC8256-01 device provides multiple types of interfaces supporting IEEE 802.3ae and IEEE 802.3ap Ethernet connections with hardware-based 10GBASE-KR auto-negotiation and training.

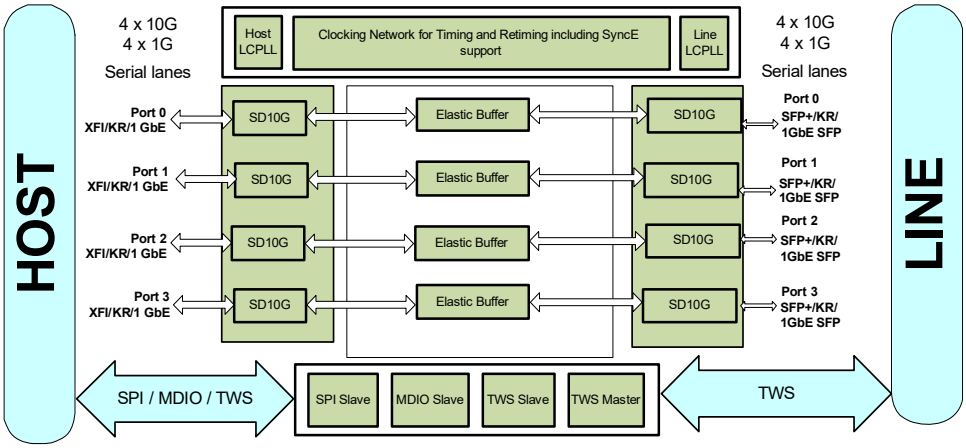
The device meets the 1 GbE SFP and SFP+ SR/LR/ER/ZR host requirements in accordance with the SFF MSA specifications and compensates for optical impairments in SFP+ applications and degradations of the PCB.

The high-speed serial input receiver compensates for loss of optical and copper media performance or margin due to inter-symbol interference (ISI). The high-speed serial transmit output features a 3-tap FIR filter output buffer fully compliant with the 10GBASE-KR standard to provide full 10GBASE-KR support, including 10GBASE-KR state machine, for auto-negotiation and link optimization. The transmit path incorporates a multitap output driver to provide flexibility to meet the demanding 10GBASE-KR (IEEE 802.3ap) Tx output launch requirements.

The serial ports support 1.25 Gbps and 10 Gbps modes. Each channel consists of a receiver (Rx) and a transmitter (Tx) subsection. Programmable reference clock inputs (HREFCK and LREFCK) support the modes along with clock and data recovery (CDR) in the Rx and Tx subsections of all channels. Each channel of the device can be in a different mode within the limitations of the available reference clocks, while ensuring the Rx and Tx subsections within a channel are in the same mode.

The following illustration shows a high-level block diagram.

Figure 1 • **Block Diagram**



2.3 Features

The main features of the VSC8256-01 device include:

- Support for protocol-agnostic repeater operation (jitter clean-up) at very low latency and power consumption
- Compliant with IEEE 802.3ae and SFF-8431 electrical (SFI) specifications
- Support for 9.95 Gbps WAN, 10.3125 Gbps LAN, and 1.25 Gbps Ethernet
- Support for standard SFP+ applications
- Support for 10GBASE-KR (IEEE 802.3ap) for 10G backplanes
- Support for ITU-T recommendation G.709 (OTN) OTU2, OTU1e, and OTU2e line rates
- Adaptive equalization receiver and programmable multitap transmitter pre-emphasis
- SPI (preferred), MDIO, and two-wire serial slave management interfaces
- VScope™ input signal monitoring integrated circuitry
- Host-side and line-side loopbacks with BIST functions
- Programmable analog signal, invert, amplitude, slew, pre-emphasis, and equalization
- Flexible clocking options
- Passive copper cable support for lowest connectivity cost

2.4 Applications

Target applications for the VSC8256-01 device include switching, IP edge router connectivity, rack mount connectivity through backplane, fiber and copper cable connectivity, and standalone server access (in LAN on motherboard designs or separate network adapters).

- Multi-port serial-to-serial signal conditioning
- 10GBASE-KR-compliant backplane transceivers
- Multi-port XFI/10GBASE-KR to SFI/SFP+ 10 GbE switch cards, router cards, and network adapters

The following figures illustrate various device applications.

Figure 2 • **SFP+ Transceiver**

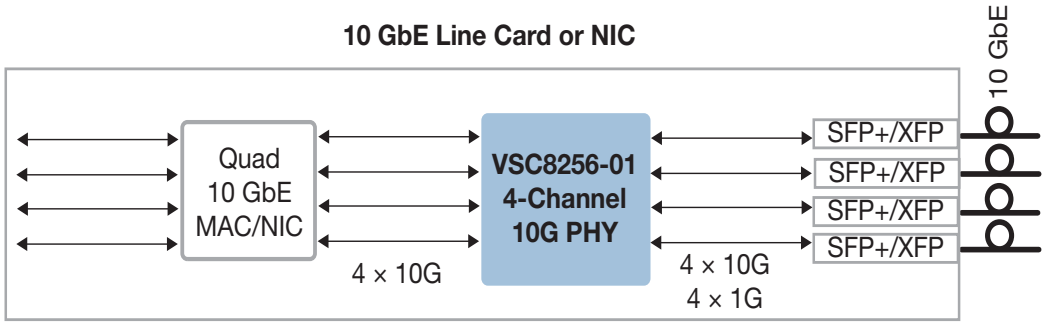
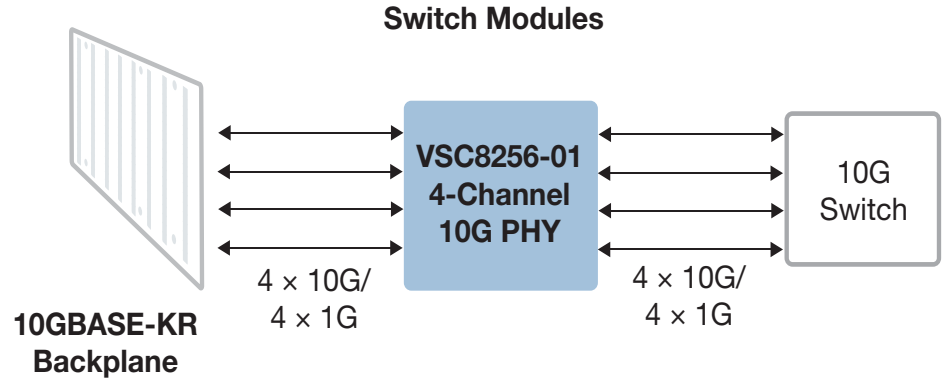


Figure 3 • **Backplane Equalization Application**



3 Functional Descriptions

This section includes a functional block diagram, information on the operating modes, and descriptions of the major functional blocks of the VSC8256-01 device.

3.1 Data Path Overview

VSC8256-01 supports a protocol agnostic Ethernet-bypass mode.

Ingress and egress data flow is relative to the line-side interface.

Both the host-side and the line-side interfaces are 10G SFI, 10GBASE-KR, or SGMII. Each lane has the following main sections.

- Line and host PMA: The PMA section contains the high speed serial I/O interfaces, an input equalization circuit, a 10GBASE-KR compliant output buffer and a SerDes. Additionally, the PMAs also generate all the clocks.
- 10GBASE-KR: Supports 10GBASE-KR training and auto-negotiation. The 10GBASE-KR driver includes programmable equalization accomplished by a three-tap finite impulse response (FIR) structure (IEEE 802.3ap compliant). Three-tap delays are achieved by three flip-flops clocked by the high speed serial clock (10G in 10G mode, 1 GHz in 1G mode). 10GBASE-KR auto-negotiation is supported on either the line side or the host side, but not both sides simultaneously.
- Loopbacks: Includes both system and network loopbacks to enhance engineering debugging and manufacturing testing capability.
- Management: Contains status and configuration registers, and the serial management interface logic to access them.

3.1.1 Ingress and Egress Operation

The VSC8256-01 can be defined as a protocol-agnostic repeater. Data is received by the line-side interface (SFP+/1 GbE), deserialized, and passed to the host-side serializer through an elastic buffer that absorbs phase jitter/wander. In this mode, the transmit (serializer) clock is required to be synchronous to the incoming recovered clock. A digital synchronization block with filtering capabilities down to the khz range is used to align the receive and transmit clocks. As a result, the input jitter is filtered completely. Each direction (ingress and egress) is identical.

The following table lists the interface data rates for the device's Ethernet mode.

Table 1 • **Repeater Interface Data Rates**

Operating Mode	Line-side Data Rate (Gbps)	Host-Side Interface	Host-Side Data Rate (Gbps)
10G LAN	1 x 10.3125	10G LAN	1 x 10.3125
1 GbE	1 x 1.25	1 GbE	1 x 1.25
10G OTU2	1 x 10.709	OTU2	1 x 10.709
10G OTU1e	1 x 11.049	OTU1e	1 x 11.049
10G OTU2e	1 x 11.095	OTU2e	1 x 11.095

3.2 Physical Media Attachment (PMA)

The PMA section consists of receiver (Rx) and transmitter (Tx) subsections. The receiver accepts data from the serial data input RXIN and sends the parallel data to the elastic buffer. A data rate clock also accompanies the parallel data. The transmitter accepts parallel data from the elastic buffer and transmits at serial data output TXOUT. A loopback at the data path is also provided to connect the Rx and the Tx subsections.

To support different data rates, each PMA contains a flexible frequency synthesizer that generates the necessary clocks. The PMA also has four fully programmable clock outputs, CKOUT[0:3], that may be used to output various clock domains from the PMA.

3.2.1 Reference Clock

The VSC8256-01 device uses differential input CML level reference clocks. LREFCK and HREFCK are required at all times and have to be synchronous. They may be 125 MHz or 156.25 MHz. This rate must be selected at power-up using the MODE[1:0] pins. LREFCK and HREFCK are multiplied to generate the reference clocks for all the SerDes blocks in the line and host-side interfaces respectively.

The following table shows the MODE pin settings for the various LREFCK frequencies.

Table 2 • **Selecting LREFCK Frequency**

MODE1 Pin	MODE0 Pin	Frequency
0	0	156.25 MHz (default)
1	0	125 MHz

3.2.2 VScope™ Input Signal Monitoring Integrated Circuit

The VScope™ input signal monitoring integrated circuit displays the input signal before it is digitized by the CDR. The two primary configurations are as follows:

- Unity Gain Amplifier monitors the 10 Gbps input signals before signal processing and equalization. VScope input signal monitoring integrated circuit acts as a virtual scope to effectively observe the received data signal before it has been processed. The autonomous adaptive filter taps must first be disabled and the front-end receiver must be set for operation as a linear, unity gain amplifier. In this mode, all DFE taps are set to zero. This mode does not require an adaptive algorithm.
- Link Monitor provides the link margin. VScope input signal monitoring integrated circuit enables design engineers and system developers to monitor signals remotely without disrupting the data integrity of a live data path. By monitoring the health of a given link, optical or electrical, various types of signal degradation can be identified and corrected.

Note: The VScope input signal monitoring integrated circuit feature is only available in the 10G operation mode.

3.2.3 10GBASE-KR

The VSC8256-01 device implements the 10GBASE-KR standard in hardware with no additional firmware requirement for 10GBASE-KR backplane rate auto-negotiation and link training per IEEE 802.3 clause 72 and 73. The 10GBASE-KR output driver itself may be used outside the 10GBASE-KR backplane application and is set by programming the registers.

3.2.3.1 Rate Auto-Negotiation

The VSC8256-01 device supports auto-detection between 1.25 Gbps and 10.3125 Gbps data rates, according to the IEEE 802.3ap Clause 73. The auto-negotiation/auto-detection feature switches the CRU rate selection to different rates.

Rate auto-negotiation enables devices at both ends of a link segment to advertise abilities, acknowledge receipt, and discover the common modes of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The auto-negotiation function allows the devices to switch between the various operational modes in an orderly fashion, permits management to disable or enable the auto-negotiation function, and allows management to select a specific operational mode. The auto-negotiation function also provides a parallel detection function to allow backplane Ethernet devices to connect to other backplane Ethernet devices that have auto-negotiation disabled and interoperate with legacy devices that do not support Clause 73 Auto-Negotiation.

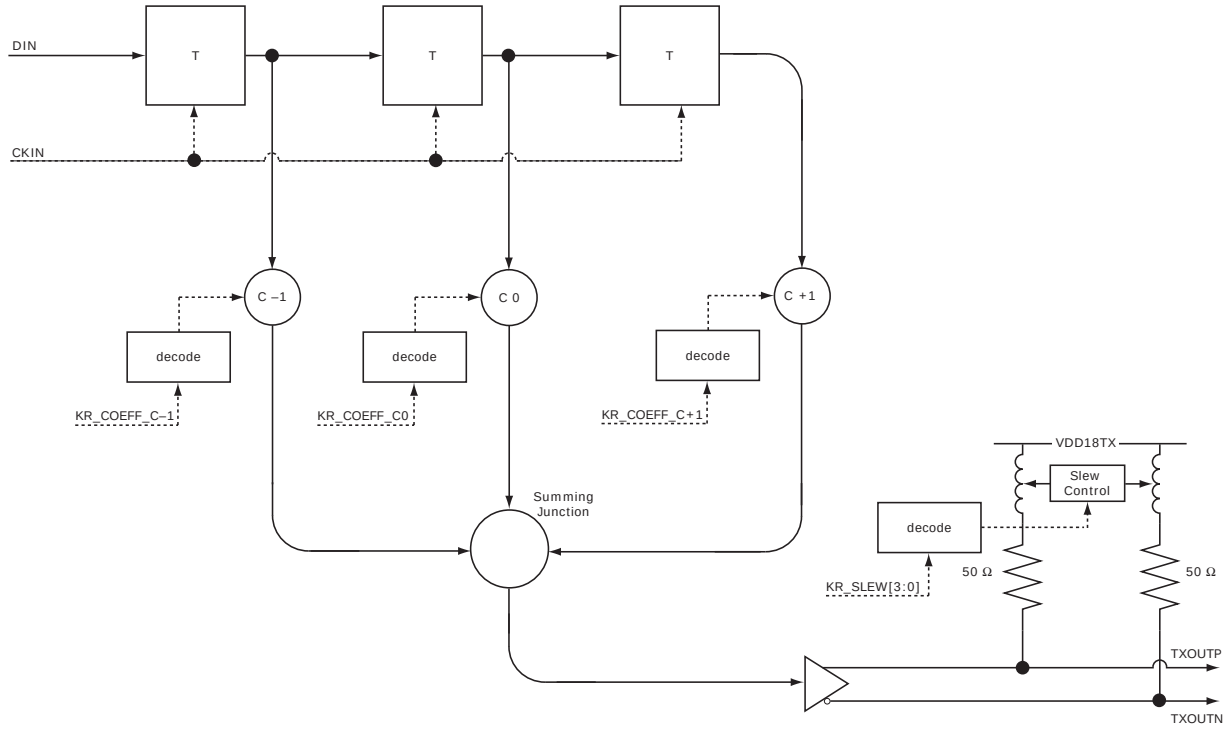
3.2.3.2 Training

The purpose of training is to establish optimal settings for the VSC8256-01 device and the link partner. For more information about the training function, see IEEE 802.3ap Clause 72.

3.2.3.3 Output Driver

The high-speed output driver includes programmable equalization accomplished by a three-tap finite impulse response (FIR) structure. The three-tap delays are achieved by three flip-flops clocked by a high-speed serial clock, as shown in the following illustration. Coefficients C(–1), C(0), and C(+1) adjust the pre-cursor, main-cursor, and post-cursor of the output waveform. The three delayed data streams, after being properly strength adjusted by their coefficients, are summed by a summing amplifier. The output driver meets the requirements defined in IEEE 802.3ap Clause 72.

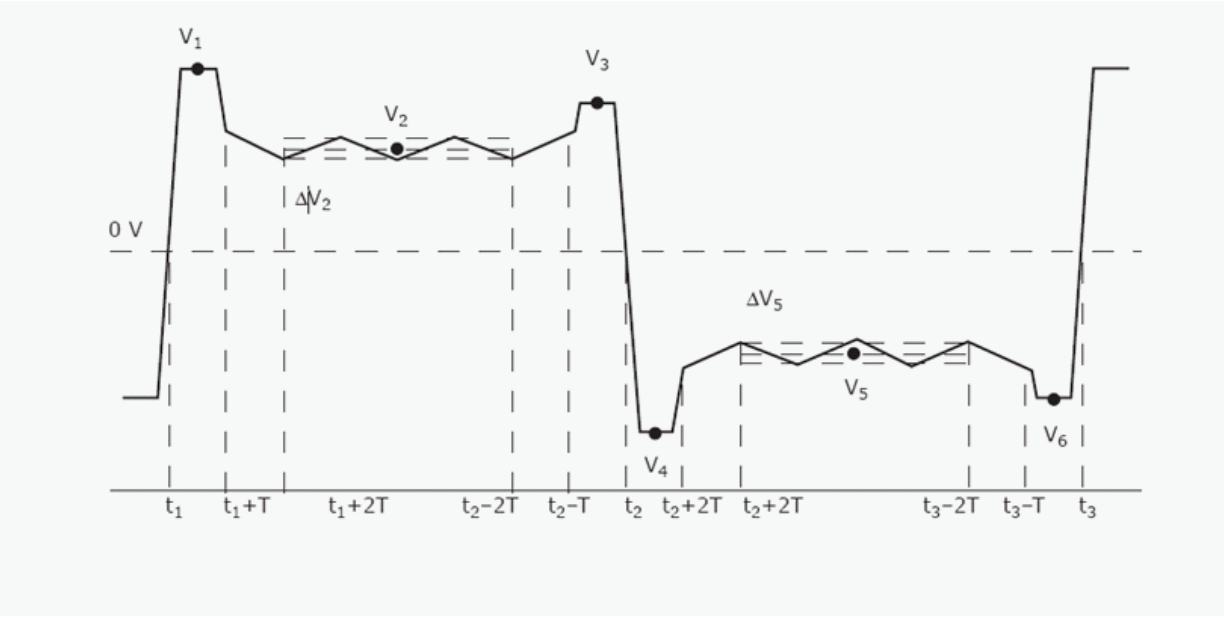
Figure 4 • **10GBASE-KR Output Driver**



The final output stage has 50 Ω back-termination with inductor peaking. The output slew rate is controlled by adjusting the effectiveness of the inductors.

The test pattern for the transmitter output waveform is the square wave test pattern with at least eight consecutive 1s. The following illustration shows the transmitter output waveform test, based on voltages V1 through V6, ΔV2, and ΔV5.

Figure 5 • **10GBASE-KR Test Pattern**



The output waveform is manipulated through the state of the coefficient C(-1), C(0), and C(+1).

3.3 Loopback

The following table shows the name and location of the loopback modes. These modes may be extremely useful for both test and debug purposes.

Table 3 • **Line-Side Loopback**

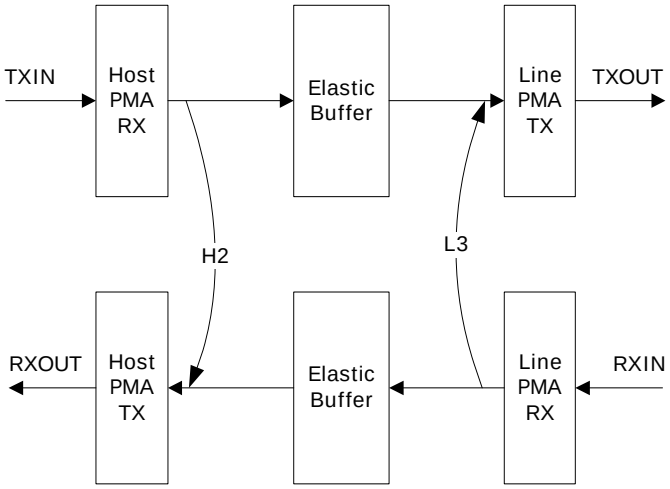
Name	Location
L3	Line PMA interface (1G and 10G)

Table 4 • **Host-Side Loopback**

Name	Location
H2	Host PMA interface (1G and 10G)

The following illustration shows the host and line-side loopbacks.

Figure 6 • **Host-Side and Line-Side Loopbacks**



3.4 Elastic Buffer

The transmit clock on each side is synchronized to the recovered clock on the opposite side through a low-pass filter. A small, elastic buffer in each direction in each channel is added to compensate for the inherent phase variation between these two clocks.

3.5 Host-Side Interface

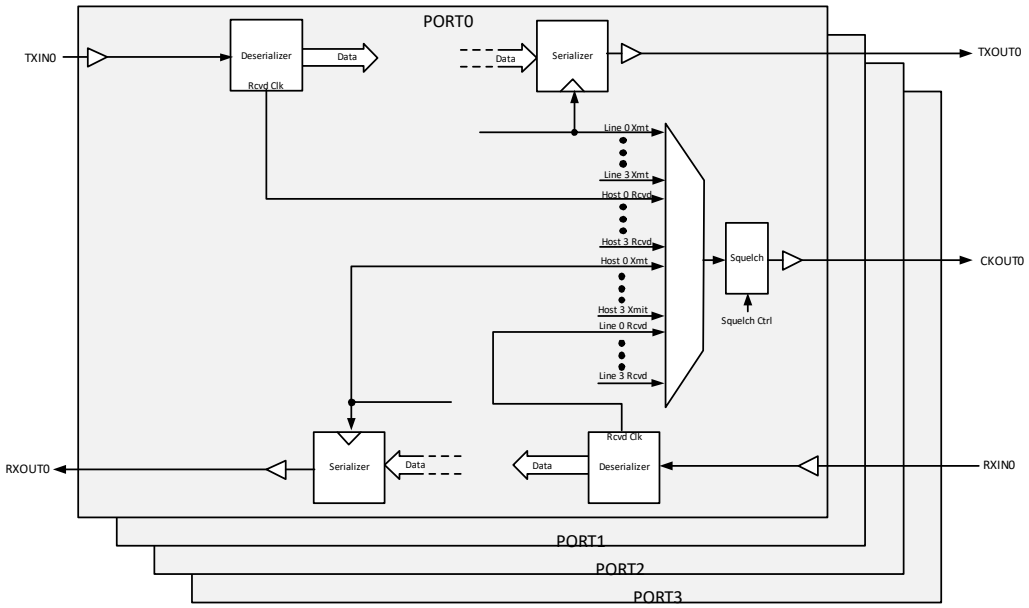
The host interface of VSC8256-01 consists of the same PMA block utilized on the line side. This interface has the same capabilities and feature set as the line side PMA discussed earlier.

3.5.1 Output Clocks

Four output clocks (CKOUT[0:3]) are available to drive legacy optics or any other purpose. Each output clock can be independently configured to source any of the recovered clocks or transmit clocks.

The following illustration shows the per-port clock outputs.

Figure 7 • **Per-Port Clock Outputs**



The rate of these clocks is the line rate divided by 32 or 64 (322.27 MHz or 161.13 MHz in 10G LAN mode, for example).

3.6 Table 2, page 6 Table 2, page 6Table 2, page 6Management Interfaces

This section contains information about the low-speed serial interfaces of the VSC8256-01 device. The primary control and monitor interfaces in the design are as follows:

- MDIO
- SPI slave
- Two-wire serial (slave)
- Two-wire serial (master)
- GPIO
- JTAG

The VSC8256-01 device supports three different interfaces for accessing status and configuration registers: MDIO, SPI slave, and two-wire serial slave. Only one of the interfaces can be active at a time. The VSC8256-01 device doesn't arbitrate between these interfaces. Users must exercise caution and ensure that multiple interfaces are not active at the same time.

The SPI slave interface is the recommended interface for accessing the status and configuration registers

The VSC8256-01 device registers are arranged according to the MDIO devices as defined in IEEE 802.3 clause 45, as shown in the following list:

- Device 1: Line PMA and line interface registers
- Device 4: Rate compensating registers
- Device 7: Line 10GBASE-KR registers
- Device 9: Host PMA and host interface registers
- Device F: Host 10GBASE-KR registers
- Device 1E: Global, SFP+, PLLs, GPIOs

3.6.1 MDIO Interface

The MDIO interface in the VSC8256-01 device complies with IEEE 802.3ae Clause 45. For more information, see the IEEE standard. The MDIO management interface consists of a bi-directional data path (MDIO) and a clock reference (MDC).

MDIO instructions can be used to read registers, write registers, and perform post-read-increment-address instructions. Due to its slow bandwidth and high latency, the MDIO interface is not recommended as the only interface to access the VSC8256-01 device.

Note: The maximum data rate of the MDIO interface is 2.5 Mbps.

The PADDR[4:2] pins select the MDIO port addresses to which the VSC8256-01 device will respond. A single VSC8256-01 device requires the use of four MDIO port addresses, one for each channel. The port address transmitted in MDIO read/write commands to access registers in a particular VSC8256-01 channel is shown in the following table. The port address is a function of the PADDR pins and a pre-programmed number indicating the channel number. Up to eight VSC8256-01 devices can be controlled by a single MDIO host.

Table 5 • **MDIO Port Addresses Per Channel**

Channel Number	Channel's Port Address
3	{PADDR[4:2], 11}
2	{PADDR[4:2], 10}
1	{PADDR[4:2], 01}
0	{PADDR[4:2], 00}

3.6.1.1 Accessing 32-Bit Data Registers

Even though the MDIO interface is defined to access 16-bit data registers, 32-bit configuration and status registers are present in the line and host MACs in 1G mode and line-side SerDes. Use the following steps when accessing registers in 32-bit blocks.

3.6.1.1.1 Write to 32-Bit Register

1. Issue address instruction specifying the MDIO address for bits [31:16].
2. Issue write instruction to write data to register bits [31:16].
3. Issue address instruction specifying the MDIO address for bits [15:0].
4. Issue write instruction to write data to register bits [15:0].

Note: Writing to the two halves of the 32-bit register in the opposite order is not permitted. Nor is it possible to write to only one-half of the register. All four MDIO instructions must be issued to write to a 32-bit register.

3.6.1.1.2 Read 32-Bit Register

1. Issue address instruction specifying the MDIO address for bits [15:0].
2. Issue read-increment instruction. The data read is the contents of register bits [15:0].
3. Issue read instruction. The data read is the contents of register bits [31:16].

Note: Perform all three steps to read a 32-bit register even when reading consecutive addresses. Issuing back-to-back read-increment instructions to read consecutive 32-bit register addresses is not supported.

Register addresses listed for the line and host MACs and SerDes apply to the SPI slave and two-wire serial slave interfaces, which support direct access to 32-bit data registers. There are two MDIO addresses for each of these 32-bit data registers: one address to access data bits [31:16] and one address to access data bits [15:0]. Contact Microsemi for support using the MDIO interface to access line and host MACs and SerDes registers.

3.6.2 SPI Slave Interface

The VSC8256-01 device supports the serial peripheral interface (SPI) for reading and writing registers for high bandwidth tasks. The SPI interface is also capable of accessing all status and configuration registers. The SPI slave port consists of a clock input (SCK), data input (MOSI), data output (MISO), and slave select input (SSN).

Note: The SPI slave interface is the recommended interface to access status and configuration registers for the rest of the device.

Drive the SSN pin low to enable the interface. The interface is disabled when SSN is high and MISO is placed into a high impedance state. The VSC8256-01 device captures the state of the MOSI pin on the rising edge of SCK. 56 data bits are captured on the MOSI pin and transmitted on the MISO pin for each SPI instruction. The serial data bits consist of 1 read/write command bit, 23 address bits, and 32 register data bits.

The 23-bit addressing scheme consists of a 2-bit channel number, a 5-bit MDIO device number, and a 16-bit register number. For example, the 23-bit register address for accessing the GPIO_0_Config_Status register in channel 1 (device number is 0x1E and register number is 0x0100) is 0x3E0100. The notion of device number conforms to MDIO register groupings. For example, device 1 is assigned to WIS registers.

The following table shows the order in which the bits are transferred on the interface. Bit 55 is transferred first, and bit 0 is transferred last. This sequence applies to both the MOSI and MISO pins.

Table 6 • **SPI Slave Instruction Bit Sequence**

Bit	Name	Description
55	Read/Write	0: Read 1: Write

Table 6 • **SPI Slave Instruction Bit Sequence *(continued)***

Bit	Name	Description
54:53	Port/Channel Number	00: Port/Channel 0 01: Port/Channel 1 10: Port/Channel 2 11: Port/Channel 3
52:48	Device Number	5-bit device number Bit 4 corresponds to SPI instruction bit 52 Bit 0 corresponds to SPI instruction bit 48
47:32	Register Number	16-bit register number Bit 15 corresponds to SPI instruction bit 47 Bit 0 corresponds to SPI instruction bit 32
31:0	Data	32-bit data Bit 31 corresponds to SPI instruction bit 31 Bit 0 corresponds to SPI instruction bit 0

The register data received on the MOSI pin during a write operation is the data value to be written to a VSC8256-01 register. Register data received on the MOSI pin during a read operation is not used, but must still be delivered to the device.

The VSC8256-01 device SPI slave has a pipelined read process. Two read instructions must be sent to read a single register. The first read instruction identifies the register address to be read. The MISO data transmitted on the second read instruction contains the register contents from the address specified in the first instruction. While a pipelined read implementation is not the most efficient use of bandwidth to read a single register, it is very efficient when performing multiple back-to-back reads. The second read instruction contains the address for the second register to be read plus the data read from the first register. The third read instruction contains the address for the third register to be read plus the data read from the second register. Register reads can continue in this fashion indefinitely. The following illustrations show the situations where back-to-back read instructions are issued.

Figure 8 • **SPI Single Register Read**

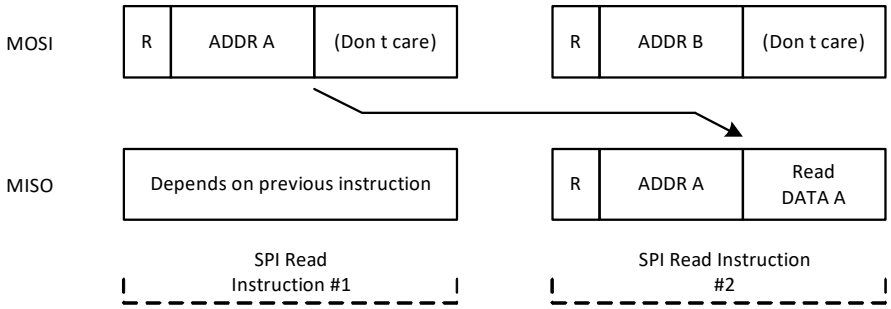
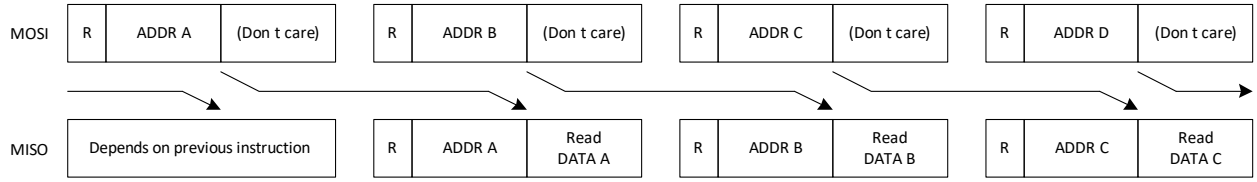
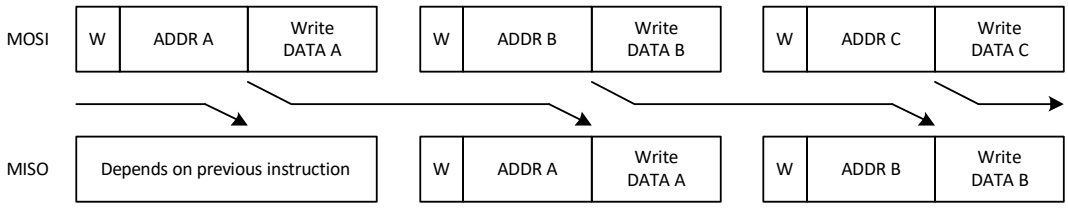


Figure 9 • **SPI Multiple Register Reads**



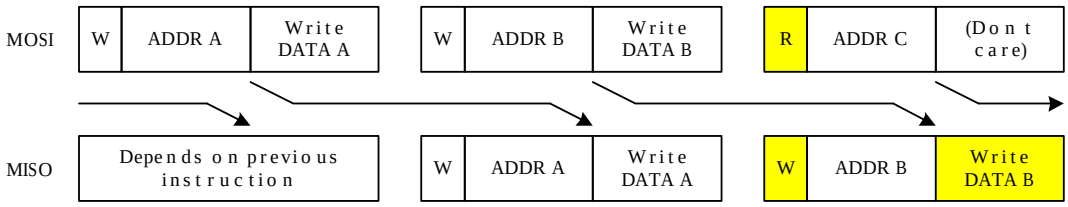
The SPI read instruction figures also point out the read/write state and address bits on the MISO output match the information received in the previous instruction. The SPI master could use this data to verify the device captured the previous instruction properly, or simply ignore the data. The following illustration shows the MISO output during write instructions reporting the previous instruction's read/write state, address, and register write data.

Figure 10 • **SPI Multiple Register Writes**



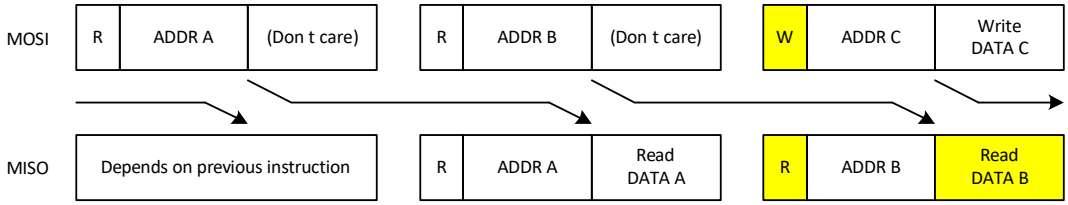
The following illustration shows that when a read instruction follows a write instruction, the MISO data during the read instruction is the data field from the previous write.

Figure 11 • **SPI Read Following Write**



The following illustration shows that when a write instruction followings a read instruction, the MISO data during the write instruction is not pipelined read data. MISO contains all 0's in the data field.

Figure 12 • **SPI Write Following Read**



Some VSC8256-01 registers are made up of less than 32 data bits. Any bits not defined for a register will return a 0 when the register is read. Reading an invalid register address will return 0x0.

There is one hazard condition to be aware of when issuing two read instructions to read a single clear-on-read register. Issuing two read instructions internally fetches data twice even though valid read data is present only in the second instruction. Fetching data also resets a clear-on-read register. The address specified in the second read instruction should be something other than the clear-on-read register address. This prevents an event causing register re-assertion occurring between the two read instructions from being cleared and never detected. The address in the second instruction can be any register not having a clear-on-read function. Device_ID is one example. The same address can be used in each read instruction when continuously polling a clear-on-read register. This works because subsequently fetched data is transmitted from the interface allowing assertion between reads to be detected. Only the last read instruction where fetched data is not transmitted should some other address in the instruction be used.

3.6.2.1 MISO Output Timing Modes

MISO changes state when SCK transitions from high to low in the default SPI operating mode. This aids in meeting hold time at the SPI master assuming the master captures the data on the rising SCK edge. The SPI port can run up to a maximum of 30 Mbps depending upon the VSC8256-01 device SCK-to-MISO timing, MISO loading SCK duty cycle, the board layout, and the external SPI master's interface timing requirements. For more information about SPI timing, see Table 25, page 31.

The SPI slave port has an alternate operating mode that allows the interface to run faster. Setting register bit SPI_CTRL.FAST_MODE=1 configures the SPI slave such that MISO changes state when SCK transitions from low to high. Thus, data is both transmitted from the SPI slave and captured by the SPI master on a rising SCK edge. The interface can run faster in this mode by using the entire SCK clock period instead of half the period to transfer data from the slave to the master. Care must be taken to

ensure the SPI master's hold time requirement is met. The following illustrations show MISO timing in the default and slave modes.

Figure 13 • **SPI Slave Default Mode**

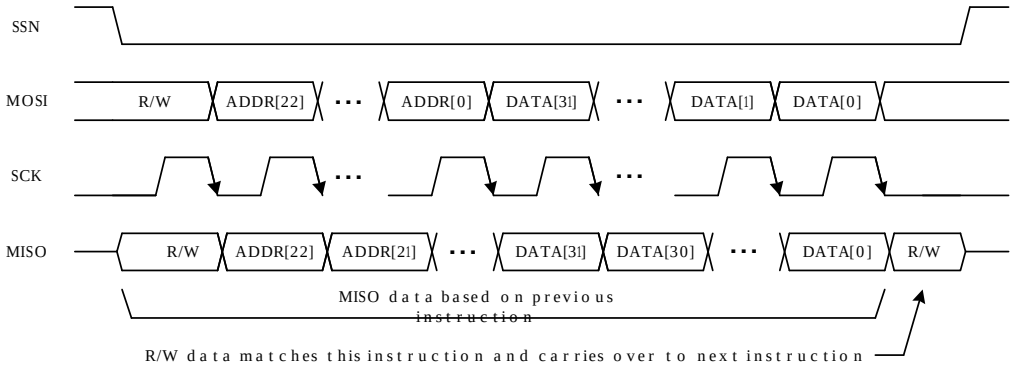
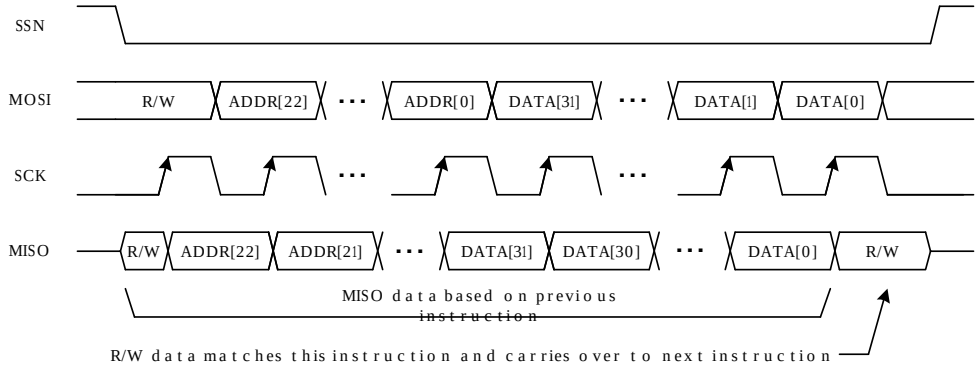


Figure 14 • **SPI Slave Fast Mode**



MISO output timing is the only difference between the two SPI modes. Sampling of MOSI on the rising SCK clock edge remains the same so writing to the VSC8256-01 device registers is identical in both modes. Thus the SPI_CTRL.FAST_MODE register setting may be modified using the SPI slave port to change the port's MISO output timing.

3.6.3 Two-Wire Serial (Slave) Interface

The VSC8256-01 device registers may be read and written using a two-wire serial slave interface. The two-wire serial slave SCL and SDA pins are multifunction general purpose I/O (GPIO) pins, GPIO_33 and GPIO_32, respectively. The GPIO pins are configured to serve SCL and SDA functions following device reset.

The slave address assigned to the VSC8256-01 device. is a function of four fixed values and the MDIO port address pins. The 7-bit slave address is {1000, PADDR4, PADDR3, PADDR2}. The use of the port address pins allows multiple VSC8256-01 devices to be serviced by a single two-wire serial (master). The maximum data transfer rate for the interface is 400 kbps.

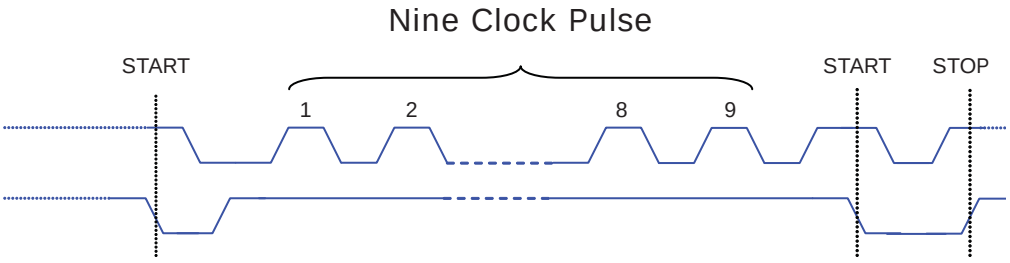
Note: The two-wire serial slave interface does not work with two-wire serial masters using 10-bit slave addresses.

A valid START condition is generated by a two-wire serial master device by transitioning the SDA line from high to low while the SCL line is high. Data is then transferred on the SDA line, most significant bit (MSB) first, with the SCL line clocking data. Data transitions during SCL low periods are valid (read) or latched (write) when SCL pulses high then low. Data transfers are acknowledged (ACK) by the receiving device for data writes and by the master for data reads. An acknowledge is signaled by holding the SDA signal low while pulsing SCL high then low. The master terminates data transfer by generating a STOP condition by transitioning SDA low to high while SCL is high.

Note: If the external two-wire serial master device gets out of sync with the two-wire serial slave interface, the master device must issue a bus reset sequence. This puts the two-wire serial slave interface back into a state that allows it to receive future two-wire serial instructions. The external two-wire serial master device and the two-wire serial slave interface can become out-of-sync and freeze the bus if either device is reset during an instruction.

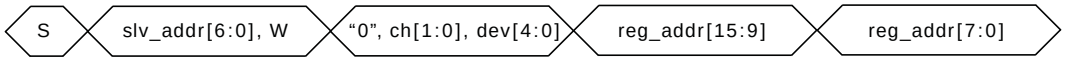
The following illustration shows a two-wire serial bus reset sequence. The reset sequence consists of a START symbol, nine SCK clock pulses while SDA is high, another START symbol, and a STOP symbol.

Figure 15 • **Two-Wire Serial Bus Reset Sequence**



Registers in the VSC8256-01 device are accessed using the 24-bit addressing scheme. The first 8 bits consist of one logic LOW, the channel number (00, 01, 10, 11), and the 5-bit MDIO device number of the register to be accessed. The next 16 bits are the register number. For example, the 24-bit register address for accessing the GPIO_0_Config_Status register in channel 1 (device number 0x1E and register number 0x0100) is 0x3E0100. The notion of device number conforms to MDIO register groupings. For example, device 2 is assigned to WIS registers. The following illustration shows the 24-bit addressing scheme used to access registers.

Figure 16 • **Two-Wire Serial Slave Register Address Format**

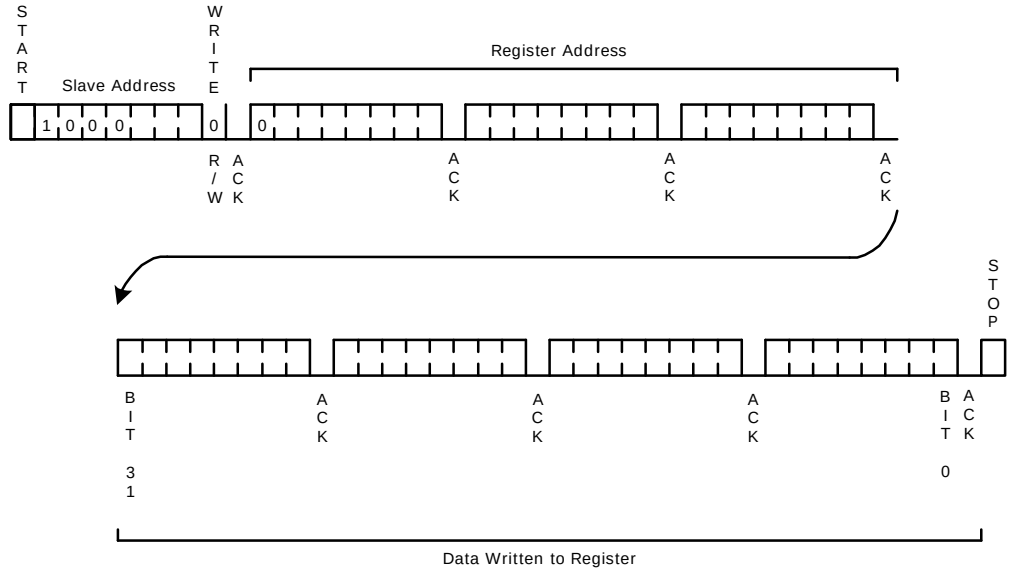


An illegal two-wire serial slave read instruction to an invalid channel number, device number, or register address will return a read value of 0x0000 when the slave address matches this device.

Four bytes of data are transferred on the two-wire serial bus after the address when a register is read or written. Data register bits [31:24] are transferred first, followed by bits [23:16], bits [15:8], and finally bits [7:0]. An ACK symbol is sent between each byte of data. Any bits not defined in a register will return a 0 when the register is read.

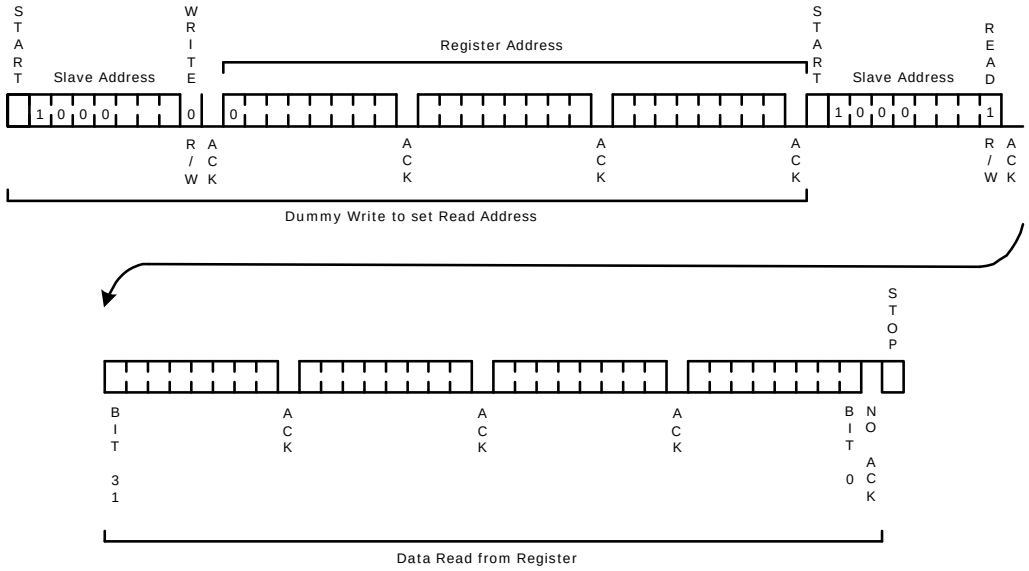
The following illustration shows the data transferred on the SDA pin during a register write operation. The R/W bit following the slave address is set to logic low to specify a write operation.

Figure 17 • **Two-Wire Serial Write Instruction**



The register address to be accessed is specified by initiating a write operation. After the slave address and three register address bytes are sent to the VSC8256-01 device, a START condition must be re-sent, followed by the slave address with the read/write bit set to logic high. The four-byte data register contents are then transmitted from the VSC8256-01 device. The two-wire serial (master) sends NO ACK after the fourth data byte to indicate it has finished reading data. The following illustration shows data transferred on the SDA pin during a register read operation.

Figure 18 • **Two-Wire Serial Read Instruction**



The two-wire serial slave interface supports sequential read and sequential write instructions.

3.6.4 Two-Wire Serial (Master) Interface

A two-wire serial master interface in the VSC8256-01 channel is available for SFP+/XFP module management. A two-wire serial master interface per channel is required because the slave address in the optics modules are identical. Two-wire serial interface instructions used to access optics module registers are initiated by writing to VSC8256-01 registers. The two-wire serial interface busses are brought out through GPIO pins by configuring the desired GPIO pins to function as SDA and SCL.

The two-wire serial master interface must be configured before initiating any instructions. The slave ID to be transmitted in the first byte of every instruction is selectable in the SLAVE_ID register. The default setting is 0x50. The interface's data rate is determined by the PRESCALE register. The default data rate is 400 kbps.

The two-wire serial master transmits instructions for slave devices with 8-bit data registers and 256 register addresses per slave ID. Always read register I2C_BUS_STATUS.I2C_BUS_BUSY or I2C_READ_STATUS_DATA.I2C_BUS_BUSY to verify the previous instruction has finished prior to initiating a new instruction. Instructions initiated when the interface is busy will be ignored. Both registers report the same interface busy status. The same busy status is reported in two registers for user convenience.

The two-wire serial master initiates a write instruction when the I2C_WRITE_CTRL register is written. The value written to I2C_WRITE_CTRL.WRITE_ADDR is the register address to be modified in the slave device. The value written to I2C_WRITE_CTRL.WRITE_DATA is the data to be written to the slave device's register. The I2C_BUS_STATUS register reports the status of the write instruction. I2C_BUS_STATUS.I2C_BUS_BUSY indicates when the instruction has finished. I2C_BUS_STATUS.I2C_WRITE_ACK=1 means the two-wire serial master received ACKs from the slave at appropriate times. I2C_BUS_STATUS.I2C_WRITE_ACK is cleared each time a new instruction is issued. If the two-wire serial master did not receive ACKs from the slave at appropriate times (I2C_BUS_STATUS.I2C_WRITE_ACK=0), the interface is likely stuck in a state waiting for the ACK. Writing a 1 to the BLOCK_LEVEL_RESET1.I2CM_RESET register will reset the two-wire serial master and release it from its stuck state. The slave device should then be put into a known state by writing any value to the I2C_RESET_SEQ register. The two-wire serial master issues a bus reset sequence when this register is written. For more information, see Two-Wire Serial (Slave) Interface, page 14.

The two-wire serial master initiates a read instruction when the I2C_READ_ADDR register is written. The value written to I2C_READ_ADDR.READ_ADDR is the register address to be accessed in the slave device. I2C_READ_STATUS_DATA.READ_DATA contains the data read from the slave device. READ_DATA is not valid until I2C_READ_STATUS_DATA.I2C_BUS_BUSY=0 to indicate the instruction completed. The two-wire serial master does not support read-increment instructions.

3.6.5 JTAG

The VSC8256-01 device has an IEEE 1149.1–2001 compliant JTAG interface. The following table shows the supported instructions and corresponding instruction register codes. The code's least significant bit is shifted into TDI first when loading an instruction (the 0 is shifted in first when loading the IDCODE instruction).

Table 7 • **JTAG Instructions and Register Codes**

Instruction	Register Code	Notes
IDCODE	111111111111111111111110	
BYPASS	111111111111111111111111	
EXTEST	111111111111111111101000	
EXTEST_PULSE	111111101111111111101000	
EXTEST_TRAIN	111111011111111111101000	
SAMPLE	111111111111111111111000	
PRELOAD	111111111111111111111000	
LV_HIGHZ	111111111111111111001111	Provides the ability to place outputs in a high impedance state to facilitate manufacturing test and PC board diagnostics. The SFP+ serial data outputs are not put into the high impedance state when this instruction is loaded in the JTAG TAP controller.

Table 7 • **JTAG Instructions and Register Codes *(continued)***

Instruction	Register Code	Notes
CLAMP	11111111111111111111101111	Provides the ability to place all outputs in a predefined state when the scan process is being used to test other devices on a PC board.

3.6.6 General Purpose I/O

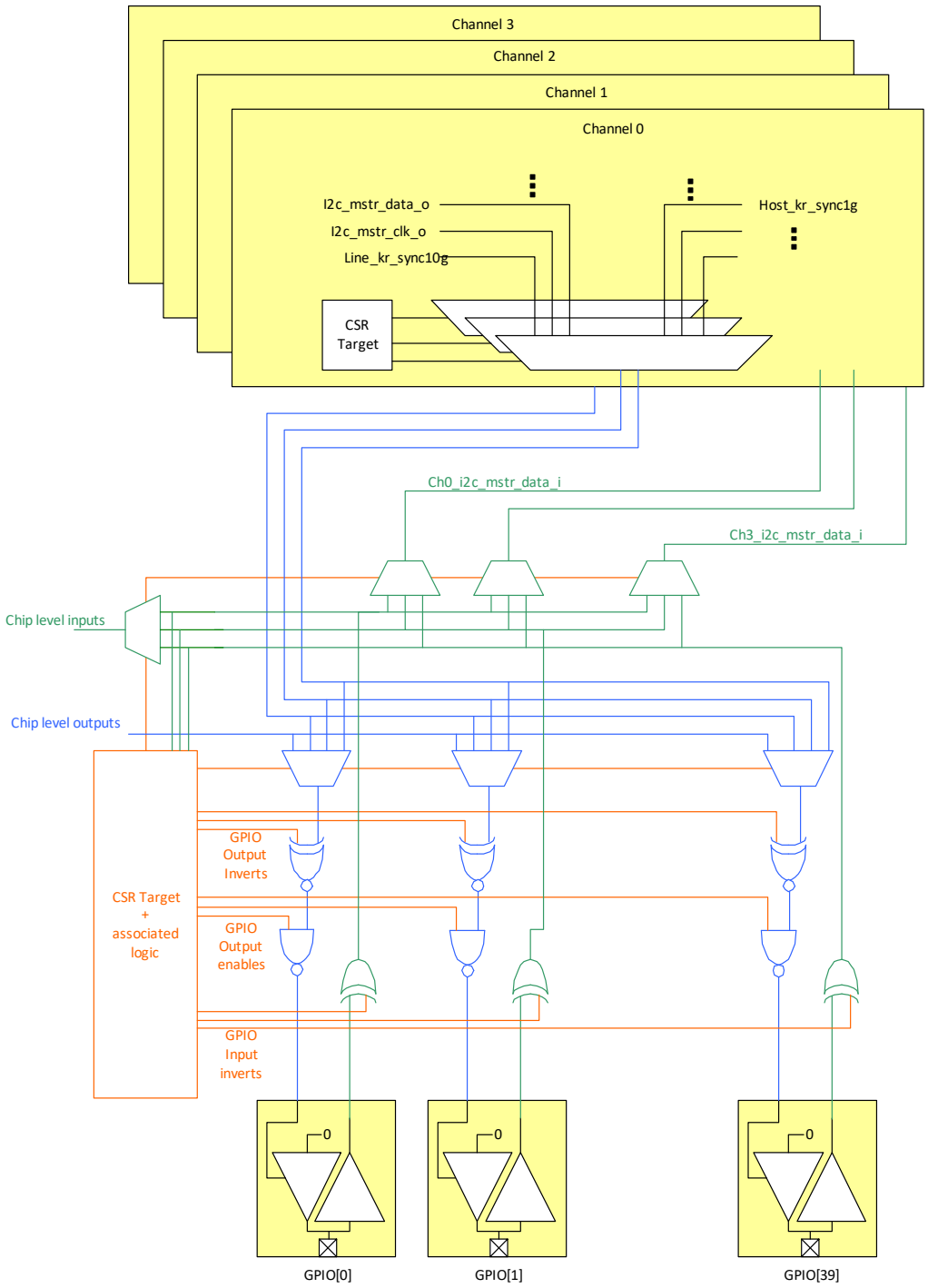
The general purpose I/O (GPIO) functions are organized into 2 groups: per-channel functions and global functions. Per-channel functions include an I2C master (often used for communicating with a module), host and line link status indications. Global functions include interrupt generation logic, an I2C slave interface, and other miscellaneous I/O configuration and control.

The 40 pins associated with the GPIO functionality are configurable; any function can be mapped to any GPIO pin. The only restriction is that for each channel, only 8 of the per-channel GPIO output functions may be used at a time.

All GPIOs are configured for open-drain operation, so if used as an output, they must have pull-up resistors connected.

The following block diagram shows the GPIO scheme.

Figure 19 • **GPIO Block Diagram**



3.6.6.1 Inputs

The input state of the GPIO pins can be routed to any of GPIO input functions in each channel, or to any of the global functions. The multiplexors for each of these functions may select any of the GPIOs, or a “0” or “1” to force the function input to a known state.

By default, GPIO32 and GPIO33 are routed to the I2C slave input data and input clock, respectively.

The current state of each GPIO input can be read, and a sticky bit corresponding to each GPIO input indicates if it has changed state. These may be useful for monitoring module status signals such as MOD_ABS, TWS_INTERRUPT, and so on.

3.6.6.2 Outputs

A set of eight multiplexors in each channel select the per-channel output functions that are routed out to each of the eight per-channel virtual GPIO outputs. These multiplexors are configured using the configuration/status module in the channel. A second level of multiplexing occurs at the GPIO pin itself, where the individual per-channel virtual outputs, as well as chip level output functions, are associated with a particular GPIO output.

There are additional chip-level functions (such as interrupts) that may also be assigned to a GPIO pin. Each output may also be configured to drive a static low or static high.

All outputs are initially disabled except for GPIO32, which is by default assigned as the I2C slave output data.

3.6.6.3 Interrupts and Interrupt Masking

The VSC8256-01 has configurable interrupt generators that can be used to flag error or alarm conditions which can, in turn, be used to prompt external controllers to take action upon certain events. Multiple blocks in a given channel contain these maskable interrupts (including line and host PMAs and rate-adaptation FIFOs). Each of the channel interrupt sources is routed to 2 interrupt generators per channel. For each per-channel interrupt generator, the sources that contribute to that interrupt are independently maskable using channel interrupt enables. Also, the status of each masked interrupt source is always readable in the channel so that the source of the interrupt can be determined quickly. Any GPIO input can be configured to produce an interrupt upon state change.

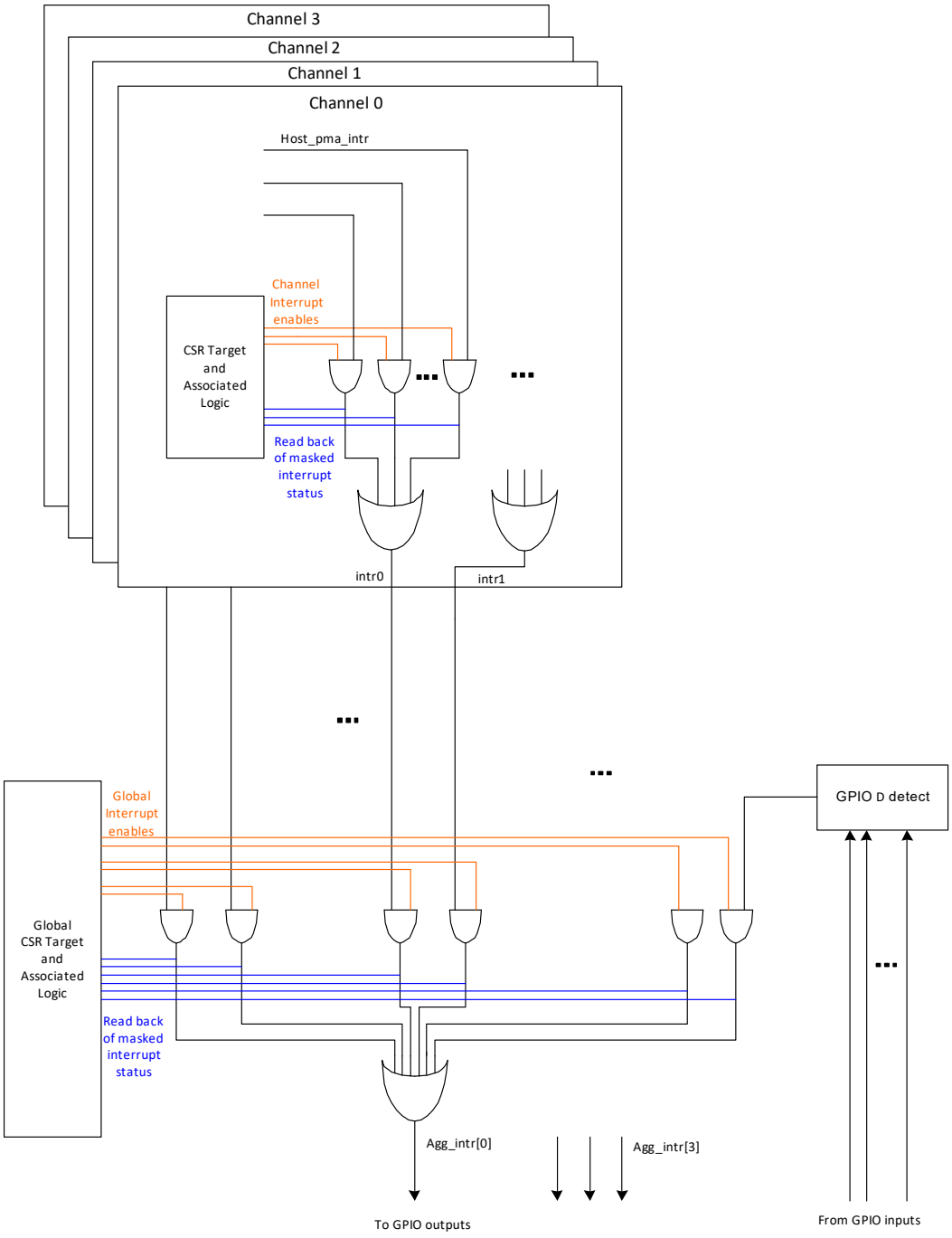
All the chip-level interrupts, as well as the 8 channel interrupts, are routed to each of 4 aggregate interrupt generators. The source of the interrupts for each aggregator is independently maskable (see note) using global interrupt enables, and the masked status of each interrupt is readable in the global target for quick determination of the source of the interrupt.

Note: While there are four interrupt generators, in the case of GPIO input state change detection, there is only one mask shared among all four interrupt aggregators.

Any GPIO may be configured to output the state of any of the 4 interrupts.

The following figure shows an overview of the interrupt blocks.

Figure 20 • **Interrupt Scheme**



4 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8256-01 device.

4.1 DC Characteristics

This section contains the DC specifications for the VSC8256-01 device.

4.1.1 Low-Speed Inputs and Outputs

The following tables list the DC specifications for the LVTTL inputs and outputs for the VSC8256-01 device. LVTTL inputs are 3.3 V tolerant when VDDTTL is 2.5 V.

Table 8 • **LVTTL Input and Push/Pull Output DC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, LVTTL	V_{OH_TTL}	1.8	V_{DDTTL}	V	V_{DDTTL} = 2.5 V and I_{OH} = –4 mA
Output low voltage, LVTTL	V_{OL}		0.5	V	V_{DDTTL}/V_{DDMDIO} = 2.5 V and I_{OL} = 4 mA
Input high voltage	V_{IH}	1.7	V_{DDTTL}	V	V_{DDTTL}/V_{DDMDIO} = 2.5 V
Input low voltage	V_{IL}		0.8	V	V_{DDTTL}/V_{DDMDIO} = 2.5 V
Input high current	I_{IH}		500	µA	$V_{IH} = V_{DDTTL}/V_{DDMDIO}$
Input low current	I_{IL}	–100		µA	V_{IL} = 0 V

Table 9 • **LVTTLOD Input and Open-Drain Output DC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, open drain	V_{OH_OD}	See note[1]	V_{DDTTL}	V	V_{DDTTL}/V_{DDMDIO} = 2.5 V and I_{OH} = –4 mA
Input high leakage current, open drain	I_{OZH}		100	µA	
Output low voltage (open drain)	V_{OL}		0.5	V	V_{DDTTL}/V_{DDMDIO} = 2.5 V and I_{OL} = 4 mA
Input high voltage	V_{IH}	1.7	V_{DDTTL}	V	V_{DDTTL}/V_{DDMDIO} = 2.5 V
Input low voltage	V_{IL}		0.8	V	V_{DDTTL}/V_{DDMDIO} = 2.5 V
Input high current	I_{IH}		500	µA	$V_{IH} = V_{DDTTL}/V_{DDMDIO}$
Input low current	I_{IL}	–100		µA	V_{IL} = 0 V

1. Determined by the loading current of the other devices connecting to this pin, the I_{OZH} current of this pin, and the value of the pull-up resistor used.

4.1.2 Reference Clock

The following table lists the DC specifications for the reference clock for the VSC8256-01 device.

Table 10 • **Reference Clock DC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
HREFCK/LREFCK differential input swing, high[1]	$\Delta V_{I_DIFF_HIGH}$	1100	2400	mV_{P-P}	LVPECL reference clock input
HREFCK/LREFCK differential input swing, low[1]	$\Delta V_{I_DIFF_LOW}$	200	1200	mV_{P-P}	CML reference clock input
SREFCK differential input swing	ΔV_{I_DIFF}	200	2400	mV_{P-P}	

1. An API call is used to set the input swing to be high or low.

4.2 AC Characteristics

This section contains the AC specifications for the VSC8256-01 device. The specifications apply to all channels. All SFI inputs and outputs should be AC-coupled, and should work in differential.

4.2.1 Receiver Specifications

The specifications in the following table correspond to line-side 10G receiver input, SFI point D. Point D assumes that the input is from a compliant point C output and a compliant SFI or XFI channel according to the SFP+ standard (SFF-8431) or the XFP multisource agreement (INF-8077i). The measurement is done with a 9 dB channel loss unless stated otherwise.

The SFI and XFI input of the 10G receiver are tested and characterized to support the ITU-T recommendation G.709 (OTN) OTU2, OTU1e, and OTU2e line rates (10.709 Gbps, 11.049 Gbps, and 11.095 Gbps) with a channel loss of 6.5 dB or less.

Note: For additional details regarding OTN line rates and the corresponding electrical characteristics, contact your Microsemi representative.

The CDR lock time at the 10G input to the PMA is 5 µs, maximum.

Table 11 • **Host- and Line-Side 10G Receiver Input (SFI Point D)**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input data rate		9.95328 – 100 ppm	10.3125	10.3125 + 100 ppm	Gbps	10 Gbps LAN/WAN
Input linear mode differential input data swing	$\Delta VRXIN_{LINEAR}$	180		600	mV	Voltage modulation amplitude (VMA)
Input limiting mode differential input data swing	$\Delta VRXIN_{LIMITING}$	300		850	mV	Measured peak-to-peak
Input AC common-mode voltage	V_{CM}			15	mV_{RMS}	
Differential return loss	RL_{SDD11}			–12	dB	0.01 GHz to 2.8 GHz
Differential return loss	RL_{SDD11}			–8.15 + 13.33 x $\log_{10}$(f/5.5 GHz)	dB	2.8 GHz to 11.1 GHz

Table 11 • **Host- and Line-Side 10G Receiver Input (SFI Point D) *(continued)***

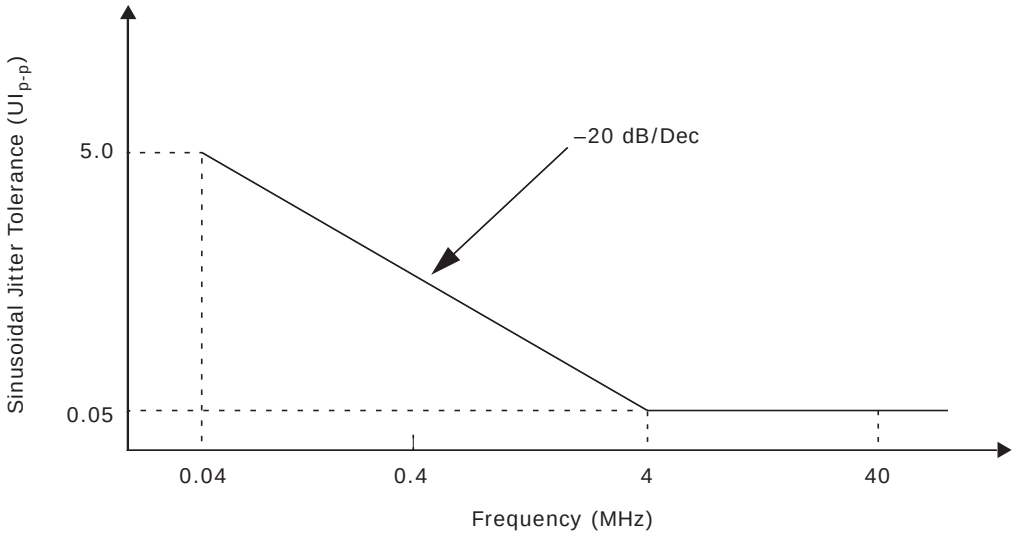
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Reflected differential to common-mode conversion	RL_{SCD11}			–15	dB	0.01 GHz to 11.1 GHz

Table 12 • **Host- and Line-Side 10G Receiver Input (SFI Point C")**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
99% jitter	$99\%_{JIT_p\text{-}p}$			0.42	UI	
Pulse width shrinkage jitter	$DDPWS_{JIT_p\text{-}p}$			0.3	UI	
Total jitter tolerance	$TOL_{JIT_P\text{-}P}$			0.70	UI	
Eye mask X1	X1			0.35	UI	
Eye mask Y1	Y1	150			mV	
Eye mask Y2	Y2			425	mV	
Waveform distortion penalty	WDPc			9.3	dBe	BER 1E–12. This parameter of DAC is measured with 7dB SFI channel loss.
Voltage modulation amplitude	VMA	180			mV	BER 1E–12. This parameter of DAC is measured with 7dB SFI channel loss.
Optical sensitivity (ROP), back-to-back, 10.3 Gbps	S_{B2B}			–24	dBm	BER 1E–12, PRBS31 and 10 GbE frame. 5.76 dB SFI channel loss.
Optical sensitivity (ROP), with fiber plant, 10.3 Gbps	S_{FIBER}			–21	dBm	95 km single-mode fiber, BER 1E–12, PRBS31 and 10 GbE frame. 5.76 dB SFI channel loss.
Chromatic dispersion penalty	F_{CDP}			3	dB	1600 ps/nm. 5.76 dB SFI channel loss.
OSNR vs BER with fiber plant, 10.7 Gbps	$OSNR_{FEC}$	16			dB	95 km single-mode fiber, BER 7E–4, 5.76 dB SFI channel loss.

The following illustration shows the sinusoidal jitter tolerance for the SFI datacom.

Figure 21 • **SFI Datacom Sinusoidal Jitter Tolerance**



The following table lists the 10G input jitter specifications for the VSC8256-01 device.

Table 13 • **Host- and Line-Side SONET 10G Input Jitter**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input data rate, 10 Gbps WAN		9.95328 – 100 ppm	9.95328	9.95328 + 100 ppm	Gbps	
Sinusoidal jitter tolerance, 9.95 Gbps	SJ_T	2x jitter mask				GR-253 according to SONET OC-192 standard

The following table lists the line-side 1.25 Gbps SFI input specifications for the VSC8256-01 device.

Table 14 • **Host- and Line-Side 1.25 Gbps SFI Input**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input data rate, 1.25 Gbps		1.25 – 100 ppm	1.25	1.25 + 100 ppm	Gbps	1.25 Gbps mode
Differential input return loss	RLI_{SDD11}			–10	dB	50 MHz to 625 MHz
Differential input return loss	RLI_{SDD11}			–10 + 10 x log (f/625 MHz)	dB	625 MHz to 1250 MHz
Total jitter tolerance	TJ_T			0.749	UI	Jitter above 637 kHz (IEEE 802.3 clause 38.5)
Deterministic jitter	DJ			0.462	UI_{P-P}	Jitter above 637 kHz (IEEE 802.3 clause 38.5)
Eye mask Y1	Y1	125			mV	
Eye mask Y2	Y2			600	mV	

4.2.2 Transmitter Specifications

This section includes the transmitter specifications.

The specifications in the following table correspond to line-side 10G transmitter output, SFI point B. Point B is after a standard-compliant SFI or XFI channel, as defined in the SFP+ standard (SFF-8431) or the XFP multisource agreement (INF-8077i). The measurement is done with a 9 dB channel loss unless stated otherwise.

The SFI and XFI output of the 10G transmitter are tested and characterized to support ITU-T recommendation G.709 (OTN) OTU2, OTU1e, and OTU2e line rates (10.709 Gbps, 11.049 Gbps, and 11.095 Gbps) with a channel loss of 6.5 dB or less.

Note: For additional details regarding OTN line rates and the corresponding electrical characteristics, contact your Microsemi representative.

Table 15 • **Host- and Line-Side 10G Transmitter Output (SFI Point A)**

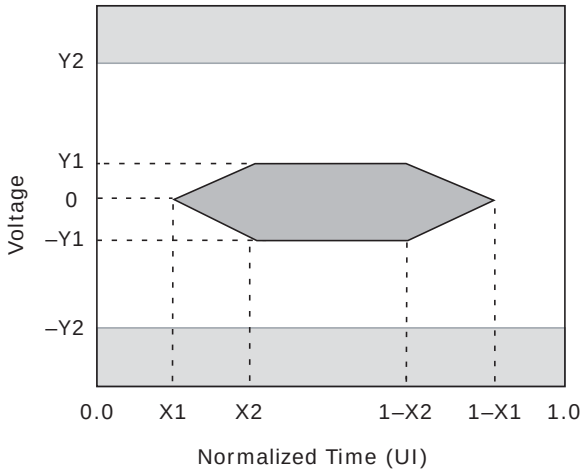
Parameter	Symbol	Minimum	Maximum	Unit	Condition
Termination mismatch	ΔZ_M		5	%	
Differential return loss	SDD22		–12	dB	0.01 GHz to 2.8 GHz
Differential return loss	SDD22		–8.15 + 13.33 x $\log_{10}$(f/5.5 GHz)	dB	2.8 GHz to 11.1 GHz
Common-mode return loss	SCC22		–9	dB	0.01 GHz to 4.74 GHz
Common-mode return loss	SCC22		–8.15 + 13.33 x $\log_{10}$(f/5.5 GHz)	dB	4.74 GHz to 11.1 GHz

Table 16 • **Host- and Line-Side 10G Transmitter Output (SFI Point B)**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
AC common-mode voltage	V_{OCM_AC}		15	mV_{RMS}	
Total jitter	TJ		0.28	UI	
Data-dependant jitter	DDJ		0.1	UI	
Pulse shrinkage jitter	DDPWS		0.055	UI	
Uncorrelated jitter	UJ		0.023	UI_{RMS}	
Eye mask X1	X1		0.12	UI	
Eye mask X2	X2		0.33	UI	
Eye mask Y1	Y1	95		mV	Tested at 7 dB SFI channel loss.
Eye mask Y2	Y2		350	mV	

The following illustration shows the compliance mask associated with the Tx SFI transmit differential output.

Figure 22 • **SFI Transmit Differential Output Compliance Mask**



The following table shows the transmit path output specifications for SFI point B. These DAC parameters are measured with 7 dB SFI channel loss.

Table 17 • **Transmitter SFP+ Direct Attach Copper Output AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
SFP+ direct attach copper voltage modulation amplitude, peak-to-peak	V_{MA}	300		mV	See SFF-8431 section D.7.
SFP+ direct attach copper transmitter Q_{SQ}	Q_{SQ}	63.1			See SFF-8431 section D.8.
SFP+ direct attach copper output AC common-mode voltage			12	mV (RMS)	See SFF-8431 section D.15.
SFP+ direct attach copper output TWDPc	TWDPc		10.7	dB	Electrical output measured using SFF-8431 Appendix G, including copper direct attach stressor.

The following table shows that the 10 Gbps transmitter operating in 10GBASE-KR mode complies with IEEE 802.3 clause 72.7.

Table 18 • **10 Gbps Transmitter 10GBASE-KR AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Signalling speed	T_{BAUD}	10.3125 – 100 ppm	10.3125 + 100 ppm	Gbps	
Differential output return loss	RLO_{SDD22}		–9 –9 + 12 x log (f/2.5 GHz)	dB	50 MHz to 2.5 GHz 2.5 GHz to 7.5 GHz R_L = 100 Ω ± 1%
Common mode return loss	RLO_{CM}		–6 –6 + 12 x log (f/2.5 GHz)	dB	50 MHz to 2.5 GHz 2.5 GHz to 7.5 GHz R_L = 100 Ω ± 1%
Transition time	T_R, T_F	24	47	ps	20% to 80%

Table 18 • **10 Gbps Transmitter 10GBASE-KR AC Characteristics *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Random jitter	RJ		0.16	UI	BER 1E–12, 0.151 UI for junction temperature ≤ 100 °C
Deterministic jitter	DJ		0.15	UI	
Duty cycle distortion (part of DJ)	DCD		0.035	UI	
Total jitter	TJ		0.28	UI	

The following table shows the transmit path optical jitter specifications for point A, measured using COTS SFP-10G module.

Table 19 • **Host- and Line-Side Optical 10G Output Jitter**

Parameter	Symbol	Maximum	Unit	Condition
Total jitter, 20 kHz to 80 MHz	TJ	180	mUI_{P-P}	60 second gating time
Total jitter, 4 MHz to 80 MHz	TJ	100	mUI_{P-P}	60 second gating time

The following table lists the line-side 1.25 Gbps SFI output specifications for the VSC8256-01 device.

Table 20 • **Host- and Line-Side 1.25 Gbps SFI Output**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Differential output return loss	RLO_{SDD22}		–10	dB	50 MHz to 625 MHz
Differential output return loss	RLO_{SDD22}		–10 + 10 x log(f/625 MHz)	dB	625 MHz to 1250 MHz
Common mode return loss	RLO_{CM}		–6	dB	50 MHz to 625 MHz
Deterministic jitter	DJ		0.1	UI	Measured according to IEEE 802.3 clause 38.5
Total jitter	TJ		0.24	UI	Measured according to IEEE 802.3 clause 38.5
Eye mask Y1	Y1	150		mV	SFF-8431 1G specification
Eye mask Y2	Y2		500	mV	SFF-8431 1G specification

4.2.3 Timing and Reference Clock

The following table lists the reference clock specifications (LREFCK, SREFCK, and HREFCK) for the VSC8256-01 device.

Table 21 • **Reference Clock AC Characteristics**

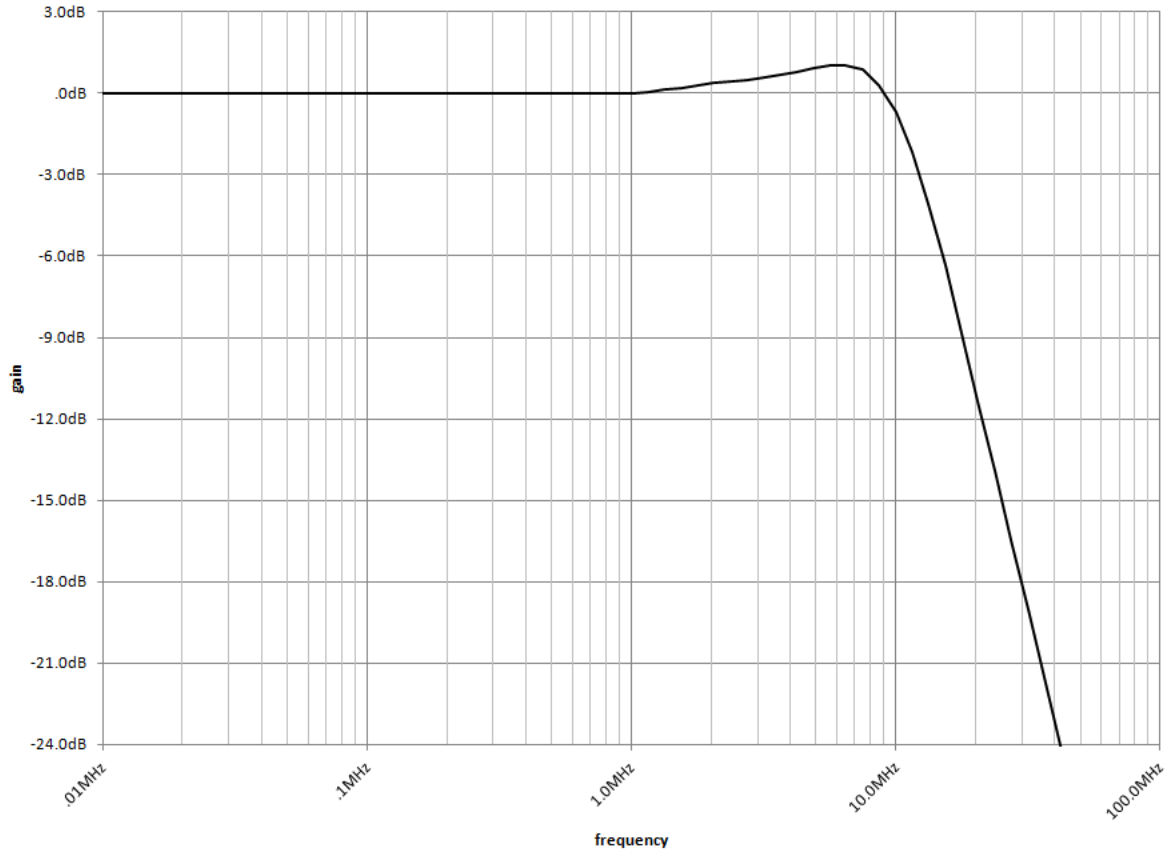
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Reference clock frequency	f_{REFCLK}	125		156.25	MHz	
Reference clock frequency accuracy	f_R	– 100 ppm		100 ppm	MHz	

Table 21 • **Reference Clock AC Characteristics *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Rise time and fall time	t_R, t_F			0.4	ns	Within ± 200 mV relative to VDD x 2/3
Reference clock duty cycle	DC	40		60	%	
Jitter tolerance for LREFCLK and HREFCLK	$JTL_{LREF/HREF}$		0.7		ps	For 2 KHz to 20 MHz

The following illustration shows the worst-case clock jitter transfer characteristic for the LREFCK input.

Figure 23 • **LREFCK/HREFCLK to Data Output Jitter Transfer**



4.2.4 Two-Wire Serial (Slave) Interface

This section contains information about the AC specifications for the two-wire serial slave interface for the VSC8256-01 device.

Table 22 • **Two-Wire Serial Interface AC Characteristics**

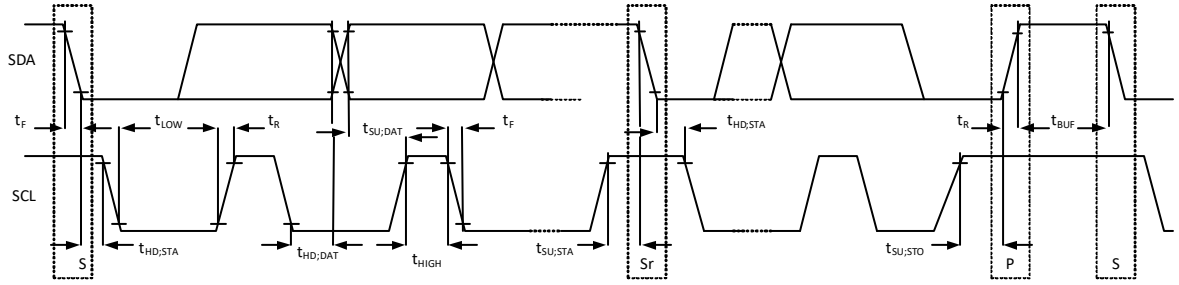
		Standard		Fast Mode		
Parameter	**Symbol**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Unit**
Serial clock frequency	f_{SCL}		100		400	kHz

Table 22 • **Two-Wire Serial Interface AC Characteristics *(continued)***

		Standard		Fast Mode		
Parameter	**Symbol**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Unit**
Hold time START condition after this period, the first clock pulse is generated	$t_{HD:STA}$	4.0		0.6		µs
Low period of SCL	t_{LOW}	4.7		1.3		µs
High period of SCL	t_{HIGH}	4.0		0.6		µs
Data hold time	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU:DAT}$	250		100		ns
Rise time for SDA and SCL	t_R		1000		300	ns
Fall time for SDA and SCL	t_F		300		300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0		0.6		µs
Bus free time between a STOP and START	t_{BUF}	4.7		1.3		µs
Capacitive load for SCL and SDA bus line	C_B		400		330	pF
External pull-up resistor[1]	R_P	900	$8 \times 10^{-7}/C_B$	900	$3 \times 10^{-7}/C_B$	Ω

1. Minimum value is determined from I_{OL} and internal reliability requirements. Maximum value is determined by load capacitance. Microsemi recommends 10 kΩ for typical applications in which capacitance loads are below the specified minimums.

Figure 24 • **Two-Wire Serial Interface Timing**



S = START, P = STOP, and Sr = repeated START.

4.2.5 MDIO Interface

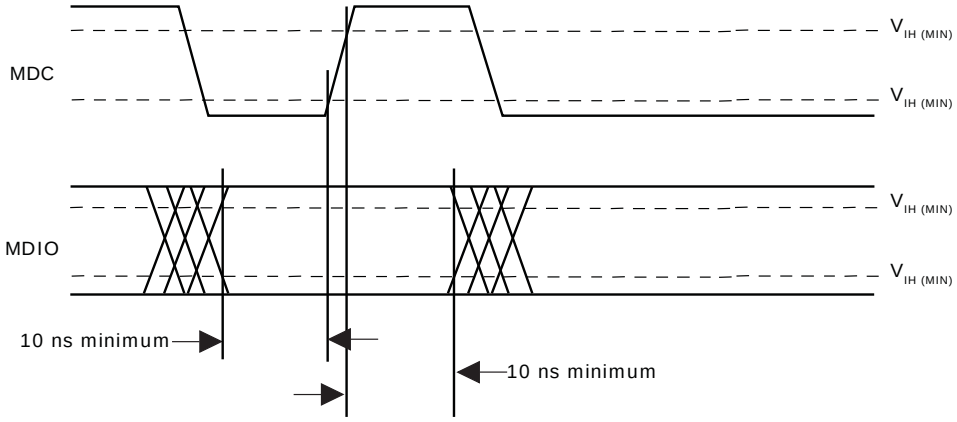
This section contains information about the AC specifications for the MDIO interface for the VSC8256-01 device.

Table 23 • **MDIO Interface AC Characteristics**

Parameter	**Symbol**	**Minimum**	**Maximum**	**Unit**
MDIO data hold time	t_{HOLD}	10		ns
MDIO data setup time	t_{SU}	10		ns
Delay from MDC rising edge to MDIO data change	t_{DELAY}		300	ns
MDC clock rate	f		2.5	MHz

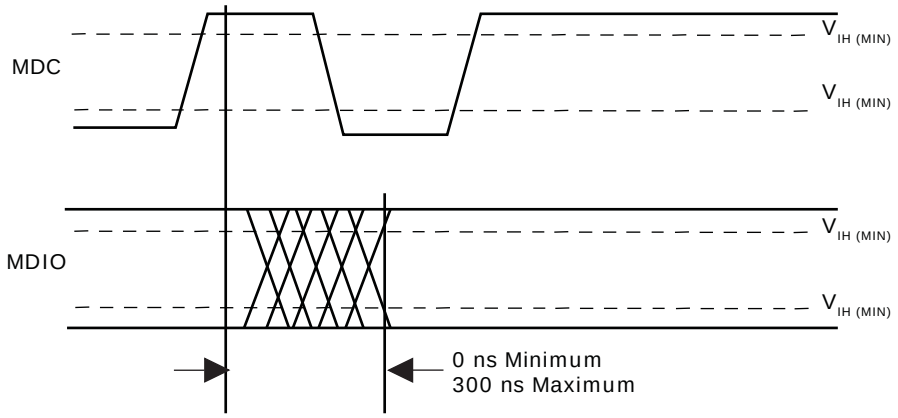
The following illustration shows the timing with the MDIO sourced by STA.

Figure 25 • **Timing with MDIO Sourced by STA**



The following illustration shows the timing with the MDIO sourced by MMD.

Figure 26 • **Timing with MDIO Sourced by MMD**



The following table lists the clock output specifications the device.

Table 24 • **Clock Output AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
CKOUT[0:3]N/P jitter generation	JG_{C64}		15	ps_{RMS}	10 kHz to 10 MHz
CKOUT[0:3]N/P differential output swing	ΔV	650	900	mV_{P-P}	

4.2.6 SPI Slave Interface

This section contains information about the AC specifications for the four-pin SPI slave interface used to read and write registers. The maximum clock rate is 30 MHz, and it is configurable.

Table 25 • **SPI Slave Interface AC Characteristics**

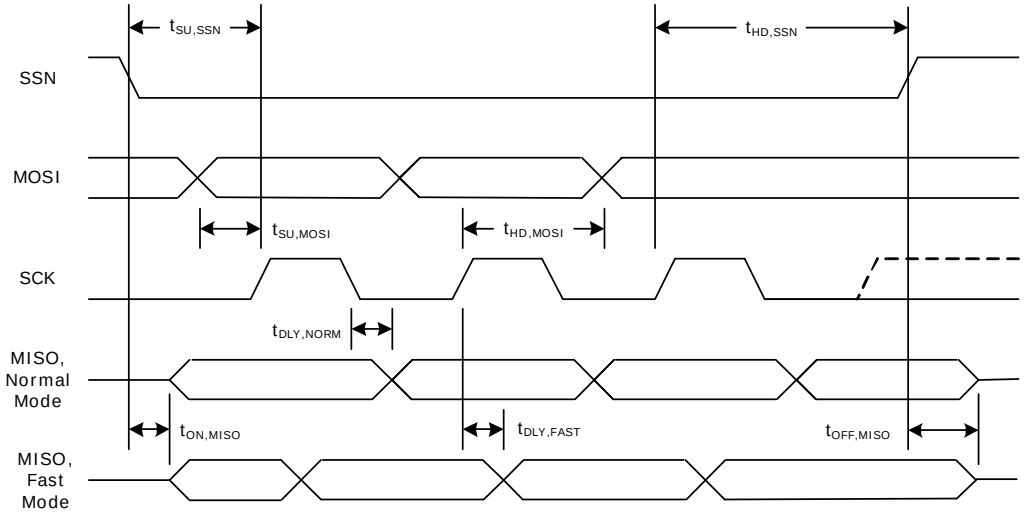
Parameter	Symbol	Minimum	Maximum	Unit	Condition
MOSI data setup time	$t_{SU,\ MOSI}$	10		ns	
MOSI data hold time	$t_{HD,\ MOSI}$	10		ns	
SSN data setup time	$t_{SU,\ SSN}$	15		ns	SSN transition low to enable interface

Table 25 • **SPI Slave Interface AC Characteristics *(continued)***

SSN data hold time	$t_{HD, SSN}$	SCK clock period + 15		ns	SSN transition high to enable interface
SSN transition low to MISO valid	$t_{ON, MISO}$	2		ns	
SSN transition high to MISO high impedance	$t_{OFF, MISO}$		10	ns	
Falling SCK to valid MISO data, normal mode	$t_{DLY, NORM}$	14	30	ns	Maximum capacitance loading of 5 pF
			35	ns	Maximum capacitance loading of 50 pF
			36	ns	Maximum capacitance loading of 100 pF
Rising SCK to valid MISO data, fast mode	$t_{DLY, FAST}$	14	30	ns	Maximum capacitance loading of 5 pF
			35	ns	Maximum capacitance loading of 50 pF
			36	ns	Maximum capacitance loading of 100 pF

The following illustration shows the SPI interface timing.

Figure 27 • **SPI Interface Timing**



4.3 Operating Conditions

To ensure that the control pins remain set to the desired configured state when the device is powered up, perform a reset using the reset pin after power-up and after the control pins are steady for 1 ms.

Table 26 • **Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
1.0 V power supply voltage	V_{DDL} V_{DDAH} V_{DDAL}	0.94575	0.975	1.00425	V	Power rail at 0.975 V ±3%
		0.97	1.0	1.03	V	Power rail at 1.0 V ±3%
1.2 V power supply voltage	V_{DDHSL} V_{DDHSH}	1.14		1.26	V	±5%
2.5 V TTL I/O power supply voltage	V_{DDTTL} V_{DDMDIO}	2.375		2.625	V	±5%
Power consumption	P_{DD}			4.95	W	V_{DDL} = V_{DDAH}= V_{DDAL}= 1.0042 V, maximum[1] V_{DDHSH} = V_{DDHSL} = 1.26 V V_{DDTTL} = V_{DDMDIO} = 2.625 V
Clock output power	P_{DD_CLK}	0		40	mW	Per clock output
SREFCK input power	P_{DD_SREFCK}	0		60	mW	
Operating temperature[2]	T	–40		110	°C	

1. Device can be run at 1 V +3% with a worst case power of 5.1 W.
2. Minimum specification is ambient temperature, and the maximum is junction temperature.

4.4 Stress Ratings

This section contains the stress ratings for the device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 27 • **Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
1.0 V power supply voltage, potential to ground	V_{DDAH} V_{DDAL} V_{DDL}	–0.3	1.1	V
1.2 V power supply voltage, potential to ground	V_{DDHSL} V_{DDHSH}	–0.3	1.32	V
2.5 V TTL I/O power supply voltage	V_{DDTTL} V_{DDMDIO}	–0.3	2.75	V
Storage temperature	T_S	–55	125	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–250	250	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	See note[1]		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Microsemi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

5 Pin Descriptions

The VSC8256-01 device has 256 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

5.1 Pin Diagram

The following illustration shows the pin diagram for the device.

Figure 28 • **Pin Diagram**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	GND	SSN	TRSTB	SCK	TDO	TDI	RESETN	NC	NC	NC	CKOUT0P	GND	GND	GND
B	RXOUT0N	RXOUT0P	GND	MOSI	TMS	MISO	TCK	GPIO_4	GPIO_5	MODE0	MODE1	NC	CKOUT0N	GND	RXIN0P	RXIN0N
C	GND	GND	GND	TDION	TDIOP	NC	NC	NC	NC	NC	NC	NC	GND	GND	GND	GND
D	TXIN0N	TXIN0P	GND	GPIO_0	GPIO_1	GPIO_2	GPIO_3	GPIO_6	GPIO_7	GPIO_8	GPIO_9	GPIO_10	CKOUT1P	GND	TXOUT0P	TXOUT0N
E	GND	GND	GND	GPIO_11	GPIO_12	GPIO_13	GPIO_14	GPIO_15	GPIO_16	GPIO_17	GPIO_18	GPIO_19	CKOUT1N	GND	GND	GND
F	RXOUT1N	RXOUT1P	GND	VDDAH	GND	GND	VDDTTL	VDDL	GND	VDDL	VDDAL	GND	GND	GND	RXIN1P	RXIN1N
G	GND	GND	GND	VDDHSH	VDDAH	GND	GND	GND	GND	VDDAL	VDDHSL	GND	CKOUT3P	GND	GND	GND
H	TXIN1N	TXIN1P	GND	VDDHSH	VDDAH	GND	GND	GND	GND	VDDAL	VDDHSL	GND	CKOUT3N	GND	TXOUT1P	TXOUT1N
J	GND	GND	GND	VDDHSH	VDDAH	GND	GND	GND	GND	VDDAL	VDDHSL	GND	GND	GND	GND	GND
K	RXOUT2N	RXOUT2P	GND	VDDHSH	VDDAH	GND	GND	GND	GND	VDDAL	VDDHSL	GND	CKOUT2P	GND	RXIN2P	RXIN2N
L	GND	GND	GND	VDDAH	VDDMDIO	GND	VDDTTL	VDDL	GND	VDDL	VDDAL	GND	CKOUT2N	GND	GND	GND
M	TXIN2N	TXIN2P	GND	GPIO_20	GPIO_21	GPIO_22	GPIO_23	GPIO_24	GPIO_25	GPIO_26	GPIO_27	NC	GND	GND	TXOUT2P	TXOUT2N
N	GND	GND	GND	GPIO_28	GPIO_29	GPIO_30	GPIO_31	GPIO_32/I2C_SDA	GPIO_33/I2C_SCL	GPIO_34	GPIO_35	NC	SCKOUTP	GND	GND	GND
P	RXOUT3N	RXOUT3P	GND	NC	GPIO_36	GPIO_37	GPIO_38	GPIO_39	NC	NC	NC	NC	SCKOUTN	GND	RXIN3P	RXIN3N
R	GND	GND	GND	GND	MDIO	MODE2	HREFCKP	PADDR3	LREFCKP	MODE3	SREFCKP	RCOMPN	GND	GND	GND	GND
T	GND	TXIN3N	TXIN3P	GND	MDC	PADDR4	HREFCKN	PADDR2	LREFCKN	NC	SREFCKN	RCOMPP	GND	TXOUT3P	TXOUT3N	GND

5.2 Pins by Function

This section contains the functional pin descriptions for the VSC8256-01 device.

Note: All differential data or clock signals should be AC-coupled. A cap of 0.1 µF would be sufficient.

Functional Group	Name	Number	Type	Level	Description
Clock Signal	CKOUT0N	B13	O	CML	Selectable clock output channel 0, complement
Clock Signal	CKOUT0P	A13	O	CML	Selectable clock output channel 0, true
Clock Signal	CKOUT1N	E13	O	CML	Selectable clock output channel 1, complement
Clock Signal	CKOUT1P	D13	O	CML	Selectable clock output channel 1, true
Clock Signal	CKOUT2N	L13	O	CML	Selectable clock output channel 2, complement
Clock Signal	CKOUT2P	K13	O	CML	Selectable clock output channel 2, true
Clock Signal	CKOUT3N	H13	O	CML	Selectable clock output channel 3, complement
Clock Signal	CKOUT3P	G13	O	CML	Selectable clock output channel 3, true
Clock Signal	HREFCKN	T7	I	CML	Host reference clock input, complement. Must be frequency locked to LREFCKP/N.
Clock Signal	HREFCKP	R7	I	CML	Host reference clock input, true. Must be frequency locked to LREFCKP/N.
Clock Signal	LREFCKN	T9	I	CML	Line reference clock input, complement
Clock Signal	LREFCKP	R9	I	CML	Line reference clock input, true
Clock SIgnal	SCKOUTN	P13	O	CML	SyncE recovered clock output, complement
Clock Signal	SCKOUTP	N13	O	CML	SyncE recovered clock output, true
Clock Signal	SREFCKN	T11	I	CML	SyncE reference clock input, complement
Clock Signal	SREFCKP	R11	I	CML	SyncE reference clock input, true
JTAG	TCK	B7	I	LVTTL	Boundary scan, test clock input. Internally pulled high.
JTAG	TDI	A8	I	LVTTL	Boundary scan, test data input. Internally pulled high.
JTAG	TDO	A7	O	LVTTL	Boundary scan, test data output.
JTAG	TMS	B5	I	LVTTL	Boundary scan, test mode select. Internally pulled high.
JTAG	TRSTB	A5	I	LVTTL	Boundary scan, test reset input. Internally pulled high.
MDIO	MDC	T5	I	LVTTL	MDIO clock input
MDIO	MDIO	R5	B	LVTTLOD	MDIO data I/O
Miscellaneous	GPIO_0	D4	B	LVTTLOD	General purpose I/O 0

Miscellaneous	GPIO_1	D5	B	LVTTLOD	General purpose I/O 1
Miscellaneous	GPIO_2	D6	B	LVTTLOD	General purpose I/O 2
Miscellaneous	GPIO_3	D7	B	LVTTLOD	General purpose I/O 3
Miscellaneous	GPIO_4	B8	B	LVTTLOD	General purpose I/O 4
Miscellaneous	GPIO_5	B9	B	LVTTLOD	General purpose I/O 5
Miscellaneous	GPIO_6	D8	B	LVTTLOD	General purpose I/O 6
Miscellaneous	GPIO_7	D9	B	LVTTLOD	General purpose I/O 7
Miscellaneous	GPIO_8	D10	B	LVTTLOD	General purpose I/O 8
Miscellaneous	GPIO_9	D11	B	LVTTLOD	General purpose I/O 9
Miscellaneous	GPIO_10	D12	B	LVTTLOD	General purpose I/O 10
Miscellaneous	GPIO_11	E4	B	LVTTLOD	General purpose I/O 11
Miscellaneous	GPIO_12	E5	B	LVTTLOD	General purpose I/O 12
Miscellaneous	GPIO_13	E6	B	LVTTLOD	General purpose I/O 13
Miscellaneous	GPIO_14	E7	B	LVTTLOD	General purpose I/O 14
Miscellaneous	GPIO_15	E8	B	LVTTLOD	General purpose I/O 15
Miscellaneous	GPIO_16	E9	B	LVTTLOD	General purpose I/O 16
Miscellaneous	GPIO_17	E10	B	LVTTLOD	General purpose I/O 17
Miscellaneous	GPIO_18	E11	B	LVTTLOD	General purpose I/O 18
Miscellaneous	GPIO_19	E12	B	LVTTLOD	General purpose I/O 19
Miscellaneous	GPIO_20	M4	B	LVTTLOD	General purpose I/O 20
Miscellaneous	GPIO_21	M5	B	LVTTLOD	General purpose I/O 21
Miscellaneous	GPIO_22	M6	B	LVTTLOD	General purpose I/O 22
Miscellaneous	GPIO_23	M7	B	LVTTLOD	General purpose I/O 23
Miscellaneous	GPIO_24	M8	B	LVTTLOD	General purpose I/O 24
Miscellaneous	GPIO_25	M9	B	LVTTLOD	General purpose I/O 25
Miscellaneous	GPIO_26	M10	B	LVTTLOD	General purpose I/O 26
Miscellaneous	GPIO_27	M11	B	LVTTLOD	General purpose I/O 27
Miscellaneous	GPIO_28	N4	B	LVTTLOD	General purpose I/O 28
Miscellaneous	GPIO_29	N5	B	LVTTLOD	General purpose I/O 29
Miscellaneous	GPIO_30	N6	B	LVTTLOD	General purpose I/O 30
Miscellaneous	GPIO_31	N7	B	LVTTLOD	General purpose I/O 31
Miscellaneous	GPIO_32/I2C_SDA	N8	B	LVTTLOD	General purpose I/O 32 (also I2C data)
Miscellaneous	GPIO_33/I2C_SCL	N9	B	LVTTLOD	General purpose I/O 33 (also I2C clock)
Miscellaneous	GPIO_34	N10	B	LVTTLOD	General purpose I/O 34
Miscellaneous	GPIO_35	N11	B	LVTTLOD	General purpose I/O 35
Miscellaneous	GPIO_36	P5	B	LVTTLOD	General purpose I/O 36
Miscellaneous	GPIO_37	P6	B	LVTTLOD	General purpose I/O 37
Miscellaneous	GPIO_38	P7	B	LVTTLOD	General purpose I/O 38
Miscellaneous	GPIO_39	P8	B	LVTTLOD	General purpose I/O 39
Miscellaneous	MODE0	B10	I	LVTTL	Mode select input bit 0. Internally pulled low.
Miscellaneous	MODE1	B11	I	LVTTL	Mode select input bit 1. Internally pulled low.

Miscellaneous	MODE2	R6	I	LVTTL	Mode select input bit 2. Internally pulled low. Do not connect.
Miscellaneous	MODE3	R10	I	LVTTL	Mode select input bit 3. Internally pulled low. Do not connect.
Miscellaneous	PADDR2	T8	I	LVTTL	Port address bit 2. Internally pulled low.
Miscellaneous	PADDR3	R8	I	LVTTL	Port address bit 3. Internally pulled low.
Miscellaneous	PADDR4	T6	I	LVTTL	Port address bit 4. Internally pulled low.
Miscellaneous	RCOMPN	R12		Analog	Resistor comparator, complement
Miscellaneous	RCOMPP	T12		Analog	Resistor comparator, true
Miscellaneous	RESETN	A9	I	LVTTL	Reset. Low= Reset. Internally pulled high.
Miscellaneous	TDION	C4		Analog	Temperature diode, complement.
Miscellaneous	TDIOP	C5		Analog	Temperature diode, true.
Power and Ground	GND	A1	P	GND	Ground
Power and Ground	GND	A2	P	GND	Ground
Power and Ground	GND	A3	P	GND	Ground
Power and Ground	GND	A14	P	GND	Ground
Power and Ground	GND	A15	P	GND	Ground
Power and Ground	GND	A16	P	GND	Ground
Power and Ground	GND	B3	P	GND	Ground
Power and Ground	GND	B14	P	GND	Ground
Power and Ground	GND	C1	P	GND	Ground
Power and Ground	GND	C2	P	GND	Ground
Power and Ground	GND	C3	P	GND	Ground
Power and Ground	GND	C13	P	GND	Ground
Power and Ground	GND	C14	P	GND	Ground
Power and Ground	GND	C15	P	GND	Ground
Power and Ground	GND	C16	P	GND	Ground
Power and Ground	GND	D3	P	GND	Ground
Power and Ground	GND	D14	P	GND	Ground
Power and Ground	GND	E1	P	GND	Ground
Power and Ground	GND	E2	P	GND	Ground
Power and Ground	GND	E3	P	GND	Ground
Power and Ground	GND	E14	P	GND	Ground
Power and Ground	GND	E15	P	GND	Ground
Power and Ground	GND	E16	P	GND	Ground
Power and Ground	GND	F3	P	GND	Ground
Power and Ground	GND	F5	P	GND	Ground
Power and Ground	GND	F6	P	GND	Ground
Power and Ground	GND	F9	P	GND	Ground
Power and Ground	GND	F12	P	GND	Ground

Power and Ground	GND	F13	P	GND	Ground
Power and Ground	GND	F14	P	GND	Ground
Power and Ground	GND	G1	P	GND	Ground
Power and Ground	GND	G2	P	GND	Ground
Power and Ground	GND	G3	P	GND	Ground
Power and Ground	GND	G6	P	GND	Ground
Power and Ground	GND	G7	P	GND	Ground
Power and Ground	GND	G8	P	GND	Ground
Power and Ground	GND	G9	P	GND	Ground
Power and Ground	GND	G12	P	GND	Ground
Power and Ground	GND	G14	P	GND	Ground
Power and Ground	GND	G15	P	GND	Ground
Power and Ground	GND	G16	P	GND	Ground
Power and Ground	GND	H3	P	GND	Ground
Power and Ground	GND	H6	P	GND	Ground
Power and Ground	GND	H7	P	GND	Ground
Power and Ground	GND	H8	P	GND	Ground
Power and Ground	GND	H9	P	GND	Ground
Power and Ground	GND	H12	P	GND	Ground
Power and Ground	GND	H14	P	GND	Ground
Power and Ground	GND	J1	P	GND	Ground
Power and Ground	GND	J2	P	GND	Ground
Power and Ground	GND	J3	P	GND	Ground
Power and Ground	GND	J6	P	GND	Ground
Power and Ground	GND	J7	P	GND	Ground
Power and Ground	GND	J8	P	GND	Ground
Power and Ground	GND	J9	P	GND	Ground
Power and Ground	GND	J12	P	GND	Ground
Power and Ground	GND	J13	P	GND	Ground
Power and Ground	GND	J14	P	GND	Ground
Power and Ground	GND	J15	P	GND	Ground
Power and Ground	GND	J16	P	GND	Ground
Power and Ground	GND	K3	P	GND	Ground
Power and Ground	GND	K6	P	GND	Ground
Power and Ground	GND	K7	P	GND	Ground
Power and Ground	GND	K8	P	GND	Ground
Power and Ground	GND	K9	P	GND	Ground
Power and Ground	GND	K12	P	GND	Ground
Power and Ground	GND	K14	P	GND	Ground
Power and Ground	GND	L1	P	GND	Ground
Power and Ground	GND	L2	P	GND	Ground
Power and Ground	GND	L3	P	GND	Ground
Power and Ground	GND	L6	P	GND	Ground
Power and Ground	GND	L9	P	GND	Ground

Power and Ground	GND	L12	P	GND	Ground
Power and Ground	GND	L14	P	GND	Ground
Power and Ground	GND	L15	P	GND	Ground
Power and Ground	GND	L16	P	GND	Ground
Power and Ground	GND	M3	P	GND	Ground
Power and Ground	GND	M13	P	GND	Ground
Power and Ground	GND	M14	P	GND	Ground
Power and Ground	GND	N1	P	GND	Ground
Power and Ground	GND	N2	P	GND	Ground
Power and Ground	GND	N3	P	GND	Ground
Power and Ground	GND	N14	P	GND	Ground
Power and Ground	GND	N15	P	GND	Ground
Power and Ground	GND	N16	P	GND	Ground
Power and Ground	GND	P3	P	GND	Ground
Power and Ground	GND	P14	P	GND	Ground
Power and Ground	GND	R1	P	GND	Ground
Power and Ground	GND	R2	P	GND	Ground
Power and Ground	GND	R3	P	GND	Ground
Power and Ground	GND	R4	P	GND	Ground
Power and Ground	GND	R13	P	GND	Ground
Power and Ground	GND	R14	P	GND	Ground
Power and Ground	GND	R15	P	GND	Ground
Power and Ground	GND	R16	P	GND	Ground
Power and Ground	GND	T1	P	GND	Ground
Power and Ground	GND	T4	P	GND	Ground
Power and Ground	GND	T13	P	GND	Ground
Power and Ground	GND	T16	P	GND	Ground
Power and Ground	VDDAH	F4	P	Supply	1.0 V power supply for host side analog
Power and Ground	VDDAH	G5	P	Supply	1.0 V power supply for host side analog
Power and Ground	VDDAH	H5	P	Supply	1.0 V power supply for host side analog
Power and Ground	VDDAH	J5	P	Supply	1.0 V power supply for host side analog
Power and Ground	VDDAH	K5	P	Supply	1.0 V power supply for host side analog
Power and Ground	VDDAH	L4	P	Supply	1.0 V power supply for host side analog
Power and Ground	VDDAL	F11	P	Supply	1.0 V power supply for line side analog
Power and Ground	VDDAL	G10	P	Supply	1.0 V power supply for line side analog
Power and Ground	VDDAL	H10	P	Supply	1.0 V power supply for line side analog

Power and Ground	VDDAL	J10	P	Supply	1.0 V power supply for line side analog
Power and Ground	VDDAL	K10	P	Supply	1.0 V power supply for line side analog
Power and Ground	VDDAL	L11	P	Supply	1.0 V power supply for line side analog
Power and Ground	VDDHSH	G4	P	Supply	1.2 V power supply for host side IOs
Power and Ground	VDDHSH	H4	P	Supply	1.2 V power supply for host side IOs
Power and Ground	VDDHSH	J4	P	Supply	1.2 V power supply for host side IOs
Power and Ground	VDDHSH	K4	P	Supply	1.2 V power supply for host side IOs
Power and Ground	VDDHSL	G11	P	Supply	1.2 V power supply for line side IOs
Power and Ground	VDDHSL	H11	P	Supply	1.2 V power supply for line side IOs
Power and Ground	VDDHSL	J11	P	Supply	1.2 V power supply for line side IOs
Power and Ground	VDDHSL	K11	P	Supply	1.2 V power supply for line side IOs
Power and Ground	VDDL	F8	P	Supply	1.0 V power supply for chip core
Power and Ground	VDDL	F10	P	Supply	1.0 V power supply for chip core
Power and Ground	VDDL	L8	P	Supply	1.0 V power supply for chip core
Power and Ground	VDDL	L10	P	Supply	1.0 V power supply for chip core
Power and Ground	VDDMDIO	L5	P	Supply	MDIO power supply
Power and Ground	VDDTTL	F7	P	Supply	LVTTL power supply
Power and Ground	VDDTTL	L7	P	Supply	LVTTL power supply
Receive and Transmit Path	RXIN0N	B16	I	CML	Line receive channel 0 input data, complement
Receive and Transmit Path	RXIN0P	B15	I	CML	Line receive channel 0 input data, true
Receive and Transmit Path	RXIN1N	F16	I	CML	Line receive channel 1 input data, complement
Receive and Transmit Path	RXIN1P	F15	I	CML	Line receive channel 1 input data, true
Receive and Transmit Path	RXIN2N	K16	I	CML	Line receive channel 2 input data, complement
Receive and Transmit Path	RXIN2P	K15	I	CML	Line receive channel 2 input data, true
Receive and Transmit Path	RXIN3N	P16	I	CML	Line receive channel 3 input data, complement
Receive and Transmit Path	RXIN3P	P15	I	CML	Line receive channel 3 input data, true
Receive and Transmit Path	RXOUT0N	B1	O	CML	Host transmit channel 0 output data, complement

Receive and Transmit Path	RXOUT0P	B2	O	CML	Host transmit channel 0 output data, true
Receive and Transmit Path	RXOUT1N	F1	O	CML	Host transmit channel 1 output data, complement
Receive and Transmit Path	RXOUT1P	F2	O	CML	Host transmit channel 1 output data, true
Receive and Transmit Path	RXOUT2N	K1	O	CML	Host transmit channel 2 output data, complement
Receive and Transmit Path	RXOUT2P	K2	O	CML	Host transmit channel 2 output data, true
Receive and Transmit Path	RXOUT3N	P1	O	CML	Host transmit channel 3 output data, complement
Receive and Transmit Path	RXOUT3P	P2	O	CML	Host transmit channel 3 output data, true
Receive and Transmit Path	TXIN0N	D1	I	CML	Host receive channel 0 input data, complement
Receive and Transmit Path	TXIN0P	D2	I	CML	Host receive channel 0 input data, true
Receive and Transmit Path	TXIN1N	H1	I	CML	Host receive channel 1 input data, complement
Receive and Transmit Path	TXIN1P	H2	I	CML	Host receive channel 1 input data, true
Receive and Transmit Path	TXIN2N	M1	I	CML	Host receive channel 2 input data, complement
Receive and Transmit Path	TXIN2P	M2	I	CML	Host receive channel 2 input data, true
Receive and Transmit Path	TXIN3N	T2	I	CML	Host receive channel 3 input data, complement
Receive and Transmit Path	TXIN3P	T3	I	CML	Host receive channel 3 input data, true
Receive and Transmit Path	TXOUT0N	D16	O	CML	Line transmit channel 0 output data, complement
Receive and Transmit Path	TXOUT0P	D15	O	CML	Line transmit channel 0 output data, true
Receive and Transmit Path	TXOUT1N	H16	O	CML	Line transmit channel 1 output data, complement
Receive and Transmit Path	TXOUT1P	H15	O	CML	Line transmit channel 1 output data, true
Receive and Transmit Path	TXOUT2N	M16	O	CML	Line transmit channel 2 output data, complement
Receive and Transmit Path	TXOUT2P	M15	O	CML	Line transmit channel 2 output data, true
Receive and Transmit Path	TXOUT3N	T15	O	CML	Line transmit channel 3 output data, complement
Receive and Transmit Path	TXOUT3P	T14	O	CML	Line transmit channel 3 output data, true
Reserved/No Connect	NC	A10			No connect.

Reserved/No Connect	NC	A11			No connect.
Reserved/No Connect	NC	A12			No connect.
Reserved/No Connect	NC	B12			No connect.
Reserved/No Connect	NC	C6			No connect.
Reserved/No Connect	NC	C7			No connect.
Reserved/No Connect	NC	C8			No connect.
Reserved/No Connect	NC	C9			No connect.
Reserved/No Connect	NC	C10			No connect.
Reserved/No Connect	NC	C11			No connect.
Reserved/No Connect	NC	C12			No connect.
Reserved/No Connect	NC	M12			No connect.
Reserved/No Connect	NC	N12			No connect.
Reserved/No Connect	NC	P4			No connect.
Reserved/No Connect	NC	P9			No connect.
Reserved/No Connect	NC	P10			No connect.
Reserved/No Connect	NC	P11			No connect.
Reserved/No Connect	NC	P12			No connect.
Reserved/No Connect	NC	T10			No connect.
SPI	MISO	B6	O	LVTTL	SPI slave data output
SPI	MOSI	B4	I	LVTTL	SPI slave data input. Internally pulled low.
SPI	SCK	A6	I	LVTTL	SPI slave clock input. Internally pulled low.
SPI	SSN	A4	I	LVTTL	SPI slave chip select input. Internally pulled high.

6 Package Information

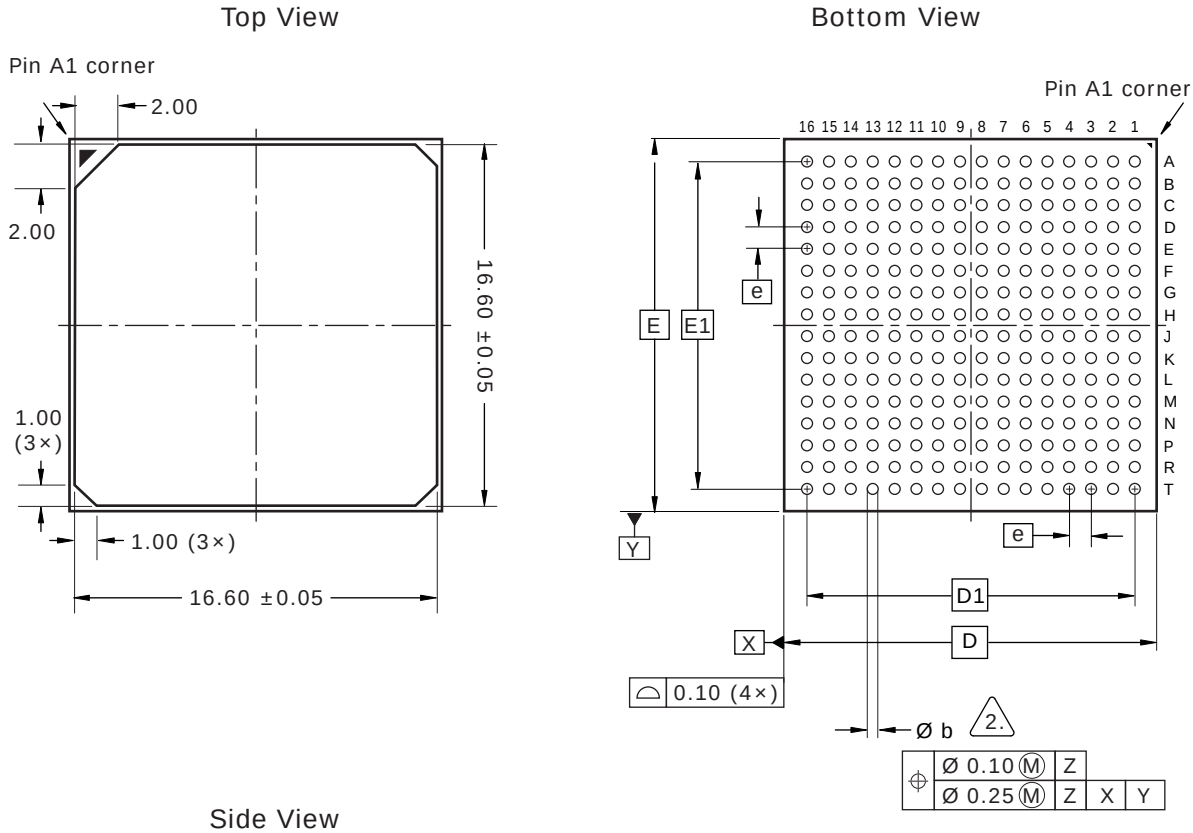
The VSC8256-01YMR package is a lead-free (Pb-free), 256-pin, flip chip ball grid array (FCBGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 2.7 mm maximum height.

Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

6.1 Package Drawing

The following illustration shows the package drawing for the VSC8256-01 device. The drawing contains the top view, bottom view, side view, detail views, dimensions, tolerances, and notes.

Figure 29 • **VSC8256-01 Package**



Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A	2.20	2.45	2.70
A1	0.31		0.41
D		17.00 BSC	
E		17.00 BSC	
D1		15.00 BSC	
E1		15.00 BSC	
e		1.00 BSC	
b	0.44	0.54	0.64

Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.
3. Radial true position is represented by typical values.

6.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p

PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 28 • **Thermal Resistances**

Symbol	°C/W	Parameter
θ_{JCtop}	0.7	Die junction to package case top
θ_{JB}	13	Die junction to printed circuit board
θ_{JA}	18	Die junction to ambient
θ_{JMA} at 1 m/s	14.5	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	11.9	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using BGA packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

7 Design Considerations

This section provides information about design considerations for the VSC8256-01 device.

7.1 SPI bus speeds

The maximum speed enabled on the 4-pin slave SPI bus is 15.4 MHz in normal mode and 30 MHz in fast mode. The maximum speed for the 3-pin push out only SPI is 40 MHz.

7.2 Device clocking

Use the LREFCLK and the HREFCK inputs for the line-side and host-side PLLs, respectively. Both LREFCLK and HREFCK inputs are required at all times and must be synchronous. They can be 125 MHz or 156.25 MHz

Use the API call to set up the HREFCLK and LREFCLK pins for low swing or high swing clock inputs.

7.3 Low-power mode and SerDes calibration

SerDes re-initialization and re-calibration is required when the PHY comes out of the low power mode.

Use the API to enable the required low power and re-calibration functionality

7.4 PHY ID error with VDDLR

The VSC8256, VSC8257, and VSC8258 devices are designed to be pin compatible. However, the VSC8256 repeater has the hardware design option to ground all VDDLR core supply rails to save power on dedicated VSC8256 designs. If the goal is to achieve a three-way population option and the VDDLR supply rails of the VSC8256 are not grounded, a read of the chip ID will erroneously return “VSC8257.”

Special care should be taken when calling the API to configure the PHY.

VSC8256 can still be used on boards designed for either the VSC8257 or VSC8258 and still enable the power savings of the VSC8256. Contact Microsemi for hardware design guidelines.

7.5 KR autonegotiation/training

The 10BASE-KR autonegotiation and link training function is disabled for compatibility reasons. During VSC8256 initialization, the host-side transmitter clock is set to synchronize to the line-side receiver clock, and the line-side transmitter clock is set to synchronize to the host-side receiver clock.

7.6 1G mode operation

Designers should be aware of the following restrictions when operating the device in 1G mode.

- The host-side transmitter must be configured to lock to the host-side receiver.
- The 1G physical coding sublayer (PCS) that implements 1000BASE-X (as specified by IEEE 802.3, clause 36) and autonegotiation (as specified by IEEE 802.3, clause 37) is not present in the VSC8256, which acts as a pass-through device.
- 1G CuSFP operation at 1.25G data rate is supported on the data path. 100M data rate through oversampling in 1G mode would also work through the data path. However, because there is no autonegotiation handling in the VSC8256, either the autoneg must be disabled or the autonegotiation performed between the host MAC chip and the SFP+ module without the intervention of the VSC8256 device.

8 Ordering Information

The VSC8256YMR-01 package is a lead-free (Pb-free), 256-pin, flip chip ball grid array (FCBGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 2.7 mm maximum height.

Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8256-01 device.

Table 29 • **Ordering Information**

Part Order Number	Description
VSC8256YMR-01	Lead-free, 256-pin FCBGA with a 17 mm × 17 mm body size, 1 mm pin pitch, and 2.7 mm maximum height.