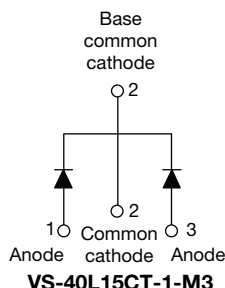
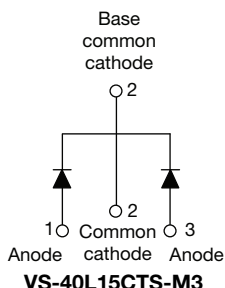
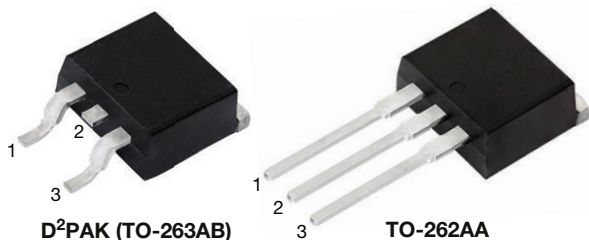


High Performance Schottky Rectifier, 2 x 20 A



FEATURES

- 125 °C T_J operation (V_R < 5 V)
- Center tap module
- Optimized for OR-ing applications
- Ultralow forward voltage drop
- High frequency operation
- High purity, high temperature epoxy encapsulation for enhanced mechanical strength and moisture resistance
- Guard ring for enhanced ruggedness and long term reliability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 245 °C
- Designed and qualified according to JEDEC®-JESD 47
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



DESCRIPTION

The center tap Schottky rectifier module has been optimized for ultralow forward voltage drop specifically for the OR-ing of parallel power supplies. The proprietary barrier technology allows for reliable operation up to 125 °C junction temperature. Typical applications are in parallel switching power supplies, converters, reverse battery protection, and redundant power subsystems.

PRIMARY CHARACTERISTICS

I _{F(AV)}	2 x 20 A
V _R	15 V
V _F at I _F	0.33 V
I _{RM} max.	600 mA at 100 °C
T _J max.	125 °C
E _{AS}	10 mJ
Package	D ² PAK (TO-263AB), TO-262AA
Circuit configuration	Common cathode

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
I _{F(AV)}	Rectangular waveform	40	A
V _{RRM}		15	V
I _{FSM}	t _p = 5 μs sine	700	A
V _F	19 A _{pk} , T _J = 125 °C (per leg, typical)	0.25	V
T _J		-55 to +125	°C

VOLTAGE RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VS-40L15CTS-M3 VS-40L15CT-1-M3	UNITS
Maximum DC reverse voltage	V _R	T _J = 100 °C	15	V
Maximum working peak reverse voltage	V _{RWM}			

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current, see fig. 5	$I_{F(AV)}$	50 % duty cycle at $T_C = 85^\circ\text{C}$, rectangular waveform	20	A
per leg			40	
Maximum peak one cycle non-repetitive surge current per leg, see fig. 7	I_{FSM}	5 μs sine or 3 μs rect. pulse	700	
		10 ms sine or 6 ms rect. pulse	330	
Non-repetitive avalanche energy per leg	E_{AS}	$T_J = 25^\circ\text{C}$, $I_{AS} = 2\text{ A}$, $L = 6\text{ mH}$	10	mJ
Repetitive avalanche current per leg	I_{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T_J maximum $V_A = 1.5 \times V_R$ typical	2	A

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	TYP.	MAX.	UNITS
Maximum forward voltage drop per leg See fig. 1	$V_{FM}^{(1)}$	19 A	-	0.41	V
		40 A	-	0.52	
		19 A	0.25	0.33	
		40 A	0.37	0.50	
Reverse leakage current per leg See fig. 2	$I_{RM}^{(1)}$	$T_J = 25^\circ\text{C}$	-	10	mA
		$T_J = 100^\circ\text{C}$	-	600	
Threshold voltage	$V_{F(TO)}$	$T_J = T_J$ maximum	0.182		V
Forward slope resistance	r_t		7.6		m Ω
Maximum junction capacitance per leg	C_T	$V_R = 5\text{ V}_{DC}$ (test signal range 100 kHz to 1 MHz), 25°C	-	2000	pF
Typical series inductance per leg	L_S	Measured lead to lead 5 mm from package body	8	-	nH
Maximum voltage rate of change	dV/dt	Rated V_R	10 000		V/ μs

Note(1) Pulse width < 300 μs , duty cycle < 2 %**THERMAL - MECHANICAL SPECIFICATIONS**

PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction temperature range		T _J		-55 to +125	°C
Maximum storage temperature range		T _{Stg}		-55 to +150	
Maximum thermal resistance, junction to case per leg		R _{thJC}	DC operation See fig. 4	1.5	°C/W
Typical thermal resistance, case to heatsink		R _{thCS}	Mounting surface, smooth and greased	0.50	
Maximum thermal resistance, junction to ambient		R _{thJA}	DC operation	40	
Approximate weight				2	g
				0.07	oz.
Mounting torque	minimum		Non-lubricated threads	6 (5)	kgf · cm (lbf · in)
	maximum			12 (10)	
Marking device			Case style D ² PAK (TO-263AB)	40L15CTS	
			Case style TO-262AA	40L15CT-1	

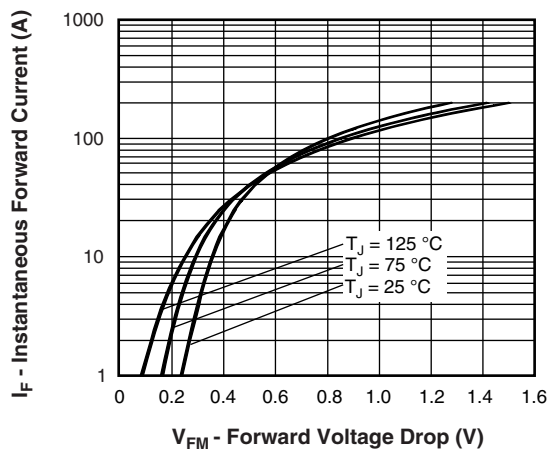


Fig. 1 - Maximum Forward Voltage Drop Characteristics

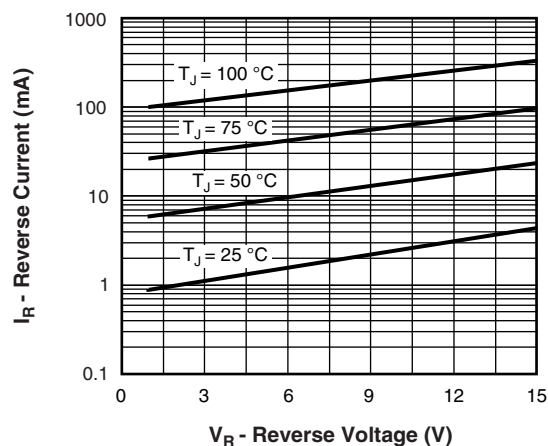


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

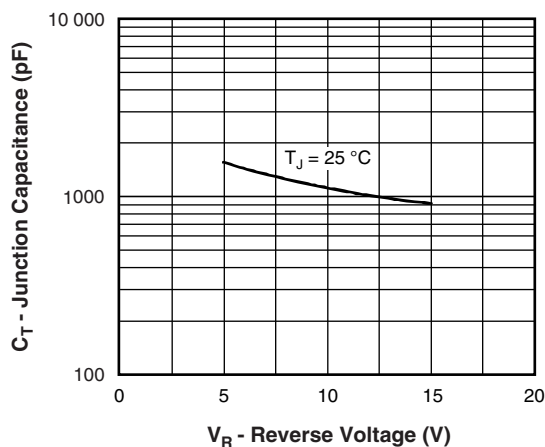
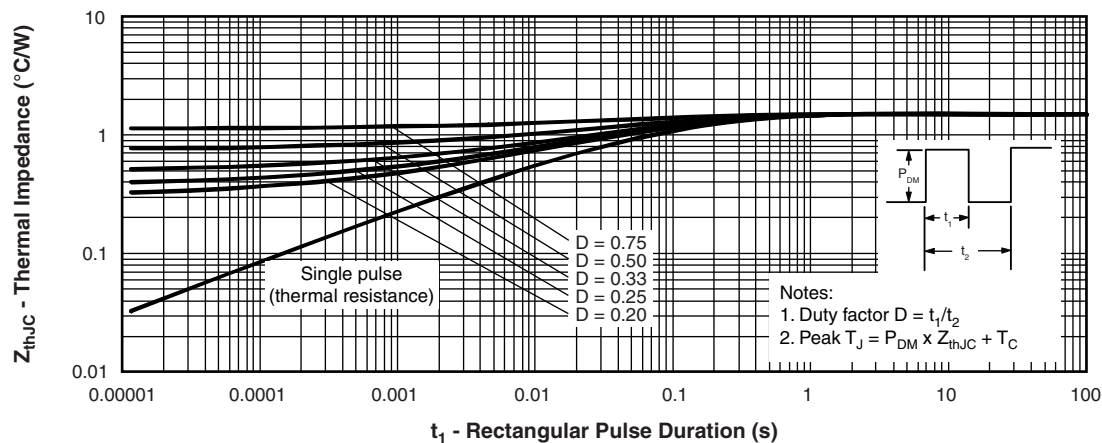


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

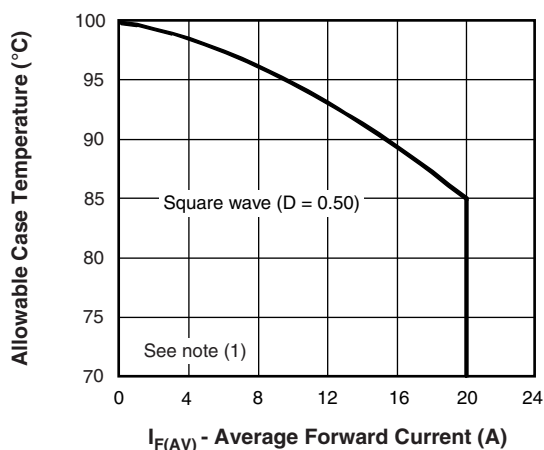


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

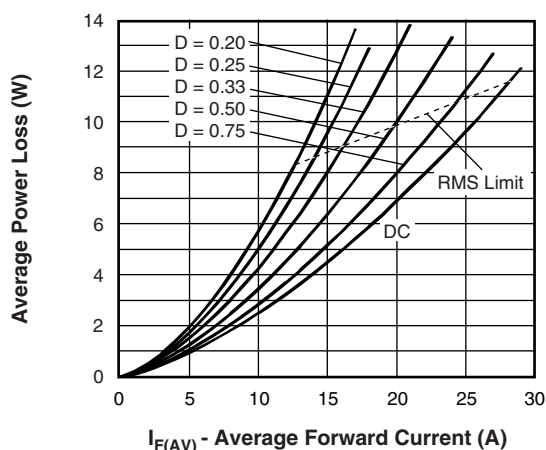


Fig. 6 - Forward Power Loss Characteristics

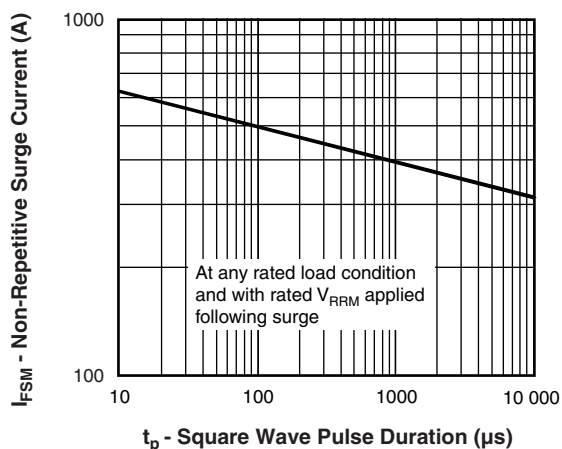


Fig. 7 - Maximum Non-Repetitive Surge Current

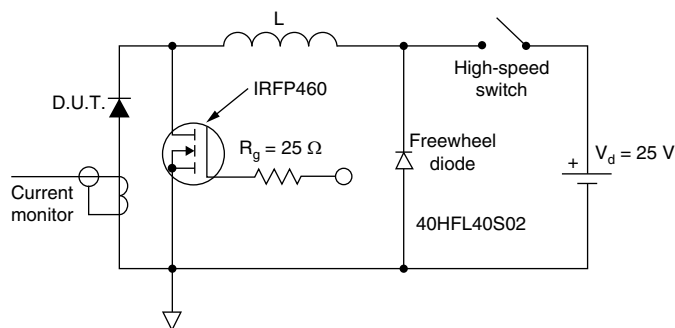


Fig. 8 - Unclamped Inductive Test Circuit

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$;
 P_d = forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 P_{dREV} = inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R

ORDERING INFORMATION TABLE

Device code	VS-	40	L	15	C	T	S	TRL	-M3
	1	2	3	4	5	6	7	8	9

- 1 - Vishay Semiconductors product
- 2 - Current rating (40 A)
- 3 - L = Schottky "L" series
- 4 - Voltage rating (15 V)
- 5 - C = common cathode
- 6 - T = TO-220
- 7 -
 - S = D²PAK (TO-263AB)
 - -1 = TO-262AA
- 8 -
 - None = tube
 - TRL = tape and reel (left oriented - for D²PAK (TO-263AB) only)
 - TRR = tape and reel (right oriented - for D²PAK (TO-263AB) only)
- 9 - -M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free

ORDERING INFORMATION (Example)		
PREFERRED P/N	BASE QUANTITY	PACKAGING DESCRIPTION
VS-40L15CTS-M3	50	Antistatic plastic tubes
VS-40L15CTSTRL-M3	800	13" diameter plastic tape and reel
VS-40L15CTSTRR-M3	800	13" diameter plastic tape and reel
VS-40L15CT-1-M3	50	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS		
Dimensions	D ² PAK (TO-263AB)	www.vishay.com/doc?96164
	TO-262AA	www.vishay.com/doc?96165
Part marking information	D ² PAK (TO-263AB)	www.vishay.com/doc?95444
	TO-262AA	www.vishay.com/doc?95443
Packaging information		www.vishay.com/doc?96424

D²PAK

DIMENSIONS in millimeters and inches

Conforms to JEDEC® outline D²PAK (SMD-220)



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	0.00	0.254	0.000	0.010	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
H	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	-	1.65	-	0.066	3
L2	1.27	1.78	0.050	0.070	
L3	0.25 BSC		0.010 BSC		
L4	4.78	5.28	0.188	0.208	

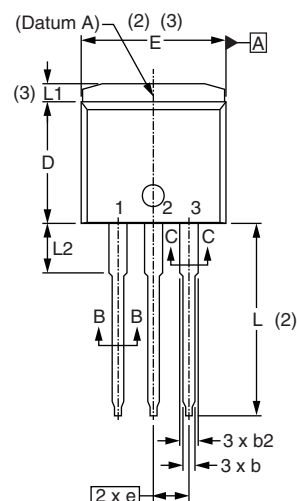
Notes

- Dimensioning and tolerancing per ASME Y14.5 M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
- Thermal pad contour optional within dimension E, L1, D1 and E1
- Dimension b1 and c1 apply to base metal only
- Datum A and B to be determined at datum plane H
- Controlling dimension: inch
- Outline conforms to JEDEC® outline TO-263AB

TO-262

DIMENSIONS in millimeters and inches

Modified JEDEC® outline TO-262

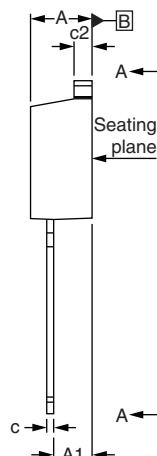


$\Phi 0.010 \text{ (M)} \text{ (B)}$



Lead assignments

- Diodes**
 1. - Anode (two die)/open (one die)
 2., 4. - Cathode
 3. - Anode



Section A - A



Section B - B and C - C
 Scale: None

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	2.03	3.02	0.080	0.119	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
L	13.46	14.10	0.530	0.555	
L1	-	1.65	-	0.065	3
L2	3.36	3.71	0.132	0.146	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
- (3) Thermal pad contour optional within dimension E, L1, D1 and E1
- (4) Dimension b1 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Outline conform to JEDEC TO-262 except A1 (maximum), b (minimum), D1 (minimum) and L2 where dimensions derived the actual package outline



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