VNQ690SP

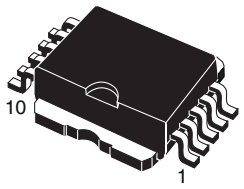
Quad channel high side solid state relay

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VNQ690SP	90mΩ(1)	10A	36V

1. Per each channel.

- CMOS compatible inputs
- Off state open load detection
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power dissipation
- Protection against loss of ground and loss of V_{CC}
- Reverse battery protection(a)



PowerSO-10

Description

The VNQ690SP is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving resistive or inductive loads with one side connected to ground.

This device has four independent channels. Built-in thermal shutdown and output current limitation protect the chip from over temperature and short circuit.

a. See *Application schematic on page 16*

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-10	VNQ690SP	VNQ690SP13TR

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1 Block diagram and pin description

Figure 1. Block diagram

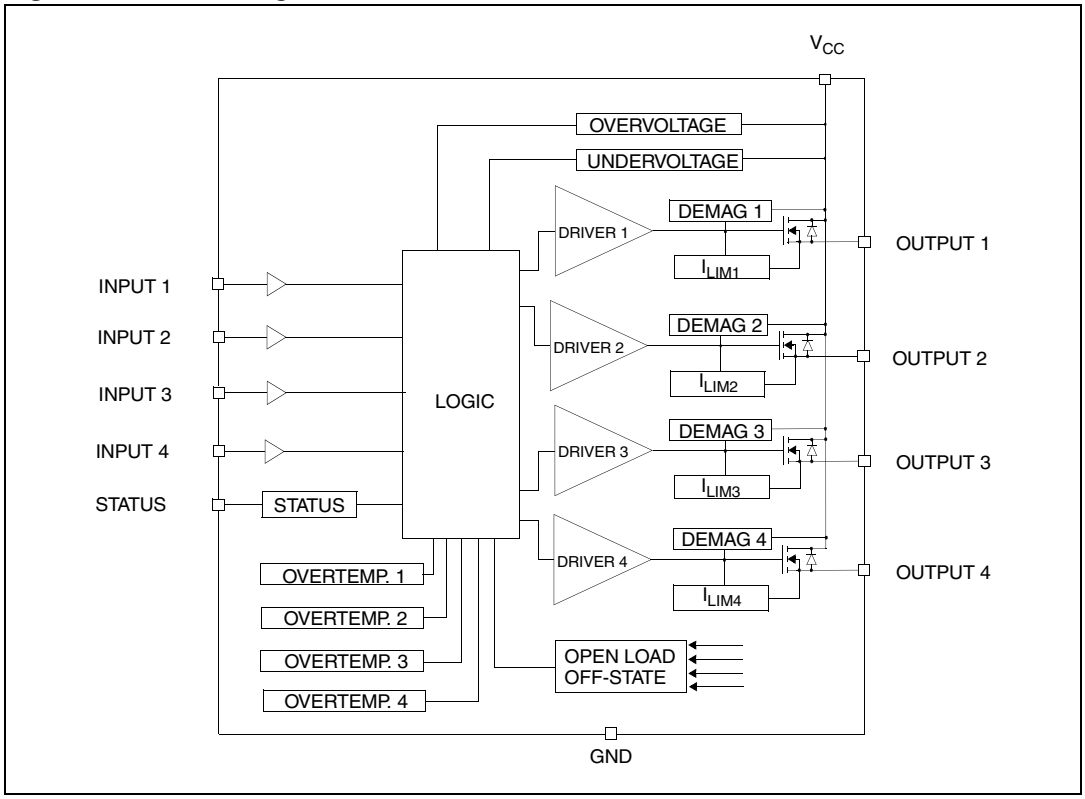


Figure 2. Configuration diagram (top view)

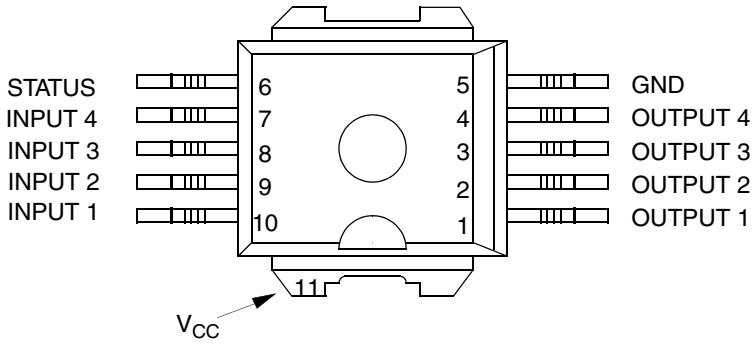


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	41	V
- V_{CC}	Reverse DC supply voltage	- 0.3	V
I_{OUT}	DC output current, per each channel	Internally limited	A
I_R	Reverse DC output current, per each channel	- 15	A
I_{IN}	Input current	+/- 10	mA
I_{STAT}	Status current	+/- 10	mA
I_{GND}	DC ground current at $T_C \leq 25°C$	-200	mA
V_{ESD}	Electrostatic discharge (human body model: R=1.5KΩ; C = 100pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000	 V V V V
E_{MAX}	Maximum switching energy ($L = 0.38mH$; $R_L = 0\Omega$; $V_{bat} = 13.5V$; $T_{jstart} = 150ºC$; $I_L = 14A$)	53	mJ
P_{tot}	Power dissipation at $T_C = 25°C$	78	W
T_j	Junction operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data (per island)

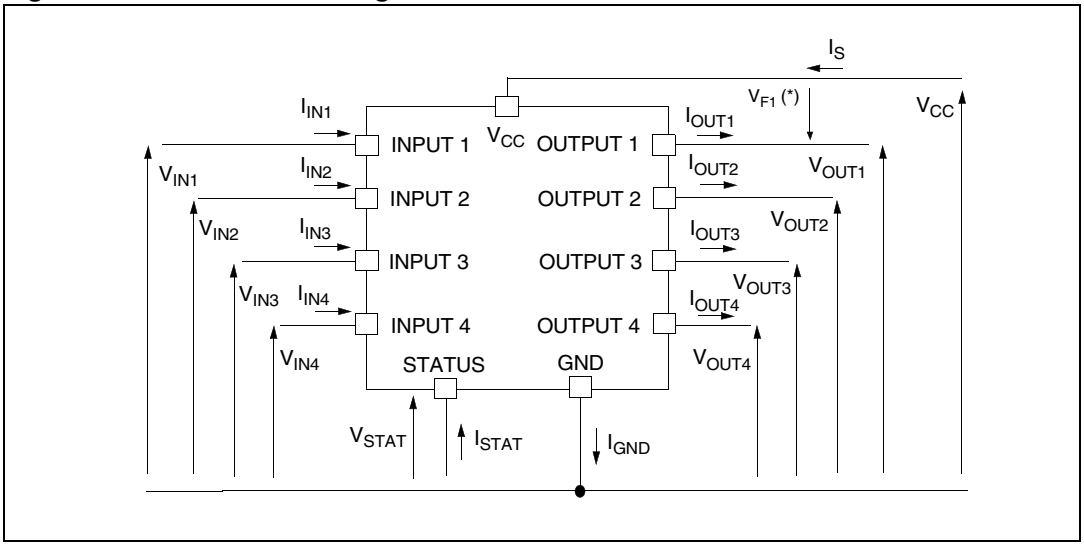
Symbol	Parameter	Value		Unit
$R_{thj\text{-}lead}$	Thermal resistance junction-case	2		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (one chip ON)	52(1)	37(2)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35 µm thick).
2. When mounted on a standard single-sided FR-4 board with 6cm^2 of Cu (at least 35 µm thick).

2.3 Electrical characteristics

Values specified in this section are for 6V < V_{CC} < 24V; -40°C < T_j < 150°C, unless otherwise stated.

Figure 3. Current and voltage conventions



Note: *V_{Fn} = V_{CCn} - V_{OUTn} during reverse battery condition.*

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}(1)	Operating supply voltage		6	13	36	V
V_{USD}(1)	Undervoltage shutdown		3.5	4.6	6	V
V_{UVhyst}(1)	Undervoltage hysteresis		0.2		1	V
V_{OV}(1)	Overvoltage shutdown		36			V
V_{OVhyst}(1)	Overvoltage hysteresis		0.25			V
R_{ON}	On state resistance	I_{OUT} = 1A; T_j = 25°C 9V < V_{CC} < 18V I_{OUT} = 1A;T_j = 150°C 9V < V_{CC} < 18V			90 180	mΩ mΩ
I_S(1)	Supply current	Off State; V_{CC} = 13.5V; V_{IN} = V_{OUT} = 0V Off State; V_{CC} = 13.5V; V_{IN} = V_{OUT} = 0V; T_j = 25°C On State; V_{CC} = 13V; V_{IN} = 3.25V; 9V < V_{CC} < 18V		12 12 6	40 25 12	µA µA mA

Table 5. Power (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off1)}$	Off state output current	$V_{IN} = V_{OUT} = 0V$	0		50	µA
$I_{L(off2)}$	Off state output current	$V_{IN} = 0V$; $V_{OUT} = 3.5V$	-75		0	µA
$I_{L(off3)}$	Off state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125°C$			5	µA
$I_{L(off4)}$	Off state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25°C$			3	µA

1. Per device.

Table 6. Protections

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15	25	°C
I_{lim}	DC short circuit current	$9V < V_{CC} < 36V$ $6V < V_{CC} < 36V$	10	14	20 20	A A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 2A$; $V_{IN} = 0V$; $L = 6mH$	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V
V_{STAT}	Status low output voltage	I_{STAT}=1.6mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT}=5V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT}=5V			25	pF
V_{SCL}	Status clamp voltage	I_{STAT}=1mA I_{STAT}=-1mA	6	6.8 -0.7	8	V V

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- $I_{OUT} = 0.9A$; $T_j = 150°C$			0.6	V

Table 8. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 13Ω channels 1,2,3,4 (see *Figure 5*)		30		µs
$t_{d(off)}$	Turn-off delay time	R_L = 13Ω channels 1,2,3,4 (see *Figure 5*)		30		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 13Ω channels 1,2,3,4 (see *Figure 5*)		See *Figure 10*		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 13Ω channels 1,2,3,4 (see *Figure 5*)		See *Figure 12*		V/µs

Table 9. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Input low level current	V_{IN} = 1.25V	1			µA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	Input high level current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = -1mA	6	6.8 - 0.7	8	V V

Table 10. Openload detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SDL}	Status delay	See *Figure 4*			20	µs
V_{OL}	Openload voltage detection threshold	V_{IN} = 0V	1.5	2.5	3.5	V
t_{DOL}	Openload detection delay at turn-off	V_{CC} = 18V			300	µs

Figure 4. Status timings

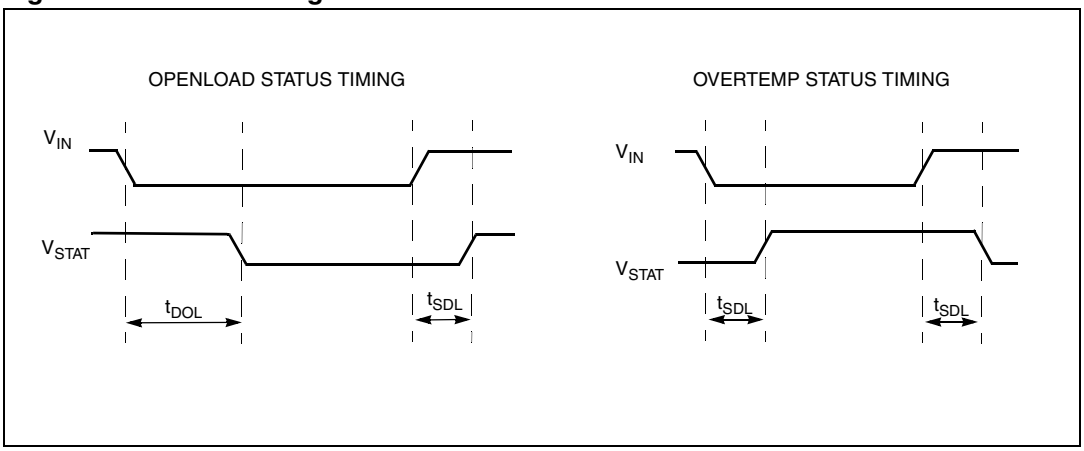


Figure 5. Switching characteristics

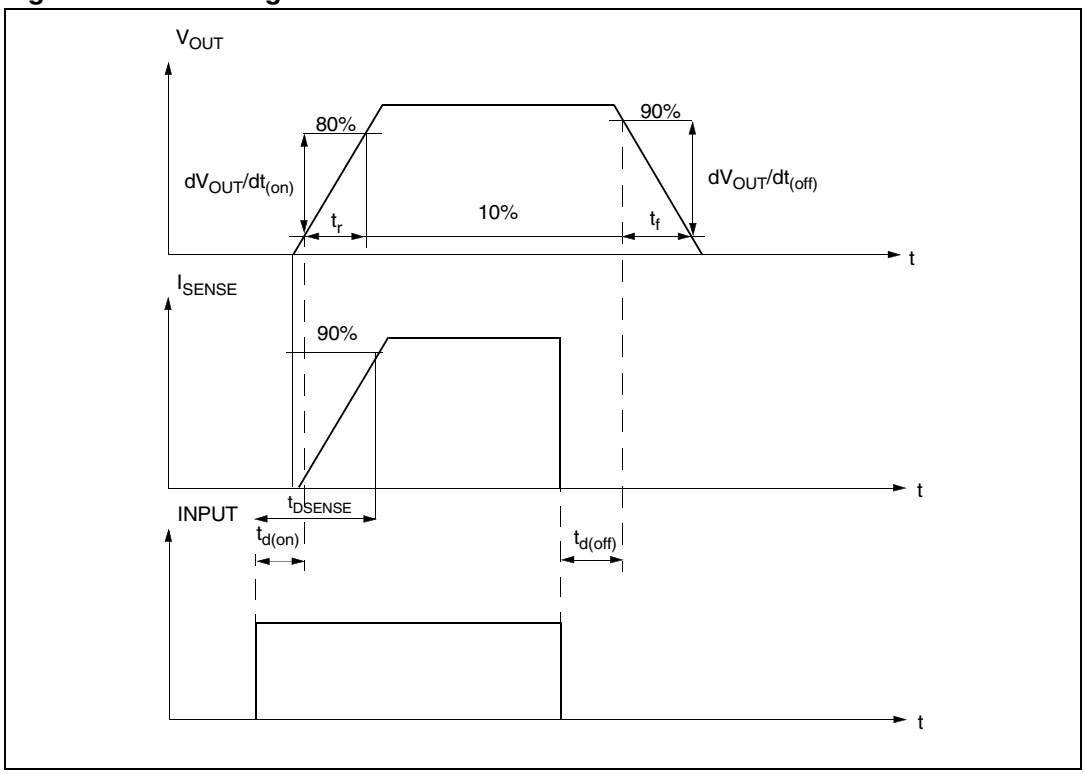


Table 11. Truth table

Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H	L X	H H
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H

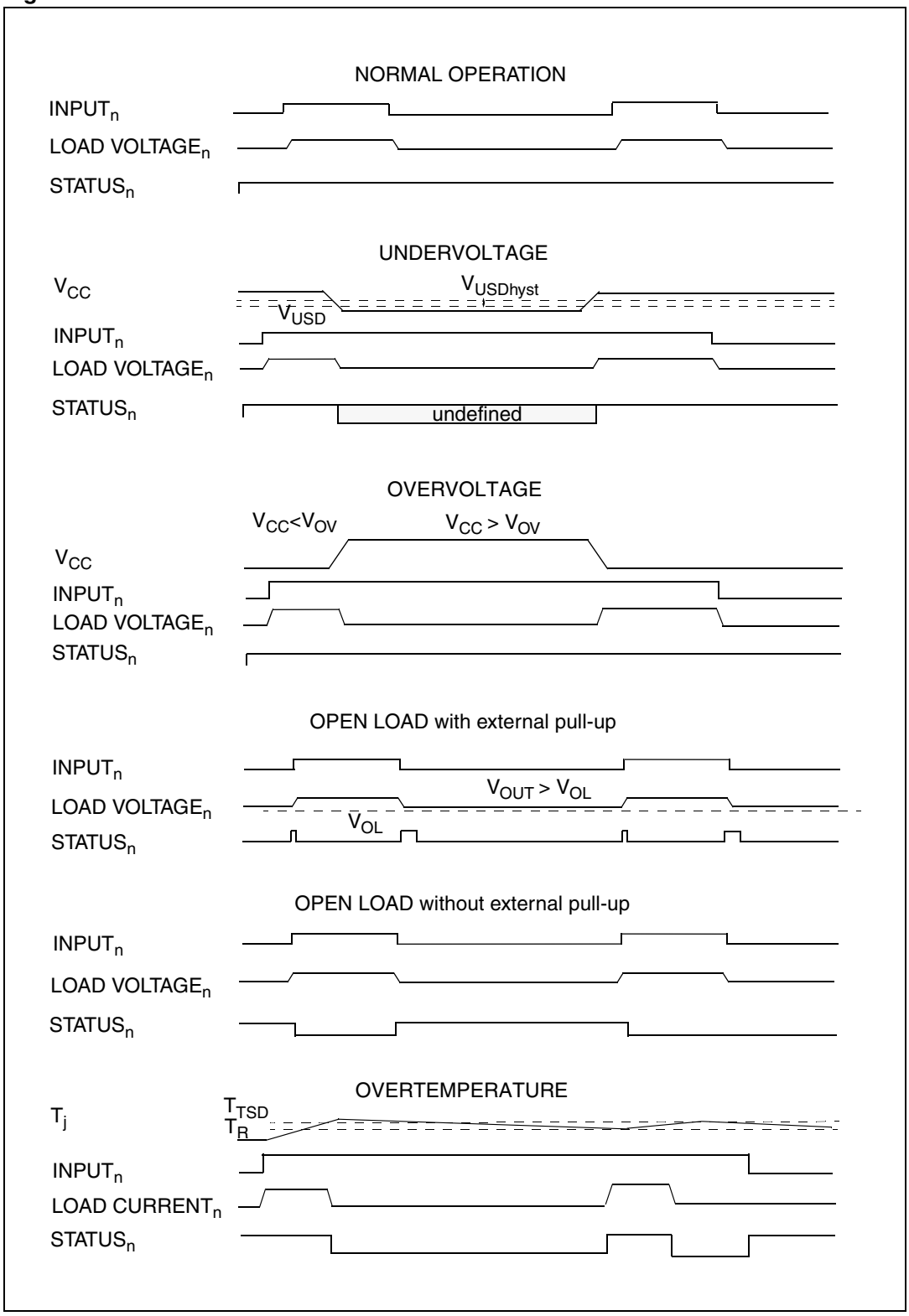
Table 12. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V	- 50V	- 75V	- 100V	2ms, 10Ω
2	+ 25V	+ 50V	+ 75V	+ 100V	0.2ms, 10Ω
3a	- 25V	- 50V	- 100V	- 150V	0.1µs, 50Ω
3b	+ 25V	+ 50V	+ 75V	+ 100V	0.1µs, 50Ω
4	- 4V	- 5V	- 6V	- 7V	100ms, 0.01Ω
5	+ 26.5V	+ 46.5V	+ 66.5V	+ 86.5V	400ms, 2Ω

ISO T/R 7637/1 Test pulse	Test level			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off state output current

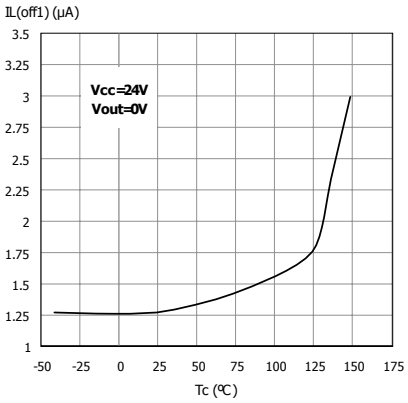


Figure 8. High level input current

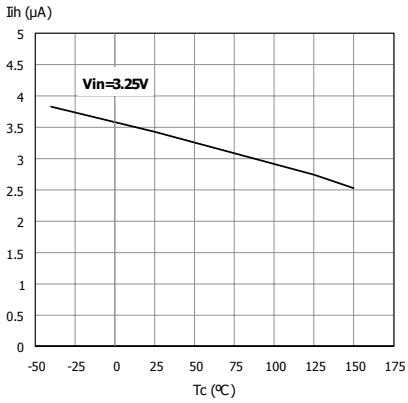


Figure 9. Input clamp voltage

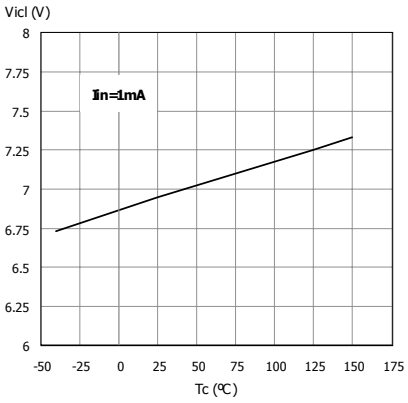


Figure 10. Turn-on voltage slope

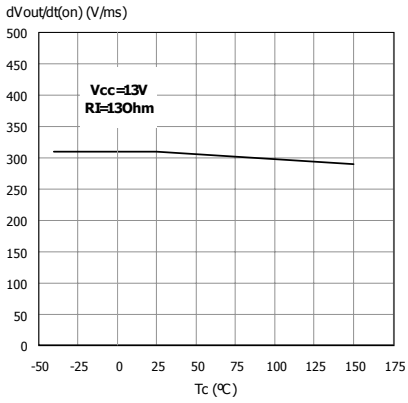


Figure 11. Overvoltage shutdown

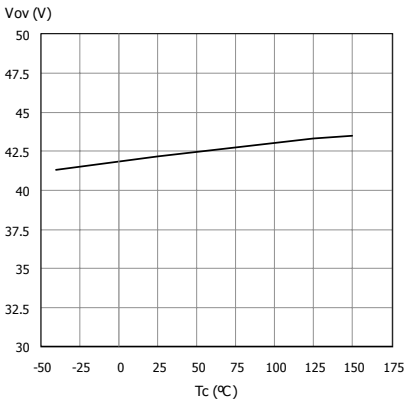


Figure 12. Turn-off voltage slope

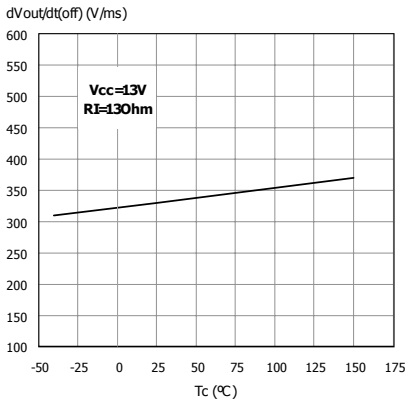


Figure 13. I_{LIM} vs T_{case}

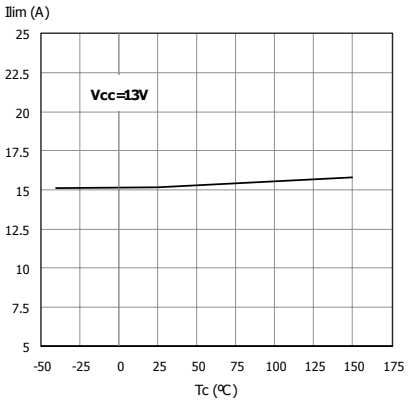


Figure 14. On state resistance vs V_{CC}

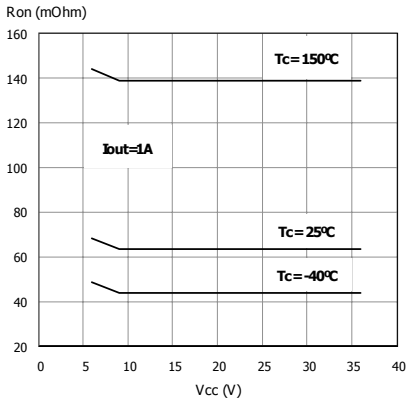


Figure 15. Input high level

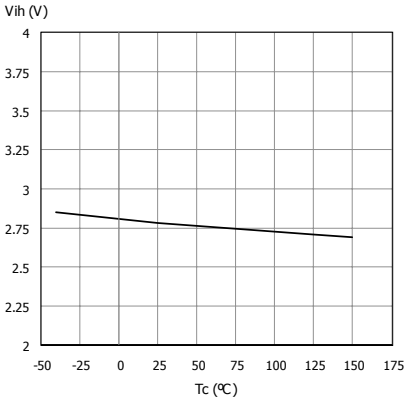


Figure 16. Input hysteresis voltage

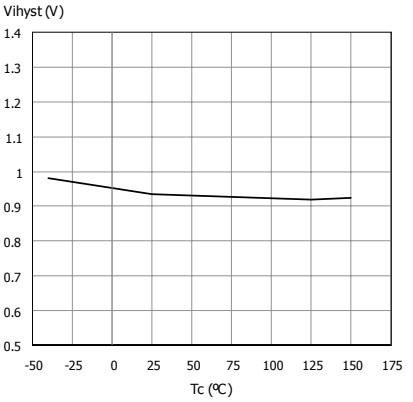


Figure 17. On state resistance vs Tcase

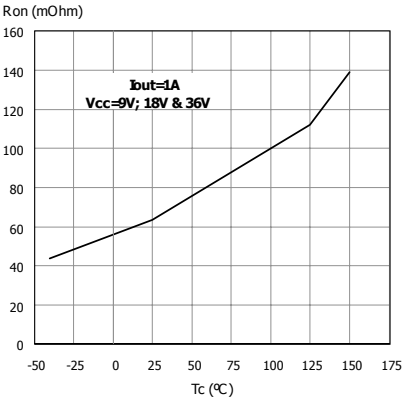


Figure 18. Input low level

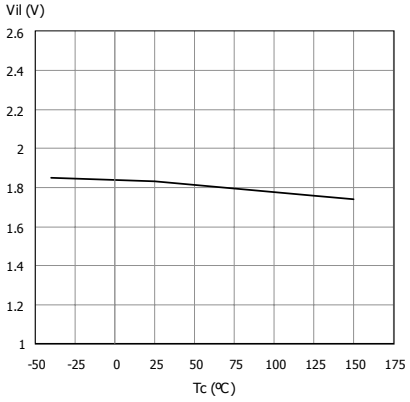


Figure 19. Status leakage current

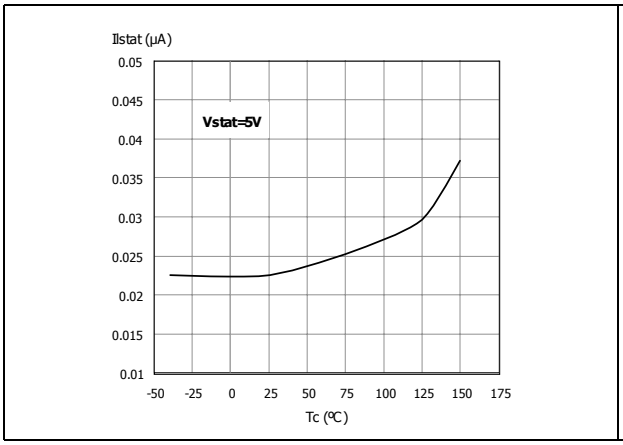


Figure 20. Status low output voltage

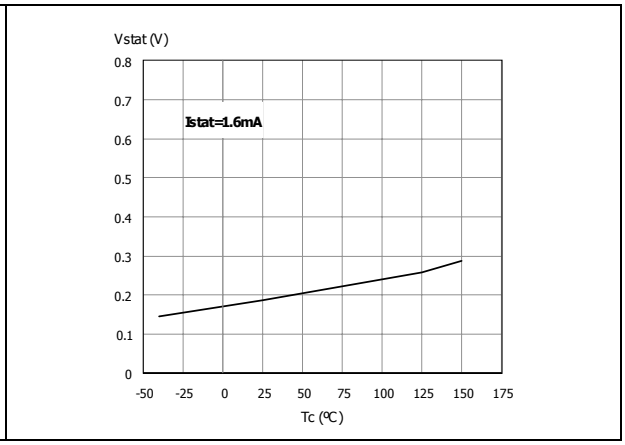


Figure 21. Status clamp voltage

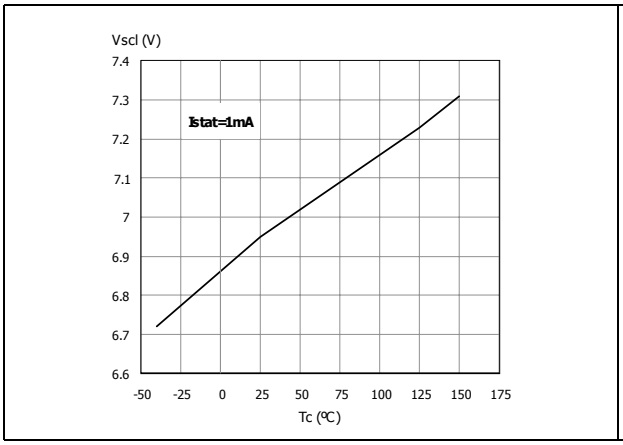
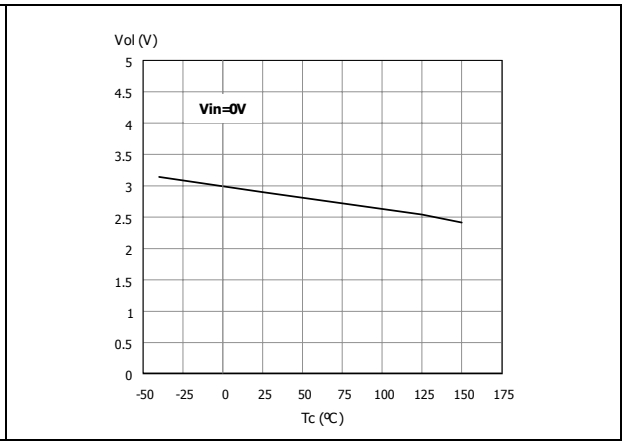
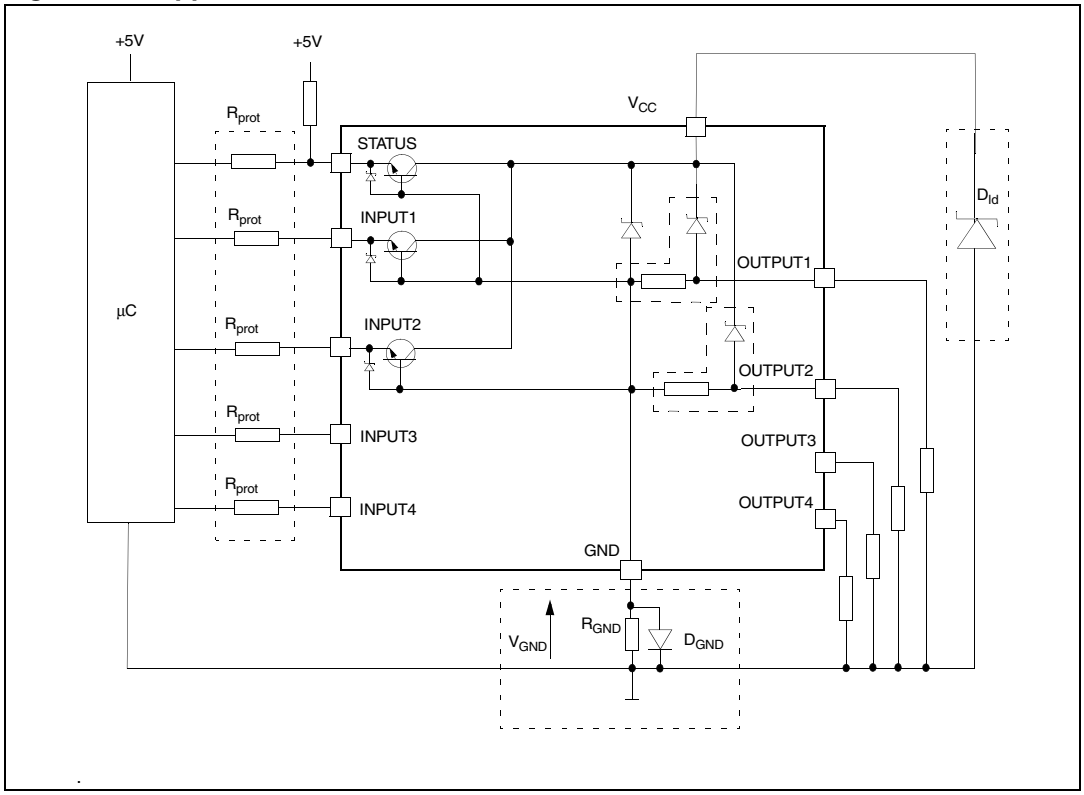


Figure 22. Openload Off state detection threshold



3 Application information

Figure 23. Application schematic



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600mV / 2 (I_{S(on)max})$
2. $R_{GND} \geq (- V_{CC}) / (- I_{GND})$

where $- I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (- V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in the ISO T/R 7637/1 table.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os:

$$- V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

V_{CCpeak} = - 100V

$I_{latchup} \geq$ 20mA

$V_{OH\mu C} \geq$ 4.5V

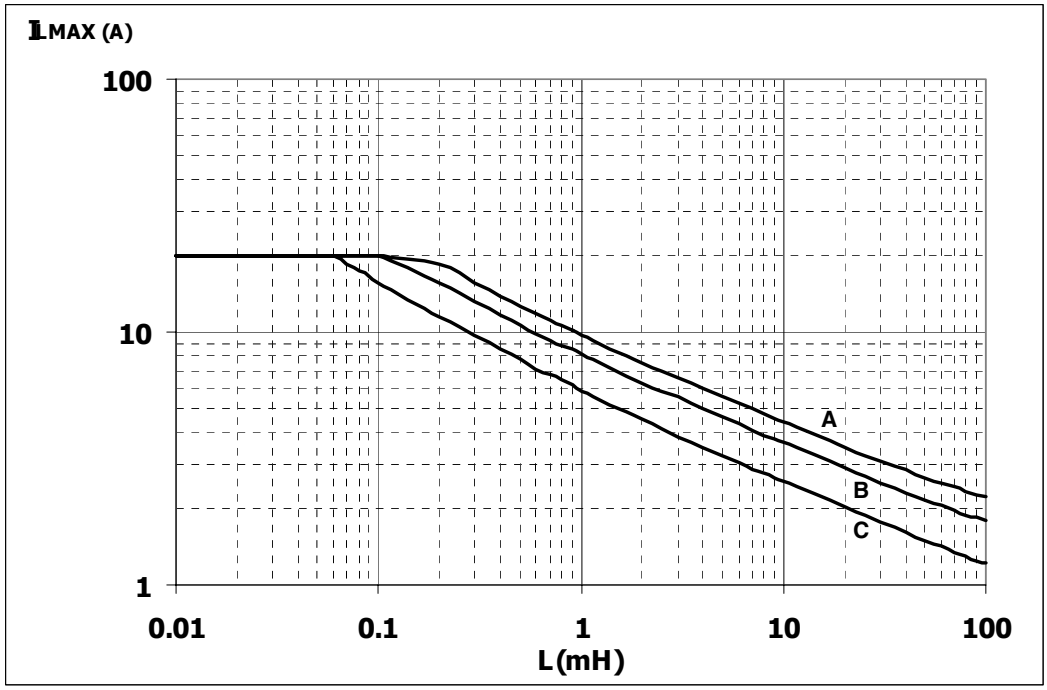
5kΩ $\leq R_{prot} \leq$ 65kΩ

Recommended values are:

R_{prot} = 10kΩ

3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

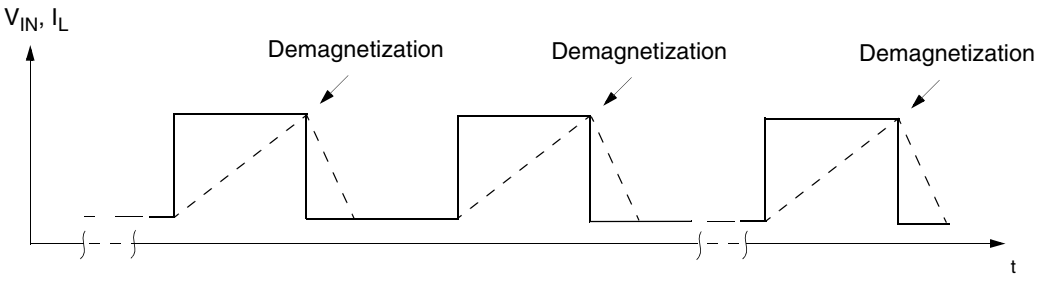
Figure 24. Maximum turn-off current versus load inductance



A = single pulse at T_{Jstart} = 150ºC

B= repetitive pulse at T_{Jstart} = 100ºC

C= repetitive pulse at T_{Jstart} = 125ºC



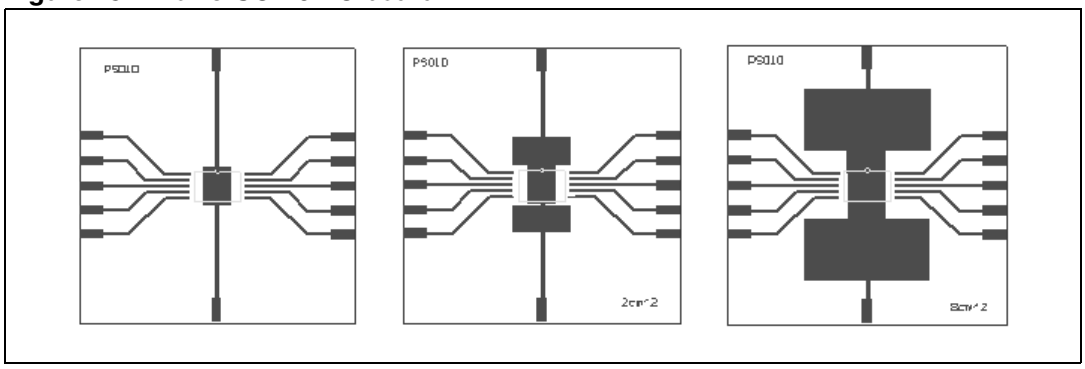
Note: Values are generated with R_L = 0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 PowerSO-10 thermal data

Figure 25. PowerSO-10 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm, Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 26. $R_{thi\text{-}amb}$ Vs PCB copper area in open box free air condition

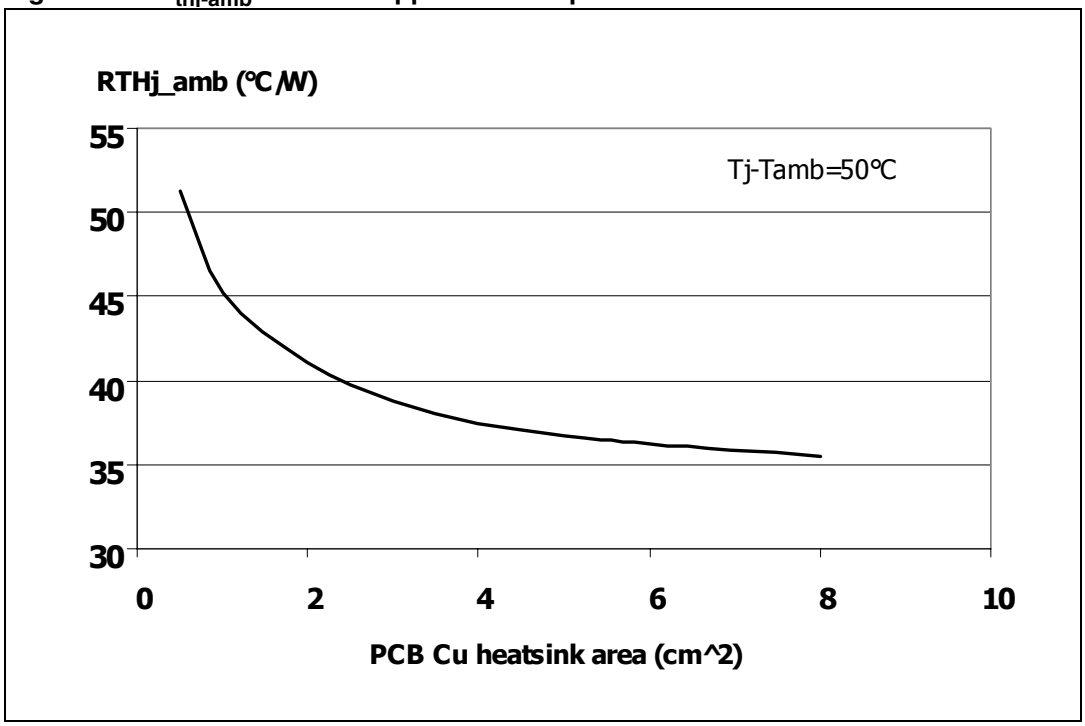
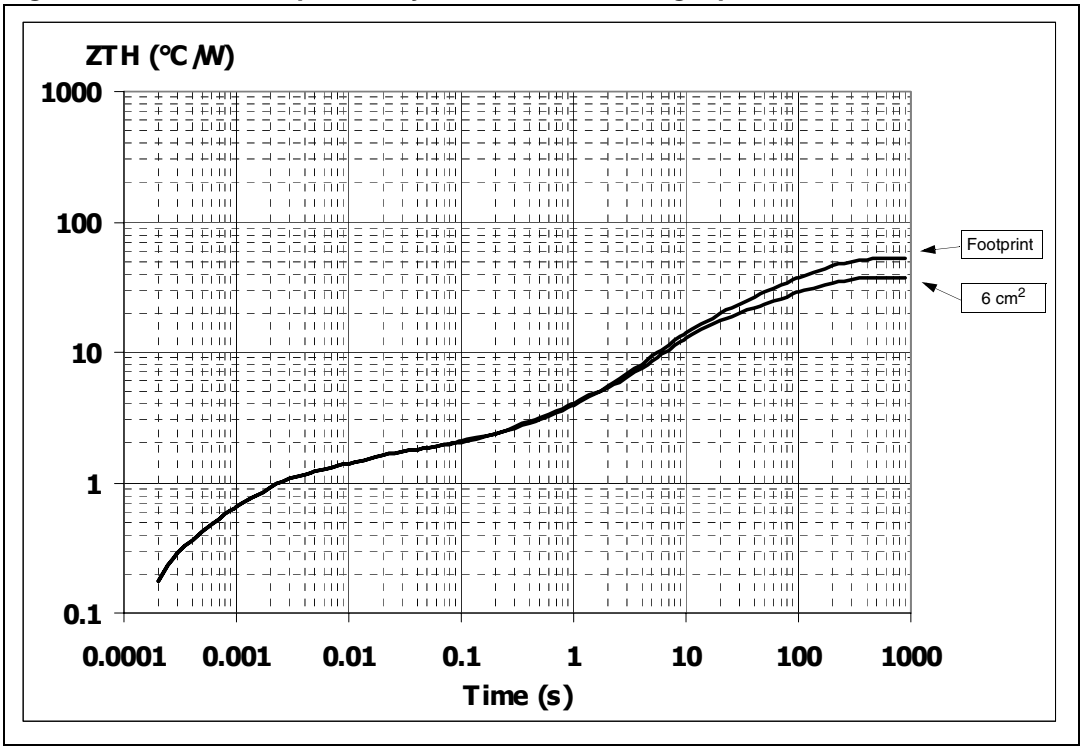


Figure 27. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 28. Thermal fitting model of a quad channel HSD in PowerSO-10

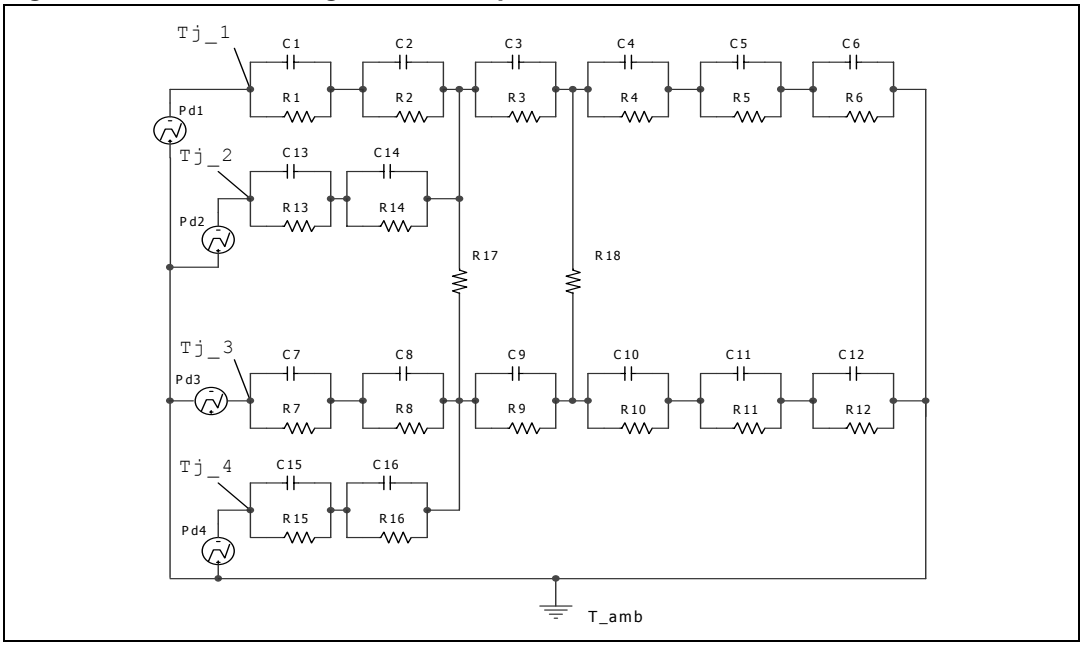


Table 13. Thermal parameters

Area / island (cm^2)	Footprint	6
R1 = R7 = R13 = R15 (°C/W)	0.18	
R2 = R8 = R14 = R16 (°C/W)	0.8	
R3 = R9 (°C/W)	0.7	
R4 = R10 (°C/W)	0.8	
R5 = R11 (°C/W)	13	
R6 = R12 (°C/W)	37	22
C1 = C7 = C13 = C15 (W.s/°C)	0.0006	
C2 = C8 = C14 = C16 (W.s/°C)	1.5E-03	
C3 = C9 (W.s/°C)	1.75E-02	
C4 = C10 (W.s/°C)	0.4	
C5 = C11 (W.s/°C)	0.75	
C6 = C12 (W.s/°C)	3	5
R17 = R18 (°C/W)	150	

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

5.2 PowerSO-10 mechanical data

Figure 29. PowerSO-10 package dimensions

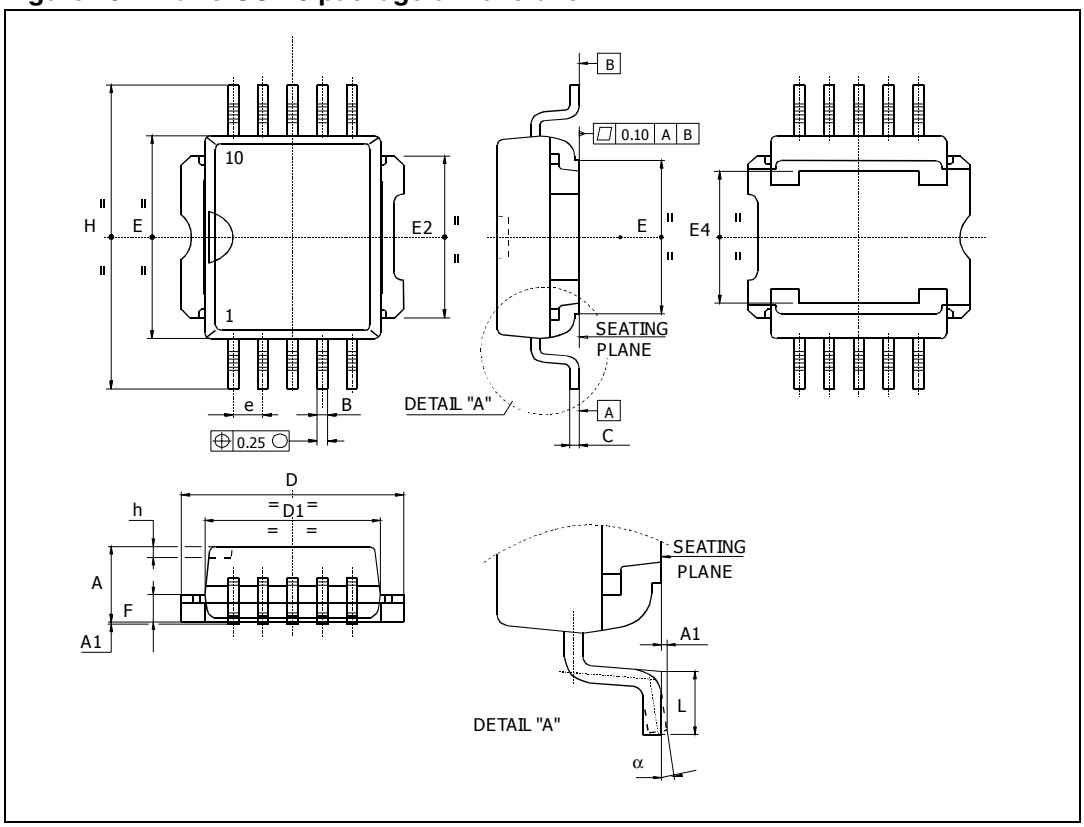


Table 14. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	3.35		3.65
A(1)	3.4		3.6
A1	0		0.10
B	0.40		0.60
B(1)	0.37		0.53
C	0.35		0.55
C(1)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2(1)	7.30		7.50
E4	5.90		6.10
E4(1)	5.90		6.30
e		1.27	
F	1.25		1.35
F(1)	1.20		1.40
H	13.80		14.40
H(1)	13.85		14.35
h		0.50	
L	1.20		1.80
L(1)	0.80		1.10
α	0°		8°
α(1)	2°		8°

1. Muar only POA P013P.

5.3 PowerSO-10 packing information

Figure 30. PowerSO-10 suggested pad layout

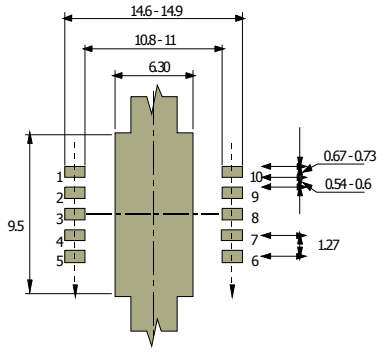
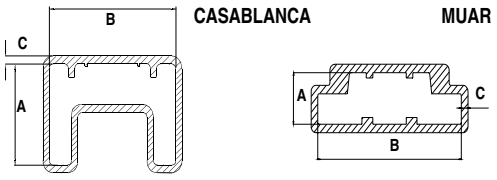


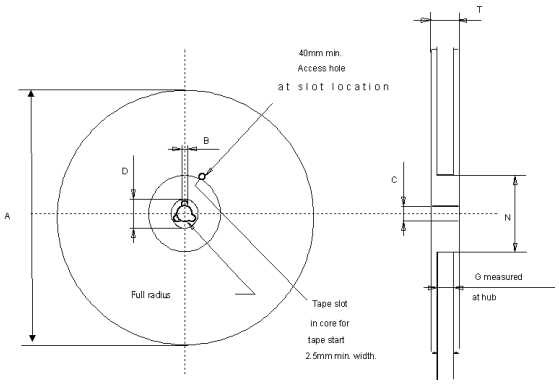
Figure 31. PowerSO-10 tube shipment (no suffix)



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 32. SO-28 tape and reel shipment (suffix "TR")



Reel dimensions

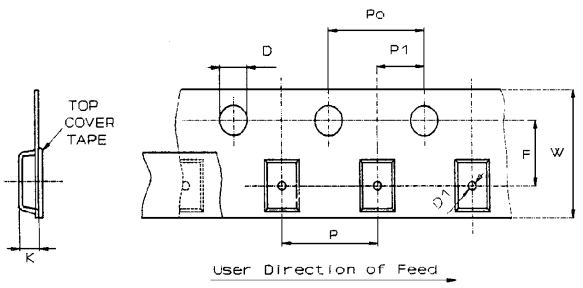
Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

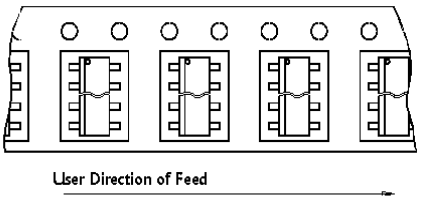
Tape dimensions

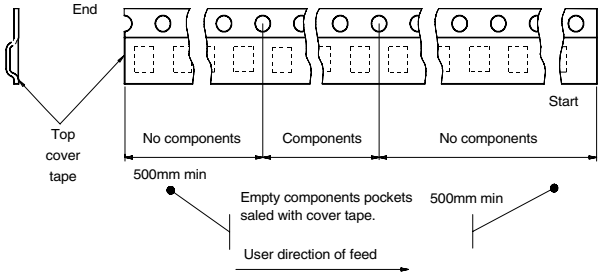
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 15. Document revision history

Date	Revision	Changes
09-Sep-2004	1	Initial release.
04-Mar-2008	2	Minor changes. Current and voltage convention update (page 2). Configuration diagram (top view) & suggested connections for unused and n.c. pins insertion (page 3). 6 cm2 Cu condition insertion in thermal data table (page 3). V_{CC} - output diode section update (page 4). Protections note insertion (page 4) Revision history table insertion (page 18). Disclaimers update (page 19).
02-Dec-2008	3	Document reformatted and restructured. Added contents, list of tables and figures. Added *ECOPACK® packages* information.

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