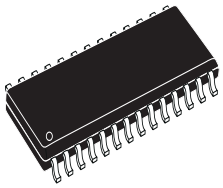
VNQ600A(8960)

QUAD CHANNEL HIGH SIDE SOLID STATE RELAY

TYPE	$R_{DS(on)}$(*)	I_{lim}	V_{CC}
VNQ600A(8960)	30mΩ	25A	36 V

(*) Per each channel at V_{CC}=13V

- DC SHORT CIRCUIT CURRENT: 25A
- CMOS COMPATIBLE INPUTS
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE & OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST: LOSS OF GROUND & LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (**)



SO-28 (DOUBLE ISLAND)

ORDER CODES		
PACKAGE	**TUBE**	**T&R**
SO-28	VNQ600A(8960)	VNQ600A(8960)TR

DESCRIPTION

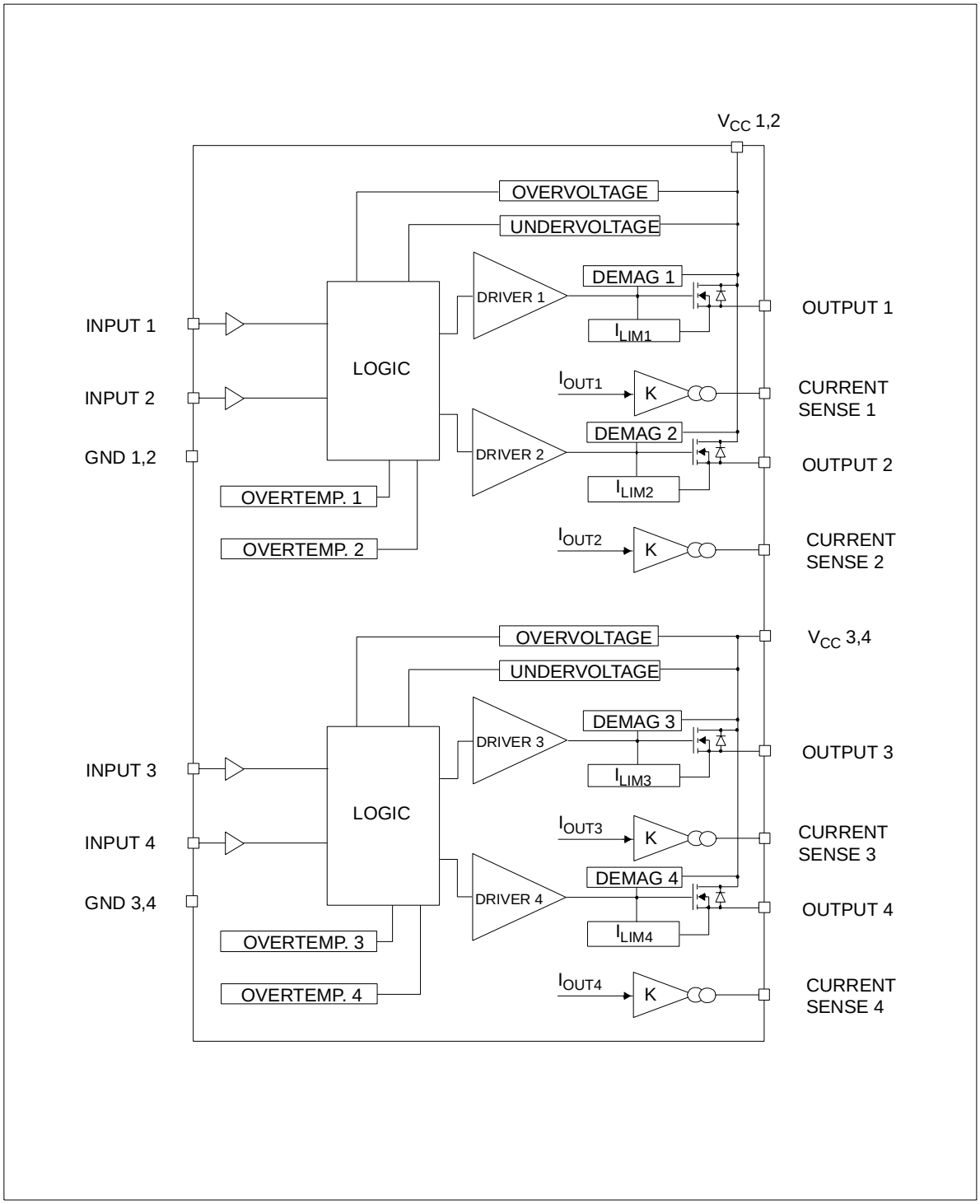
The VNQ600A(8960) is a quad HSD formed by assembling two VND600 chips in the same SO-28 package. The VND600 is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology. The VNQ600A(8960) is intended for driving any type of multiple loads with one side connected to ground. This device has four independent channels and four analog sense outputs which deliver currents proportional to the outputs currents. Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

ABSOLUTE MAXIMUM RATING

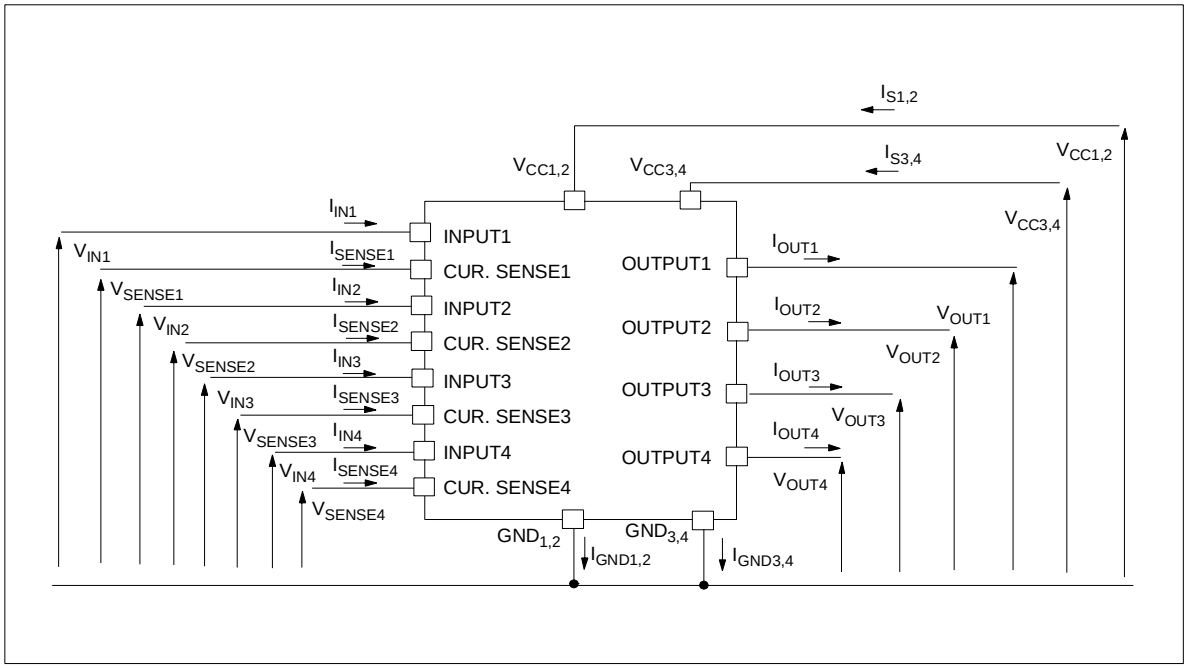
Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (continuous)	41	V
$-V_{CC}$	Reverse supply voltage (continuous)	-0.3	V
I_{OUT}	Output current (continuous), for each channel	15	A
I_R	Reverse output current (continuous), for each channel	-15	A
I_{IN}	Input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
I_{GND}	Ground current at $T_{pins} \leq 25°C$ (continuous)	-200	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - CURRENT SENSE - OUTPUT - V_{CC}	 4000 2000 5000 5000	 V V V V
E_{MAX}	Maximum Switching Energy (L=0.11mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_L=40A)	126	mJ
P_{tot}	Power dissipation (per island) at T_{lead}=25°C	6.25	W
T_j	Junction operating temperature	Internally Limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

(**) See application schematic at page 9.

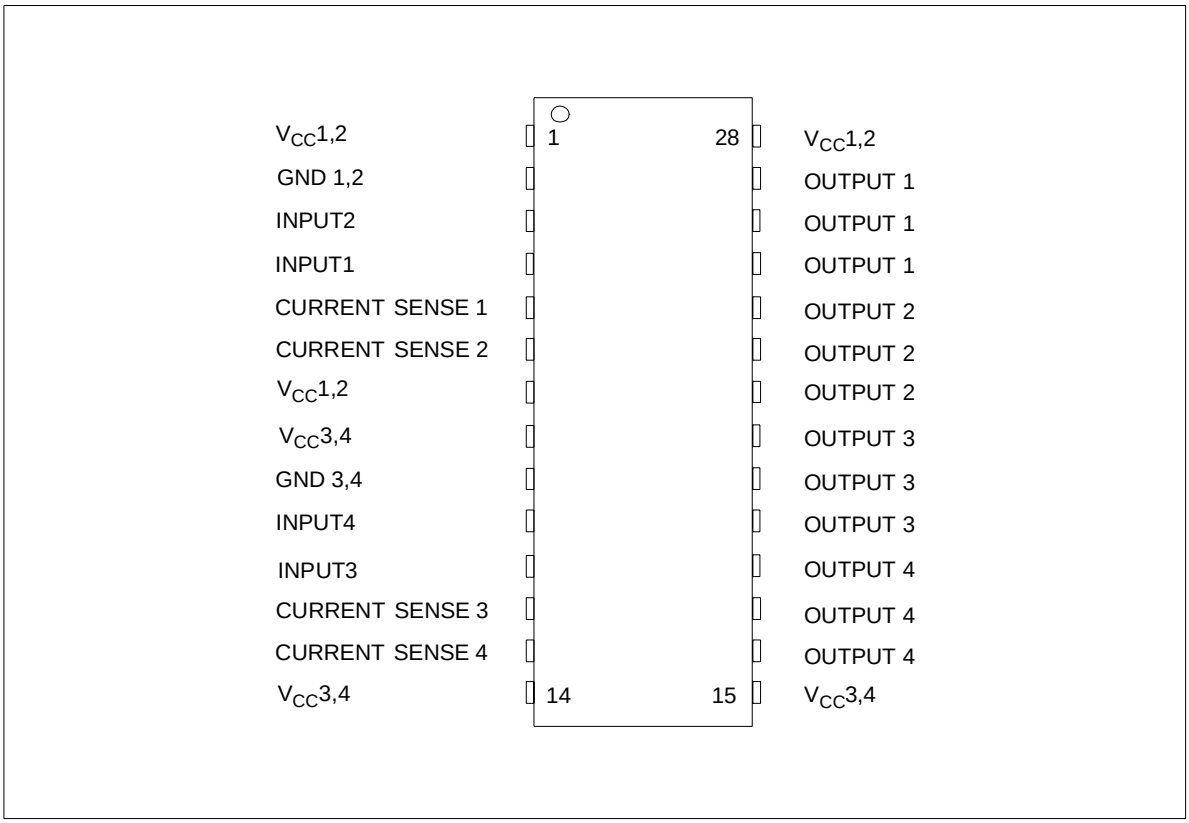
BLOCK DIAGRAM



CURRENT AND VOLTAGE CONVENTIONS



CONNECTION DIAGRAM (TOP VIEW)



THERMAL DATA (Per island)

Symbol	Parameter	Value	Unit
$R_{thj\text{-}lead}$	Thermal resistance Junction-lead	20	°C/W
$R_{thj\text{-}amb}$	Thermal resistance Junction-ambient (one chip ON)	60 (*)	°C/W
$R_{thj\text{-}amb}$	Thermal resistance Junction-ambient (two chips ON)	46 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C; unless otherwise specified)

(Per each channel)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC} (**)	Operating supply voltage		5.5	13	36	V
V_{USD} (**)	Undervoltage shut-down		3	4	5.5	V
V_{OV} (**)	Overvoltage shut-down		36			V
R_{ON}	On state resistance	I_{OUT}1,2,3,4=5A; T_j=25°C; V_{CC}=13V			30	mΩ
		I_{OUT}1,2,3,4=5A; T_j=25°C; 8V < V_{CC} < 36V			32	mΩ
		- 40°C < T_j < 150°C; V_{CC}=13V			60	mΩ
V_{clamp}	Clamp Voltage	I_{CC}=20mA (see note 1)	41	48	55	V
I_S (**)	Supply current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V		12	40	µA
		Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j=25°C		12	25	µA
		On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A; R_{SENSE}=3.9KΩ			6	mA
$I_{L(off1)}$	Off state output current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25°C			3	µA

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{D(on)}$	Turn-on delay time	R_L=2.6Ω channels 1,2,3,4 (see fig. 1)		40		µs
$t_{D(off)}$	Turn-off delay time	R_L=2.6Ω channels 1,2,3,4 (see fig. 1)		40		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L=2.6Ω channels 1,2,3,4 (see fig. 1)		0.20		V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L=2.6Ω channels 1,2,3,4 (see fig. 1)		0.20		V/µs

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	DC Short circuit current	V_{CC}=13V	25	40	70	A
		5.5V<V_{CC}<36V			70	A
T_{TSD}	Thermal shut-down temperature		150	175	200	°C
T_R	Thermal reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
V_{demag}	Turn-off output voltage clamp	I_{OUT}=2A; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.5A; T_j= -40°C...+150°C		50		mV

(**) Per island

CURRENT SENSE (9V < V_{CC}< 16V) (See Fig. 3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	$I_{OUT1,2}$=0.35A; V_{SENSE}=0.5V; T_j= -40°C...+150°C	3300	4350	6000	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=0.5A; V_{SENSE}=0.5V; other channels open; T_j= -40°C...150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=2A; V_{SENSE}=2.5V; T_j=-40°C T_j= 25°C...+150°C	3900 4150	4850 4850	6000 5800	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=5A; V_{SENSE}=4V; other channels open; T_j=-40°C...150°C	-6		+6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=4A; V_{SENSE}=4V; T_j=-40°C T_j= 25°C...+150°C	4150 4400	4900 4900	6000 5750	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=15A; V_{SENSE}=4V; other channels open; T_j=-40°C...150°C	-6		+6	%
$V_{SENSE1,2}$	Max analog sense output voltage	V_{CC}=5.5V; $I_{OUT1,2}$=2A; R_{SENSE}=10KΩ V_{CC}>8V; $I_{OUT1,2}$=4A; R_{SENSE}=10KΩ	2 4			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC}=13V; R_{SENSE}=3.9KΩ		5		V
$R_{VSENSEH}$	Analog Sense Output Impedance in Overtemperature Condition	V_{CC}=13V; T_j>T_{TSD}; All channels open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 2)			500	µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage				1.25	V
V_{IH}	High level input voltage		3.25			V
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
I_{IL}	Low level input current	V_{IN}=1.25V	20	65		µA
I_{IH}	High level input current	V_{IN}=3.25V		75	110	µA
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}= -1mA	6	6.8 -0.7	8	V V

Note 1: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.
Note 2: current sense signal delay after positive input slope.

Note: Sense pin doesn't have to be left floating.

TRUTH TABLE (per channel)

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	Test Levels I	Test Levels II	Test Levels III	Test Levels IV	Test Levels Delays and Impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1µs, 50Ω
3b	+25V	+50V	+75V	+100V	0.1µs, 50Ω
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R 7637/1 Test Pulse	Test Levels Result I	Test Levels Result II	Test Levels Result III	Test Levels Result IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 1: Switching Characteristics (Resistive load R_L=2.6Ω)

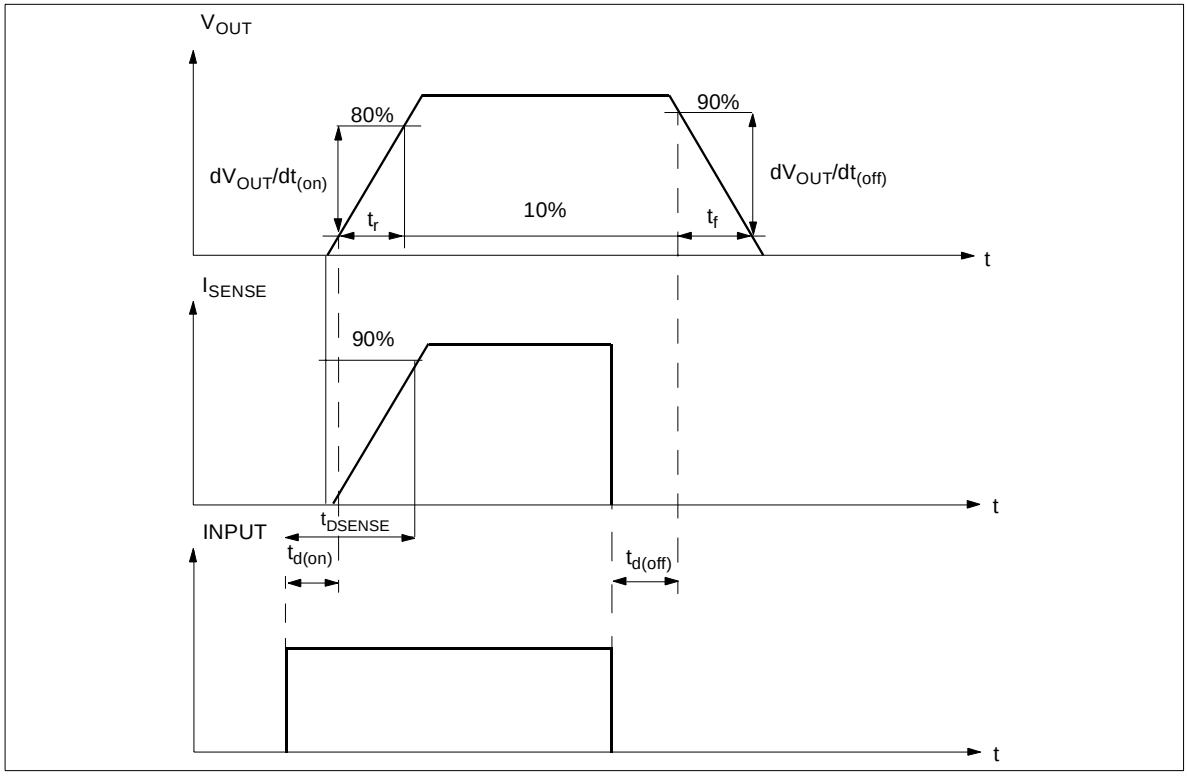
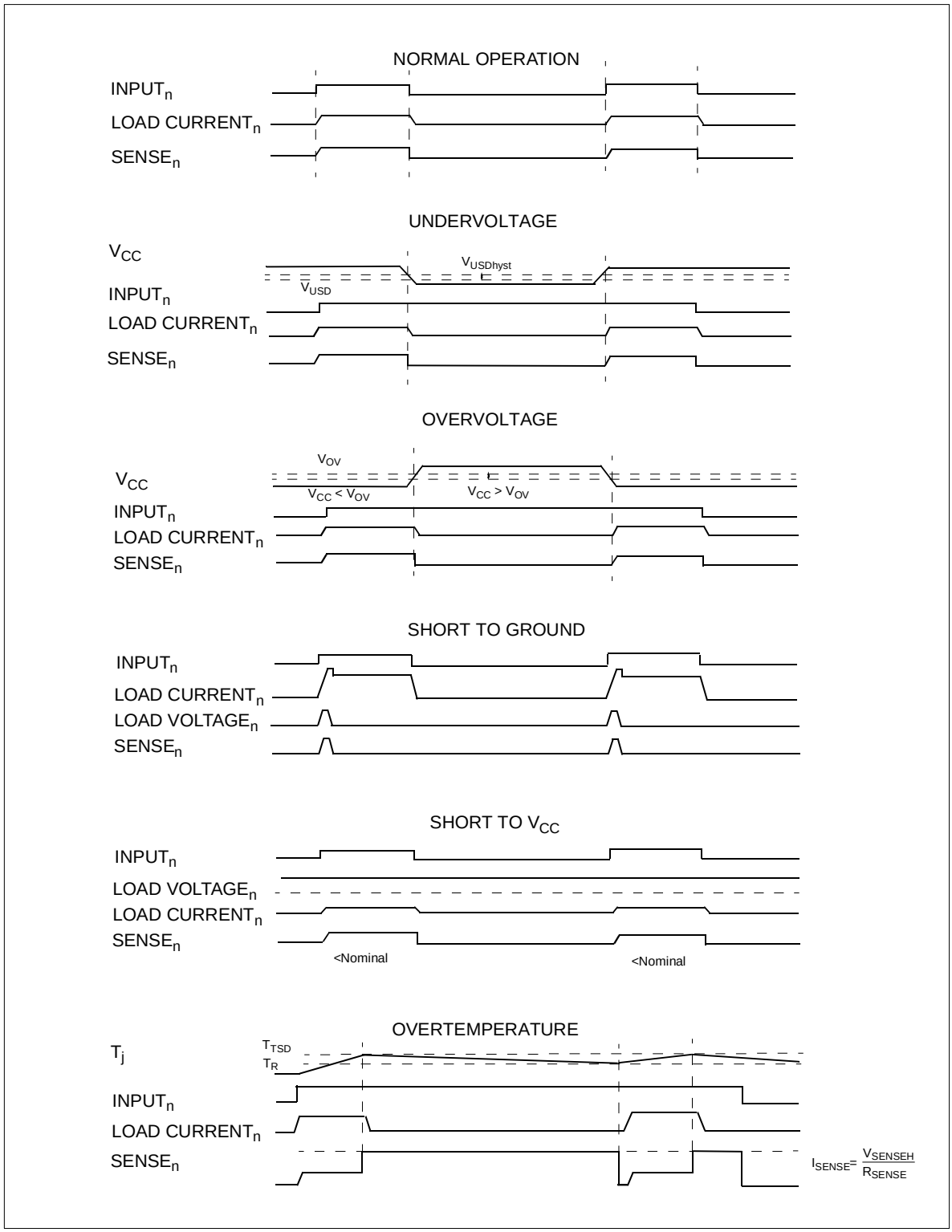
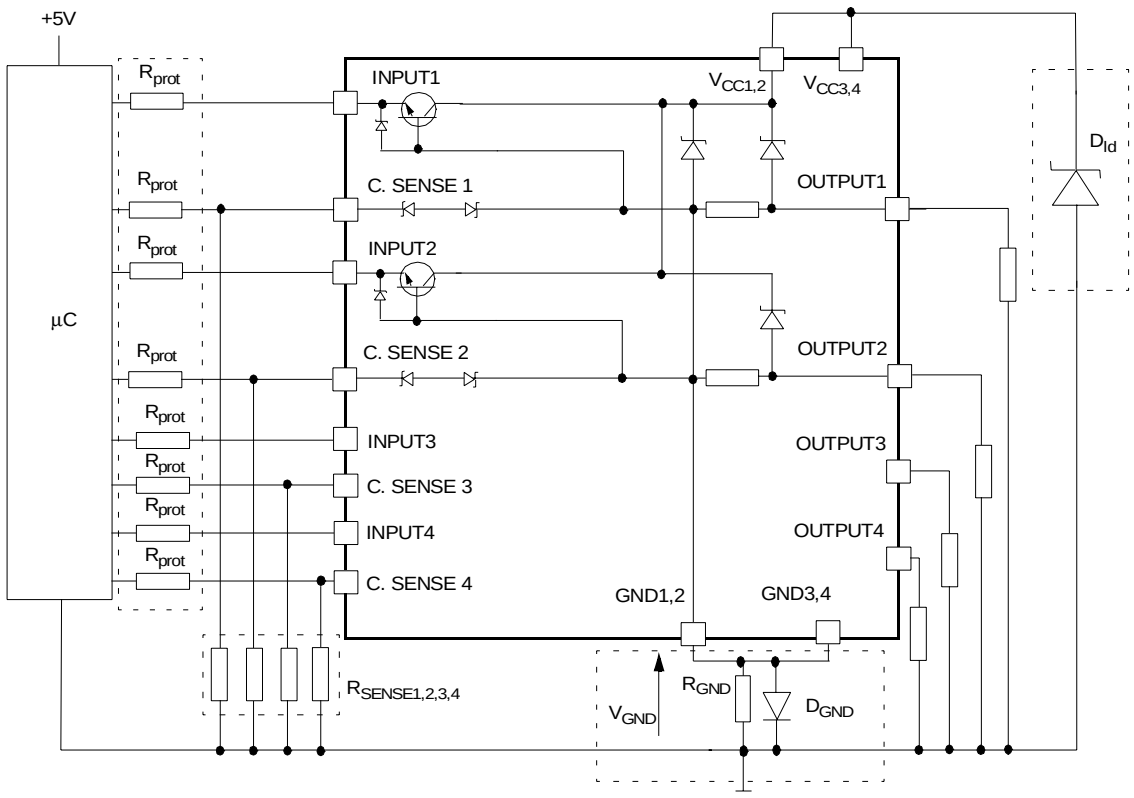


Figure 2: Waveforms (per each chip)



APPLICATION SCHEMATIC



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / 2(I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≃600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{Id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

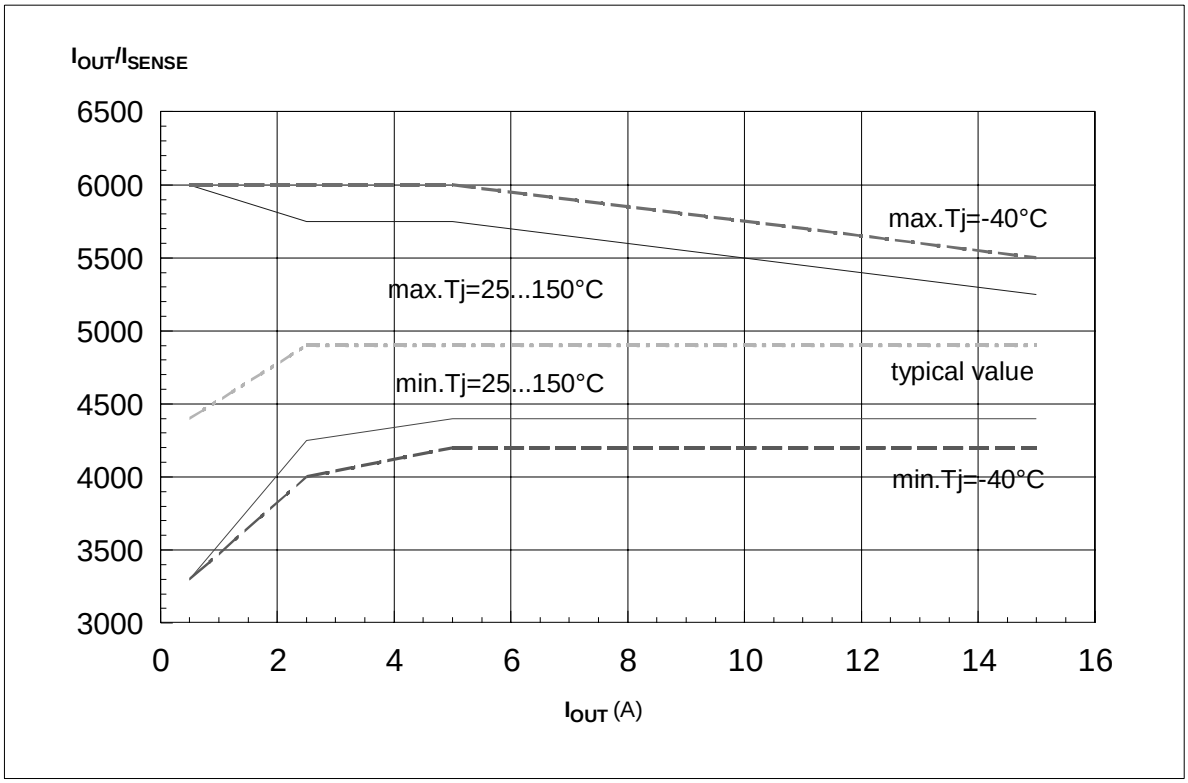
Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

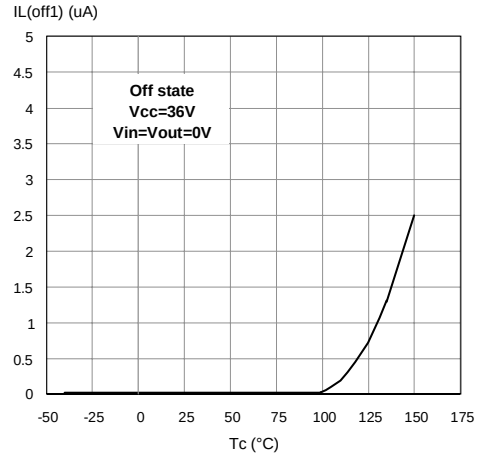
5kΩ ≤ R_{prot} ≤ 6kΩ.

Recommended R_{prot} value is 5kΩ.

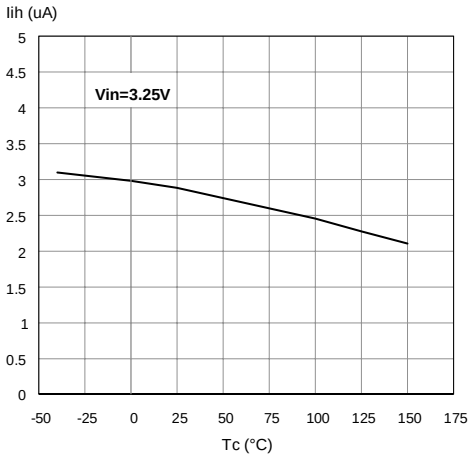
Figure 3: I_{OUT}/I_{SENSE} versus I_{OUT}



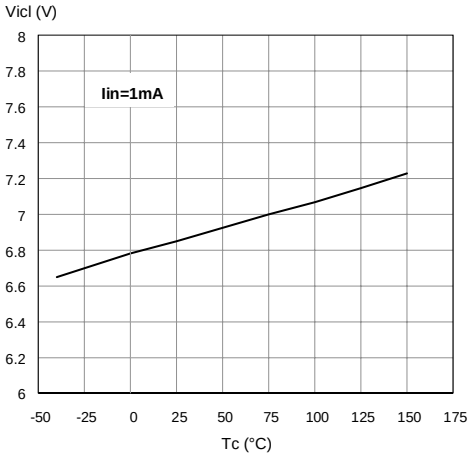
Off State Output Current



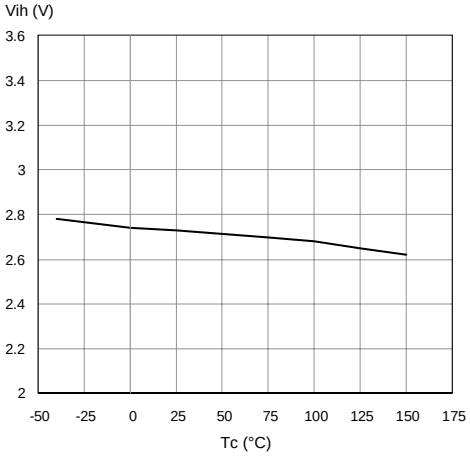
High Level Input Current



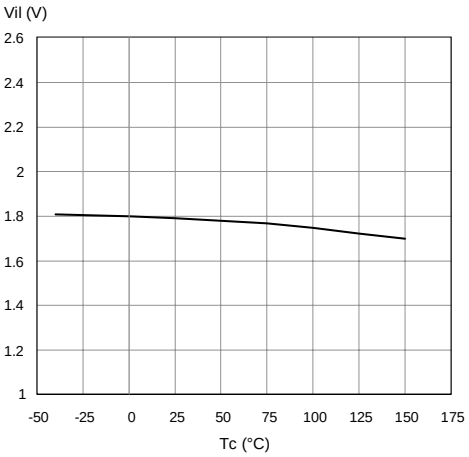
Input Clamp Voltage



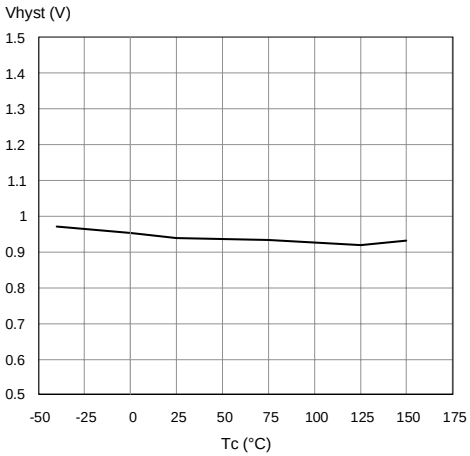
Input High Level



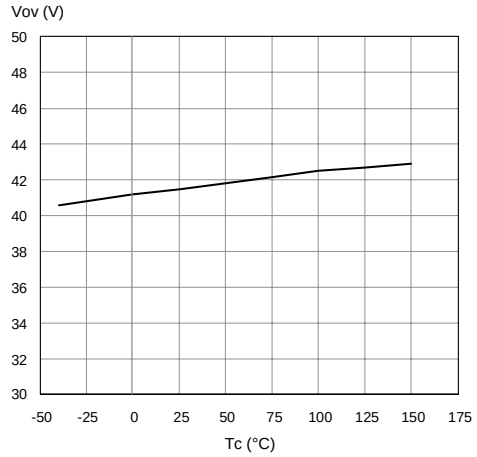
Input Low Level



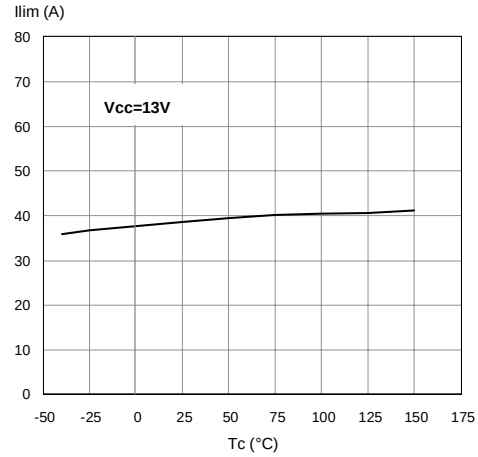
Input Hysteresis Voltage



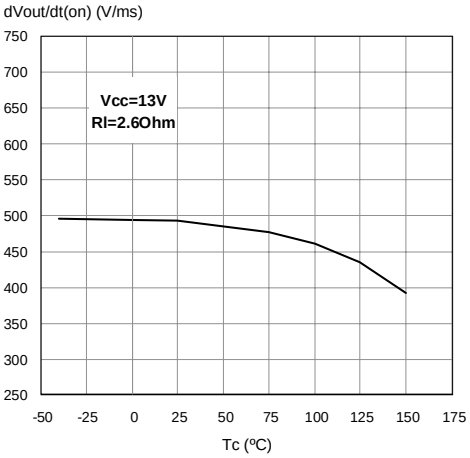
Overvoltage Shutdown



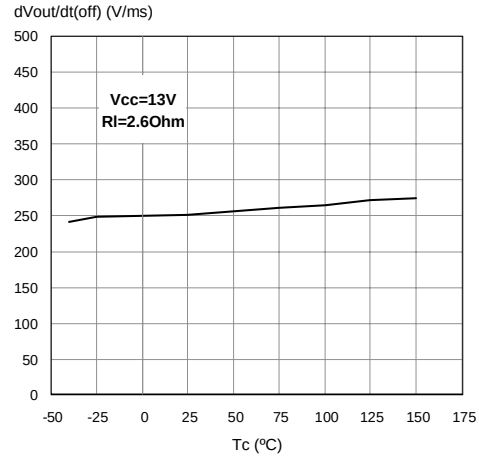
I_{LIM} Vs T_{case}



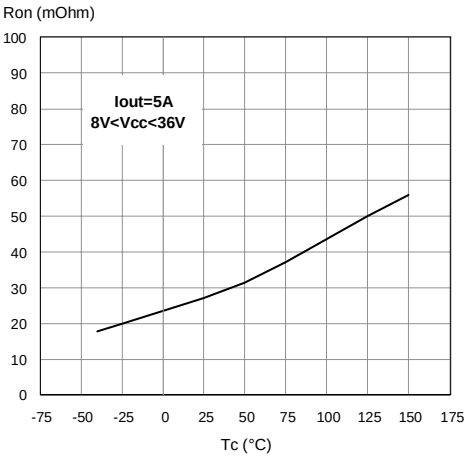
Turn-on Voltage Slope



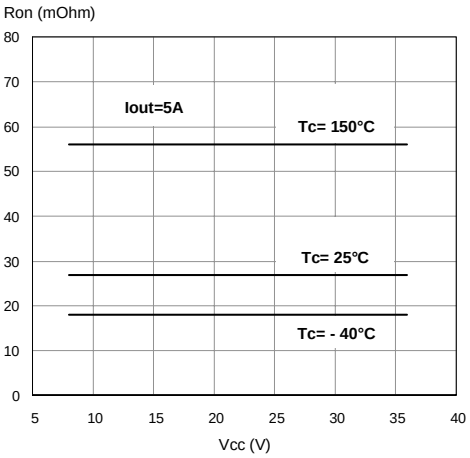
Turn-off Voltage Slope



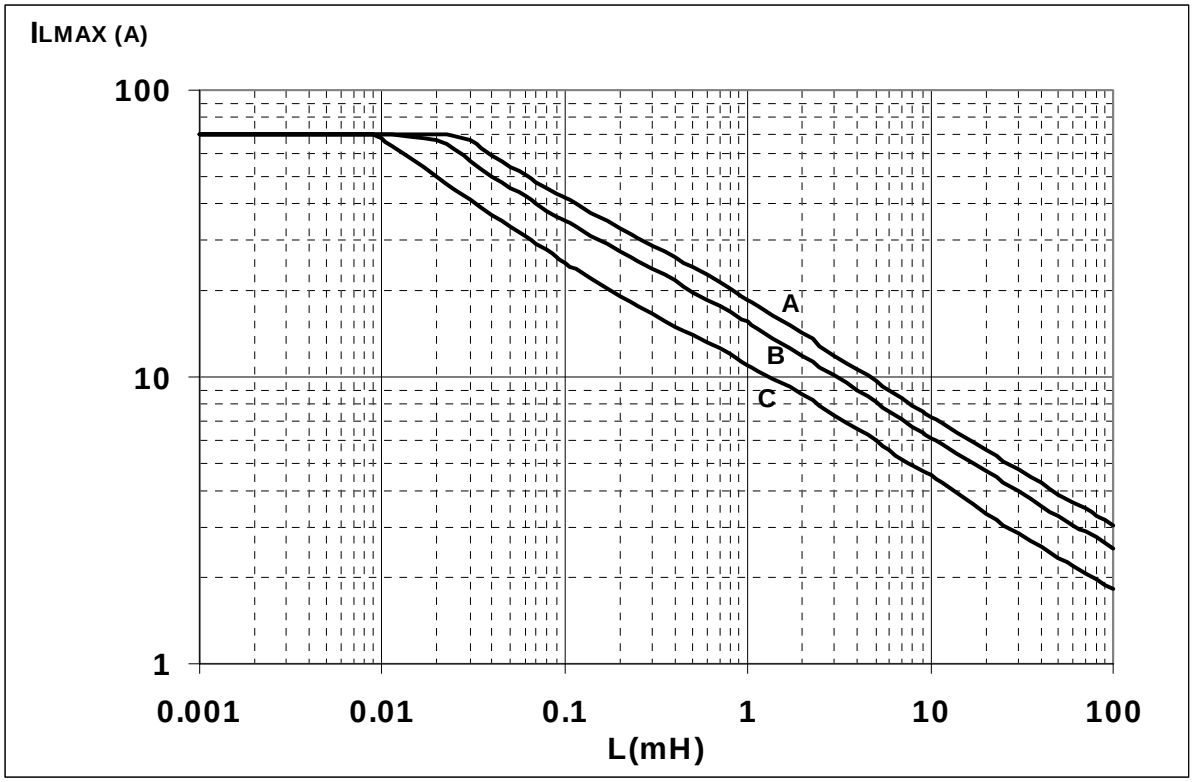
On State Resistance Vs T_{case}



On State Resistance Vs V_{CC}



Maximum turn off current versus load inductance



A = Single Pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

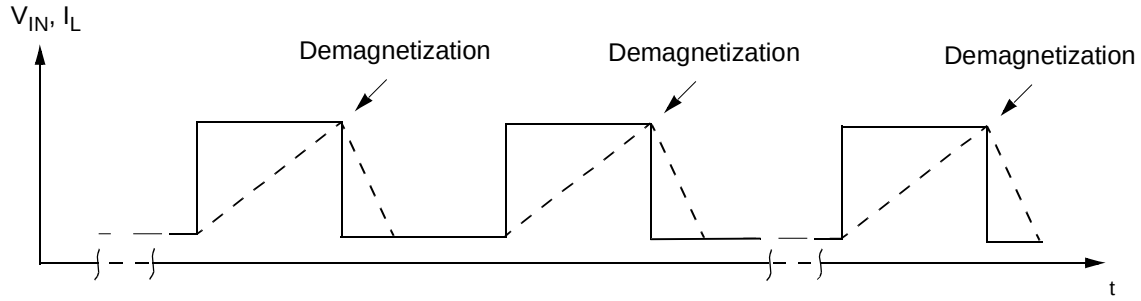
C= Repetitive Pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5V

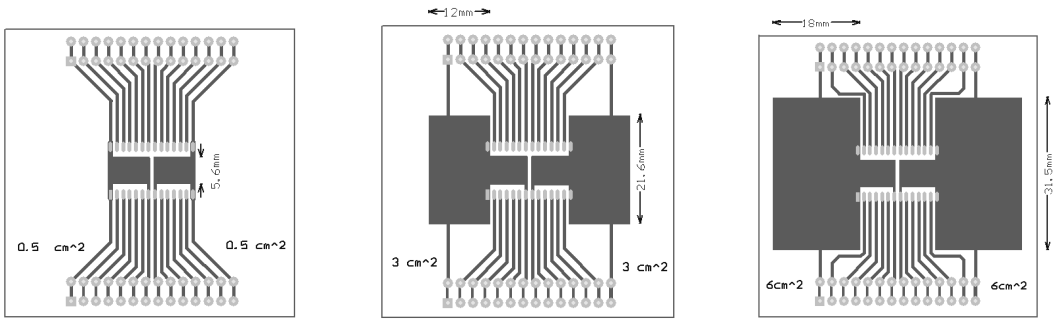
Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



SO-28 DOUBLE ISLAND THERMAL DATA

SO-28 Double island PC Board



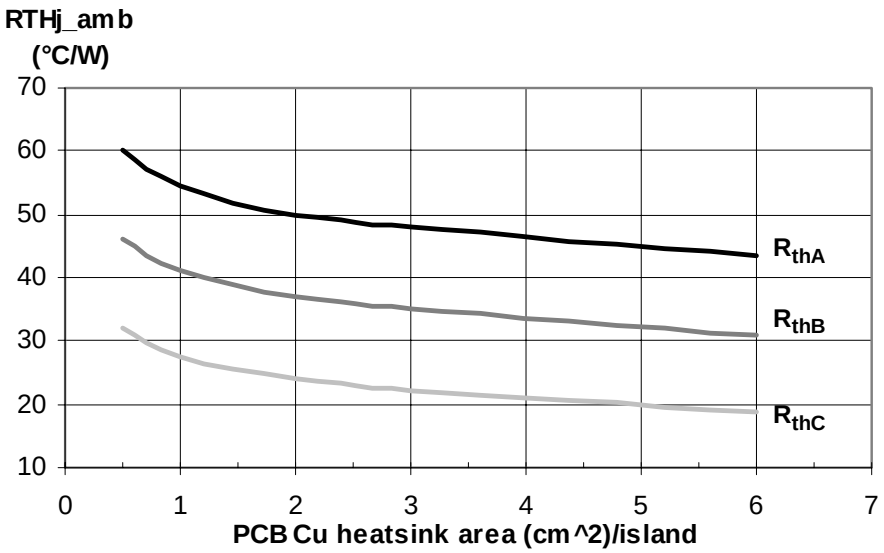
Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: 0.5cm^2, 3cm^2, 6cm^2).

Thermal calculation according to the PCB heatsink area

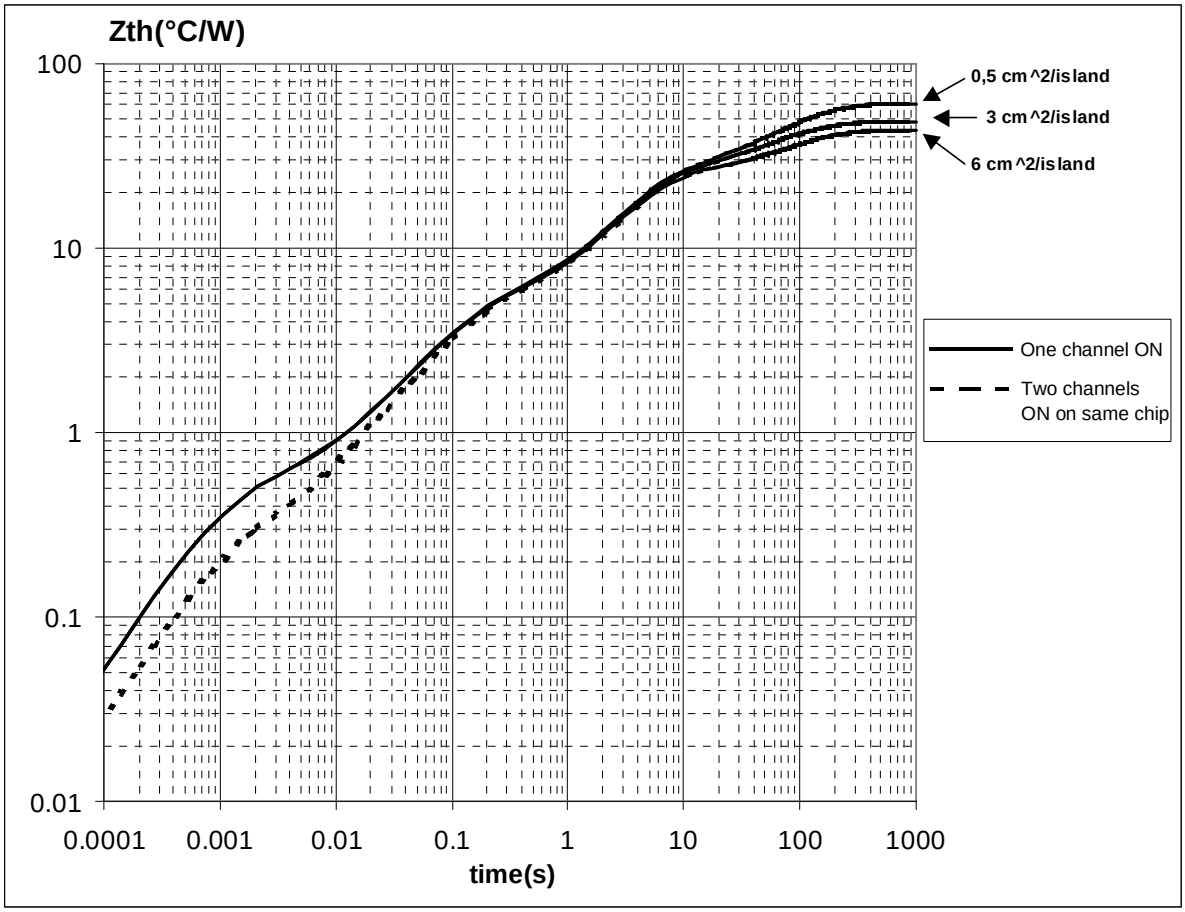
Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1}=P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

R_{thA} = Thermal resistance Junction to Ambient with one chip ON
R_{thB} = Thermal resistance Junction to Ambient with both chips ON and $P_{dchip1}=P_{dchip2}$
R_{thC} = Mutual thermal resistance

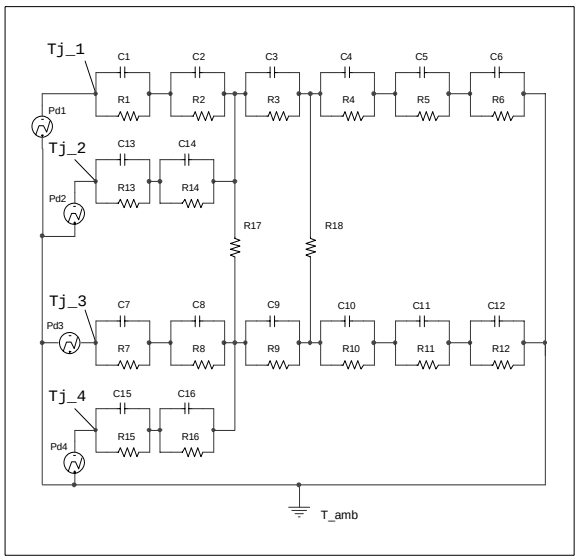
$R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition



SO-28 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a four channels HSD in SO-28



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

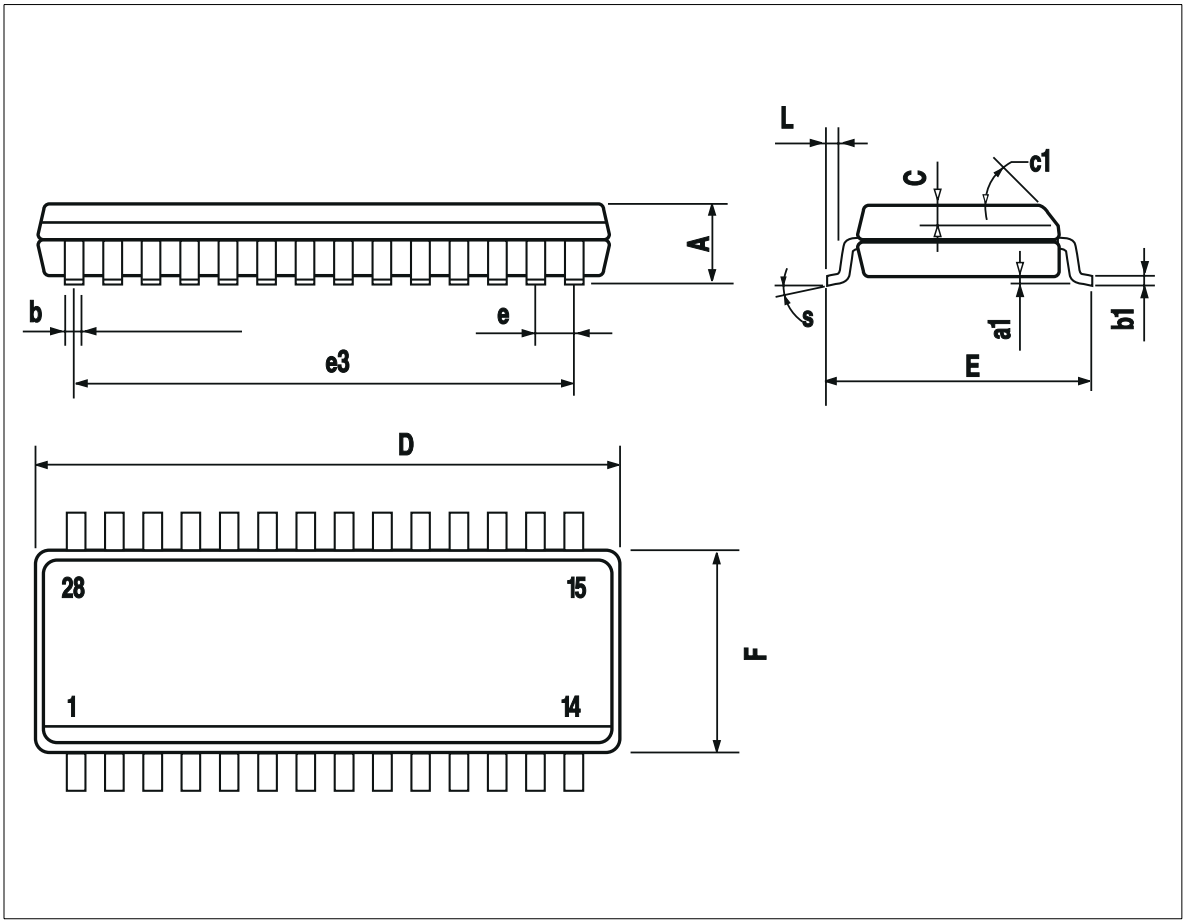
where $\delta = t_p / T$

Thermal Parameter

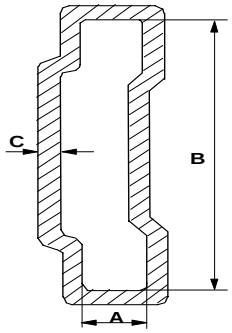
Area/island (cm^2)	0.5	6
R1=R7=R13=R15 (°C/W)	0.05	
R2=R8=R14=R16 (°C/W)	0.3	
R3=R9 (°C/W)	3.4	
R4=R10 (°C/W)	11	
R5=R11 (°C/W)	15	
R6=R12 (°C/W)	30	13
C1=C7=C13=C15 (W.s/°C)	0.001	
C2=C8=C14=C16 (W.s/°C)	5.00E-03	
C3=C9 (W.s/°C)	1.00E-02	
C4=C10 (W.s/°C)	0.2	
C5=C11 (W.s/°C)	1.5	
C6=C12 (W.s/°C)	5	8
R17=R18 (°C/W)	150	

SO-28 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.30	0.004		0.012
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	17.7		18.1	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
S	8 (max.)					



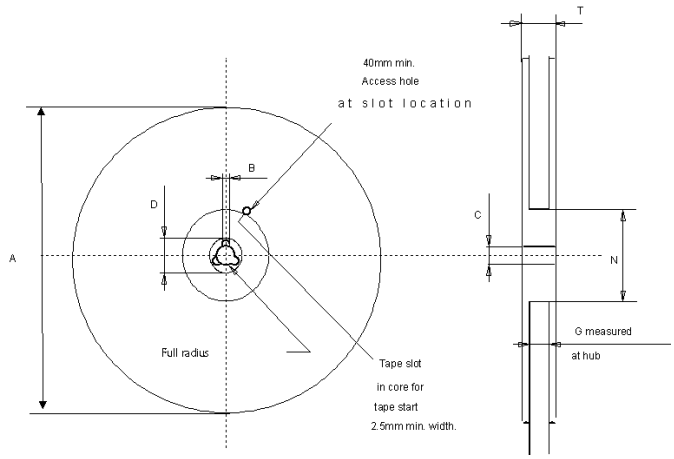
SO-28 TUBE SHIPMENT (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "TR")



REEL DIMENSIONS

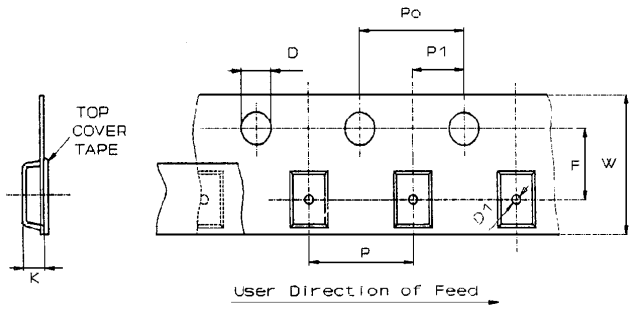
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

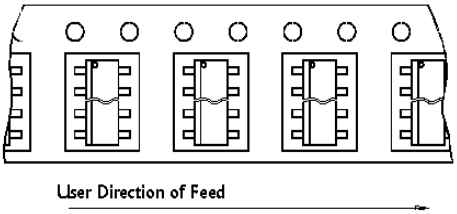
TAPE DIMENSIONS

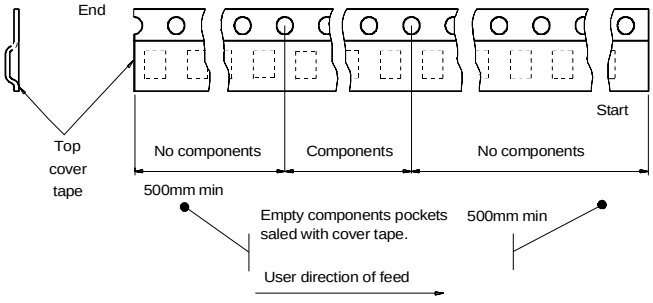
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







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