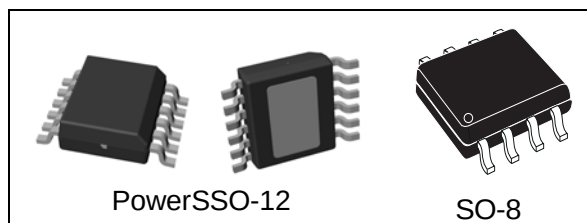


OMNIFET III

fully protected low-side driver

Datasheet - production data



Description

The VNL5030J-E and VNL5030S5-E are monolithic devices made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. Output current limitation protects the devices in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

Features

Type	V _{clamp}	R _{DS(on)}	I _D
VNL5030J-E	41 V	30 mΩ	25 A
VNL5030S5-E			

- Automotive qualified
- Drain current: 25 A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- Compliant with European directive 2002/95/EC
- Open drain status output

Table 1. Devices summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VNL5030J-E	VNL5030JTR-E
SO-8	VNL5030S5-E	VNL5030S5TR-E

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1 Block diagrams and pins configurations

Figure 1. Block diagram

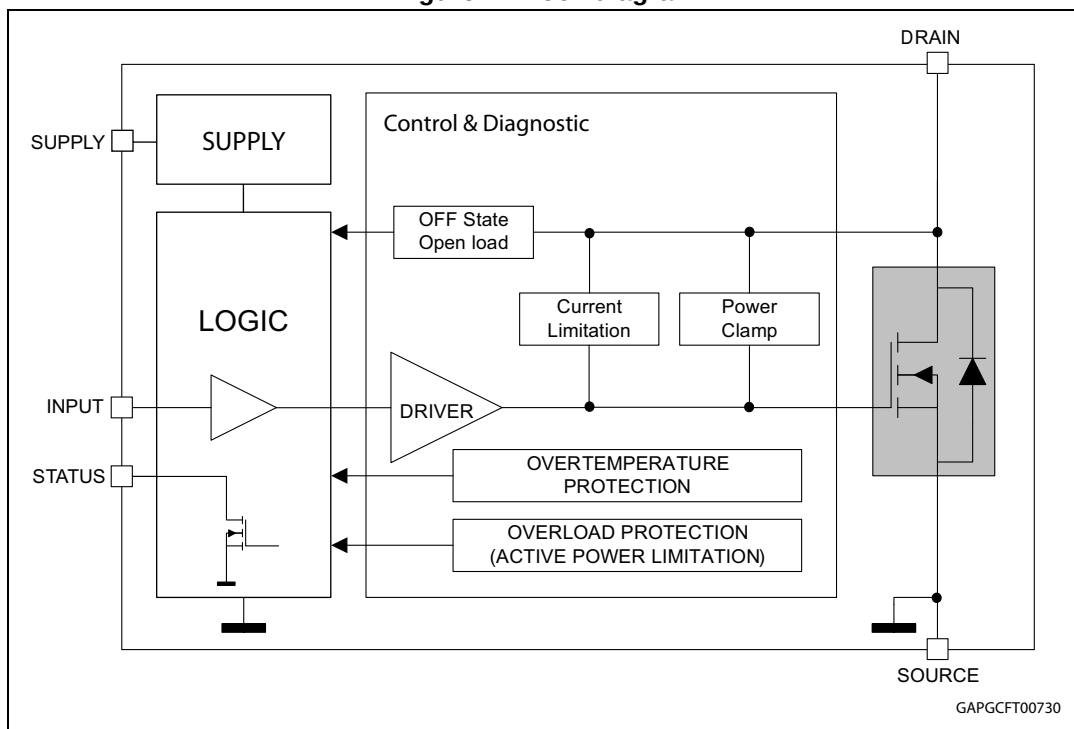


Table 2. Pin function

Name	Function
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible; it controls output switch state.
DRAIN	PowerMOS drain.
SOURCE	PowerMOS source and ground reference for the control section.
SUPPLY	Supply voltage connected to the signal part (5 V).
STATUS	Open drain digital diagnostic pin.
TAB	Exposed pad. PowerMOS drain.

Figure 2. Current and voltage conventions

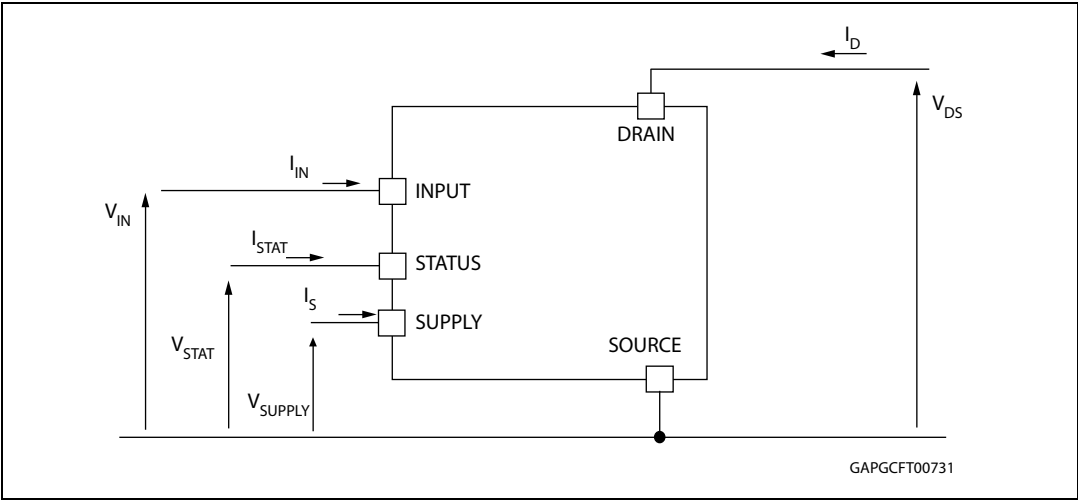


Figure 3. Configuration diagrams (top view)

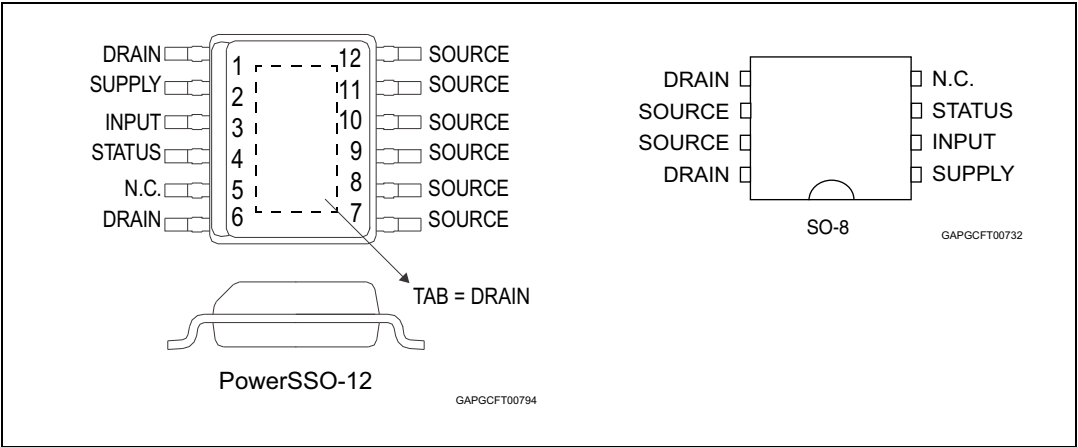


Table 3. Suggested connections for unused and N.C. pins

Connection / pin	Status	N.C.	Input
Floating	X ⁽¹⁾	X	X
To ground	Not allowed	X	Through 10 kΩ resistor

1. X: do not care.

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		PowerSSO-12	SO-8	
V_{DS}	Drain-source voltage ($V_{IN} = 0$ V)	Internally clamped		V
I_D	DC drain current	Internally limited		A
$-I_D$	Reverse DC drain current	30		A
I_S	DC supply current	-1 to 10		mA
I_{IN}	DC input current	-1 to 10		mA
I_{STAT}	DC status current	-1 to 10		mA
V_{ESD1}	Electrostatic discharge ($R = 1.5$ k Ω ; $C = 100$ pF) – DRAIN – SUPPLY, INPUT, STATUS	5000 4000		V
V_{ESD2}	Electrostatic discharge on output pin only ($R = 330$ Ω , $C = 150$ pF)	2000		V
T_j	Junction operating temperature	-40 to 150		°C
T_{stg}	Storage temperature	-55 to 150		°C
E_{AS}	Single pulse avalanche energy ($L = 1.16$ mH, $T_j = 150$ °C, $R_L = 0$, $I_{OUT} = I_{limL}$)	184		mJ

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Maximum value		Unit
		PowerSSO-12	SO-8	
$R_{thj-amb}$	Thermal resistance junction-ambient	61	101	°C/W

2.3 Electrical characteristics

Values specified in this section are for $V_{\text{SUPPLY}} = V_{\text{IN}} = 4.5 \text{ V}$ to 5.5 V , $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise stated.

Table 6. PowerMOS section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SUPPLY}	Operating supply voltage		3.5	5	5.5	V
R_{ON}	ON-state resistance	$I_D = 2.8 \text{ A}$; $T_j = 25^\circ\text{C}$; $V_{\text{SUPPLY}} = V_{\text{IN}} = 5 \text{ V}$			30	$\text{m}\Omega$
		$I_D = 2.8 \text{ A}$; $T_j = 150^\circ\text{C}$; $V_{\text{SUPPLY}} = V_{\text{IN}} = 5 \text{ V}$			60	
V_{CLAMP}	Drain-source clamp voltage	$V_{\text{IN}} = 0 \text{ V}$; $I_D = 2.8 \text{ A}$	41	46	52	V
V_{CLTH}	Drain-source clamp threshold voltage	$V_{\text{IN}} = 0 \text{ V}$; $I_D = 2 \text{ mA}$	36			V
I_{DSS}	OFF-state output current	$V_{\text{IN}} = 0 \text{ V}$; $V_{\text{DS}} = 13 \text{ V}$; $T_j = 25^\circ\text{C}$	0		3	μA
		$V_{\text{IN}} = 0 \text{ V}$; $V_{\text{DS}} = 13 \text{ V}$; $T_j = 125^\circ\text{C}$	0		5	

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	$I_D = 2.8 \text{ A}$; $V_{\text{IN}} = 0 \text{ V}$	—	0.8	—	V

Table 8. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{\text{STAT}} = 1 \text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{\text{STAT}} = 5 \text{ V}$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{\text{STAT}} = 5 \text{ V}$			100	pF
V_{STCL}	Status clamp voltage	$I_{\text{STAT}} = 1 \text{ mA}$	5.5		7	V
		$I_{\text{STAT}} = -1 \text{ mA}$		-0.7		

Table 9. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	$V_{\text{IN}} = 0.9 \text{ V}$	1			μA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	$V_{\text{IN}} = 2.1 \text{ V}$			10	μA
$V_{\text{I(hyst)}}$	Input hysteresis voltage		0.13			V

Table 9. Logic input (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ICL}	Input clamp voltage	$I_{IN} = 1 \text{ mA}$	5.5		7	V
		$I_{IN} = -1 \text{ mA}$		-0.7		

Table 10. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OI}	Open-load OFF-state voltage detection threshold	$V_{IN} = 0 \text{ V}$	0.6	1.2	1.7	V
$t_{d(oloff)}$	Delay between INPUT falling edge and STATUS falling edge in openload condition	$I_{OUT} = 0 \text{ A}$	45	425	1100	μs

Table 11. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	OFF-state; $T_j = 25^\circ\text{C}$; $V_{IN} = V_{DRAIN} = 0 \text{ V}$;		10	25	μA
		ON-state; $V_{IN} = 5 \text{ V}$; $V_{DS} = 0 \text{ V}$		25	65	
V_{SCL}	Supply clamp voltage	$I_{SCL} = 1 \text{ mA}$	5.5		7	V
		$I_{SCL} = -1 \text{ mA}$		-0.7		

Table 12. Switching characteristics⁽¹⁾

Symbol	Parameter	Test conditions	PowerSSO-12			SO-8			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on delay time	$R_L = 4.5 \Omega$; $V_{CC} = 13 \text{ V}^{(2)}$	—	7.6	—	—	7.6	—	μs
$t_{d(OFF)}$	Turn-off delay time	$R_L = 4.5 \Omega$; $V_{CC} = 13 \text{ V}^{(2)}$	—	18.8	—	—	18.8	—	μs
t_r	Rise time	$R_L = 4.5 \Omega$; $V_{CC} = 13 \text{ V}^{(2)}$	—	8	—	—	8	—	μs
t_f	Fall time	$R_L = 4.5 \Omega$; $V_{CC} = 13 \text{ V}^{(2)}$	—	9	—	—	9	—	μs
W_{ON}	Switching energy losses at turn-on	$R_L = 4.5 \Omega$; $V_{CC} = 13 \text{ V}^{(2)}$	—	0.068	—	—	0.068	—	mJ
W_{OFF}	Switching energy losses at turn-off	$R_L = 4.5 \Omega$; $V_{CC} = 13 \text{ V}^{(2)}$	—	0.077	—	—	0.077	—	mJ
Q_g	Total gate charge	$V_{SUPPLY} = V_{IN} = 5 \text{ V}$	—	6	—	—	6	—	nC

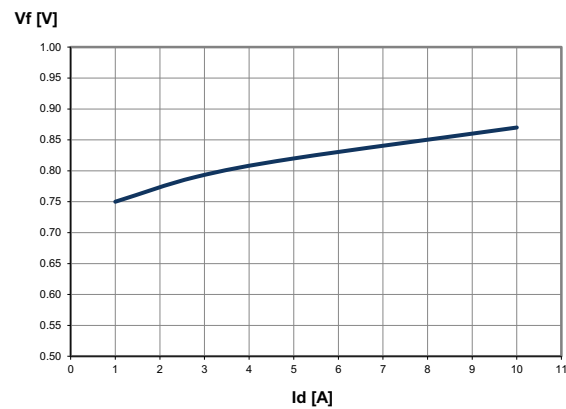
1. See [Figure 14: Application schematic](#).2. See [Figure 13: Switching characteristics](#).

Table 13. Protection and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	$V_{DS} = 13\text{ V};$ $V_{SUPPLY} = V_{IN} = 5\text{ V}$	25	35	49	A
I_{limL}	Short-circuit current during thermal cycling	$V_{DS} = 13\text{ V}; T_R < T_J < T_{TSD};$ $V_{SUPPLY} = V_{IN} = 5\text{ V}$		15		A
t_{dimL}	Step response current limit	$V_{DS} = 13\text{ V}; V_{input} = 5\text{ V}$		44		μs
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}\text{C}$

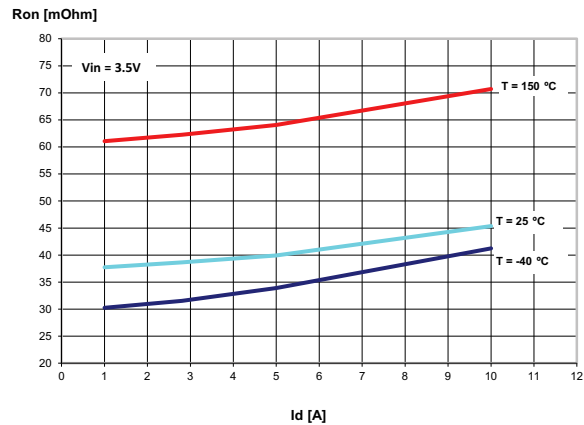
2.4 Electrical characteristics curves

Figure 4. Source diode forward characteristics



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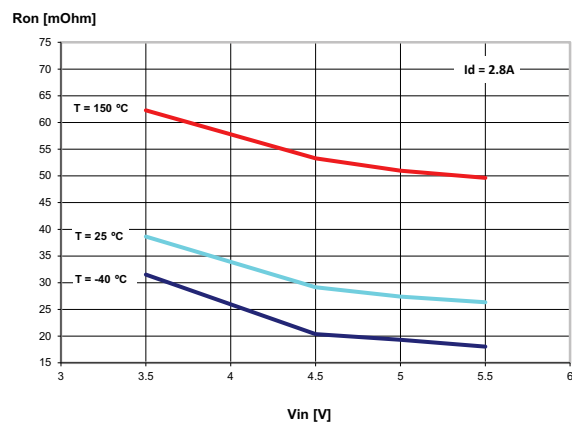
Figure 5. Static drain source on-resistance vs. drain current ($V_{IN} = 3.5$ V)



Note: Input and supply pins connected together

GAPG2207131621CFT

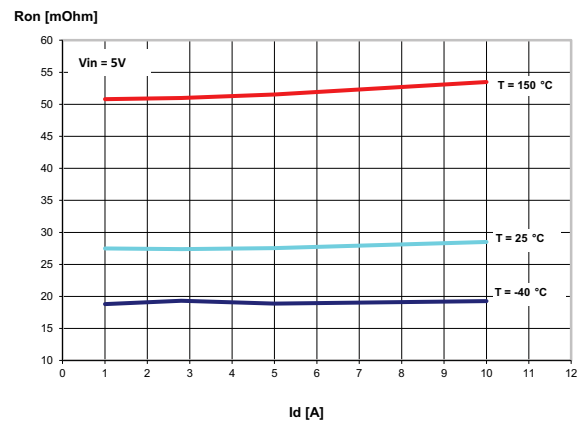
Figure 6. Static drain source on-resistance vs. input voltage



Note: Input and supply pins connected together

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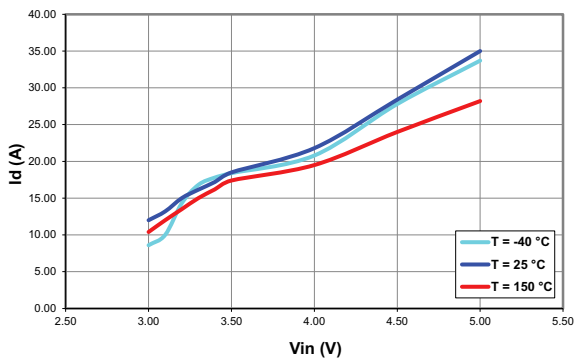
Figure 7. Static drain source on-resistance vs. drain current ($V_{IN} = 5$ V)



Note: Input and supply pins connected together

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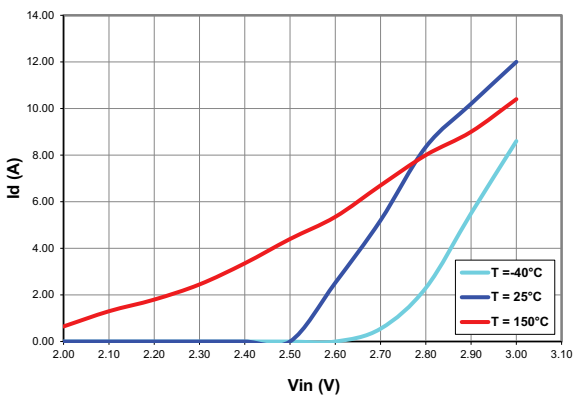
Figure 8. Transfer characteristics



Note: Input and supply pins connected together

GAPG2307130857CFT

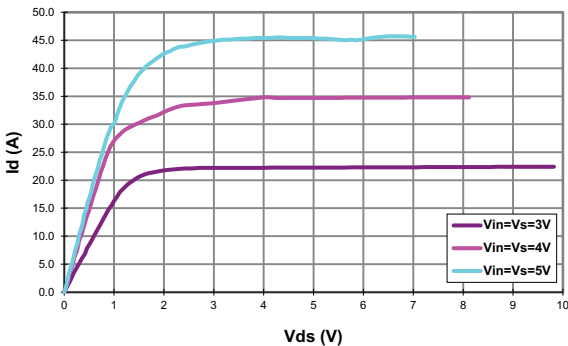
Figure 9. Transfer characteristics (inside view for $V_{IN} = 2\text{ V to }3\text{ V}$)



Note: Input and supply pins connected together

GAPG2307130859CFT

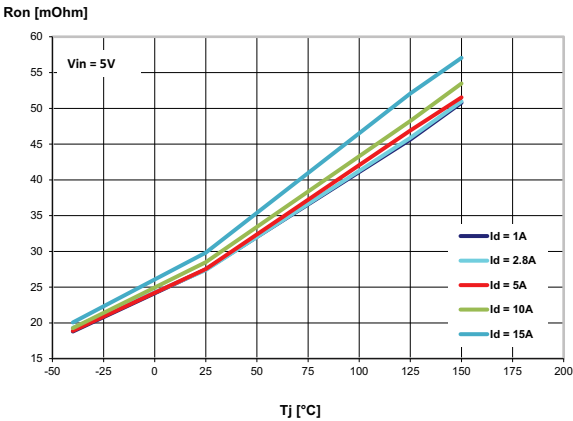
Figure 10. Output characteristics ($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$)



Note: Input and supply pins connected together

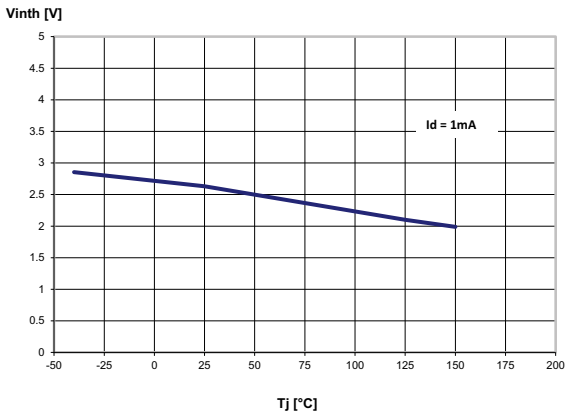
GAPG2307130907CFT

Figure 11. On-resistance vs. temperature



GAPG2307130912CFT

Figure 12. Input threshold vs. temperature



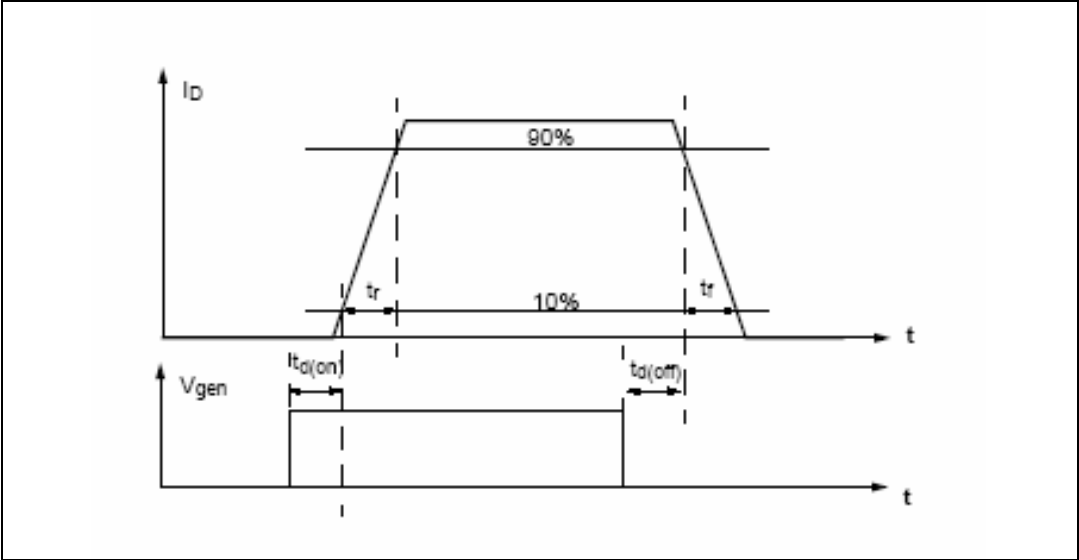
Note: Input and supply pins connected together

GAPG2307130915CFT

Table 14. Truth table

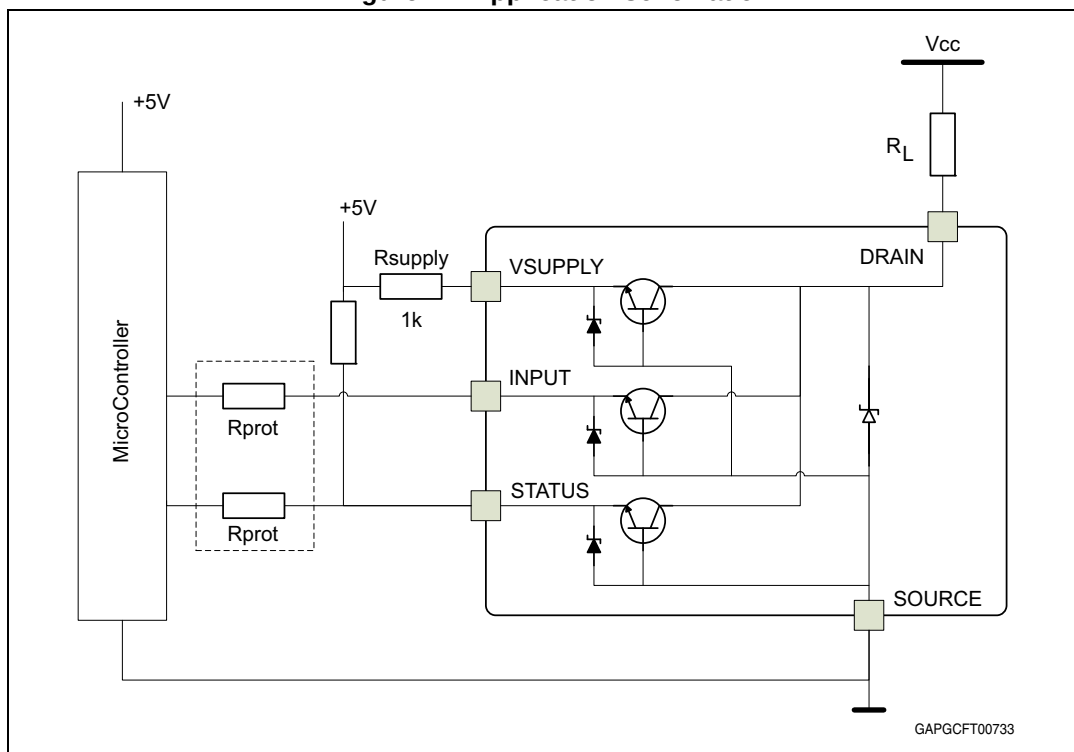
Conditions	INPUT	DRAIN	STATUS
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Overtemperature	L	H	H
	H	H	L
Undervoltage	L	H	X
	H	H	X
Output voltage < V _{OL}	L	L	L
	H	L	H

Figure 13. Switching characteristics



3 Application information

Figure 14. Application schematic



3.1 MCU I/O protection

ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up^(a). The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

Equation 1

$$\frac{0.7}{I_{latchup}} \leq R_{prot} \leq \frac{(V_{OH\mu C} - V_{IH})}{I_{IH\ max}}$$

Let:

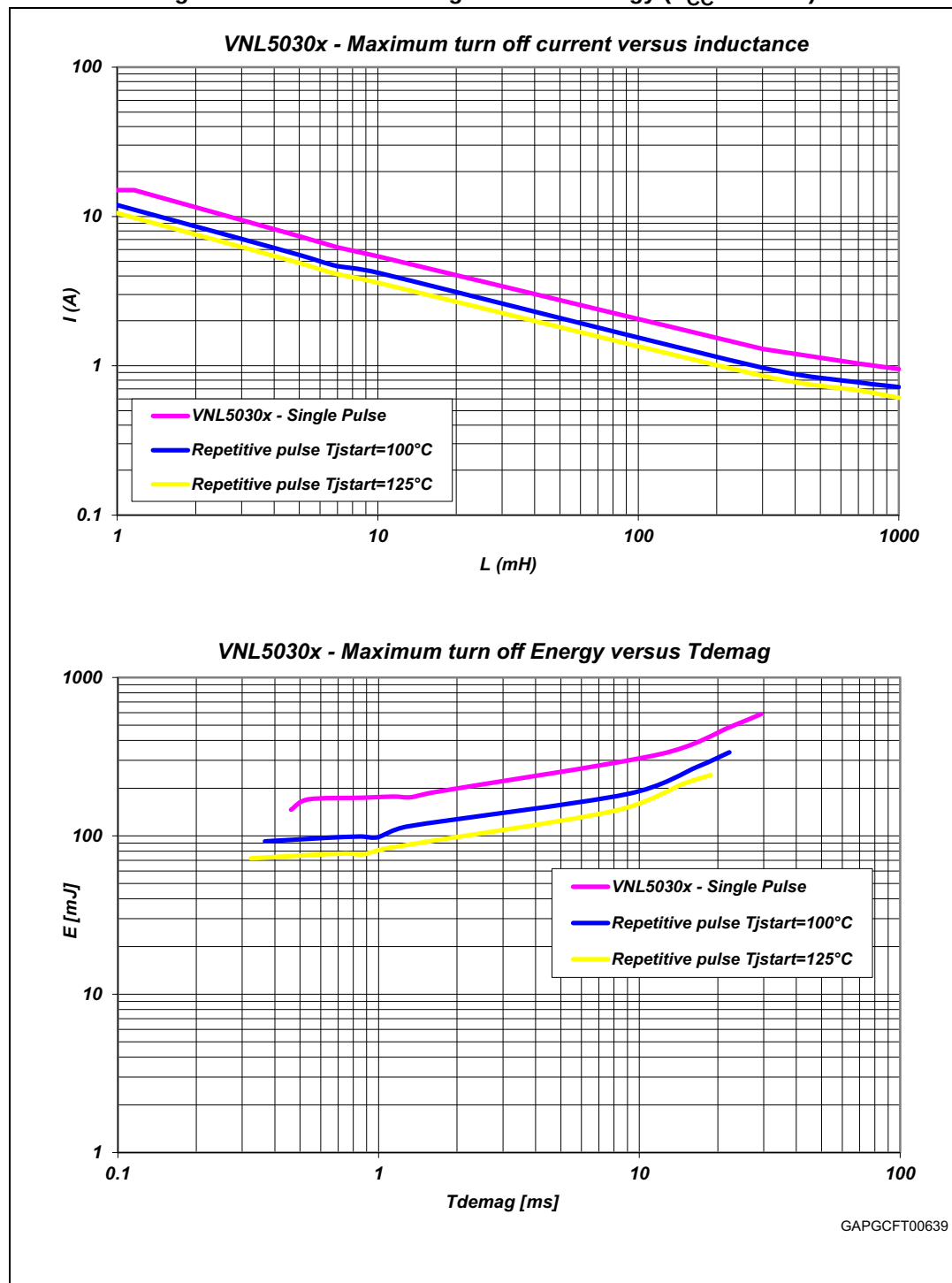
- $I_{latchup} \geq 20\ \text{mA}$
- $V_{OH\mu C} \geq 4.5\ \text{V}$
- $35\ \Omega \leq R_{prot} \leq 100\ \text{k}\Omega$

a. In case of negative transient on the drain pin.

Then, the recommended value is $R_{\text{prot}} = 1 \text{ K}\Omega$

Figure 15 shows the turn-off current drawn during the demagnetization.

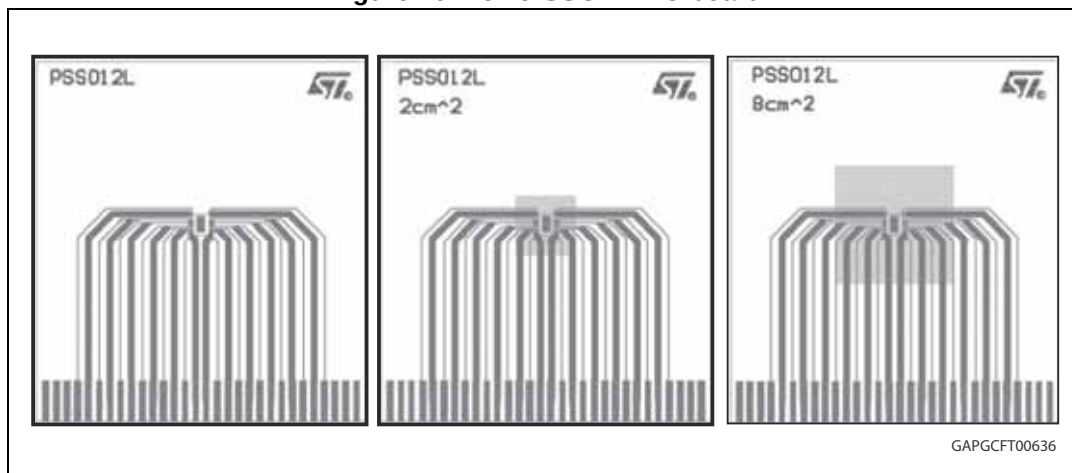
Figure 15. Maximum demagnetization energy ($V_{\text{CC}} = 13.5 \text{ V}$)



4 Package and PC board thermal data

4.1 PowerSSO-12 thermal data

Figure 16. PowerSSO-12 PC board



1. Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10%; board double layer; board dimension 77x86; board material FR4; Cu thickness 0.070mm (front and back side); thermal vias separation 1.2 mm; thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm; footprint dimension 4.1 mm x 6.5 mm).

Figure 17. PowerSSO-12 R_{thj-amb} vs PCB copper area in open box free air condition

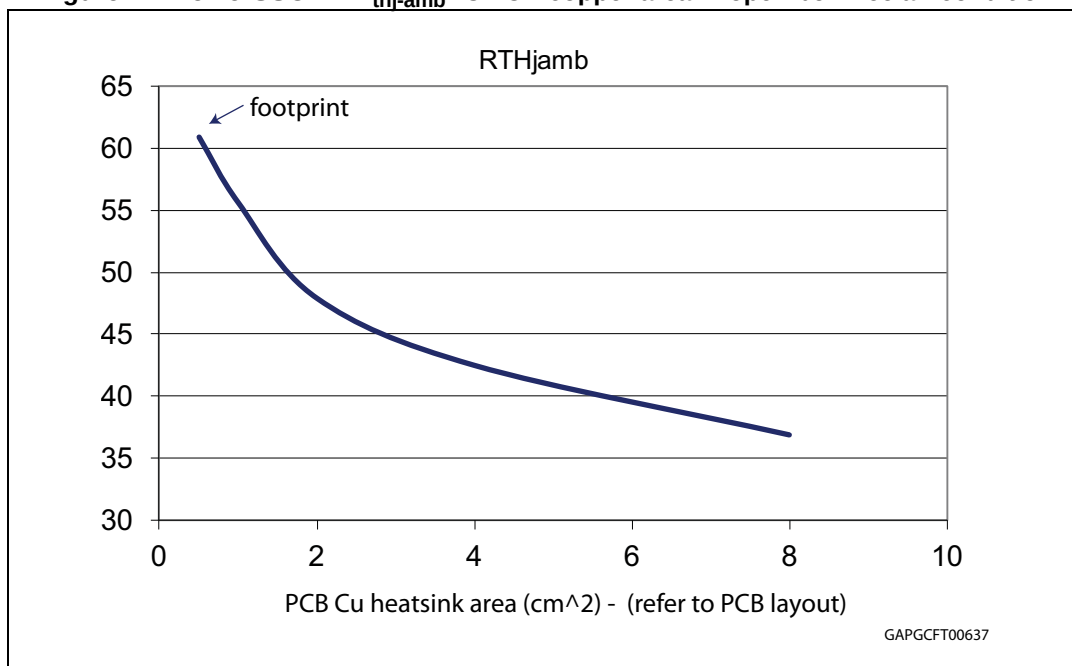
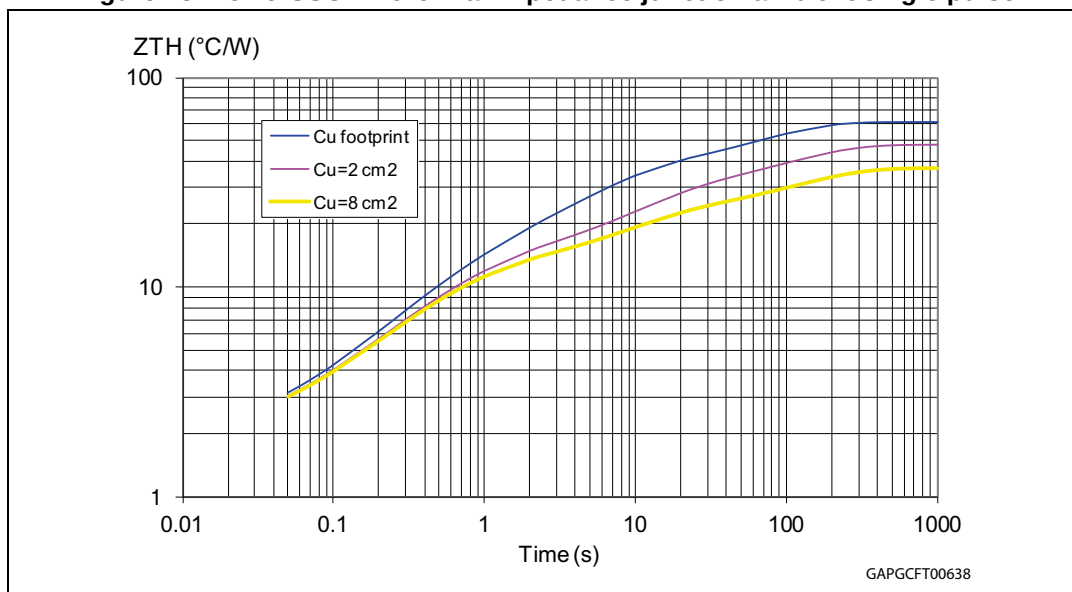


Figure 18. PowerSSO-12 thermal impedance junction ambient single pulse

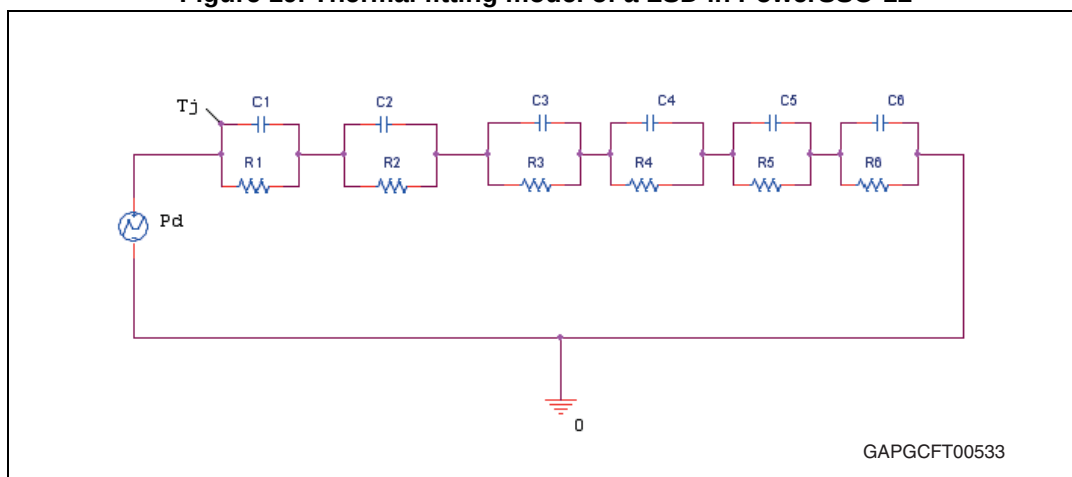


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 19. Thermal fitting model of a LSD in PowerSSO-12



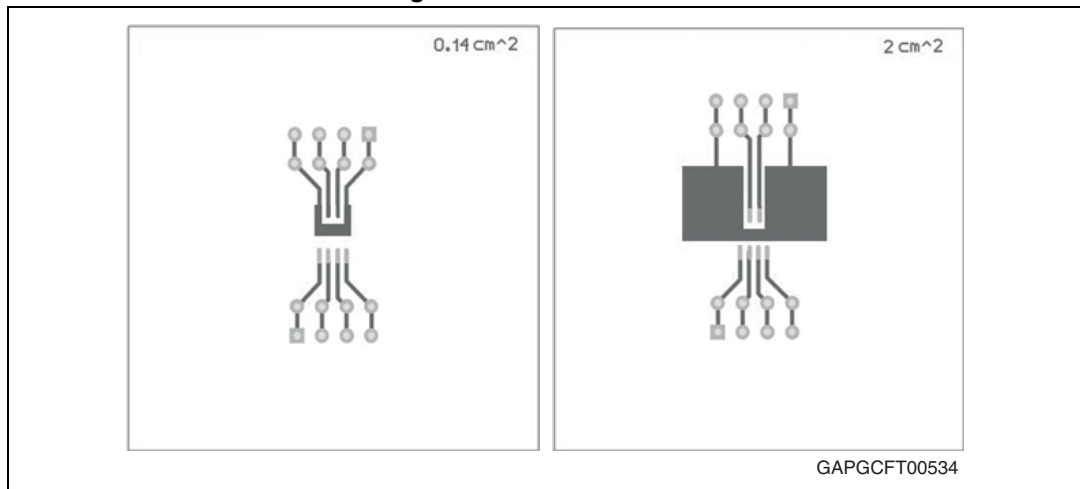
1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. PowerSSO-12 thermal parameters

Areal/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.7		
R2 (°C/W)	1.2		
R3 (°C/W)	3		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.005		
C3 (W.s/°C)	0.08		
C4 (W.s/°C)	0.1	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 SO-8 thermal data

Figure 20. SO-8 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μm (front and back side), Copper areas: from minimum pad lay-out to 2 cm^2).

Figure 21. SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition

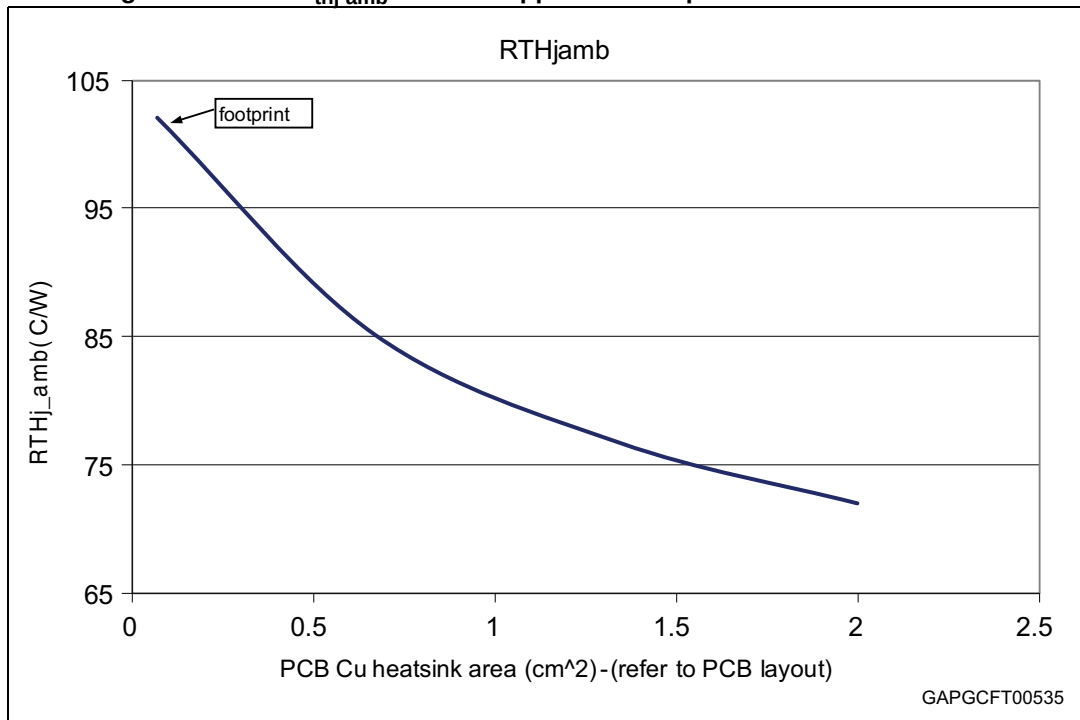
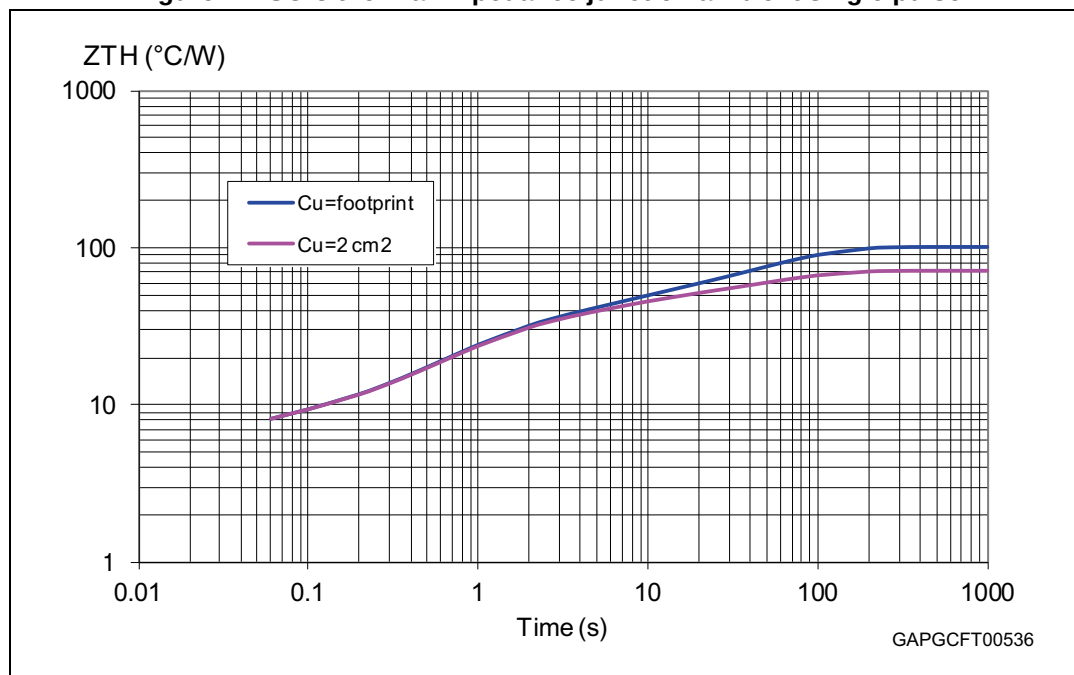
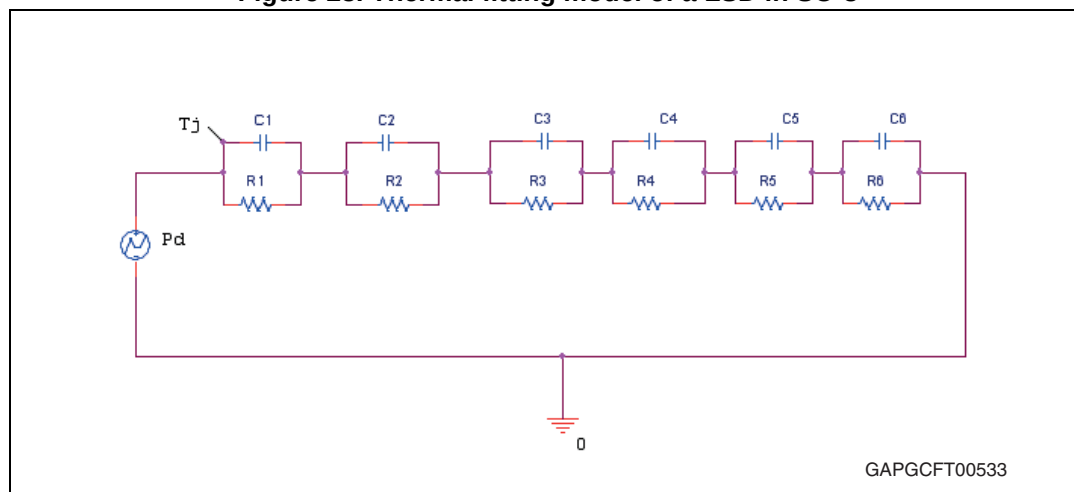


Figure 22. SO-8 thermal impedance junction ambient single pulse**Equation 3: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 23. Thermal fitting model of a LSD in SO-8

1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. SO-8 thermal parameters

Area/island (cm ²)	Footprint	2
R1 (°C/W)	0.3	
R2 (°C/W)	2.2	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.0001	
C2 (W.s/°C)	0.002	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 PowerSSO-12 mechanical data

Figure 24. PowerSSO-12 package dimensions

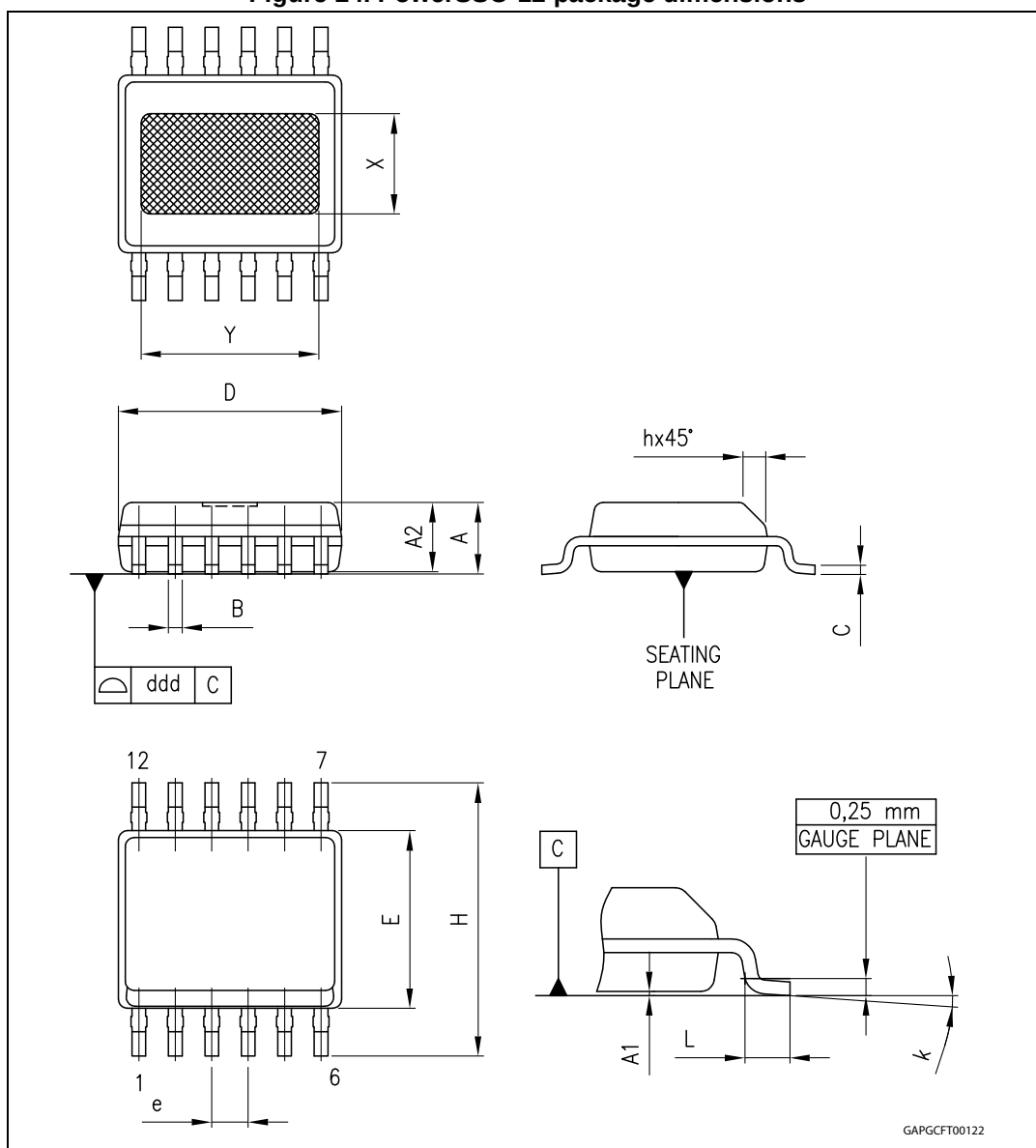


Table 17. PowerSSO-12 mechanical data

DIM.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.25		1.62	A	1.25	
A1	0		0.1	A1	0	
A2	1.10		1.65	A2	1.10	
B	0.23		0.41	B	0.23	
C	0.19		0.25	C	0.19	
D	4.8		5.0	D	4.8	
E	3.8		4.0	E	3.8	
e		0.8		e		0.8
H	5.8		6.2	H	5.8	
h	0.25		0.5	h	0.25	
L	0.4		1.27	L	0.4	
k	0°		8°	k	0°	
X	1.9		2.5	X	1.9	
Y	3.6		4.2	Y	3.6	
ddd			0.1	ddd		

5.3 SO-8 mechanical data

Figure 25. SO-8 package dimensions

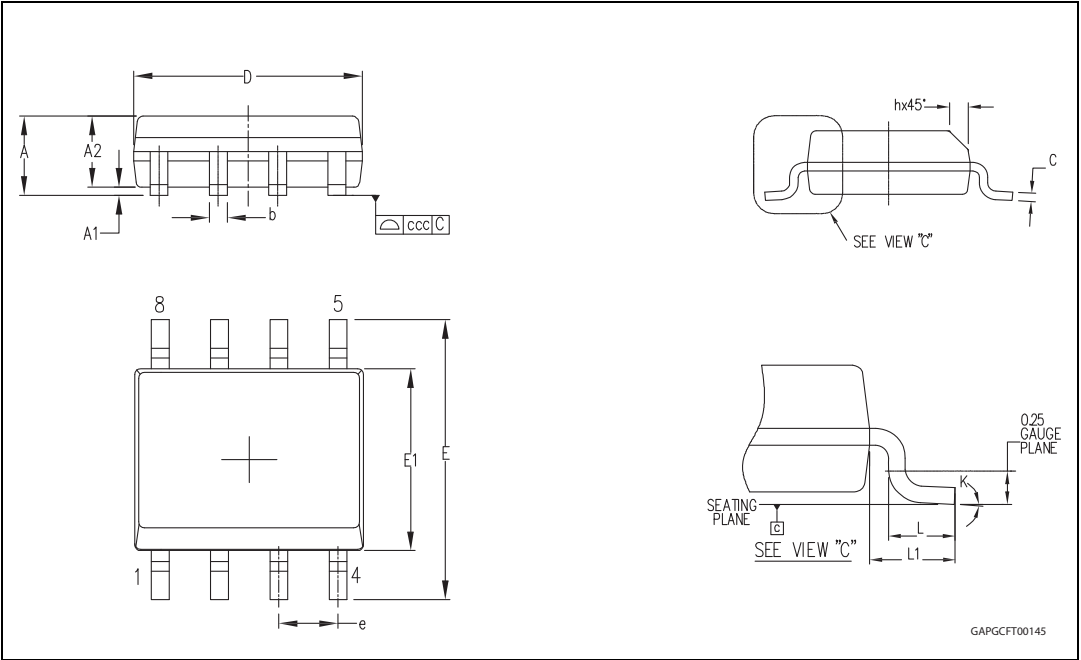


Table 18. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

5.4 PowerSSO-12 packing information

The devices can be packed in tube or tape and reel shipments (see the [Table 1: Devices summary](#)).

Figure 26. PowerSSO-12 tube shipment (no suffix)

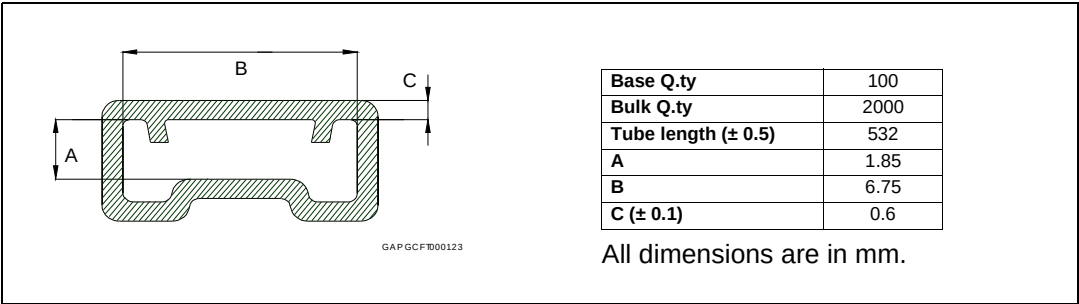
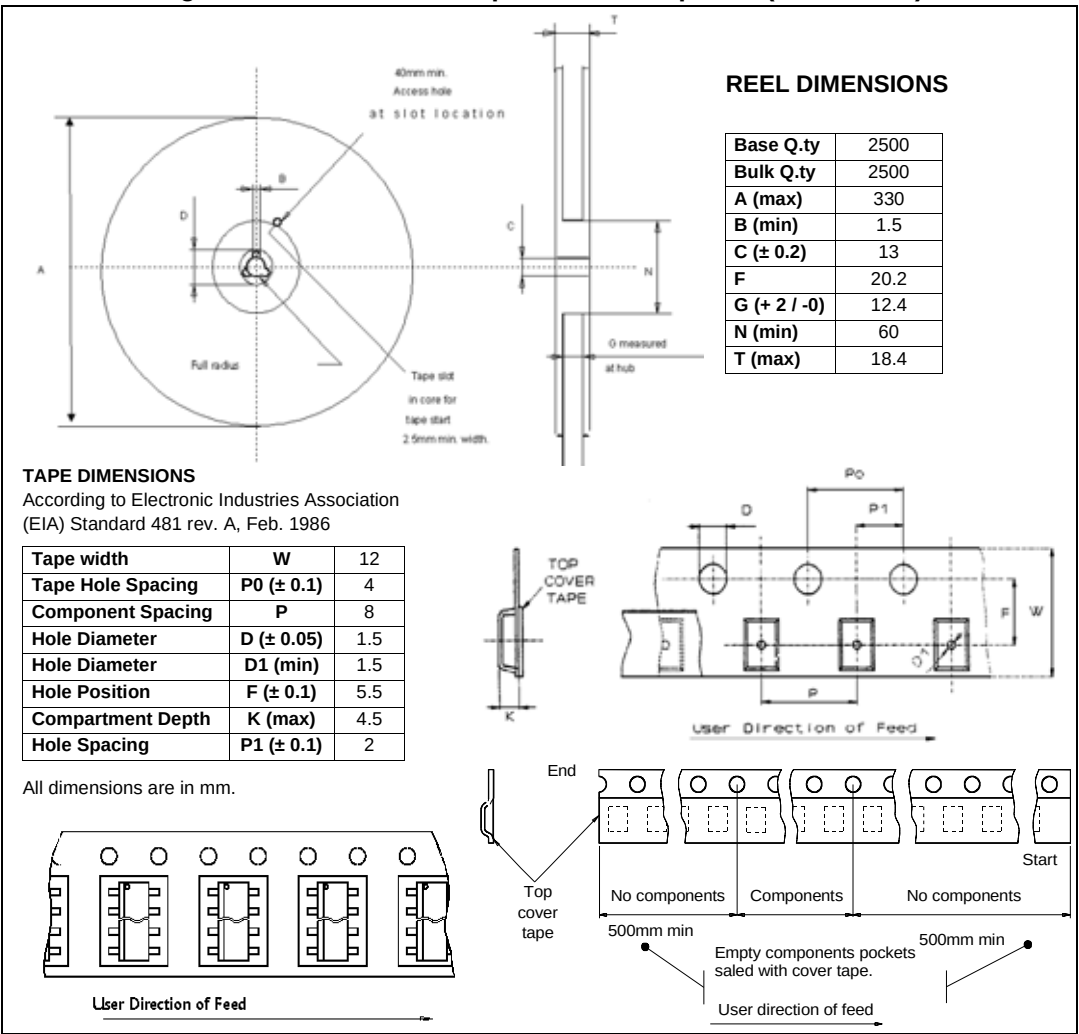


Figure 27. PowerSSO-12 tape and reel shipment (suffix “TR”)



6 Revision history

Table 19. Document revision history

Date	Revision	Changes
14-Feb-2012	1	Initial release.
14-Jun-2012	2	Updated Table 2: Pin function Updated Figure 3: Configuration diagrams (top view) Table 12: Switching characteristics : – Q _G : added row
14-Sep-2012	3	Table 4: Absolute maximum ratings : – I _D , I _S , I _{STAT} : updated values Updated Table 5: Thermal data and Table 12: Switching characteristics
15-May-2013	4	Removed Table: Input section . Updated Figure 14: Application schematic Updated Section 3.1: MCU I/O protection
18-Sep-2013	5	Updated disclaimer.
21-Nov-2013	6	Updated Features list Added Section 2.4: Electrical characteristics curves Table 11: Supply section : – I _S : updated max value Updated Figure 15: Maximum demagnetization energy (V_{CC} = 13.5 V)

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