VNH3SP30

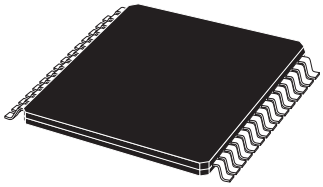
FULLY INTEGRATED H-BRIDGE MOTOR DRIVER

TYPE	$R_{DS(on)}$ (*)	I_{OUT}	V_{CCmax}
VNH3SP30	34mΩ	30 A	40 V

(*) Typical per leg at 25°C

- OUTPUT CURRENT:30 A
- 5V LOGIC LEVEL COMPATIBLE INPUTS
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CROSS-CONDUCTION PROTECTION
- LINEAR CURRENT LIMITER
- VERY LOW STAND-BY POWER CONSUMPTION
- PWM OPERATION UP TO 10 KHz
- PROTECTION AGAINST:

  LOSS OF GROUND AND LOSS OF V_{CC}

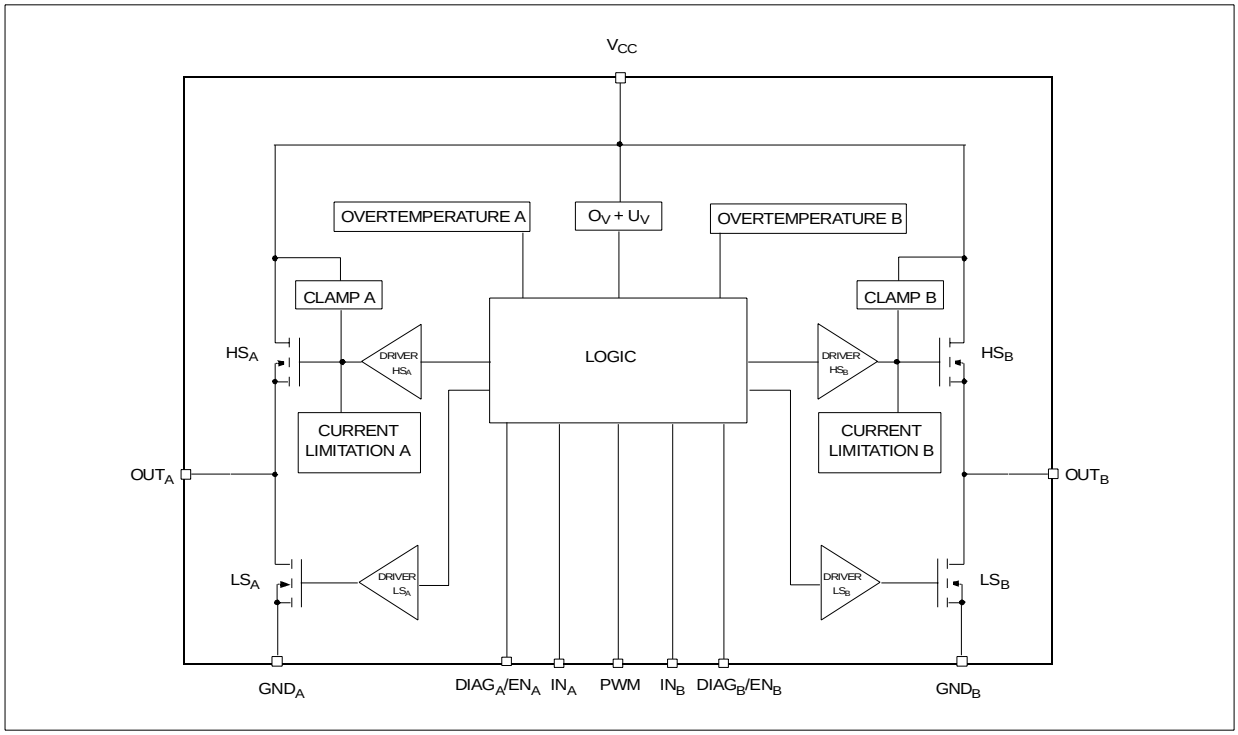


MultiPowerSO-30

DESCRIPTION

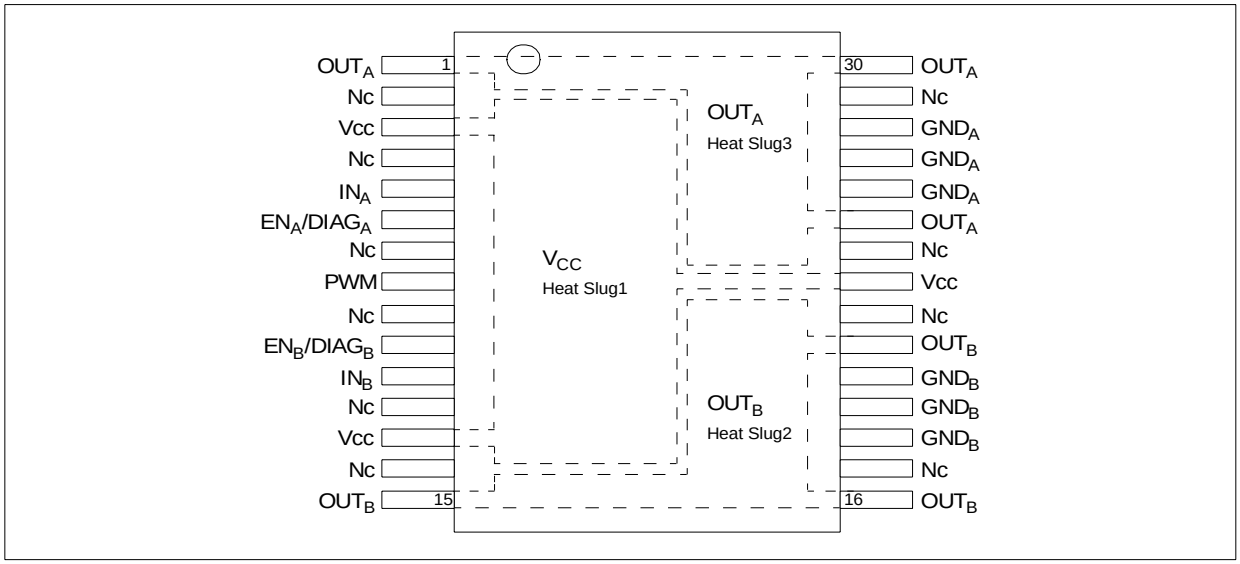
The VNH3SP30 is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic HSD and two Low-Side switches. The HSD switch is designed using STMicroelectronics VIPower M0-3 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The Low-Side switches are vertical MOSFETs manufactured using STMicroelectronics proprietary EHD ("STripFET™") process.

BLOCK DIAGRAM



The three dice are assembled in MultiPowerSO-30 package on electrically isolated leadframes. This package, specifically designed for the harsh automotive environment offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals IN_A and IN_B can directly interface to the microcontroller to select the motor direction and the brake condition. The $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The normal condition operation is explained in the truth table on page 7. The PWM, up to 10KHz, lets us to control the speed of the motor in all possible conditions. In all cases, a low level state on the PWM pin will turn off both the LS_A and LS_B switches. When PWM rises to a high level, LS_A or LS_B turn on again depending on the input pin state.

CONNECTION DIAGRAM (TOP VIEW)



PIN DEFINITIONS AND FUNCTIONS

PIN No	SYMBOL	FUNCTION
1, 25, 30	OUT_A, Heat Slug2	Source of High-Side Switch A / Drain of Low-Side Switch A
2, 4,7,9,12,14,17, 22, 24,29	NC	Not connected
3, 13, 23	VCC, Heat Slug1	Drain of High-Side Switches and Power Supply Voltage
5	IN_A	Clockwise Input
6	$EN_A/DIAG_A$	Status of High-Side and Low-Side Switches A; Open Drain Output
8	PWM	PWM Input
9	NC	Not connected
10	$EN_B/DIAG_B$	Status of High-Side and Low-Side Switches B; Open Drain Output
11	IN_B	Counter Clockwise Input
15, 16, 21	OUT_B, Heat Slug3	Source of High-Side Switch B / Drain of Low-Side Switch B
26, 27, 28	GND_A	Source of Low-Side Switch A (*)
18, 19, 20	GND_B	Source of Low-Side Switch B (*)

(*) Note: GND_A and GND_B must be externally connected together

PIN FUNCTIONS DESCRIPTION

NAME	DESCRIPTION
V_{CC}	Battery connection.
GND_A GND_B	Power grounds, must always be externally connected together.
OUT_A OUT_B	Power connections to the motor.
IN_A IN_B	Voltage controlled input pins with hysteresis, CMOS compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V_{CC}, Brake to GND, clockwise and counterclockwise).
PWM	Voltage controlled input pin with hysteresis, CMOS compatible. Gates of Low-Side FETS get modulated by the PWM signal during their ON phase allowing speed control of the motor
$EN_A/DIAG_A$ $EN_B/DIAG_B$	Open drain bidirectional logic pins. These pins must be connected to an external pull up resistor.When externally pulled low, they disable half-bridge A or B. In case of fault detection (thermal shutdown of a High-Side FET or excessive ON state voltage drop across a Low-Side FET), these pins are pulled low by the device (see truth table in fault condition).

BLOCK DESCRIPTIONS

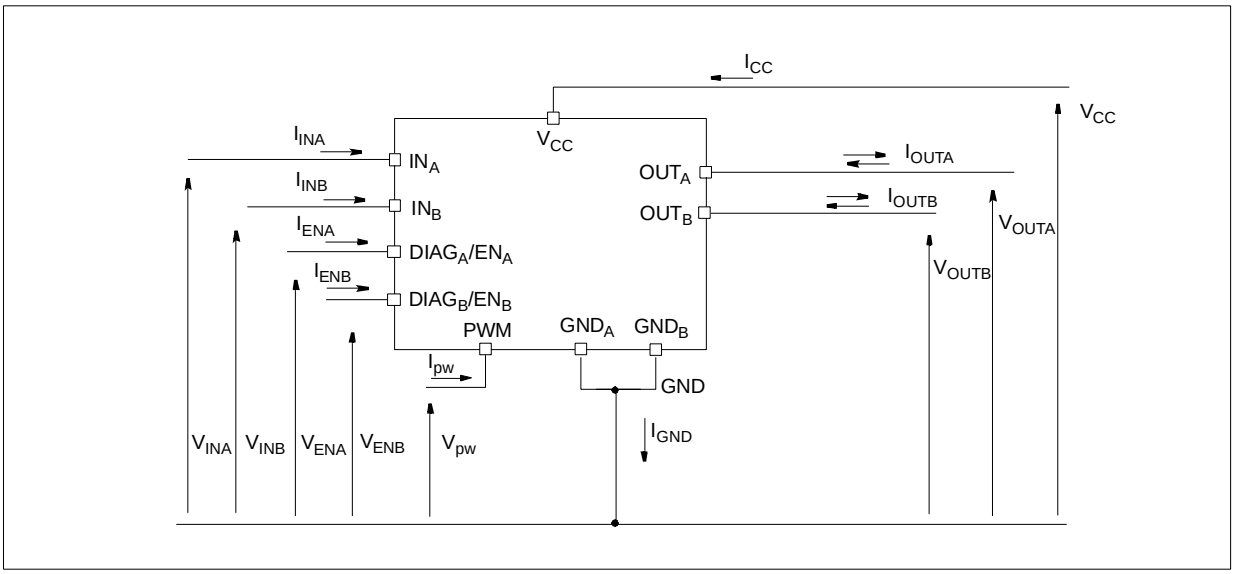
(see Electrical Block Diagram page 4)

NAME	DESCRIPTION
LOGIC CONTROL	Allows the turn-on and the turn-off of the High Side and the Low Side switches according to the truth table.
OVERVOLTAGE + UNDERVOLTAGE	Shut-down the device outside the range [5.5V..36V] for the battery voltage.
HIGH SIDE CLAMP VOLTAGE	Protect the High-Side switches from the high voltage on the battery line in all configuration for the motor.
HIGH SIDE AND LOW SIDE DRIVER	Drive the gate of the concerned switch to allow a good $R_{DS(on)}$ for the leg of the bridge.
LINEAR CURRENT LIMITER	In case of short circuit for the High-Side switch, limits the motor current by reducing its electrical characteristics.
OVERTEMPERATURE PROTECTION	In case of short-circuit with the increase of the junction's temperature, shuts-down the concerned High-Side to prevent its degradation and to protect the die.
FAULT DETECTION	Signalize an abnormal behavior of the switches in the half-bridge A or B by pulling low the concerned ENx/DIAGx pin.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3.. 40	V
I_{max1}	Maximum output current (continuous)	30	A
I_R	Reverse output current (continuous)	-30	A
I_{IN}	Input current (IN_A and IN_B pins)	+/- 10	mA
I_{EN}	Enable input current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins)	+/- 10	mA
I_{pw}	PWM input current	+/- 10	mA
V_{ESD}	Electrostatic discharge (R=1.5kΩ, C=100pF) - Logic pins - Output pins: OUT_A, OUT_B, V_{CC}	 4 5	 KV kV
T_j	Junction operating temperature	Internally Limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

See MultiPowerSO-30 Thermal Data section.

ELECTRICAL CHARACTERISTICS (V_{CC}=9V up to 18V; -40°C<T_j<150°C; unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		5.5		36	V
R_{ONHS}	On state high side resistance	I_{LOAD}=12A; T_j=25°C		23	30	mΩ
R_{ONLS}	On state low side resistance	I_{LOAD}=12A; T_j=25°C		11	15	mΩ
R_{ON}	On state leg resistance	I_{LOAD}=12A			90	mΩ
I_s	Supply current	ON state; V_{INA}=V_{INB}=5V OFF state			15 40	mA µA
V_f	High Side Free-wheeling Diode Forward Voltage	I_f=12A		0.8	1.1	V
$I_{L(off)}$	High Side Off State Output Current (per channel)	T_j=25°C; V_{OUTX}=EN_X=0V; V_{CC}=13V T_j=125°C; V_{OUTX}=EN_X=0V; V_{CC}=13V			3 5	µA µA

SWITCHING (V_{CC}=13V, R_{LOAD}=1.1Ω)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f	PWM frequency		0		10	kHz
$t_{D(on)}$	Turn-on delay time	Input rise time < 1µs (see fig. 3)		100	300	µs
$t_{D(off)}$	Turn-off delay time	Input rise time < 1µs (see fig. 3)		85	255	µs
t_r	Output voltage rise time	(see fig. 2)		1.5	3	µs
t_f	Output voltage fall time	(see fig. 2)		2	5	µs
t_{DEL}	Delay time during change of operation mode	(see fig. 1)		600	1800	µs

PROTECTION AND DIAGNOSTIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{USD}	Undervoltage shut-down				5.5	V
V_{OV}	Overvoltage shut-down		36	43		V
I_{LIM}	Current limitation		30	45		A
T_{TSD}	Thermal shut-down temperature	V_{IN} = 3.25 V	150	170	200	°C
T_{TR}	Thermal Reset Temperature		135			°C
T_{HYST}	Thermal Hysteresis		7	15		°C

PWM

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{pwl}	PWM low level voltage				1.5	V
I_{pwl}	Low level PWM pin current	V_{pw}=1.5V	1			µA
V_{pwh}	PWM high level voltage		3.25			V
I_{pwh}	High level PWM pin current	V_{pw}=3.25V			10	µA
$V_{pwhhyst}$	PWM hysteresis voltage		0.5			V
V_{pwcl}	PWM clamp voltage	I_{pw} = 1 mA I_{pw} = -1 mA	V_{CC}+0.3 -5.0	V_{CC}+0.7 -3.5	V_{CC}+1.0 -2.0	V V
V_{pwtest}	Test mode PWM pin voltage		-3.5	-2.0	-0.5	V
I_{pwtest}	Test mode PWM pin current	V_{pwtest} = -2.0V	-2000	-500		µA

LOGIC INPUT (IN_A/IN_B)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.5	V
I_{INL}	Input current	V_{IN}=1.5V	1			µA
V_{IH}	Input high level voltage		3.25			V
I_{INH}	Input current	V_{IN}=3.25V			10	µA
V_{IHYST}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	6.0 -1.0	6.8 -0.7	8.0 -0.3	V V

ENABLE (LOGIC I/O PIN)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{ENL}	Enable low level voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)			1.5	V
I_{ENL}	Low level Enable pin current	V_{EN}= 1.5V	1			µA
V_{ENH}	Enable high level voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)	3.25			V
I_{ENH}	High level Enable pin current	V_{EN}= 3.25V			10	µA
V_{EHYST}	Enable hysteresis voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)	0.5			V
V_{ENCL}	Enable clamp voltage	I_{EN}=1mA I_{EN}=-1mA	6.0 -1.0	6.8 -0.7	8.0 -0.3	V V
V_{DIAG}	Enable output low level voltage	Fault operation ($DIAG_X$/EN_X pin acts as an input pin) I_{EN}=1 mA			0.4	V

WAVEFORMS AND TRUTH TABLE

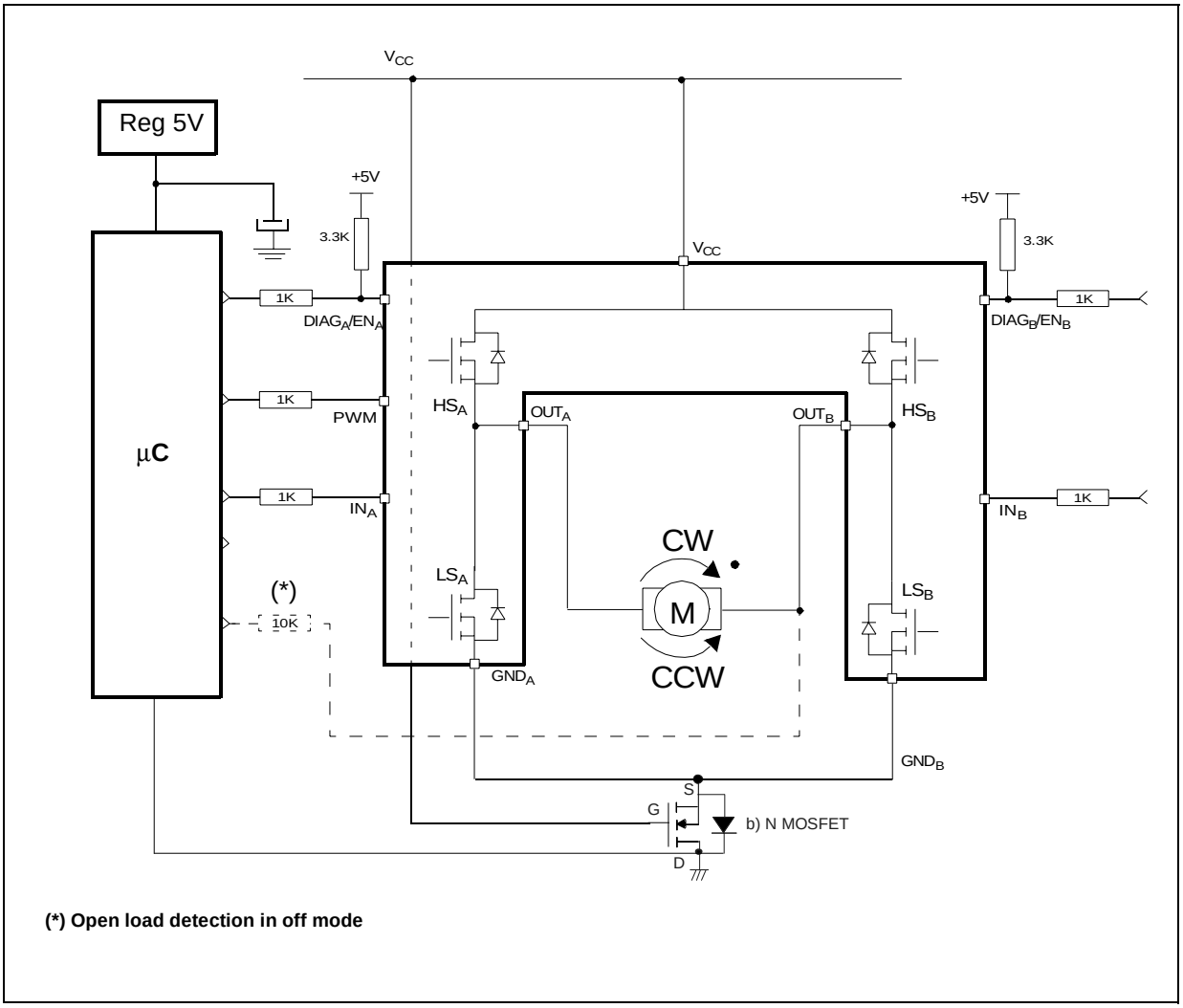
TRUTH TABLE IN NORMAL OPERATING CONDITIONS

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	Comment
1	1	1	1	H	H	Brake to V_{CC}
1	0	1	1	H	L	Clockwise
0	1	1	1	L	H	Counter cw
0	0	1	1	L	L	Brake to GND

PWM pin usage:
In all cases, a “0” on the PWM pin will turn-off both LSA and LSB switches. When PWM rises back to “1”, LS_A or LS_B turn on again depending on the input pin state.
NB: in no cases external pins (except for GND_B and GND_A) are allowed to be connected with ground.

TYPICAL APPLICATION CIRCUIT FOR DC TO 10KHz PWM OPERATION



(*) Open load detection in off mode

REVERSE BATTERY PROTECTION

Three possible solutions can be thought of:
a) a Schottky diode D connected to V_{CC} pin
b) a N-channel MOSFET connected to the GND pin (see Typical Application Circuit on page 7)
c) a P-channel MOSFET connected to the V_{CC} pin

The device sustains no more than -30A in reverse battery conditions because of the two Body diodes of the Power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH2SP30 will be pulled down to the V_{CC} line (approximately -1.5V). Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I_{Rmax} is the maximum target reverse current through µC I/Os, series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

OPEN LOAD DETECTION IN OFF-MODE

It is possible for the microcontroller to detect an open load condition by adding a simply resistor (for example 10kΩ) between one of the outputs of the bridge (for example OUT_B) and one microcontroller input. A possible sequence of inputs and enable signals is the following: IN_A=1, IN_B=X, EN_A= 1, EN_B=0.

- normal condition: OUT_A=H and OUT_B=H
- open load condition: OUT_A=H and OUT_B=L: in this case the OUT_B pin is internally pulled down to GND. This condition is detected on OUT_B pin by the microcontroller as an open load fault.

SHORT CIRCUIT PROTECTION

In case of a fault condition the $DIAG_X/EN_X$ pin is considered as an output pin by the device.
The fault conditions are:
- overtemperature on one or both high sides;
- short to battery condition on the output (saturation detection on the Low-Side Power MOSFET).

Possible origins of fault conditions may be:
OUT_A is shorted to ground ---> overtemperature detection on high side A.
OUT_A is shorted to V_{CC} ---> Low-Side Power MOSFET saturation detection. (1)
When a fault condition is detected, the user can know which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.
In any case, when a fault is detected, the faulty half bridge is latched off. To turn-on the respective output (OUT_X) again, the input signal must rise from low to high level.

(1) An internal operational amplifier compares the Drain-Source MOSFET voltage with the internal reference (2.7V Typ.). The relevant Lowside PowerMOS is switched off when its Drain-Source voltage exceeds the reference voltage.

TRUTH TABLE IN FAULT CONDITIONS (detected on OUT_A)

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B
1	1	0	1	OPEN	H
1	0	0	1	OPEN	L
0	1	0	1	OPEN	H
0	0	0	1	OPEN	L
X	X	0	0	OPEN	OPEN
X	1	0	1	OPEN	H
X	0	0	1	OPEN	OPEN

Fault Information — Protection Action

TEST MODE

The PWM pin allows to test the load connection between two half-bridges. In the test mode (V_{pwm}=-2V) the internal Power Mos gate drivers are disabled. The IN_A or IN_B inputs allow to turn-on the High Side A or B, respectively, in order to connect one side of the load at V_{CC} voltage. The check of the voltage on the other side of the load allow to verify the continuity of the load connection. In case of load disconnection the $DIAD_X/EN_X$ pin corresponding to the faulty output is pulled down.

ELECTRICAL TRANSIENT REQUIREMENTS

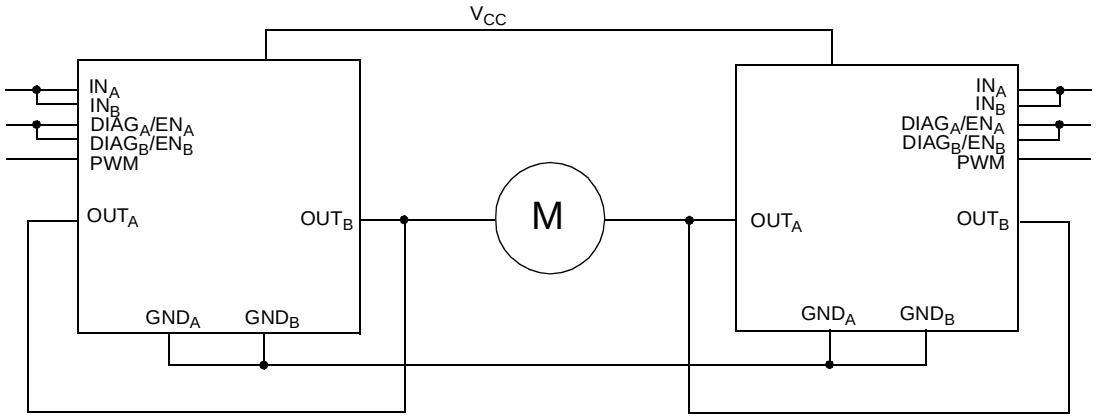
ISO T/R 7637/1 Test Pulse	Test Level I	Test Level II	Test Level III	Test Level IV	Test Levels Delays and Impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1µs, 50Ω
3b	+25V	+50V	+75V	+100V	0.1µs, 50Ω
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R 7637/1 Test Pulse	Test Levels Result I	Test Levels Result II	Test Levels Result III	Test Levels Result IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

HALF-BRIDGE CONFIGURATION

The VNH3SP30 can be used as a high power half-bridge driver achieving an on resistance per leg of 22.5mΩ. Suggested configuration is the following:



MULTI-MOTORS CONFIGURATION

The VNH3SP30 can easily be designed in multi-motors driving applications such as seat positioning systems where only one motor must be driven at a time. $DIAG_X/EN_X$ pins allow to put unused half-bridges in high impedance. Suggested configuration is the following:

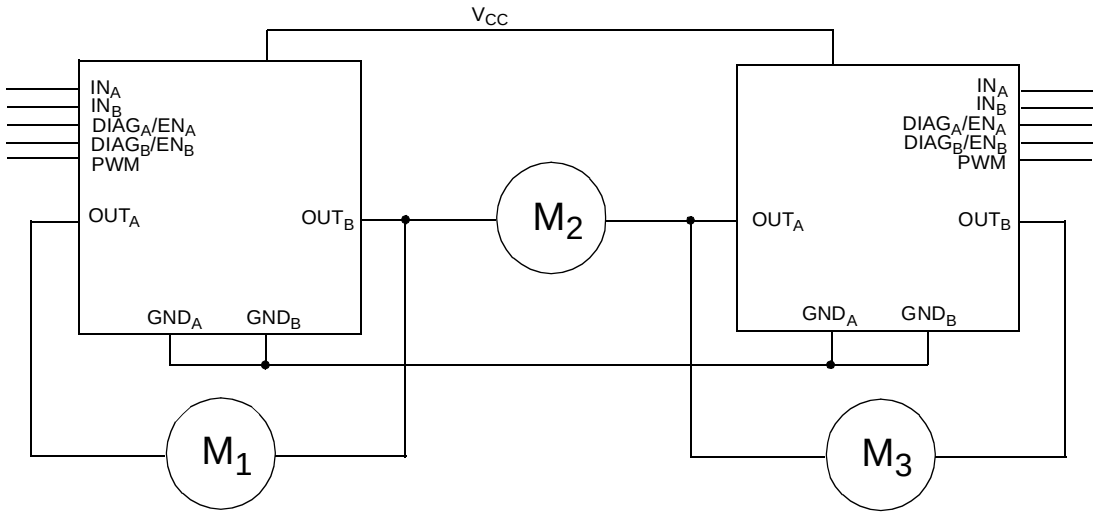


Figure 1: Definition of the delay times measurement (example of clockwise operation)

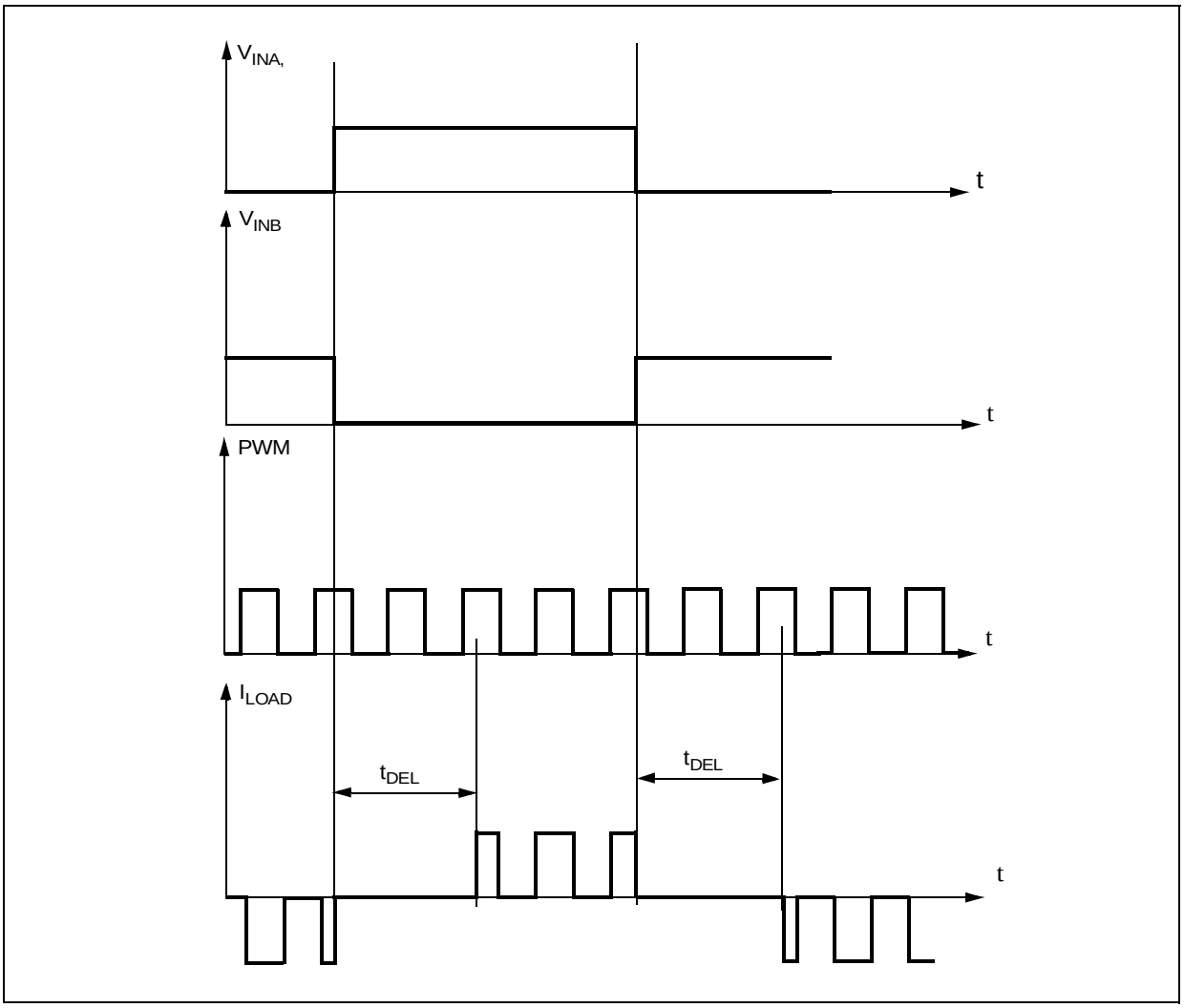


Figure 2: Definition of the Low Side Switching times

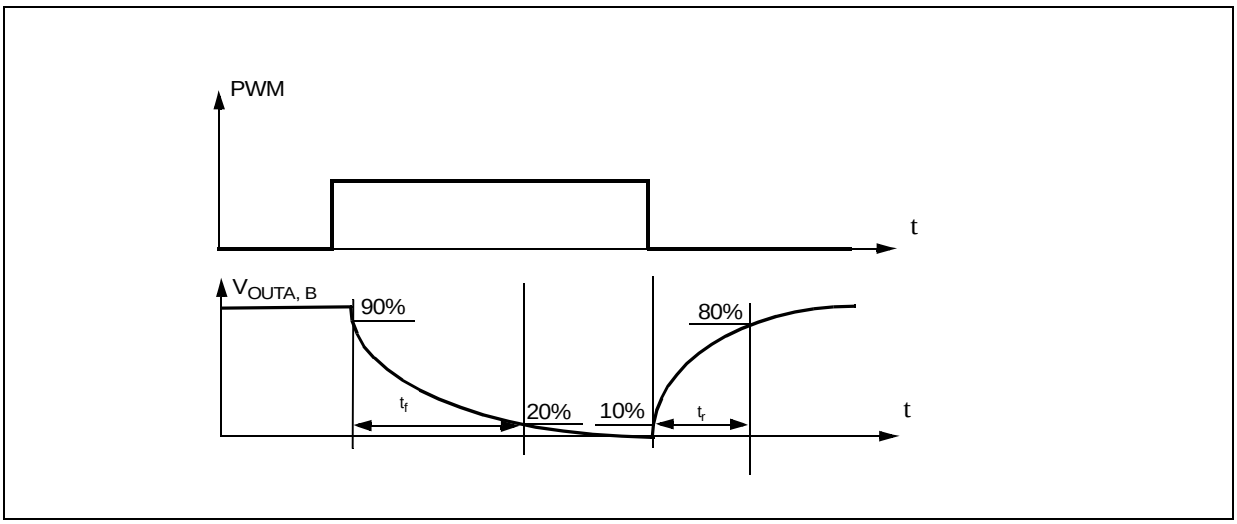
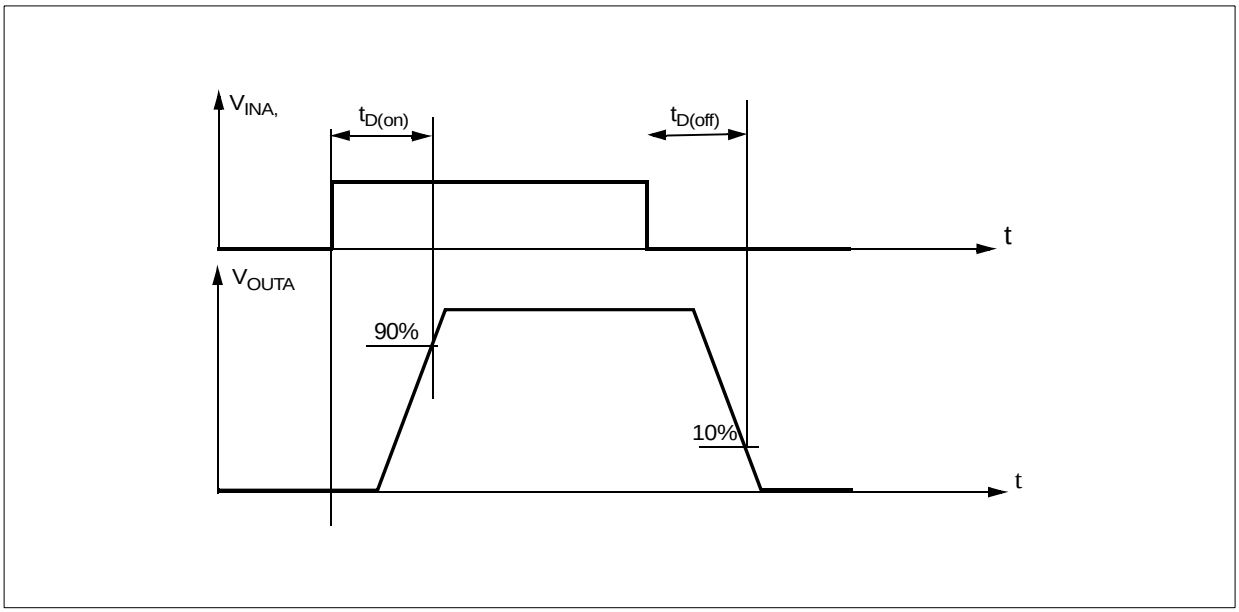
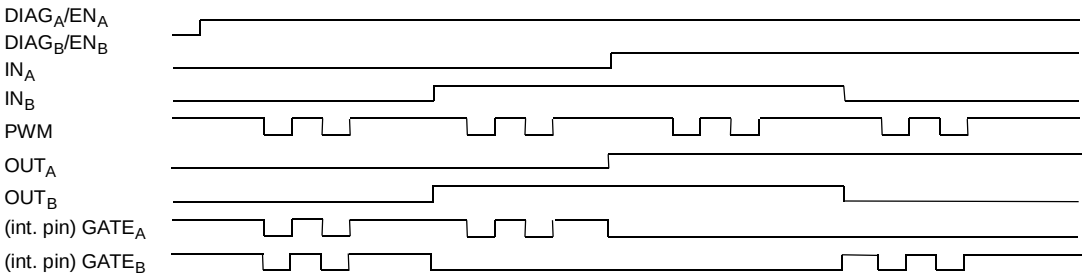


Figure 3: Definition of the High side Switching times

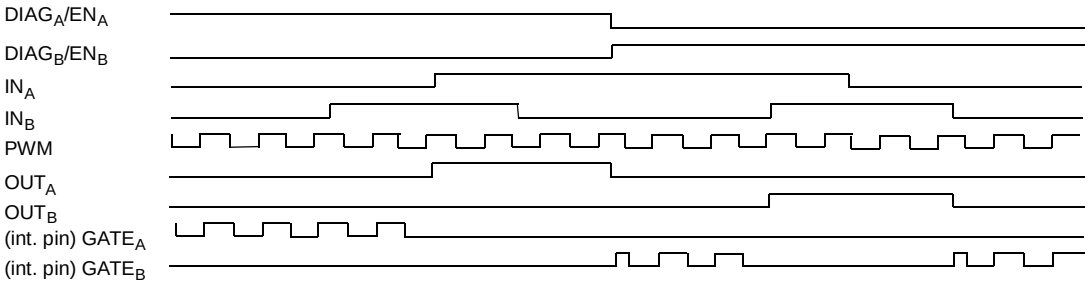


Waveforms

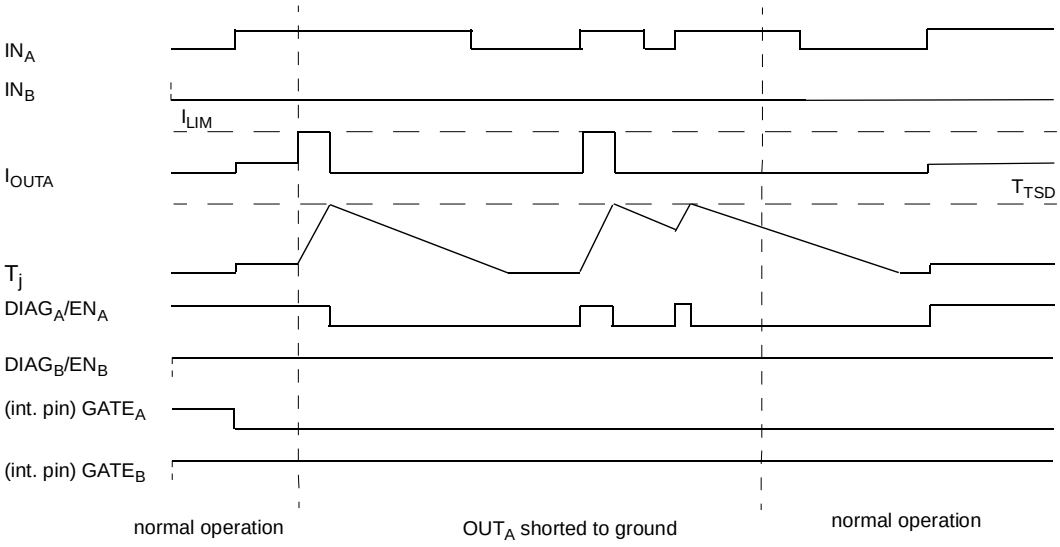
NORMAL OPERATION ($DIAG_A/EN_A$=1, $DIAG_B/EN_B$=1)



NORMAL OPERATION ($DIAG_A/EN_A$=1, $DIAG_B/EN_B$=0 and $DIAG_A/EN_A$=0, $DIAG_B/EN_B$=1)

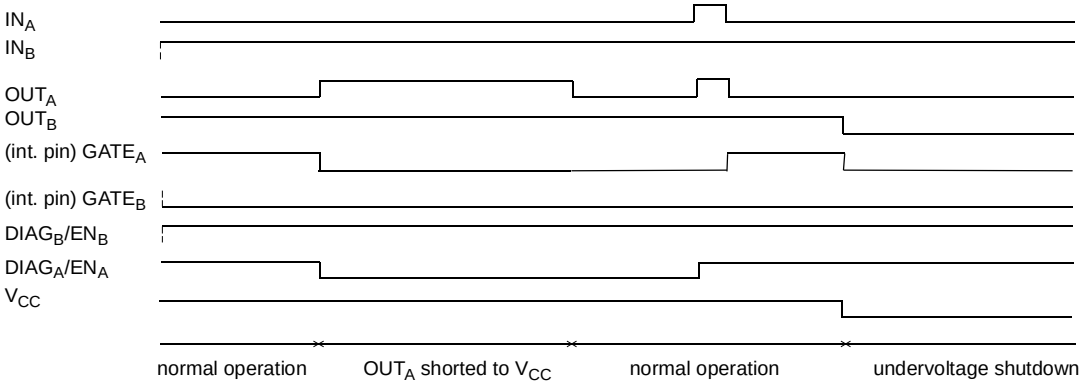


CURRENT LIMITATION/THERMAL SHUTDOWN or OUT_A SHORTED TO GROUND

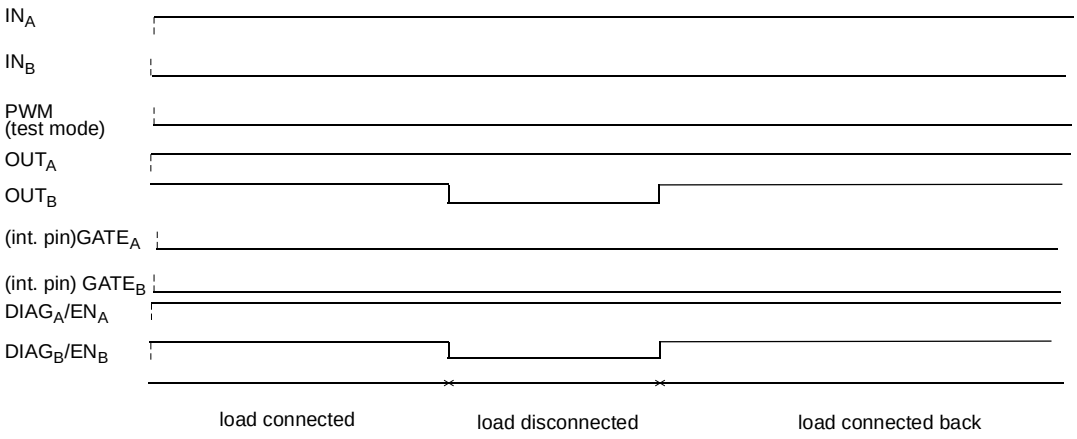


Waveforms (Continued)

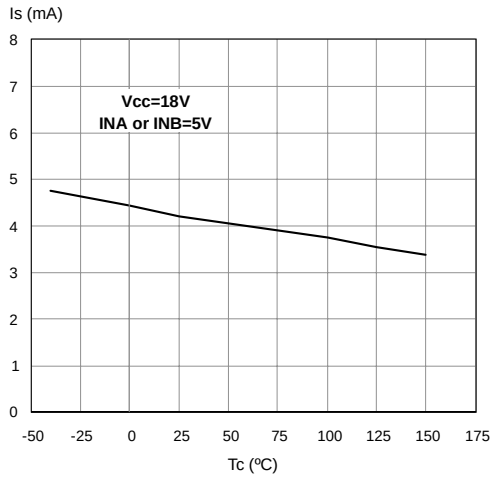
OUT_A shorted to V_{CC} and undervoltage shutdown



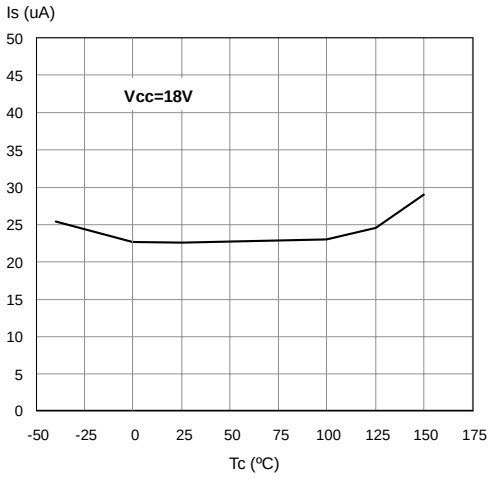
Load disconnection test (IN_A=1, PWM=-2V)



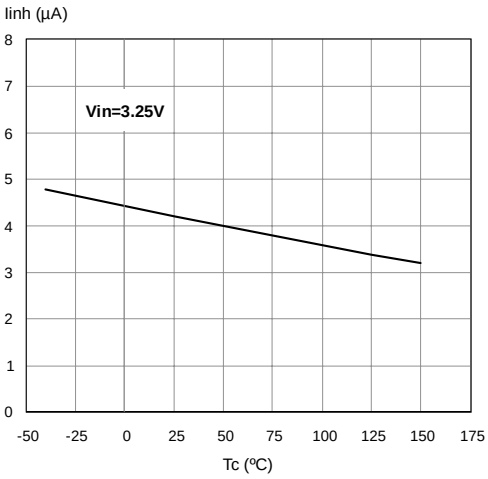
On State Supply Current



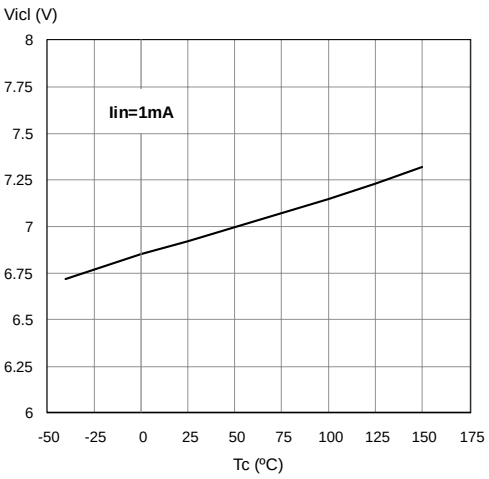
Off State Supply Current



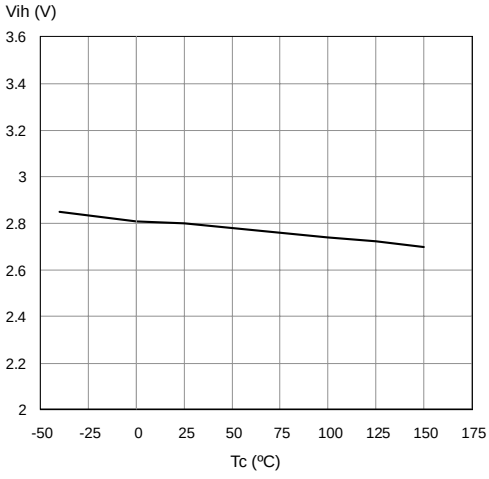
High Level Input Current



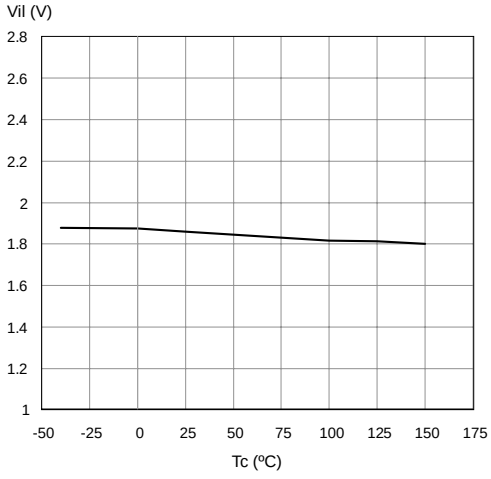
Input Clamp Voltage



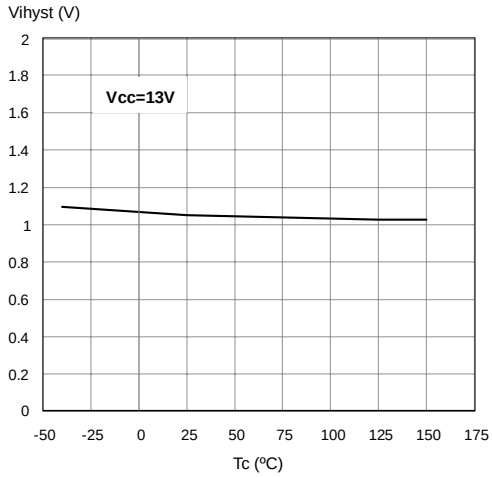
Input High Level Voltage



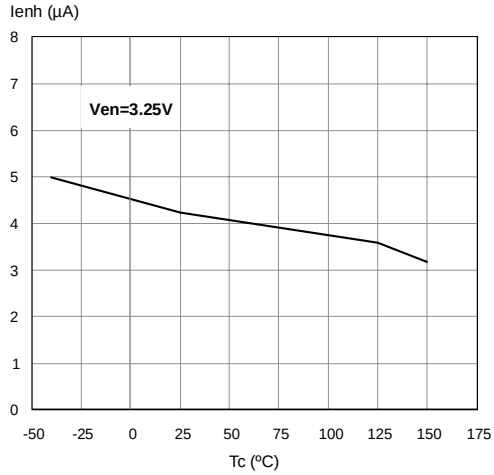
Input Low Level Voltage



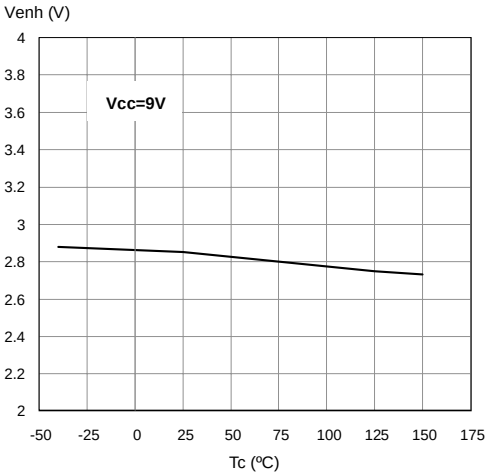
Input Hysteresis Voltage



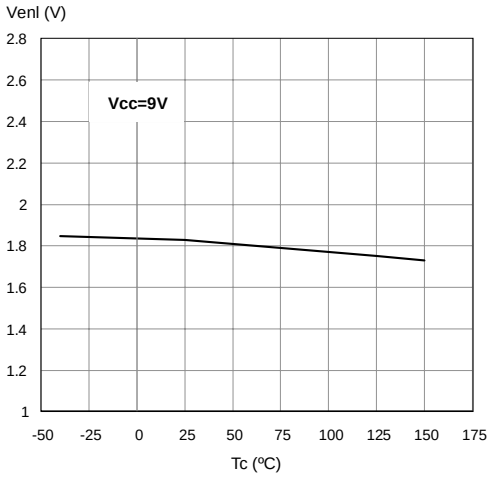
High Level Enable Pin Current



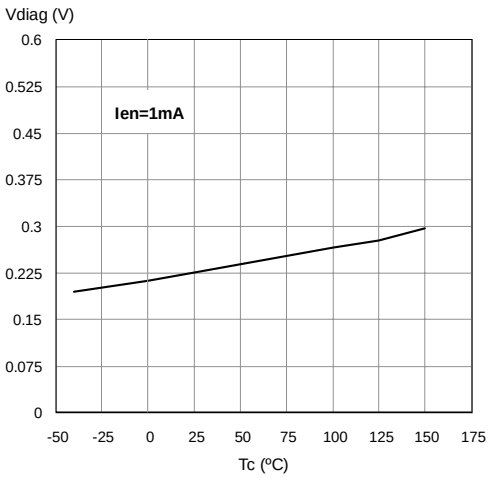
High Level Enable Voltage



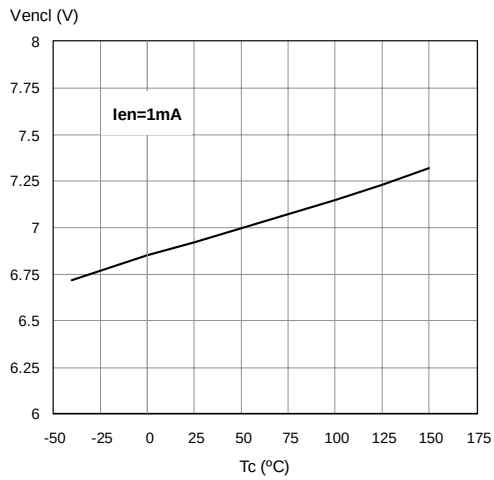
Low Level Enable Voltage



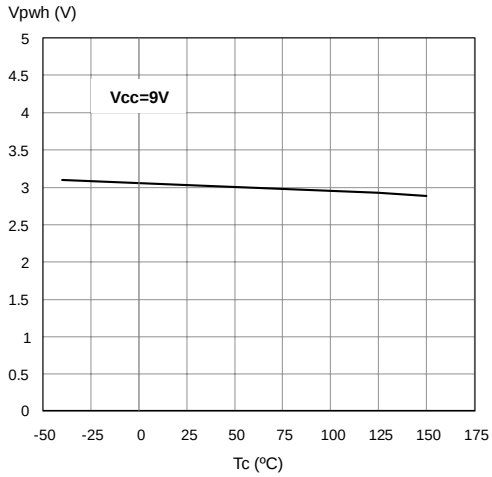
Enable Output Low Level Voltage



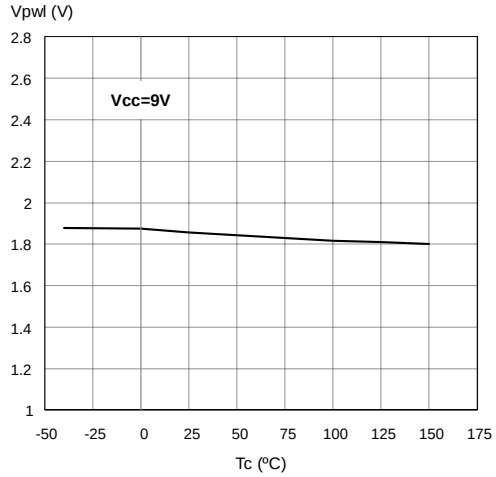
Enable Clamp Voltage



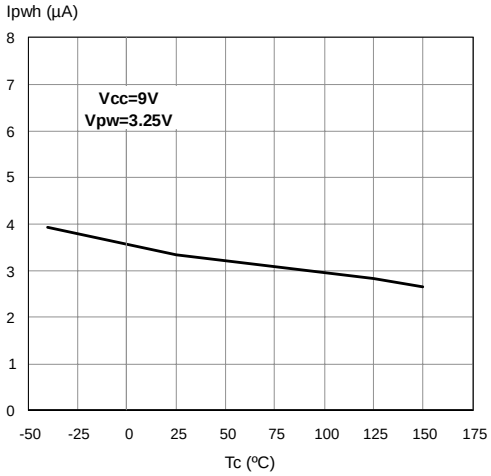
PWM High Level Voltage



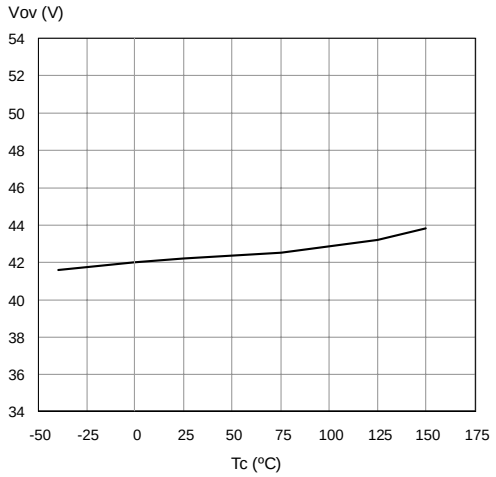
PWM Low Level Voltage



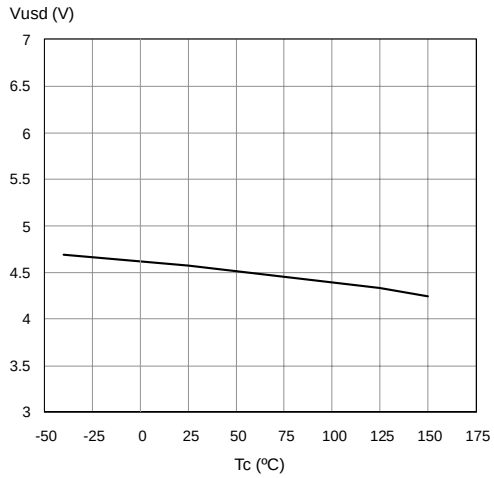
PWM High Level Current



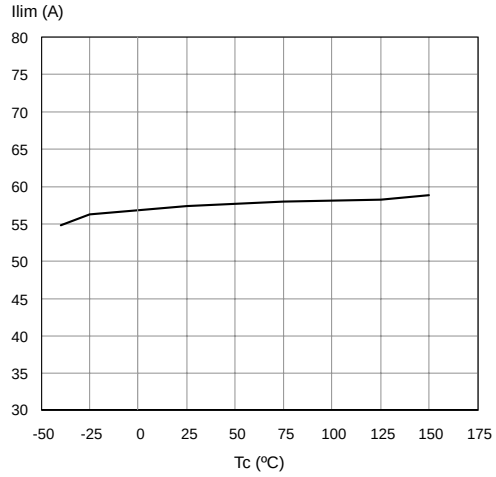
Overvoltage Shutdown



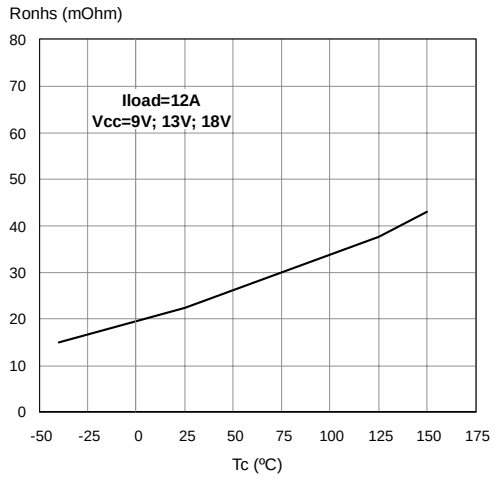
Undervoltage Shutdown



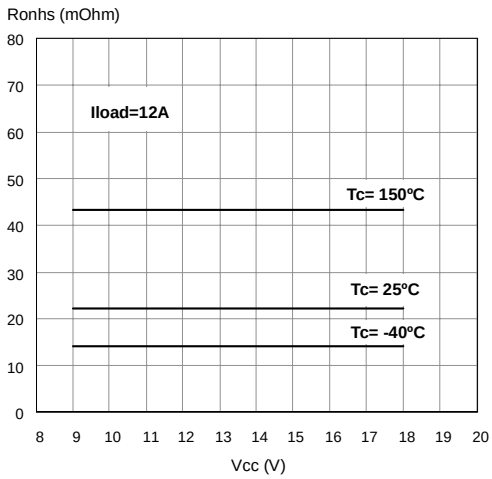
Current Limitation



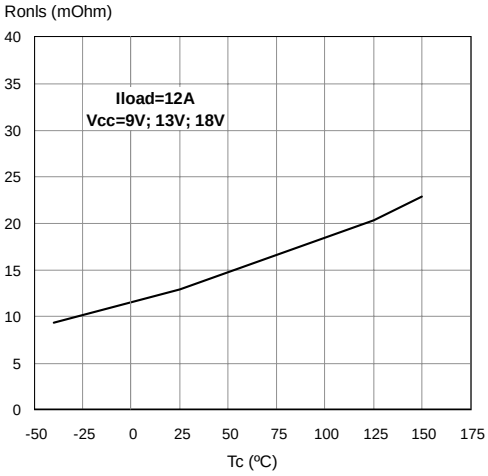
On State High Side Resistance Vs. T_{case}



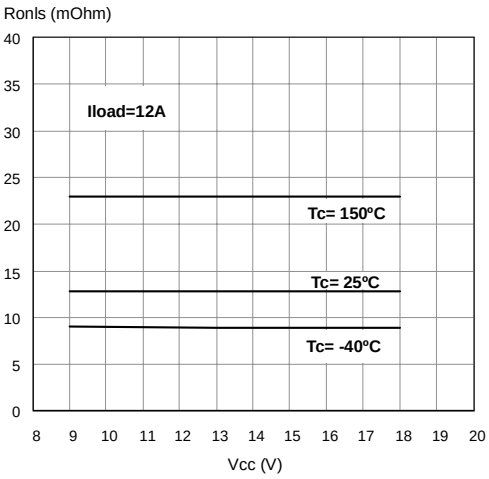
On State High Side Resistance Vs. V_{CC}



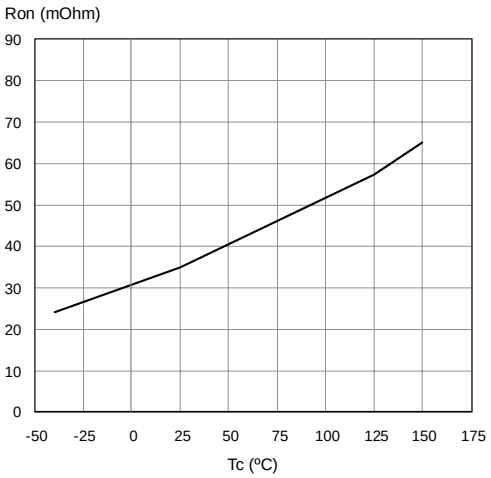
On State Low Side Resistance Vs. T_{case}



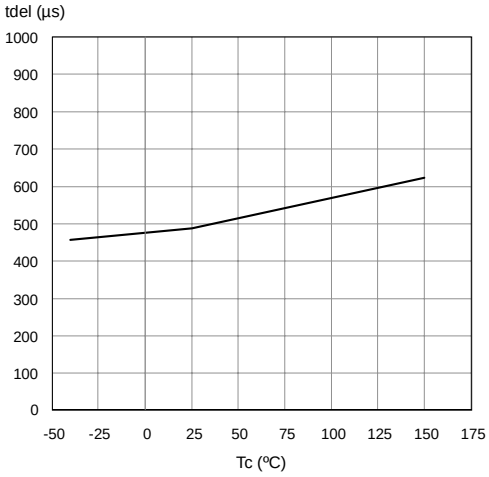
On State Low Side Resistance Vs. V_{CC}



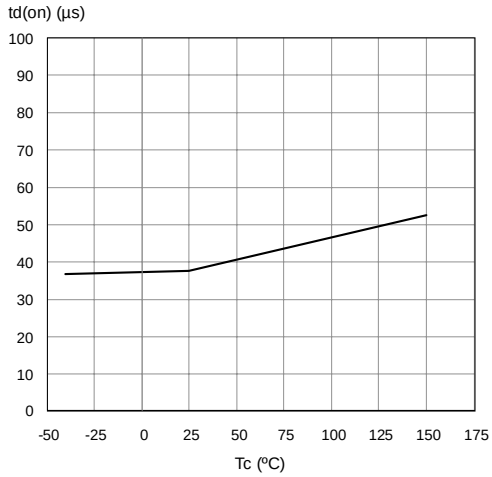
On State Leg Resistance



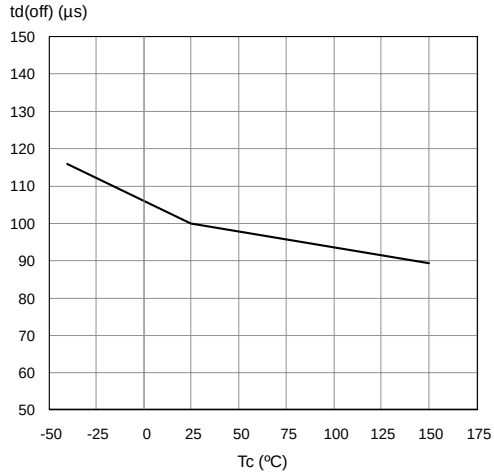
Delay Time during change of operation mode



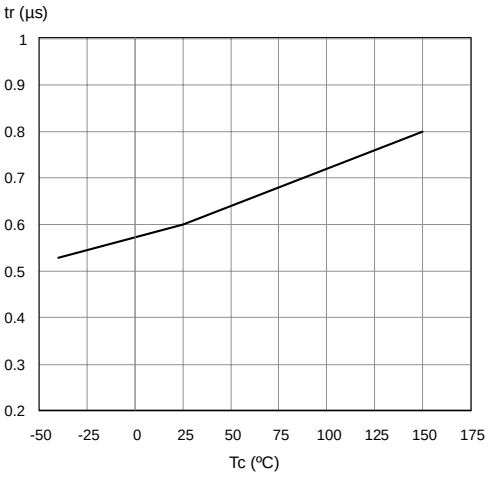
Turn-on Delay Time



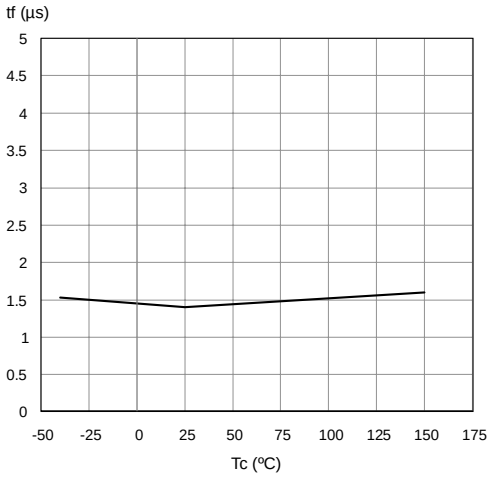
Turn-off Delay Time



Output Voltage Rise Time

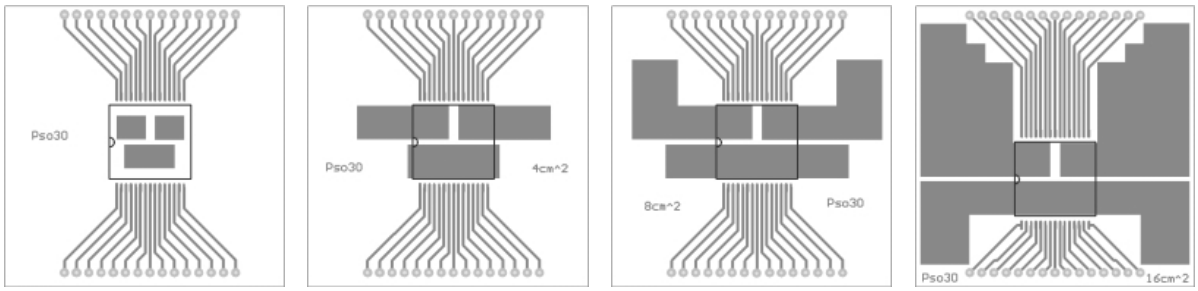


Output Voltage Fall Time



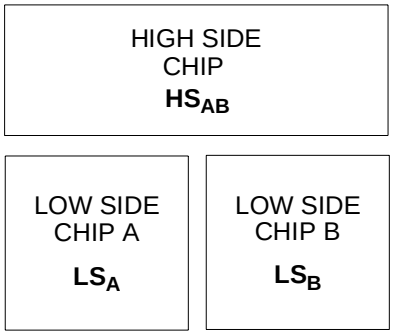
MultiPowerSO-30 THERMAL DATA

MultiPowerSO-30 PC Board

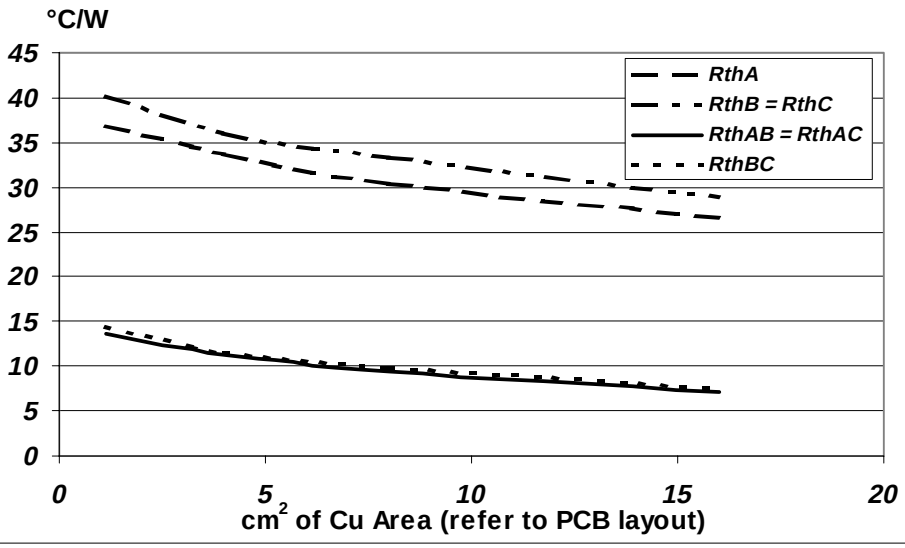


Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: from minimum pad lay-out to 16cm^2).

CHIPSET CONFIGURATION



Auto and mutual $R_{thj-amb}$ Vs PCB copper area in open box free air condition (according to page 20 definitions)



THERMAL CALCULATION IN CLOCKWISE AND ANTI-CLOCKWISE OPERATION IN STEADY-STATE MODE

HS_A	HS_B	LS_A	LS_B	T_{jHSAB}	T_{jLSA}	T_{jLSB}
ON	OFF	OFF	ON	$P_{dHSA} \times R_{thHS} + P_{dLSB} \times R_{thHSLS} + T_{amb}$	$P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLSLS} + T_{amb}$	$P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLS} + T_{amb}$
OFF	ON	ON	OFF	$P_{dHSB} \times R_{thHS} + P_{dLSA} \times R_{thHSLS} + T_{amb}$	$P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLS} + T_{amb}$	$P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLSLS} + T_{amb}$

Thermal resistances definition (values according to the PCB heatsink area)

R_{thHS} = R_{thHSA} = R_{thHSB} = High Side Chip Thermal Resistance Junction to Ambient (HS_A or HS_B in ON state)

R_{thLS} = R_{thLSA} = R_{thLSB} = Low Side Chip Thermal Resistance Junction to Ambient

R_{thHSLS} = $R_{thHSALSB}$ = $R_{thHSBLSA}$ = Mutual Thermal Resistance Junction to Ambient between High Side and Low Side Chips

R_{thLSLS} = $R_{thLSALSB}$ = Mutual Thermal Resistance Junction to Ambient between Low Side Chips

THERMAL CALCULATION IN TRANSIENT MODE (*)

$T_{jHSAB} = Z_{thHS} \times P_{dHSAB} + Z_{thHSLS} \times (P_{dLSA} + P_{dLSB}) + T_{amb}$

$T_{jLSA} = Z_{thHSLS} \times P_{dHSAB} + Z_{thLS} \times P_{dLSA} + Z_{thLSLS} \times P_{dLSB} + T_{amb}$

$T_{jLSB} = Z_{thHSLS} \times P_{dHSAB} + Z_{thLSLS} \times P_{dLSA} + Z_{thLS} \times P_{dLSB} + T_{amb}$

Single pulse thermal impedance definition (values according to the PCB heatsink area)

Z_{thHS} = High Side Chip Thermal Impedance Junction to Ambient

Z_{thLS} = Z_{thLSA} = Z_{thLSB} = Low Side Chip Thermal Impedance Junction to Ambient

Z_{thHSLS} = $Z_{thHSABLSA}$ = $Z_{thHSABLSB}$ = Mutual Thermal Impedance Junction to Ambient between High Side and Low Side Chips

Z_{thLSLS} = $Z_{thLSALSB}$ = Mutual Thermal Impedance Junction to Ambient between Low Side Chips

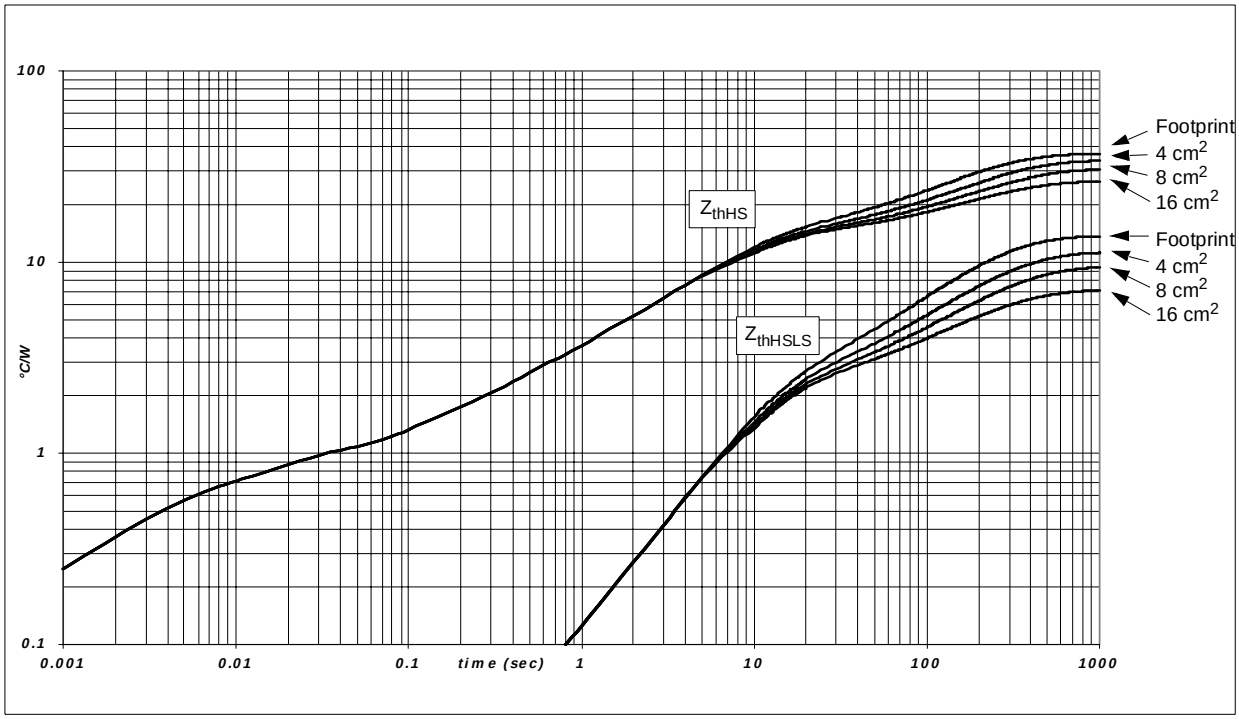
Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

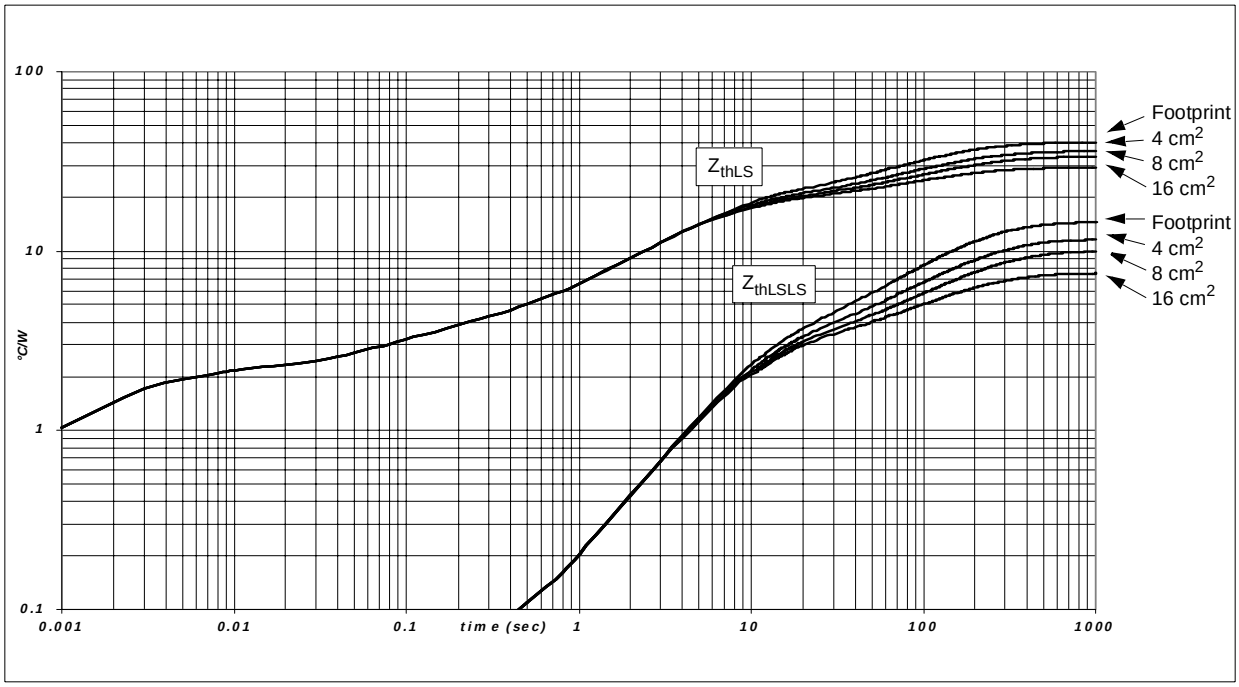
where $\delta = t_p / T$

(*) Calculation is valid in any dynamic operating condition. P_d values set by user.

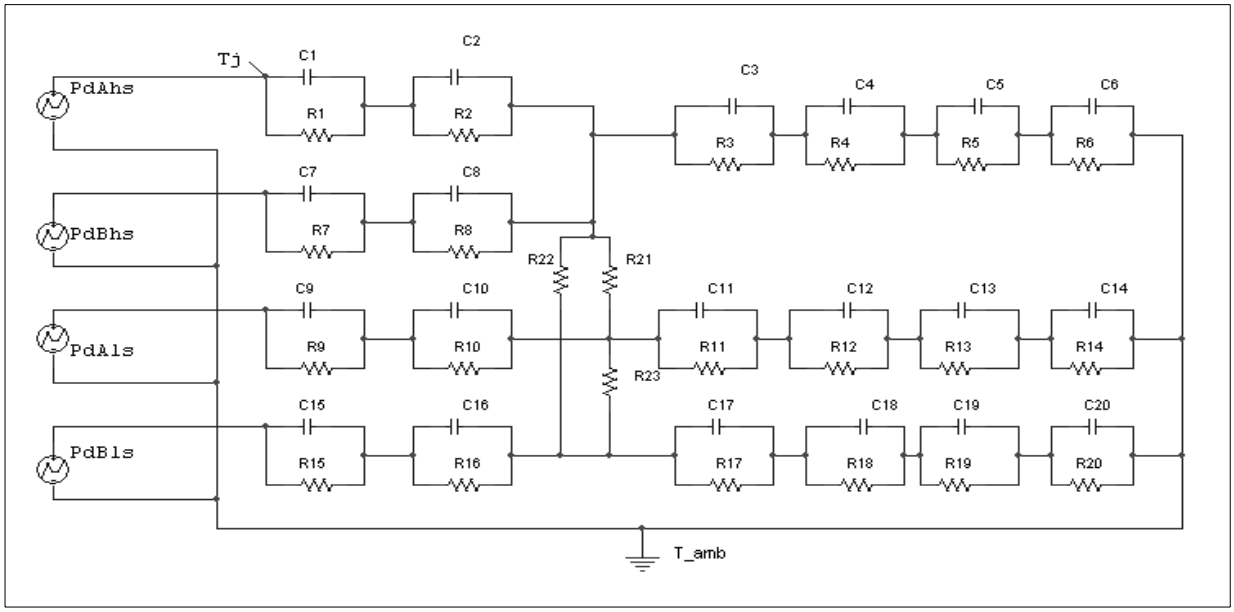
MultiPowerSO-30 HSD Thermal Impedance Junction Ambient Single Pulse



MultiPowerSO-30 LSD Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of an H-Bridge in MultiPowerSO-30



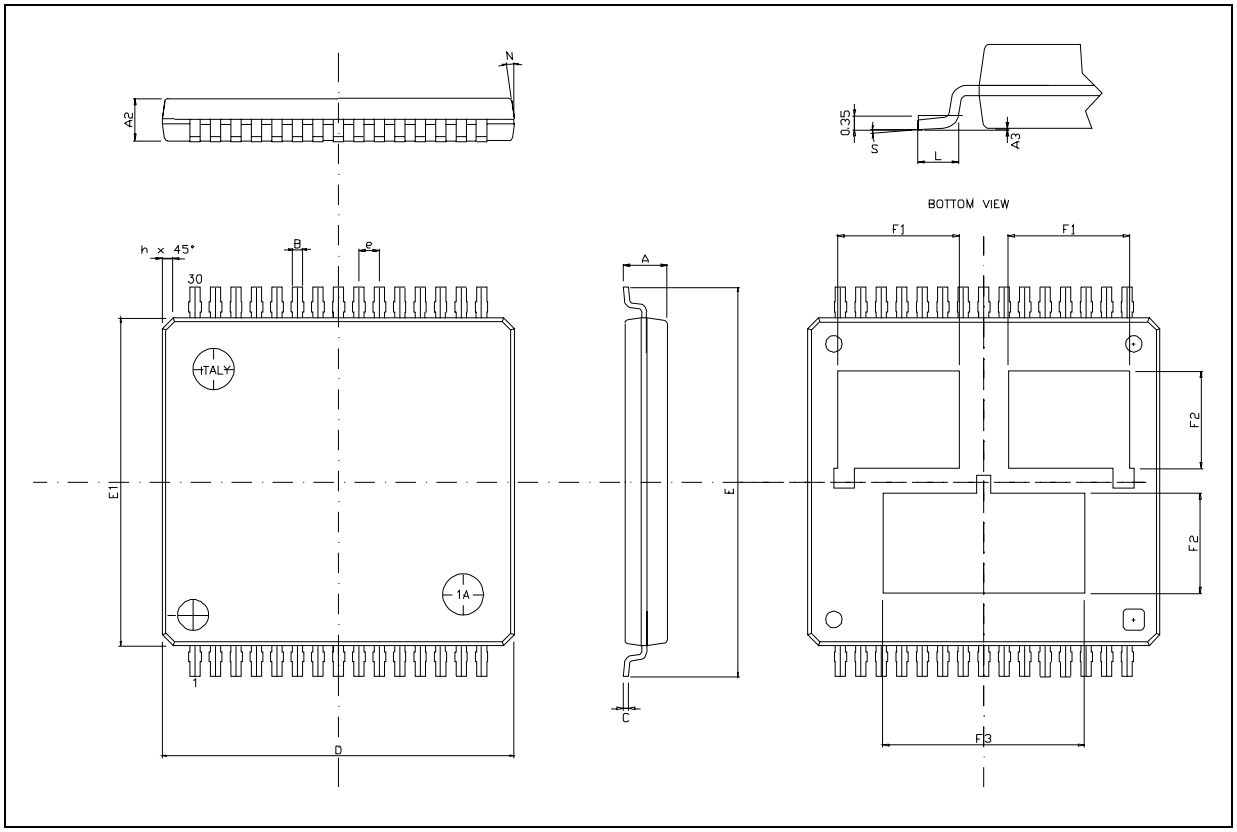
Thermal Parameter (*)

Area/island (cm^2)	Footprint	4	8	16
R1=R7 (°C/W)	0.05			
R2=R8 (°C/W)	0.3			
R3 (°C/W)	0.5			
R4 (°C/W)	1.3			
R5 (°C/W)	1.4			
R6 (°C/W)	44.7	39.1	31.6	23.7
R9=R10=R15=R16 (°C/W)	0.6			
R11=R17 (°C/W)	0.8			
R12=R18 (°C/W)	1.5			
R13=R19 (°C/W)	20			
R14=R20 (°C/W)	46.9	36.1	30.4	20.8
R21=R22=R23 (°C/W)	115			
C1=C7 (W.s/°C)	0.001			
C2=C8 (W.s/°C)	0.005			
C3 (W.s/°C)	0.02			
C4=C13=C19 (W.s/°C)	0.3			
C5 (W.s/°C)	0.6			
C6 (W.s/°C)	5	7	9	11
C9=C15 (W.s/°C)	0.001			
C10=C11=C16=C17 (W.s/°C)	0.003			
C12=C18 (W.s/°C)	0.075			
C14=C20 (W.s/°C)	2.5	3.5	4.5	5.5

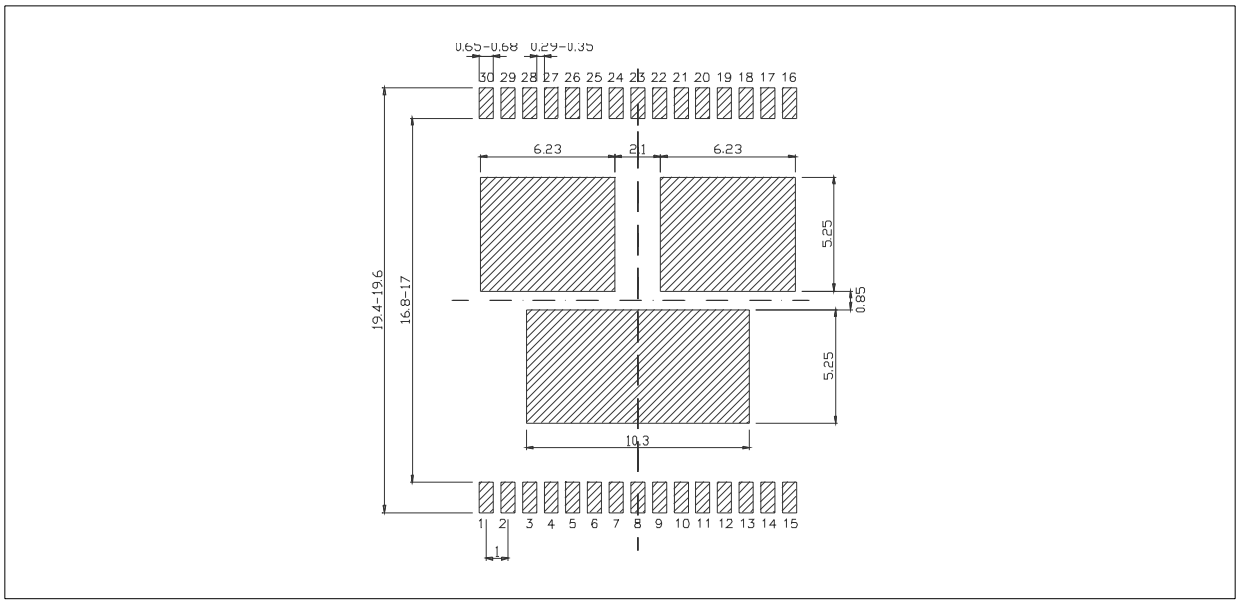
(*) The blank space means that the value is the same as the previous one.

MultiPowerSO-30 MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1
e		1	
F1	5.55		6.05
F2	4.6		5.1
F3	9.6		10.1
L	0.8		1.15
N			10deg
S	0deg		7deg



MultiPowerSO-30 SUGGESTED PAD LAY-OUT



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may results from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.
The ST logo is a trademark of STMicroelectronics

© 2004 STMicroelectronics - Printed in ITALY- All Rights Reserved.

STMicroelectronics GROUP OF COMPANIES
Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com