



VND5050AJ-E VND5050AK-E

Double channel high side driver with analog current sense
for automotive applications

Features

Max transient supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 36V
Max On-State resistance (per ch.)	R_{ON}	50 m Ω
Current limitation (typ)	I_{LIMH}	18 A
Off state supply current	I_S	2 $\mu A^{(1)}$

1. Typical value with all loads connected

■ Main

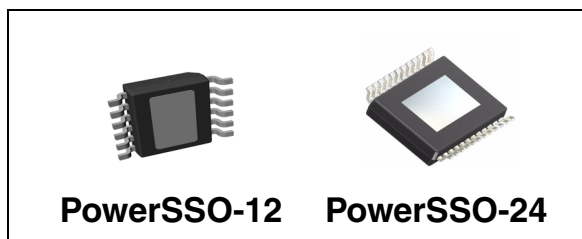
- Inrush current active management by power limitation
- Very low stand-by current
- 3.0V CMOS compatible input
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/ec european directive

■ Diagnostic Functions

- Proportional load current sense
- High current sense precision for wide range currents
- Current sense disable
- Thermal shutdown indication
- Very low current sense leakage

■ Protections

- Undervoltage shut-down
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Thermal shut down
- Reverse battery protection (see [Application schematic](#))
- Electrostatic discharge protection



Application

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VND5050AJ-E, VND5050AK-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open.

When CS_DIS is driven high, the current sense pin is in a high impedance condition.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

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1 Block diagram and pin description

Figure 1. Block diagram

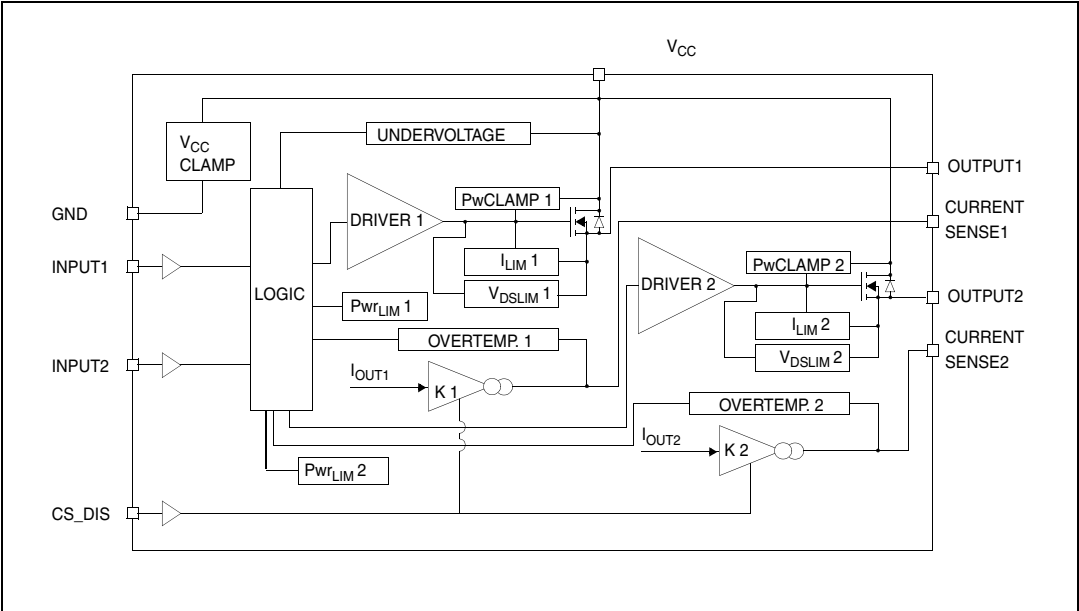


Table 1. Pin function

Name	Function
V _{CC}	Battery connection.
OUTPUT _{1,2}	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUT _{1,2}	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE _{1,2}	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

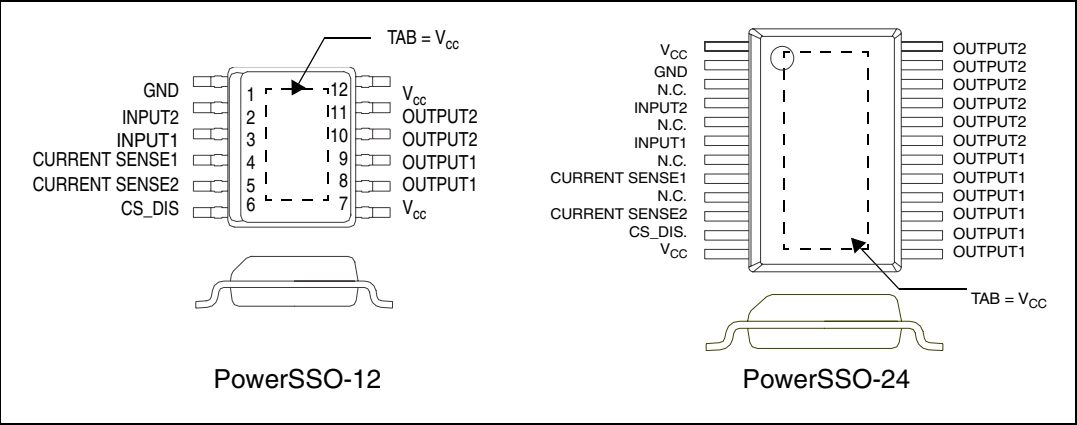


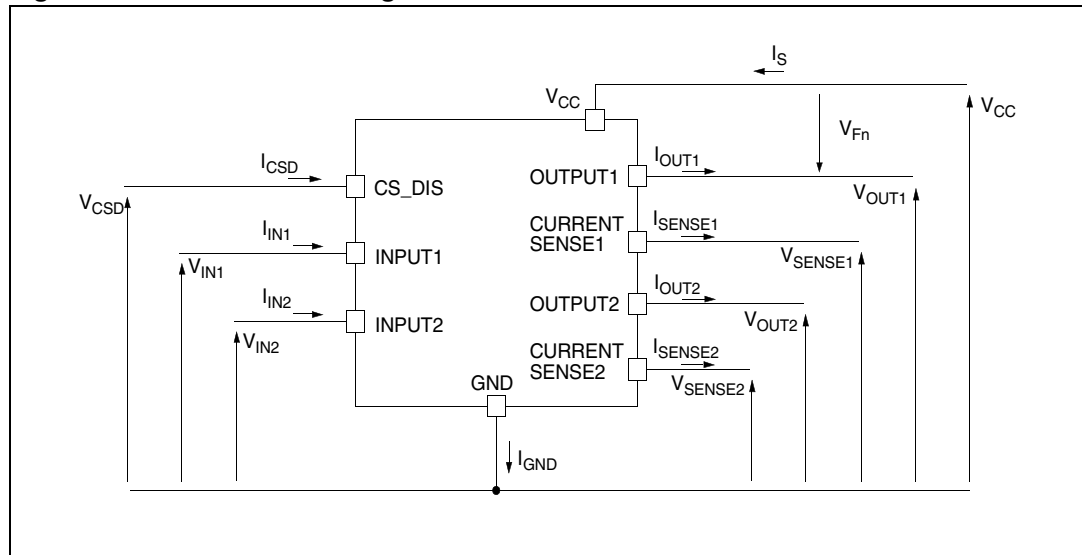
Table 2. Suggested connections for unused and N.C. pins

Connection / pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	N.R. ⁽¹⁾	X	X	X	X
To ground	Through 1K Ω resistor	X	N.R. ⁽¹⁾	Through 10K Ω resistor	Through 10K Ω resistor

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	12	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy ($L=3\text{mH}$; $R_L=0\Omega$; $V_{bat}=13.5\text{V}$; $T_{jstart}=150^\circ\text{C}$; $I_{OUT}=I_{limL}(Typ.)$)	104	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V _{ESD}	Electrostatic discharge (Human Body Model: R=1.5KΩ, C=100pF)		
	– INPUT	4000	V
	– CURRENT SENSE	2000	V
	– CS_DIS	4000	V
	– OUTPUT	5000	V
	– V _{CC}	5000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value		Unit
		PowerSSO-12	PowerSSO-24	
R _{thj-case}	Thermal resistance junction-case (Max.) (with one channel ON)	2.7	2.7	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (Max.)	See Figure 29	See Figure 33	°C/W

2.3 Electrical characteristics

$8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On state resistance ⁽²⁾	$I_{OUT} = 2A$; $T_j = 25^{\circ}C$ $I_{OUT} = 2A$; $T_j = 150^{\circ}C$ $I_{OUT} = 2A$; $V_{CC} = 5V$; $T_j = 25^{\circ}C$			50 100 65	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	$I_S = 20mA$	41	46	52	V
I_S	Supply current	Off State; $V_{CC} = 13V$; $T_j = 25^{\circ}C$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0V$ On State; $V_{CC} = 13V$; $V_{IN} = 5V$; $I_{OUT} = 0A$		2 ⁽¹⁾ 3	5 ⁽¹⁾ 6	μA mA
$I_{L(off)}$	Off state output current ⁽²⁾	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$ $V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$	0 0	0.01	3 5	μA
V_F	Output - V_{CC} diode voltage ⁽²⁾	$-I_{OUT} = 4A$; $T_j = 150^{\circ}C$			0.7	V

1. PowerMOS leakage included.

2. For each channel.

Table 6. Switching ($V_{CC} = 13V$; $T_j = 25^{\circ}C$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On delay time	$R_L = 6.5\Omega$ (see Figure 8)		25		μs
$t_{d(off)}$	Turn-Off delay time	$R_L = 6.5\Omega$ (see Figure 8)		35		μs
$dV_{OUT}/dt_{(on)}$	Turn-On voltage slope	$R_L = 6.5\Omega$	See Figure 21			V/ μs
$dV_{OUT}/dt_{(off)}$	Turn-Off voltage slope	$R_L = 6.5\Omega$	See Figure 22			V/ μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 6.5\Omega$ (see Figure 8)		0.24		mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 6.5\Omega$ (see Figure 8)		0.2		mJ

Table 7. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9V$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	5.5	-0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD} = 0.9V$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD} = 2.1V$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD} = 1mA$ $I_{CSD} = -1mA$	5.5	-0.7	7	V V

Table 8. Protections and diagnostics (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	$V_{CC} = 13V$ $5V < V_{CC} < 36V$	12	18	24 24	A A
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 13V$; $T_R < T_J < T_{TSD}$		7		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}C$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}C$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}C$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}C$
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT} = 2A$; $V_{IN} = 0$; $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 0.1A$; $T_J = -40^{\circ}C \dots +150^{\circ}C$ (see Figure 9)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8V<V_{CC}<16V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} =0.05A; V _{SENSE} =0.5V; V _{CSD} =0V; T _j = -40°C...150°C	1270	2360	3450	
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} =1A; V _{SENSE} =0.5V; V _{CSD} =0V; T _j = -40°C T _j = 25°C...150°C	1470 1570	2020 2020	2610 2470	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} =1A; V _{SENSE} = 0.5V; V _{CSD} =0V; T _J =-40 °C to 150 °C	-7		+7	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} =2A; V _{SENSE} =4V; V _{CSD} =0V; T _j = -40°C T _j = 25°C...150°C	1740 1790	2020 2020	2320 2250	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} =2 A; V _{SENSE} = 4 V; V _{CSD} =0V; T _J =-40 °C to 150 °C	-4		+4	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} =4A; V _{SENSE} =4V; V _{CSD} =0V; T _j =-40°C T _j =25°C...150°C	1880 1900	2010 2010	2160 2120	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} =4 A; V _{SENSE} = 4 V; V _{CSD} =0V; T _J =-40 °C to 150 °C	-2		+2	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} =0A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =0V; T _j =-40°C...150°C	0		1	μA
		V _{CSD} =0V; V _{IN} =5V; T _j =-40°C...150°C	0		2	μA
		I _{OUT} =2A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =5V; T _j =-40°C...150°C	0		1	μA
I _{OL}	Openload ON state current detection threshold	V _{IN} = 5V, I _{SENSE} = 5 μA	4		20	mA
V _{SENSE}	Max analog sense output voltage	I _{OUT} =4A; V _{CSD} =0V	5			V
V _{SENSEH}	Analog sense output voltage in overtemperature condition	V _{CC} =13V; R _{SENSE} =10KΩ		9		V

Table 9. Current sense (8V<V_{CC}<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SENSEH}	Analog sense output current in overtemperature condition	V _{CC} =13V; V _{SENSE} =5V		8		mA
t _{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} <4V, 0.5A<I _{out} <4A I _{SENSE} =90% of I _{SENSE max} (see Figure 4)		50	100	μs
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} <4V, 0.5A<I _{out} <4A I _{SENSE} =10% of I _{SENSE max} (see Figure 4)		5	20	μs
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} <4V, 0.5A<I _{out} <4A I _{SENSE} =90% of I _{SENSE max} (see Figure 4)		80	250	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4V, I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} =2A (see Figure 5)			65	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pin	V _{SENSE} <4V, 0.5A<I _{out} <4A I _{SENSE} =10% of I _{SENSE max} (see Figure 4)		100	250	μs

1. Parameter guaranteed by design; it is not tested.

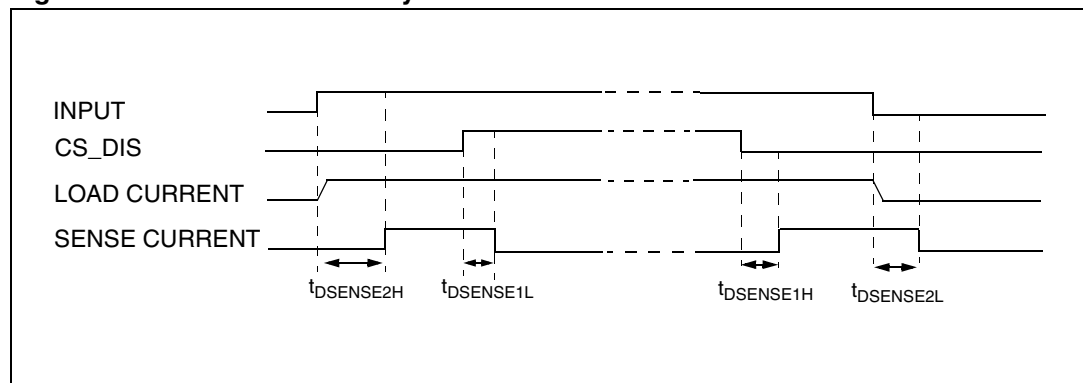
Figure 4. Current sense delay characteristics

Figure 5. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

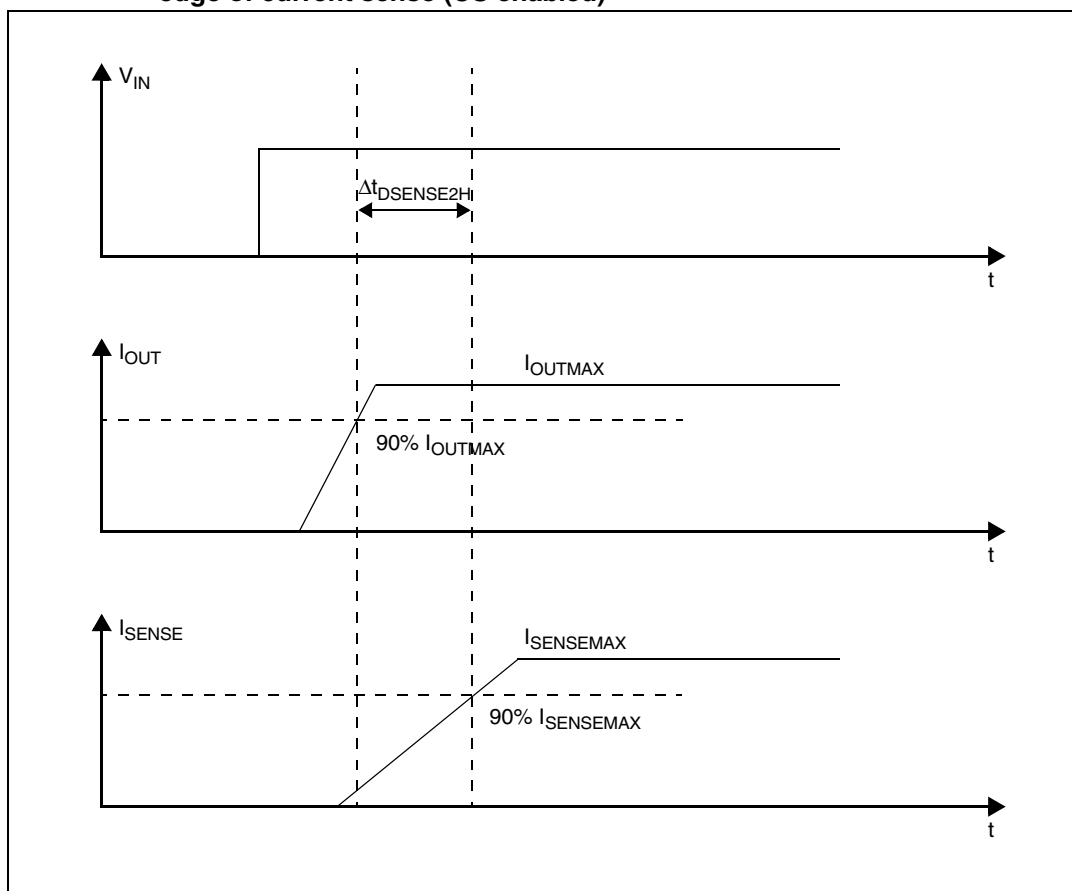


Figure 6. I_{OUT}/I_{SENSE} Vs. I_{OUT}

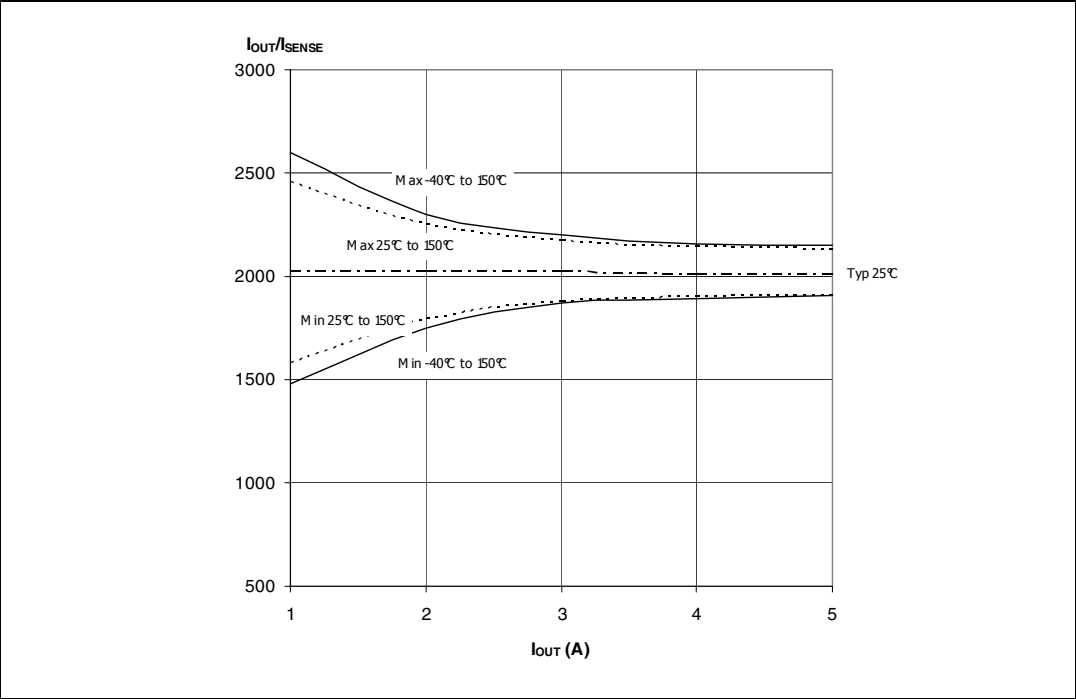
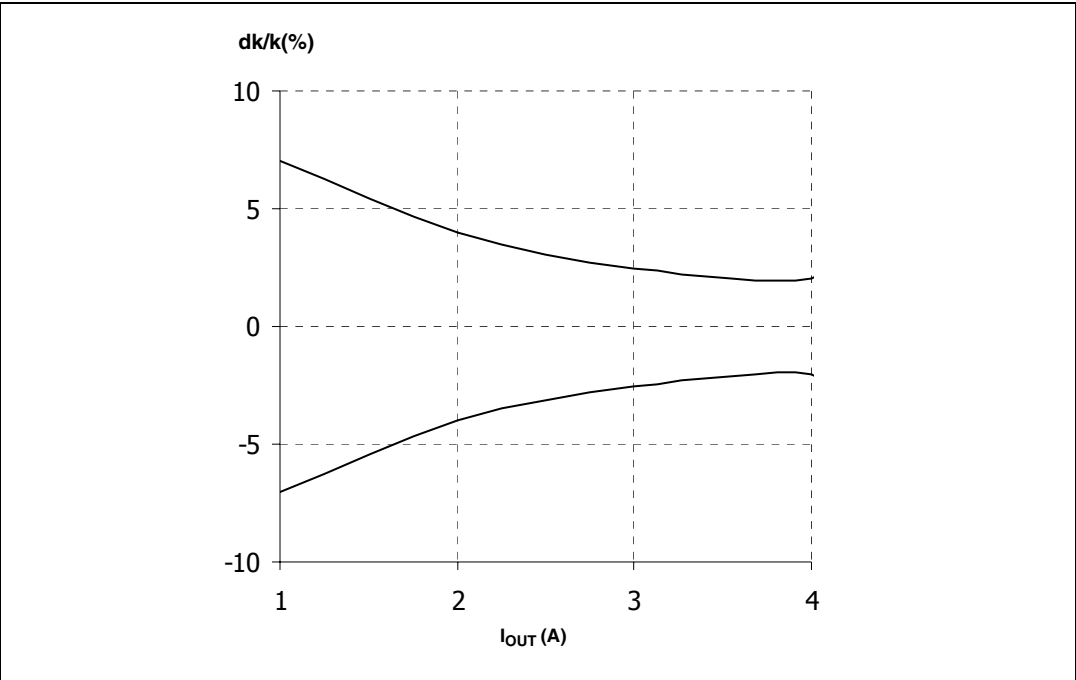


Figure 7. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 10. Truth table

Conditions	Input	Output	Sense ($V_{CSD}=0V$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Short circuit to GND ($R_{sc} \leq 10 \text{ m}\Omega$)	L	L	0
	H	L	0 if $T_j < T_{TSD}$
	H	L	V_{SENSEH} if $T_j > T_{TSD}$
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

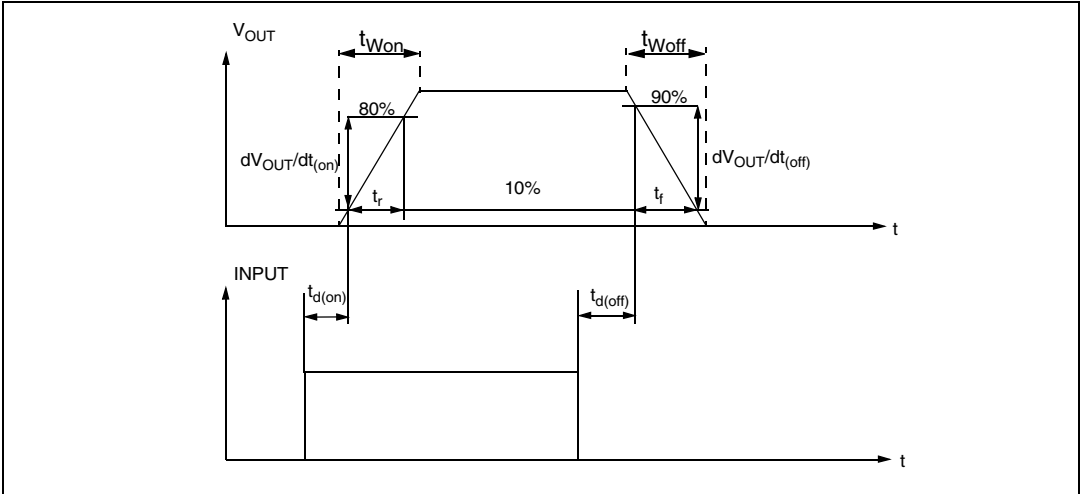


Figure 9. Output voltage drop limitation

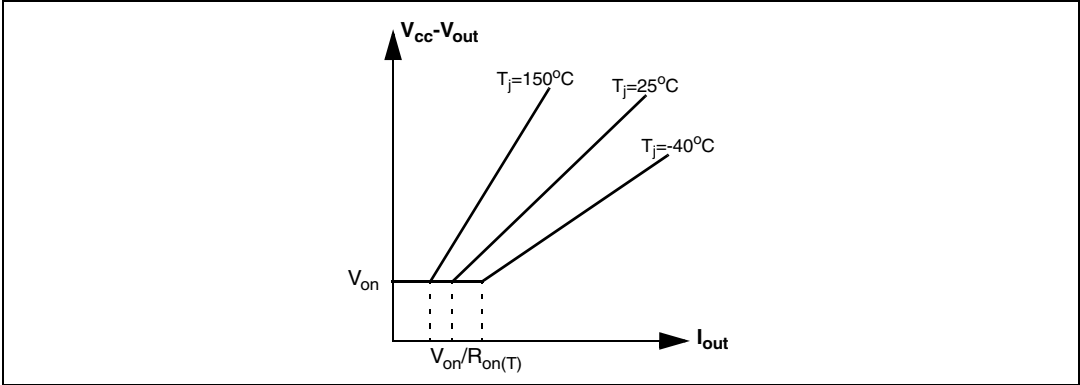


Table 11. Electrical transient requirements

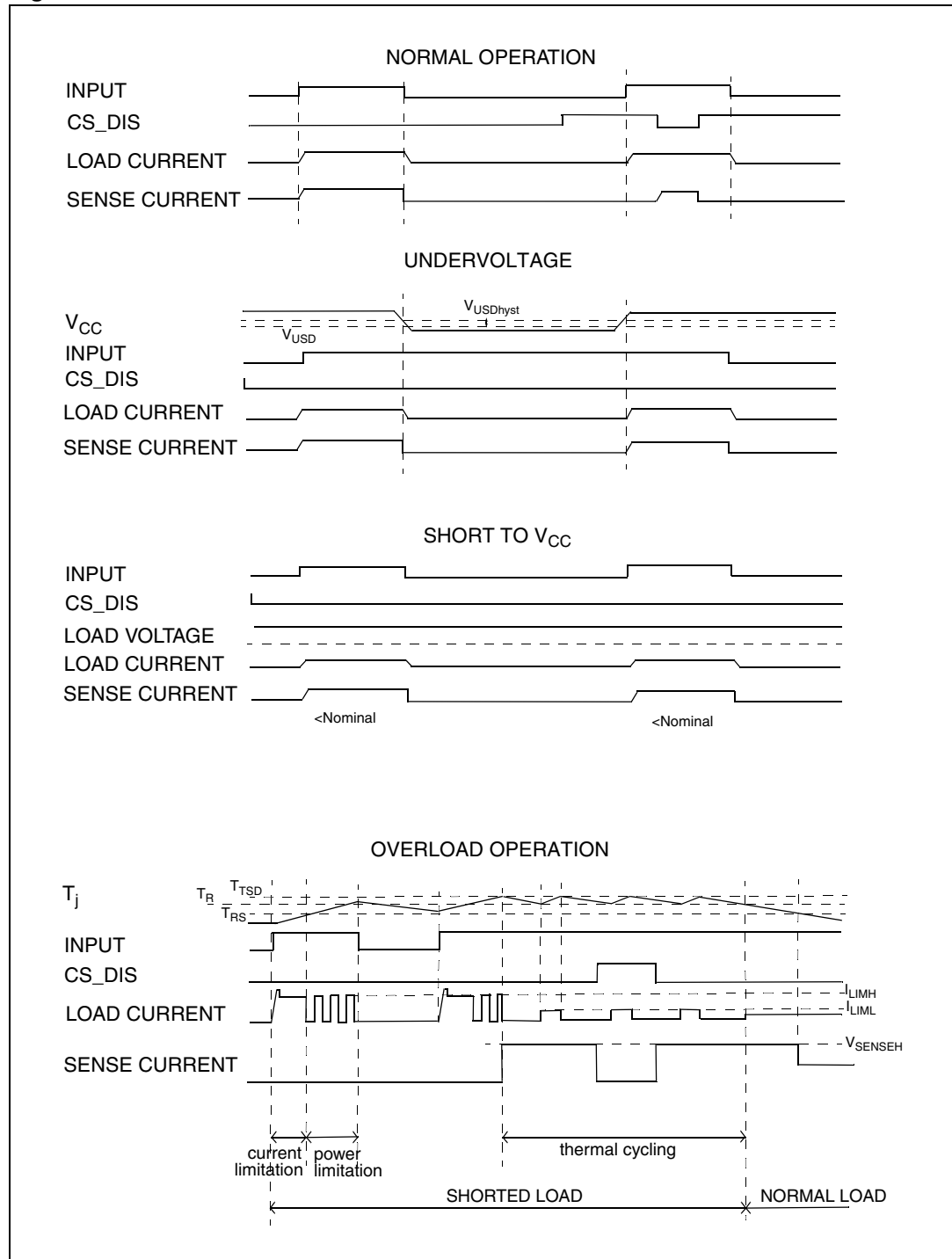
ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65V	+87V	1 pulse			400 ms, 2 Ω

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5V$ except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 10. Waveforms



2.4 Electrical characteristics curves

Figure 11. Off state output current

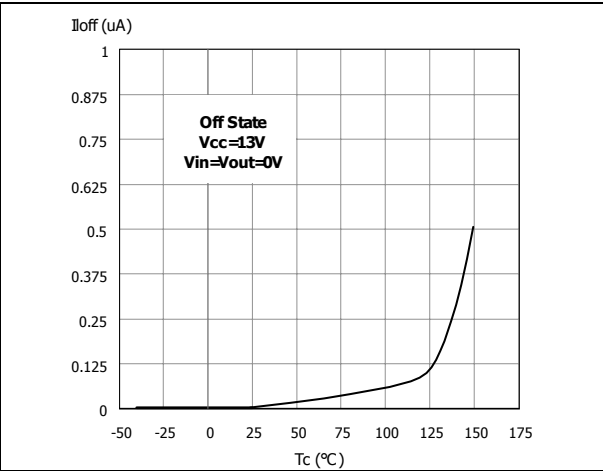


Figure 12. High level input current

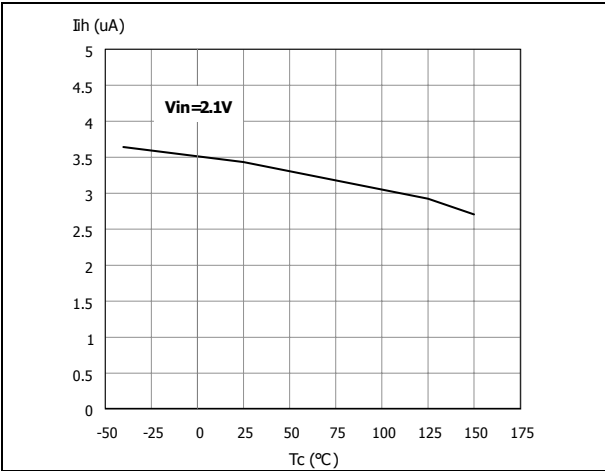


Figure 13. Input clamp voltage

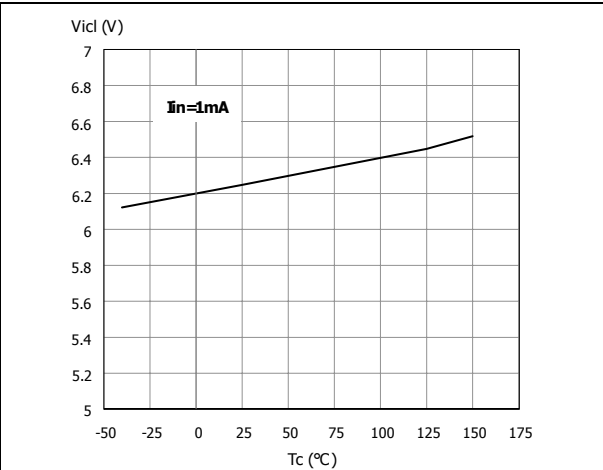


Figure 14. Input high level

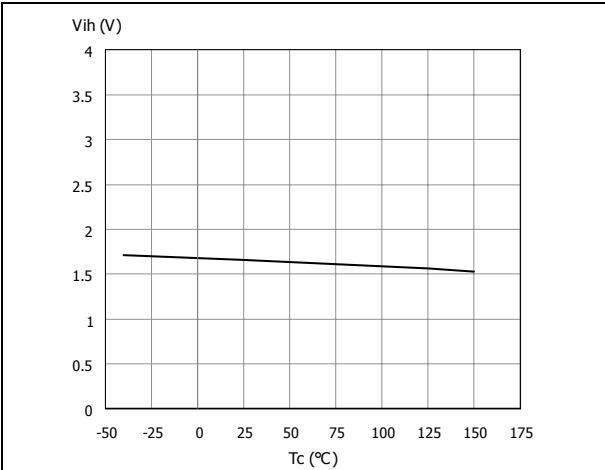


Figure 15. Input low level

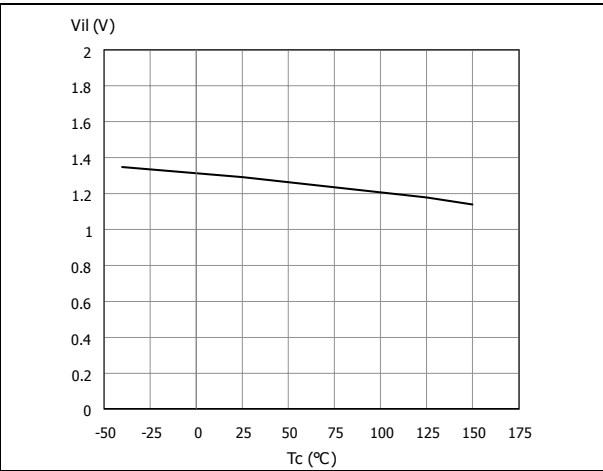


Figure 16. Input hysteresis voltage

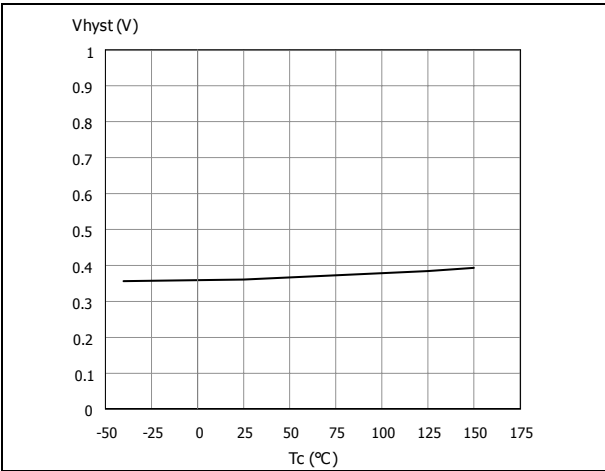


Figure 17. On state resistance Vs. T_{case}

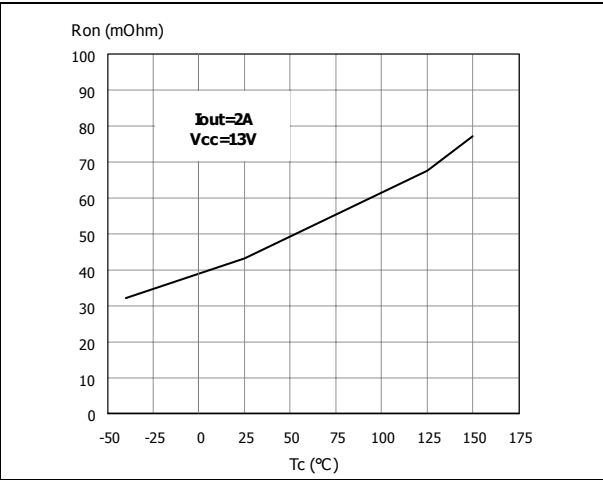


Figure 18. On state resistance Vs. V_{CC}

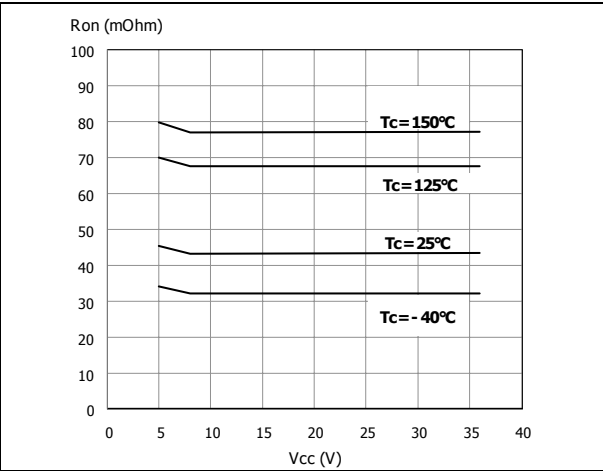


Figure 19. Undervoltage shutdown

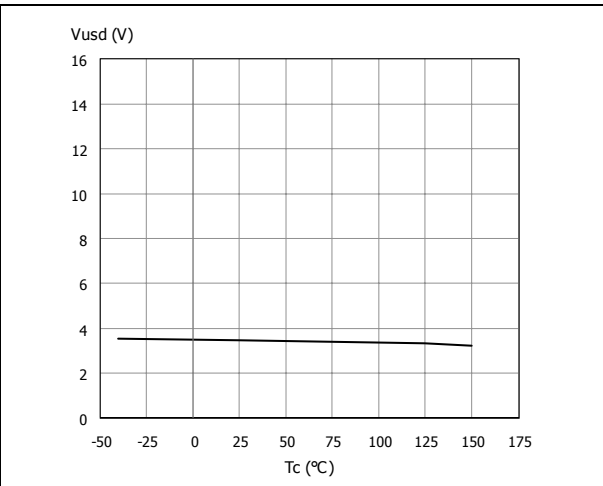


Figure 20. I_{LIMH} Vs. T_{case}

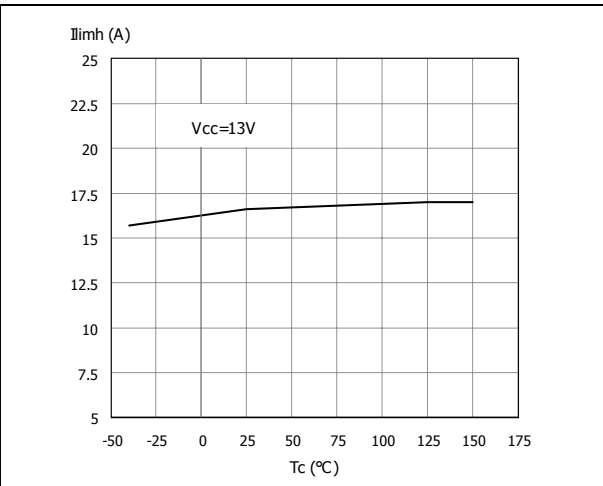


Figure 21. Turn-On voltage slope

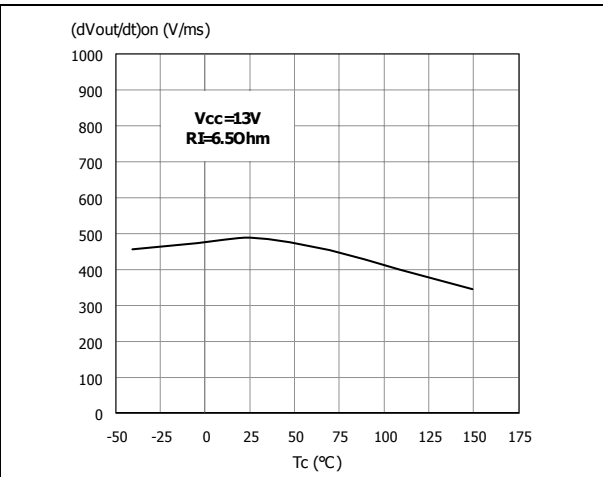


Figure 22. Turn-Off voltage slope

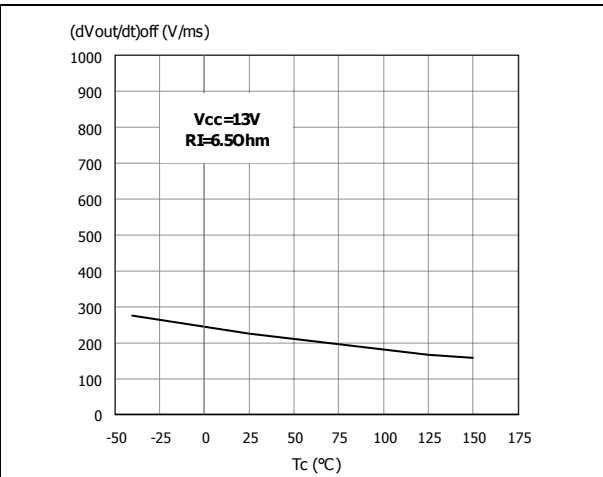


Figure 23. STAT_DIS clamp voltage

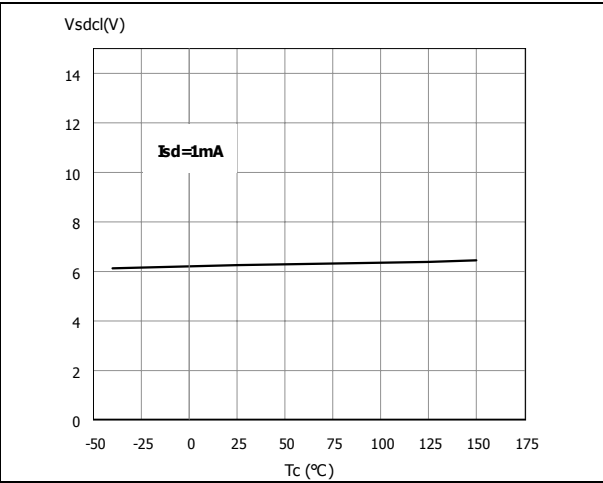


Figure 24. Low level STAT_DIS voltage

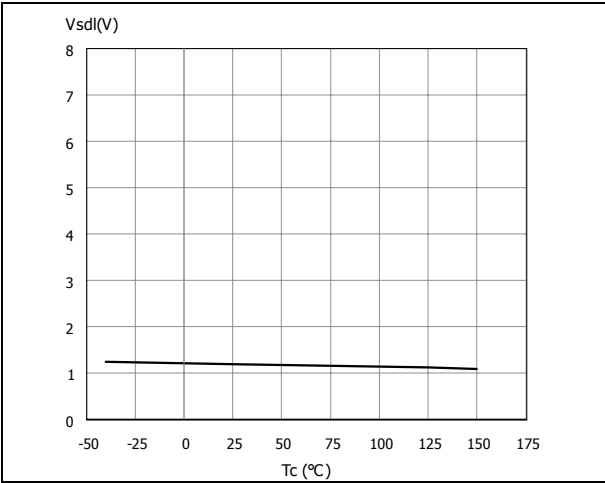
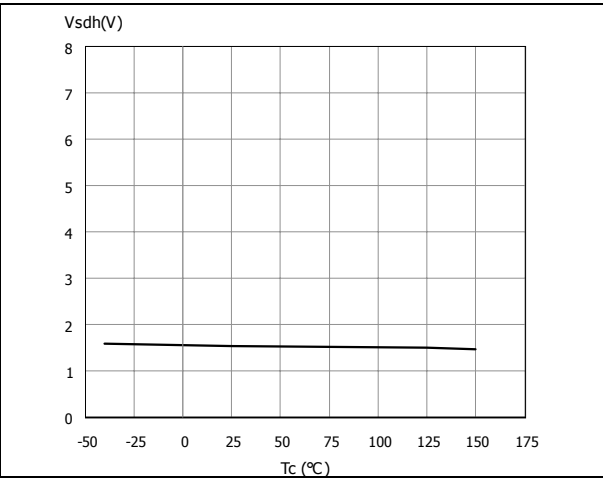
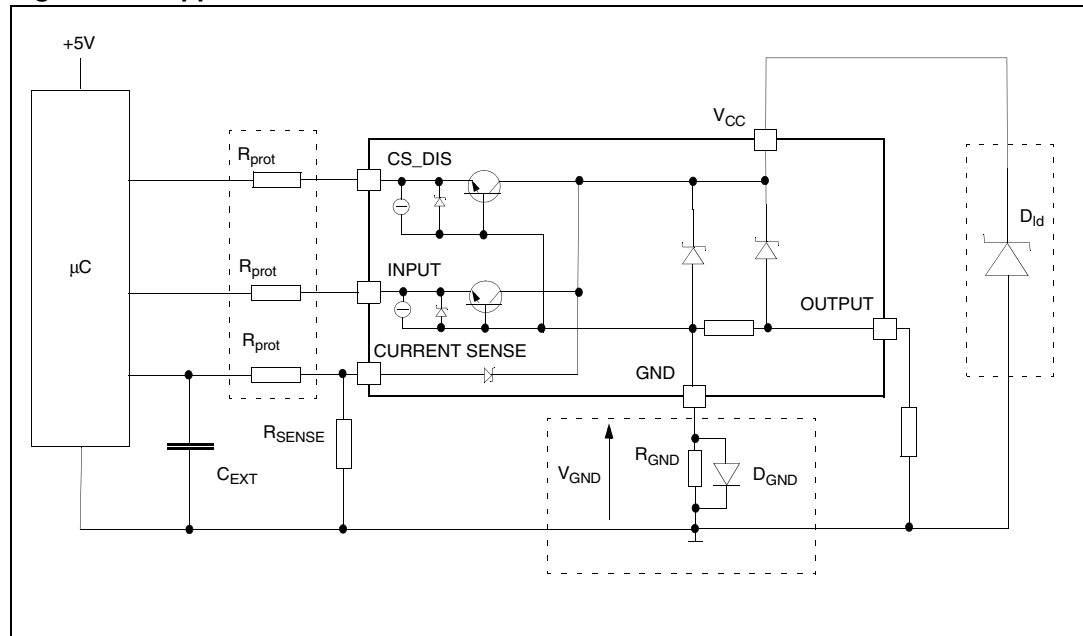


Figure 25. High level STAT_DIS voltage



3 Application information

Figure 26. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

3.1.1 Solution 1 : resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2 : diode (D_{GND}) in the ground line

A resistor ($R_{GND}=1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

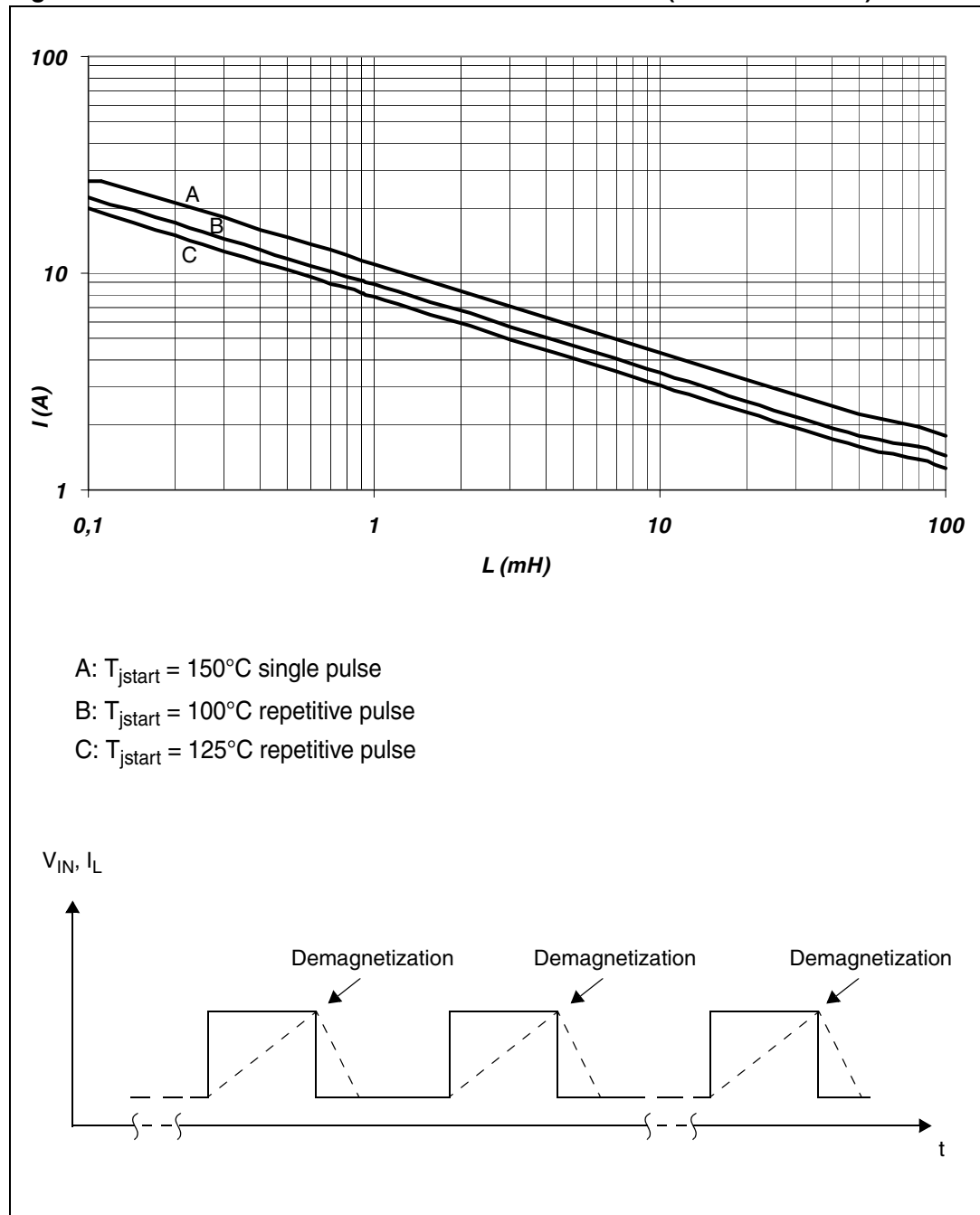
For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$, $C_{EXT} = 10nF$.

3.4 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 27. Maximum turn Off current versus inductance (for each channel)

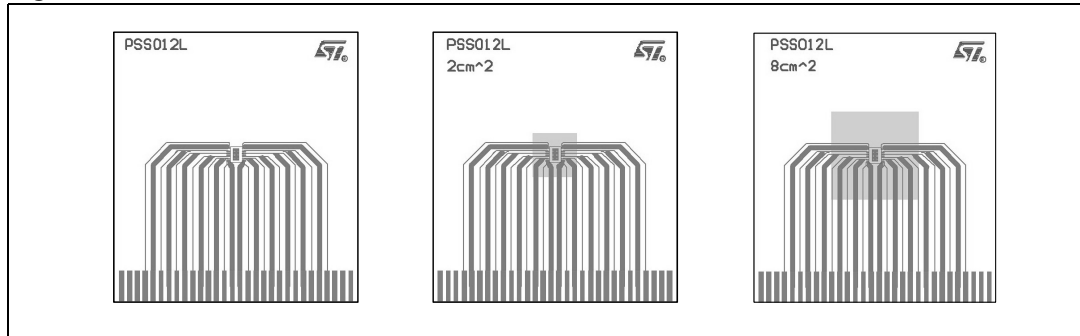


Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-12™ thermal data

Figure 28. PowerSSO-12™ PC board



Note:

Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70μm (front and back side), Copper areas: from minimum pad lay-out to 8cm²).

Figure 29. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON)

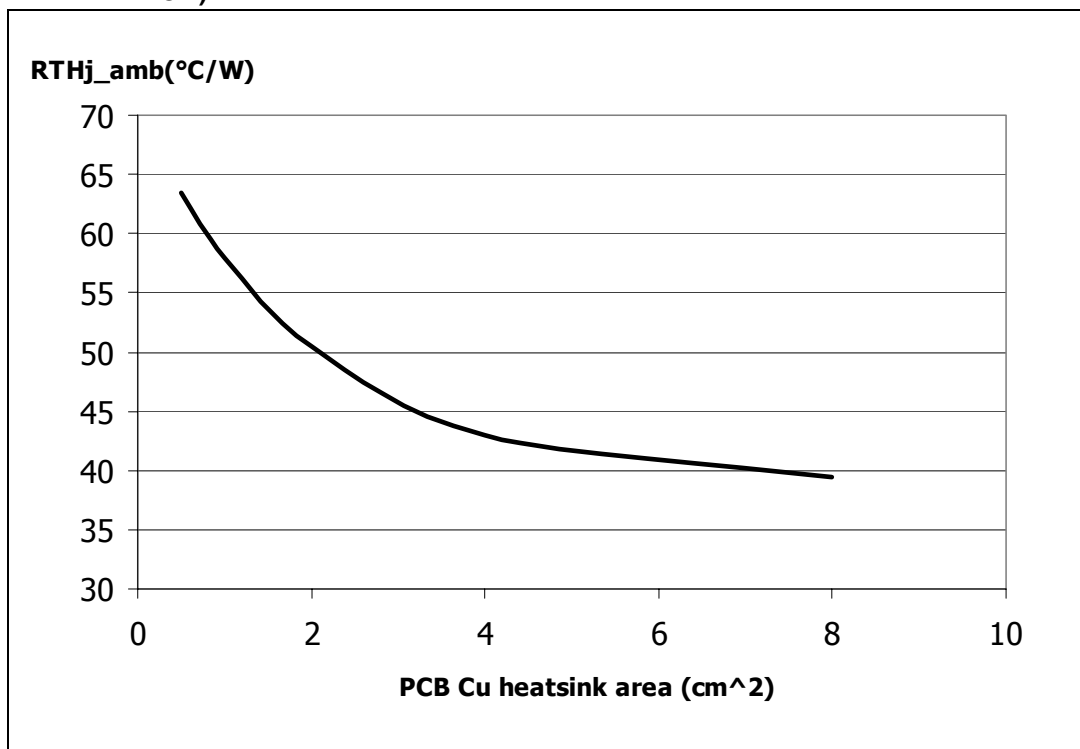
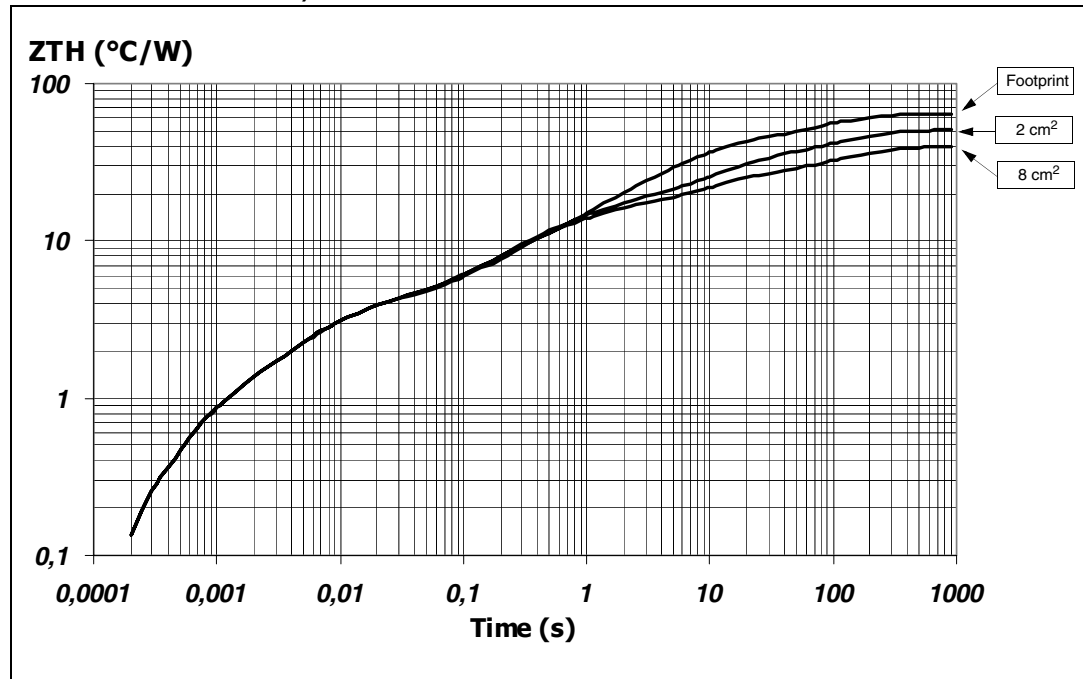


Figure 30. PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON)

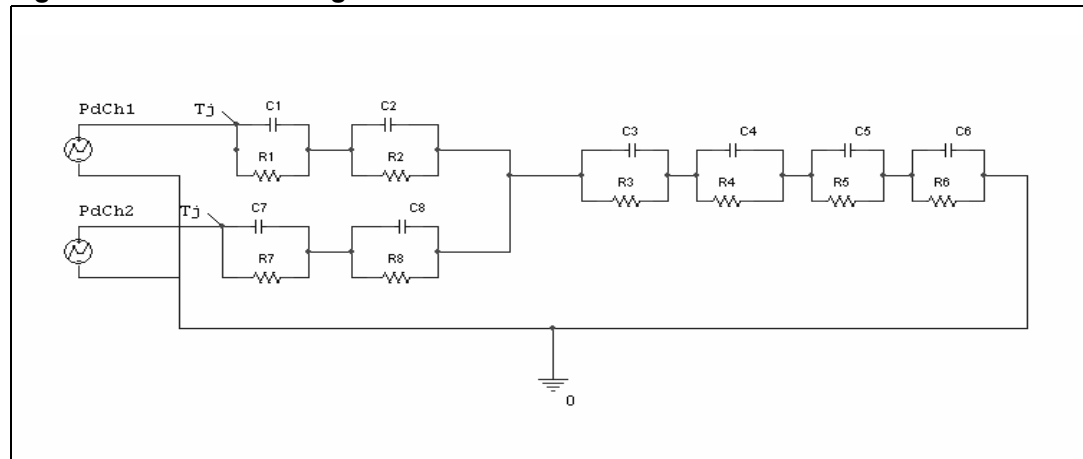


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-12™ (a)



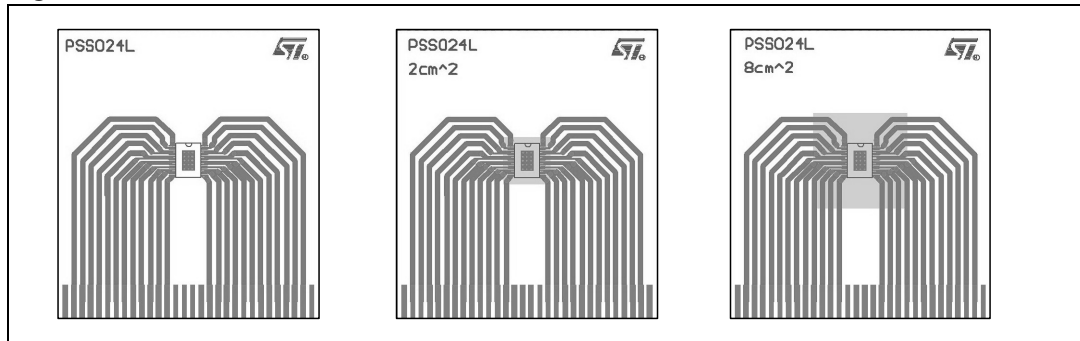
- a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 12. PowerSSO-12™ thermal parameter

Area/island (cm ²)	Footprint	2	8
R1= R7 (°C/W)	0.7		
R2= R8 (°C/W)	2.8		
R3 (°C/W)	4		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1= C7 (W.s/°C)	0.001		
C2= C8 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 PowerSSO-24™ thermal data

Figure 32. PowerSSO-24™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 μ m (front and back side), Copper areas: from minimum pad lay-out to 8cm²).

Figure 33. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON)

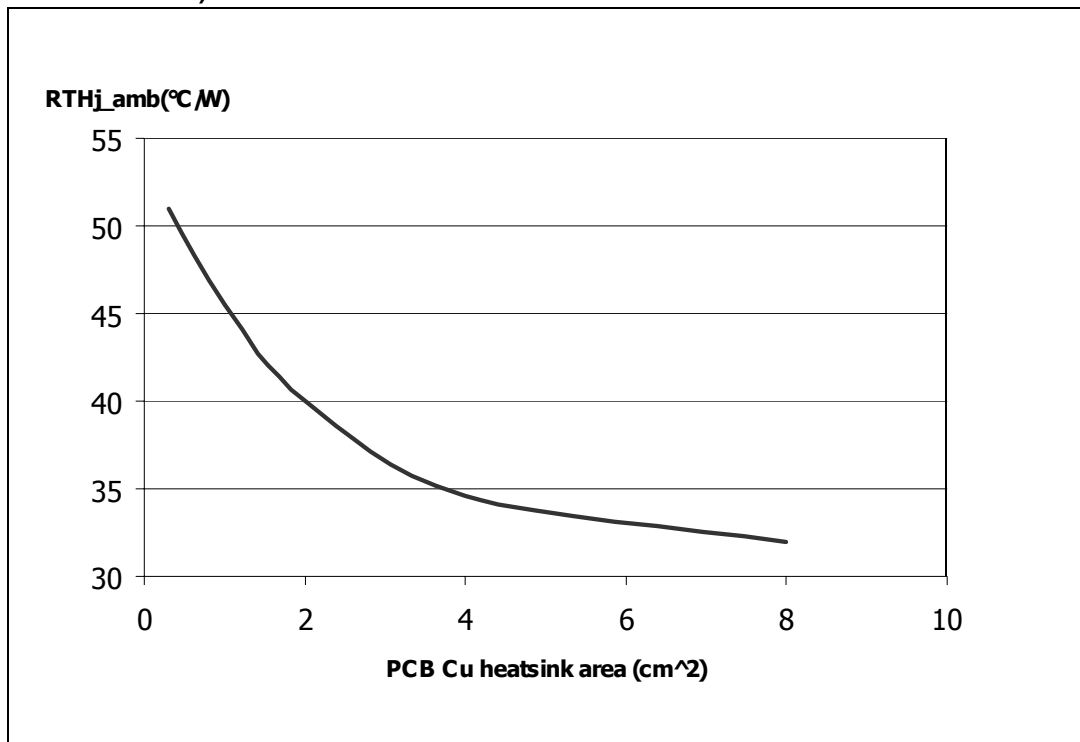
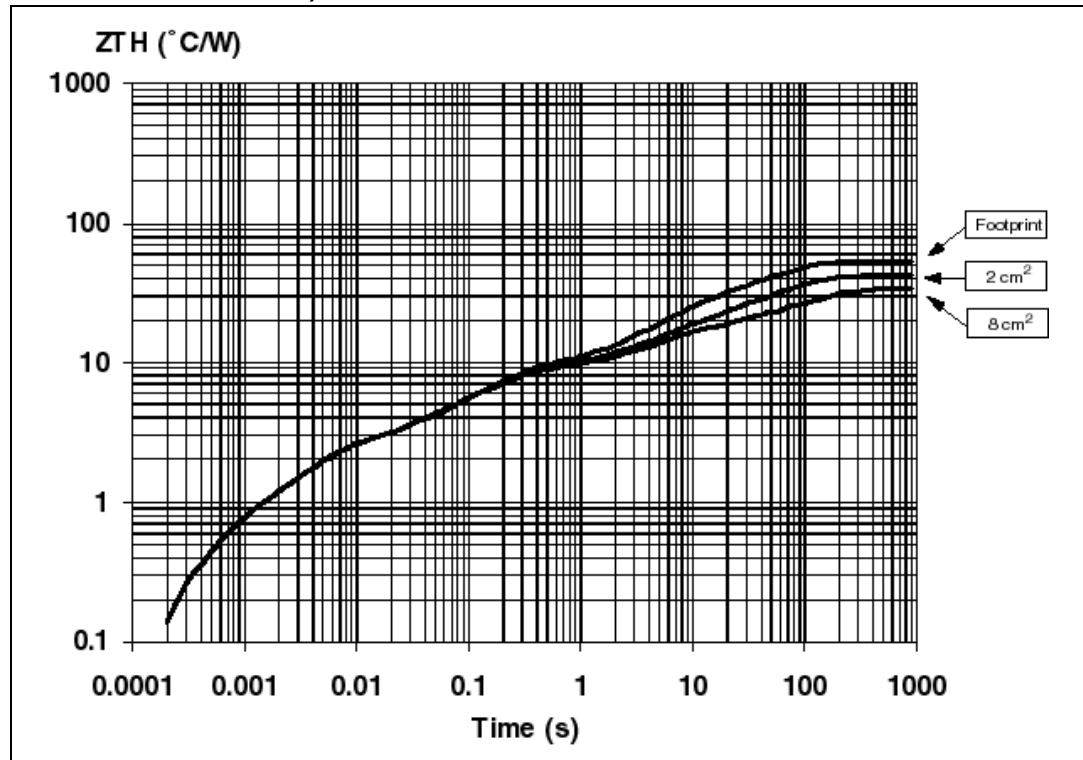


Figure 34. PowerSSO-24™ Thermal impedance junction ambient single pulse (one channel ON)

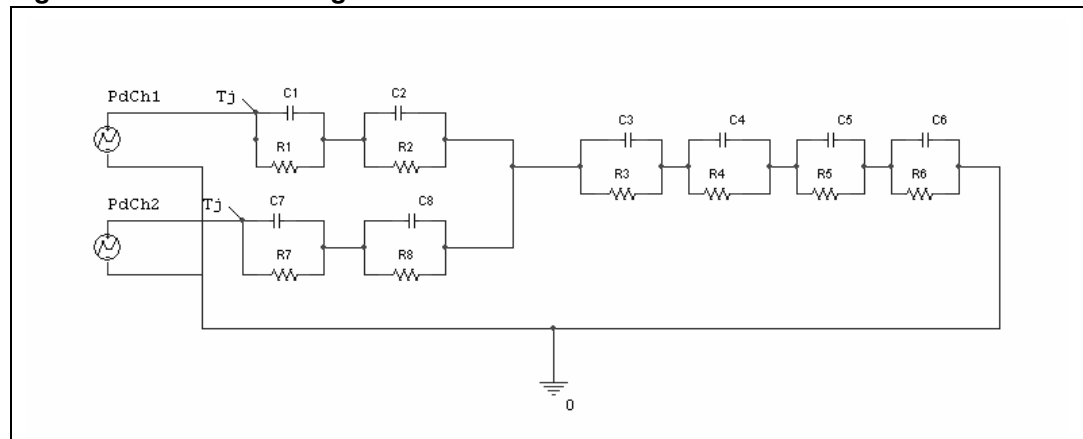


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 35. Thermal fitting model of a double channel HSD in PowerSSO-24™(b)



- b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 13. PowerSSO-24™ thermal parameter

Area/island (cm ²)	Footprint	2	8
R1=R7 (°C/W)	0.4		
R2=R8 (°C/W)	2		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1=C7 (W.s/°C)	0.001		
C2=C8 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.2 PowerSSO-12™ package information

Figure 36. PowerSSO-12™ package dimensions

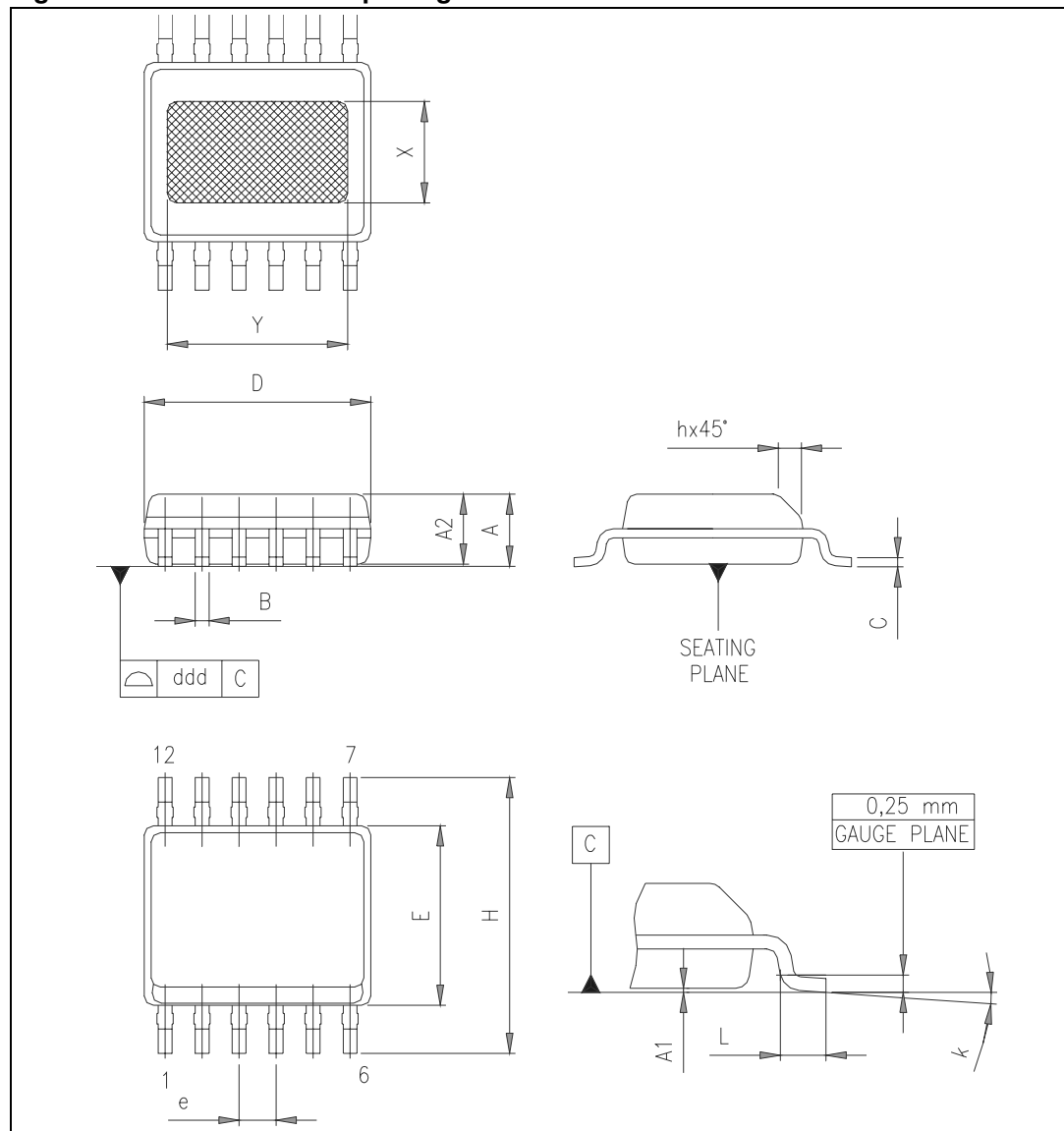


Table 14. PowerSSO-12™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.62
A1	0		0.1
A2	1.10		1.65
B	0.23		0.41
C	0.19		0.25
D	4.8		5.0
E	3.8		4.0
e		0.8	
H	5.8		6.2
h	0.25		0.5
L	0.4		1.27
k	0°		8°
X	1.9		2.5
Y	3.6		4.2
ddd			0.1

5.3 PowerSSO-24™ package information

Figure 37. PowerSSO-24™ package dimensions

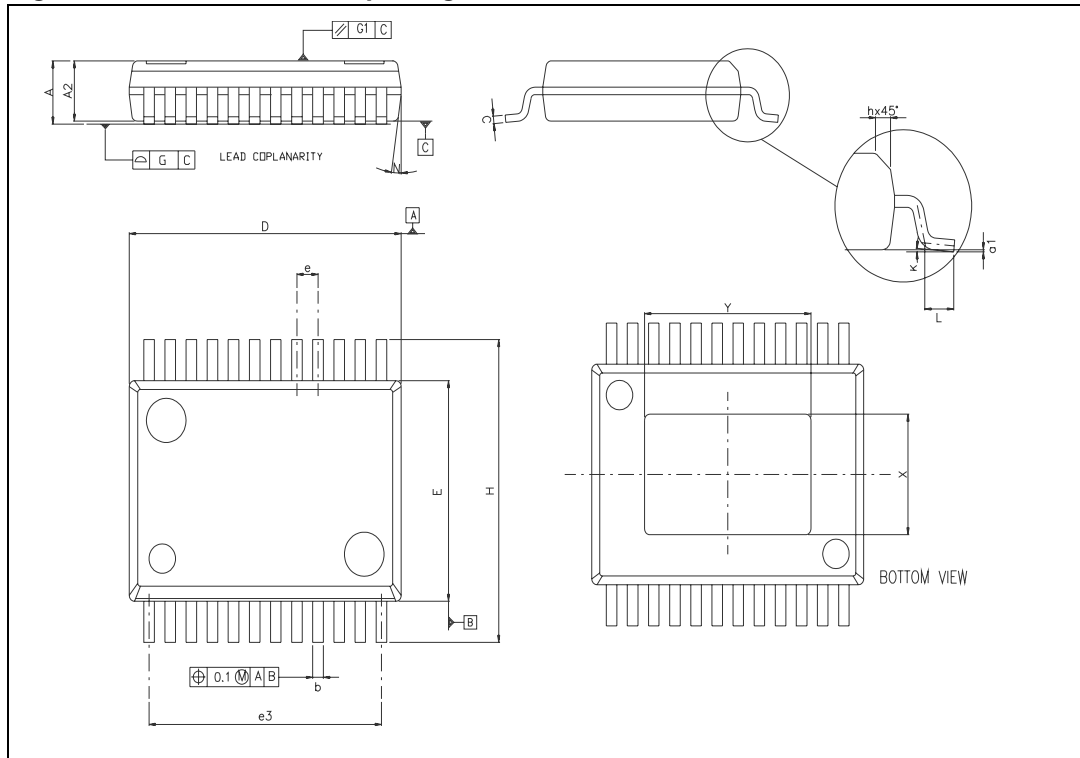


Table 15. PowerSSO-24™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06

Table 15. PowerSSO-24™ mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

5.4 PowerSSO-12™ packing information

Figure 38. PowerSSO-12™ tube shipment (no suffix)

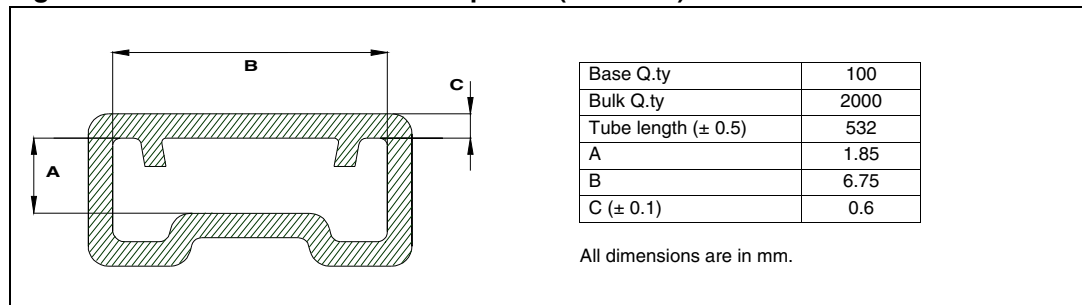
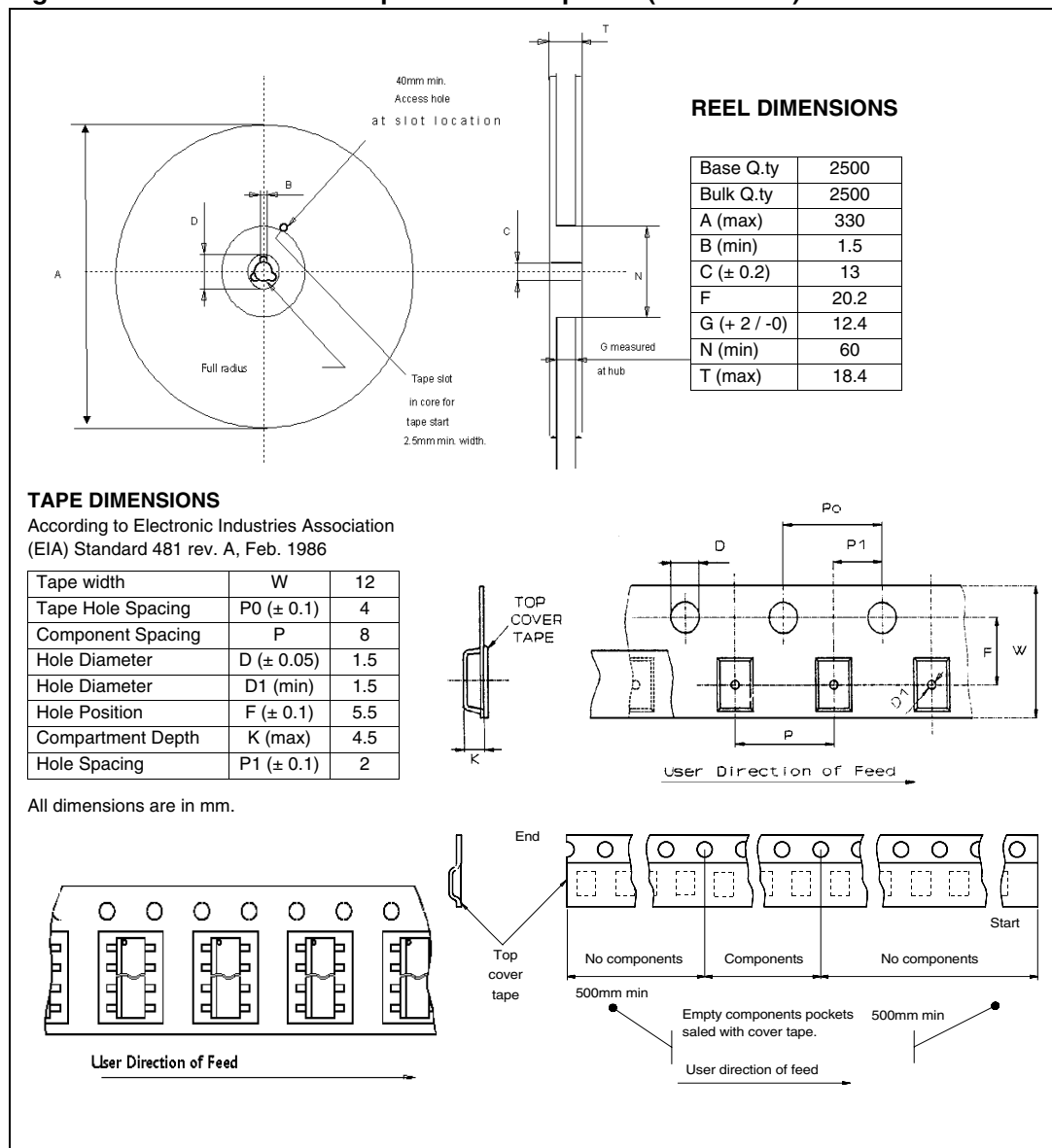


Figure 39. PowerSSO-12™ tape and reel shipment (suffix “TR”)



5.5 PowerSSO-24™ packing information

Figure 40. PowerSSO-24™ tube shipment (no suffix)

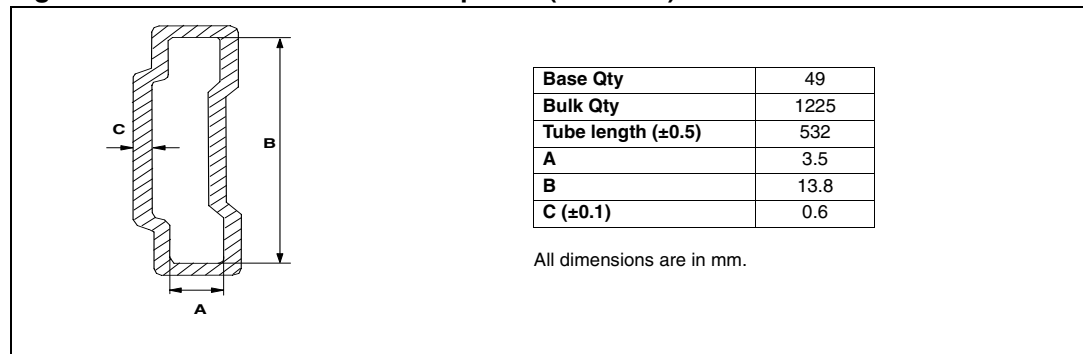
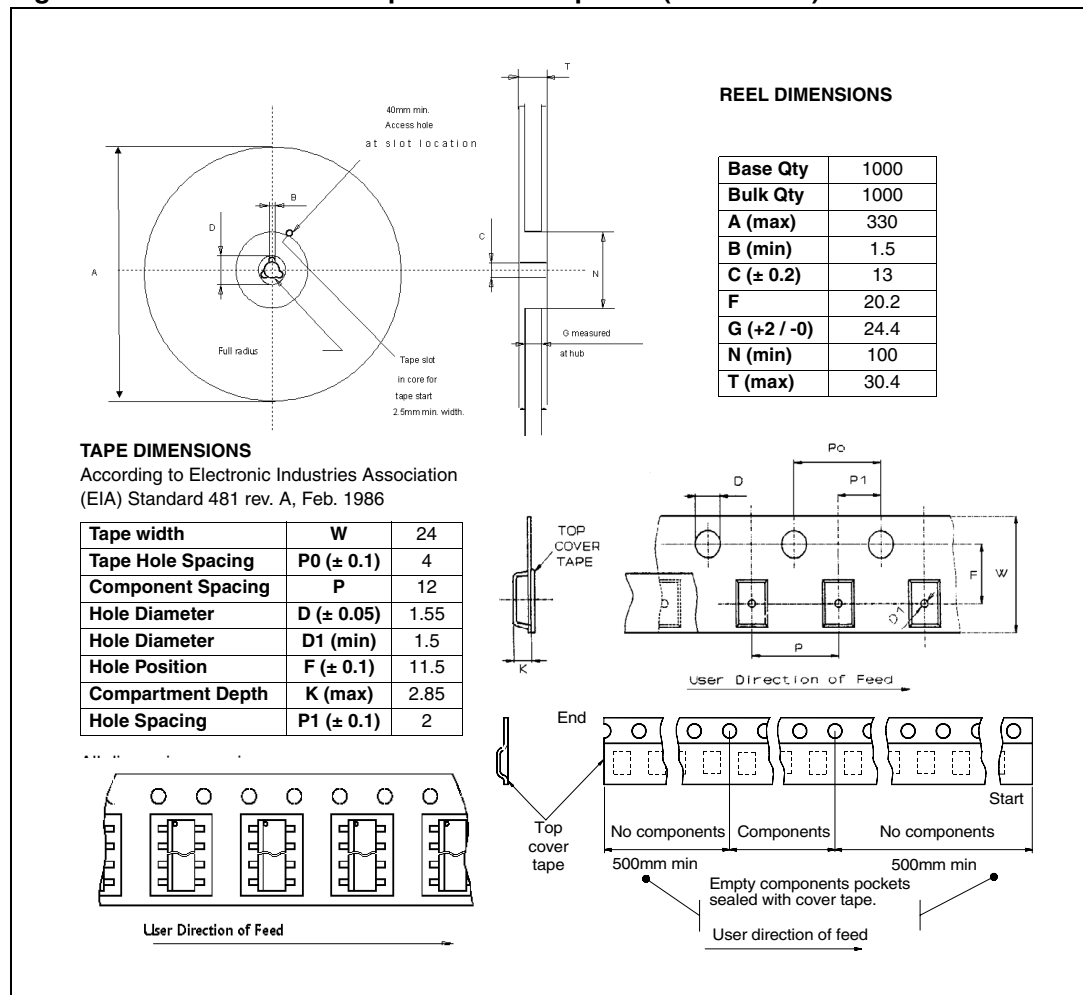


Figure 41. PowerSSO-24™ tape and reel shipment (suffix “TR”)



6 Order codes

Table 16. Device summary

Package	Order codes	
	Part number (Tube)	Part number (Tape & Reel)
PowerSSO-12	VND5050AJ-E	VND5050AJTR-E
PowerSSO-24	VND5050AK-E	VND5050AKTR-E

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
30-Mar-2006	1	Initial release.
14-Apr-2006	2	PowerSSO-24 dimensions table update.
26-Apr-2007	3	Reformatted <i>Figure 31</i> title corrected
14-May-2007	4	<i>Table 3</i> : corrected E_{MAX} value. <i>Table 9</i> : added $dk1/k1$, $dk2/k2$, $dk3/k3$, $\Delta t_{DSENSE2H}$. Added <i>Figure 5</i> . Updated <i>Figure 6</i> . Added <i>Figure 7</i> . <i>Table 11</i> : Updated test level values III and IV for test pulse 5b and notes. Added <i>Section 3.4: Maximum demagnetization energy ($V_{CC} = 13.5V$)</i> .
01-Jun-2007	5	<i>Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-12™</i> , <i>Figure 35: Thermal fitting model of a double channel HSD in PowerSSO-24™</i> : added notes.
4-Dec-2007	6	Updated <i>Table 9: Current sense ($8V < V_{CC} < 16V$)</i> : – changed $t_{DSENSE2H}$ max value from 300 μs to 250 μs . – added I_{OL} parameter. Updated <i>Section 4.1: PowerSSO-12™ thermal data</i> : – changed <i>Figure 29: $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON)</i> . – changed <i>Figure 30: PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON)</i> . – updated <i>Table 12: PowerSSO-12™ thermal parameter</i> . R3 value changed from 7 to 4 °C/W. R4 values changed from 10 /10 /10 to 8 /8 /7 °C/W.
12-Feb-2008	7	Corrected typing error in <i>Table 9: Current sense ($8V < V_{CC} < 16V$)</i> : changed I_{OL} test condition from $V_{IN} = 0V$ to $V_{IN} = 5V$.

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