VN7004AH-E

High-side driver with CurrentSense analog feedback for automotive applications

Datasheet - production data



Octapak

Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	4.9 mΩ
Current limitation (typ)	I_{LIMH}	150 A
Stand-by current (max)	I_{STBY}	0.5 µA

- Automotive qualified
- General
  - Single channel smart high-side driver with CurrentSense analog feedback
  - Very low standby current
  - Compatible with 3.0 V and 5 V CMOS outputs
- Diagnostic functions
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/ disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Loss of ground and loss of V_{CC}
  - Reverse battery
  - Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Headlamps

Description

The VN7004AH-E is a single channel high-side driver manufactured using ST proprietary VIPower® technology and housed in the Octapak package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
Octapak	VN7004AH-E	VN7004AHTR-E

This is information on a product in full production. www.st.com

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1 Block diagram and pin description

Figure 1. Block diagram

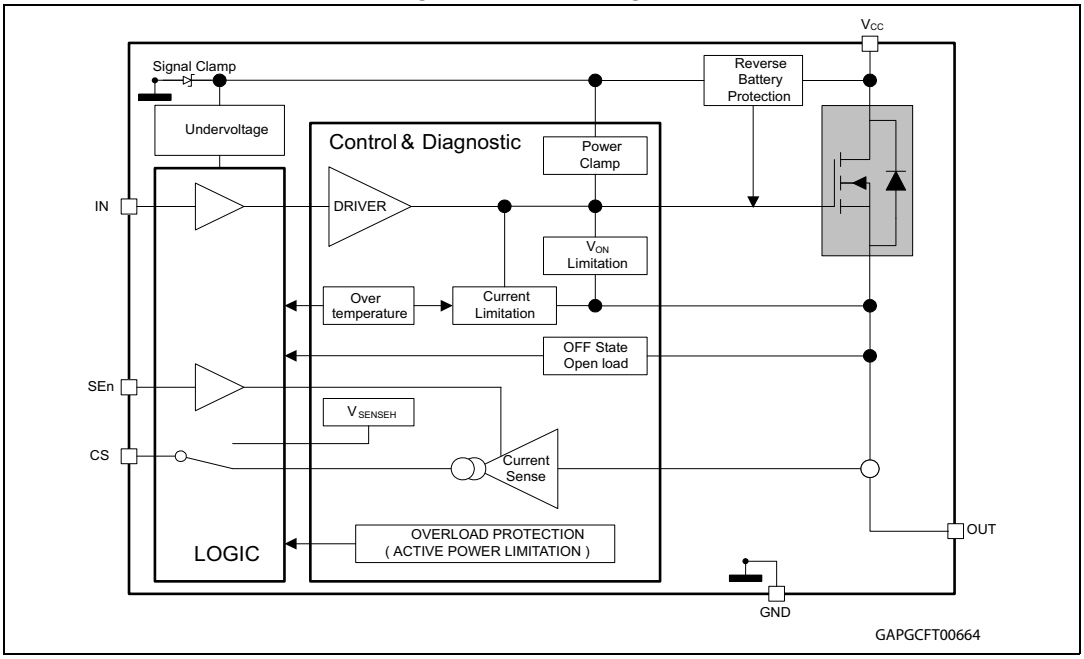


Table 2. Pin functions

Name	Function
V_{CC}	Battery connection.
OUTPUT	Power outputs. All the pins must be connected together.
GND	Ground connection.
INPUT	Voltage controlled input pin with hysteresis. Compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
CS	Analog current sense output pin delivers a current proportional to the load current.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the CurrentSense diagnostic pin.

Figure 2. Configuration diagram (top view)

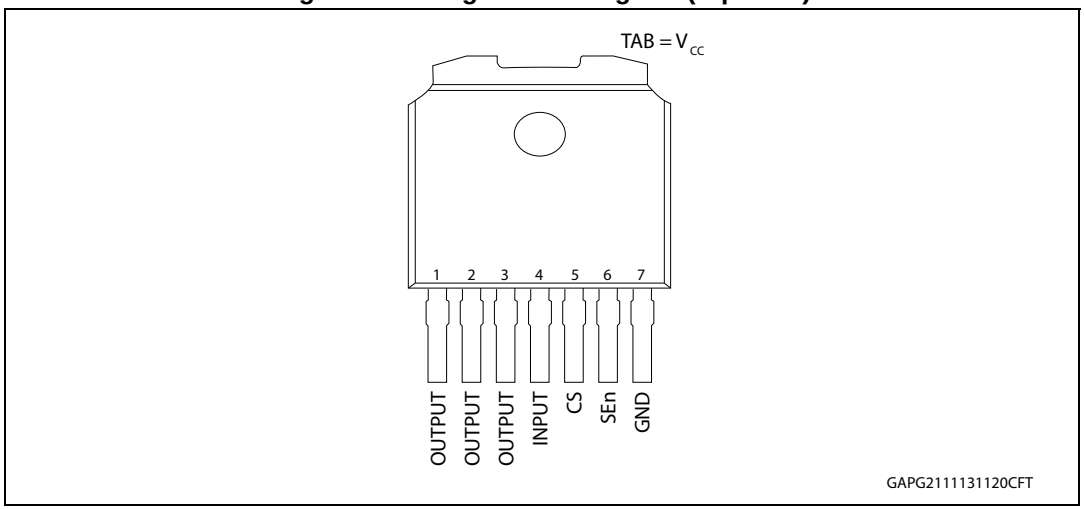


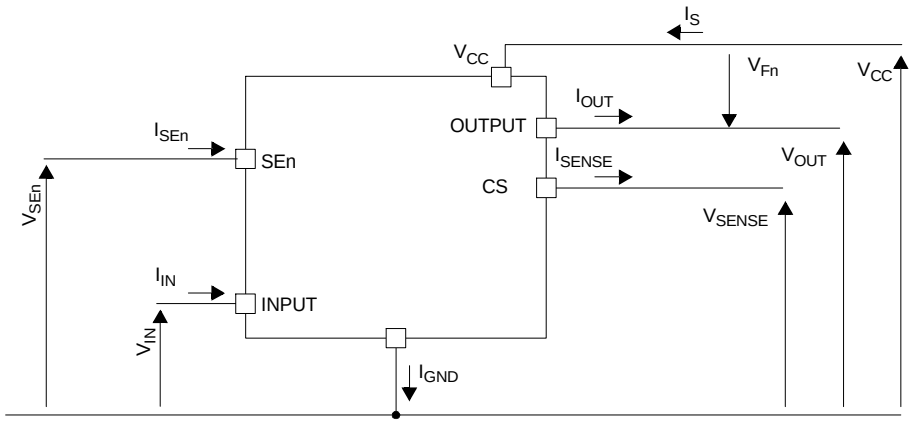
Table 3. Suggested connections for unused and not connected pins

Connection / pin	CurrentSense	N.C.	Output	Input	SEn
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: $V_F = V_{OUT} - V_{CC}$ when $V_{OUT} > V_{CC}$ and INPUt = LOW

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
V_{CC_LSC}	Maximum supply voltage for single pulse short circuit protection (L ≤ 5 µH; R_L ≥ 100 mΩ)	18	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; R_L = 4Ω)	40	
$-V_{CC}$	Reverse DC supply voltage	16	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	65	
I_{IN}	INPUT DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SENSE}	CS pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	CS pin DC output current in reverse (V_{CC} < 0 V)	-20	

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) T_{DEMAG} = 0.4 ms; I_{OUT} = 19 A; T_{jstart} = 150°C	165	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) – INPUT – CurrentSense – SEn – OUTPUT – V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (1)	2.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5) (2)	57.9	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7) (1)	15.4	

1. Device mounted on four-layers 2s2p PCB
2. Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace

2.3 Electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
R_{ON}	On-state resistance	I_{OUT} = 15 A; T_j = 25°C		4.9		mΩ
		I_{OUT} = 15 A; T_j = 150°C			9	
		I_{OUT} = 15 A; V_{CC} = 4 V; T_j = 25°C			6	
R_{ON_Rev}	R_{DSON} in reverse battery condition	V_{CC} = -13 V; I_{OUT} = -15 A; T_j = 25°C		4.9		mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA; T_j = -40°C	38			V
		I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	
I_{STBY}	Supply current in standby at V_{CC} = 13 V (1)	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} = 0 V; T_j = 85°C (2)			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{SEn} = 0 V; T_j = 125°C			3	µA
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{IN} = 5 V; V_{SEn} = 0 V; I_{OUT} = 0 A	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = 0 V; V_{IN} = 5 V; I_{OUT} = 0 A		4	6.5	mA
$I_{GND(ON)}$	Control stage current consumption in ON-state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{IN} = 5 V; I_{OUT} = 15 A			9	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage	I_{OUT} = -15 A; T_j = 150°C			0.7	V

1. PowerMOS leakage included.
2. Parameter specified by design; not subject to production test.

Table 7. Switching (V_{CC} = 13 V; -40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ (1)	Turn-on delay time at T_j = 25 °C	R_L = 0.87 Ω	10	70	120	µs
$t_{d(off)}$ (1)	Turn-off delay time at T_j = 25 °C		10	44	100	
$(dV_{OUT}/dt)_{on}$ (1)	Turn-on voltage slope at T_j = 25 °C	R_L = 0.87 Ω	0.1	0.47	0.8	V/µs
$(dV_{OUT}/dt)_{off}$ (1)	Turn-off voltage slope at T_j = 25 °C		0.1	0.49	0.8	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 0.87 Ω	—	1.6	2.7 (2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 0.87 Ω	—	1.7	2.7 (2)	mJ
t_{SKEW} (1)	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 0.87 Ω	-30	20	70	µs

1. See *Figure 6: Switching times and Pulse skew*.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 8. Logic Inputs (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		

Table 9. Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIMH}(1)	DC short circuit current	V_{CC} = 13 V; V_{DS} = 5 V	70	150	230	A
		4 V < V_{CC} < 18 V; V_{DS} = 5 V(2)			230	
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		38		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(2)		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{SEn} = 5 V;	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(2)			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40°C; V_{CC} = 13 V		60		K
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40°C	V_{CC} - 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 2.5 A		20		mV

1. Parameter guaranteed by an indirect test sequence.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 10. CurrentSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	CurrentSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		V
Current Sense characteristics						
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	6640	16300	28000	
dK_1/K_1(1)(2)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-25		25	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	10600	15650	21050	
dK_2/K_2(1)(2)	Current sense ratio drift	I_{OUT} = 15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-11		11	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 45 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	10500	15500	20500	
dK_3/K_3(1)(2)	Current sense ratio drift	I_{OUT} = 45 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-7		7	%

Table 10. CurrentSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	CurrentSense leakage current	CurrentSense disabled: V_{SEn} = 0 V;	0		0.5	µA
		CurrentSense disabled; -1 V < V_{SENSE} < 5 V(1)	-0.5		0.5	µA
		CurrentSense enabled: V_{SEn} = 5 V; V_{IN} = 5 V; I_{OUT} = 0 A;	0		2	µA
V_{OUT_CSD}(1)	Output voltage for CurrentSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ; V_{IN} = 5 V; I_{OUT} = 15 A		5		V
V_{SENSE_SAT}	CurrentSense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 kΩ; V_{SEn} = 5 V; V_{IN} = 5 V; I_{OUT} = 45 A; T_j = 150°C	5			V
I_{SENSE_SAT}(1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; T_j = 150°C	4			mA
I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; T_j = 150°C	80			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{IN} = 0 V; V_{SEn} = 5 V;	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 7*)	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; I_{OUT} = 0 A; V_{OUT} = 4 V	100	350	700	µs
$t_{D_OL_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN} = 0 V; V_{OUT} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{IN} = 0 V; V_{SEn} = 5 V; V_{OUT} = 0 V to 4 V		5	30	µs
Fault diagnostic feedback (see *Table 11*)						
V_{SENSEH}	CurrentSense output voltage in fault condition	V_{CC} = 13 V; V_{IN} = 0 V; V_{SEn} = 5 V; I_{OUT} = 0 A; V_{OUT} = 4 V; R_{SENSE} = 1 kΩ	5		6.6	V

Table 10. CurrentSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSEH}	CurrentSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
CurrentSense timings (current sense mode)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 0.87 kΩ			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 0.87 kΩ		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 0.87 kΩ		100	300	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ I_{SENSE} = 90% of $I_{SENSEMAX}$; R_L = 0.87 kΩ			200	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 0.87 kΩ		50	250	µs

1. Parameter guaranteed by design and characterization; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}

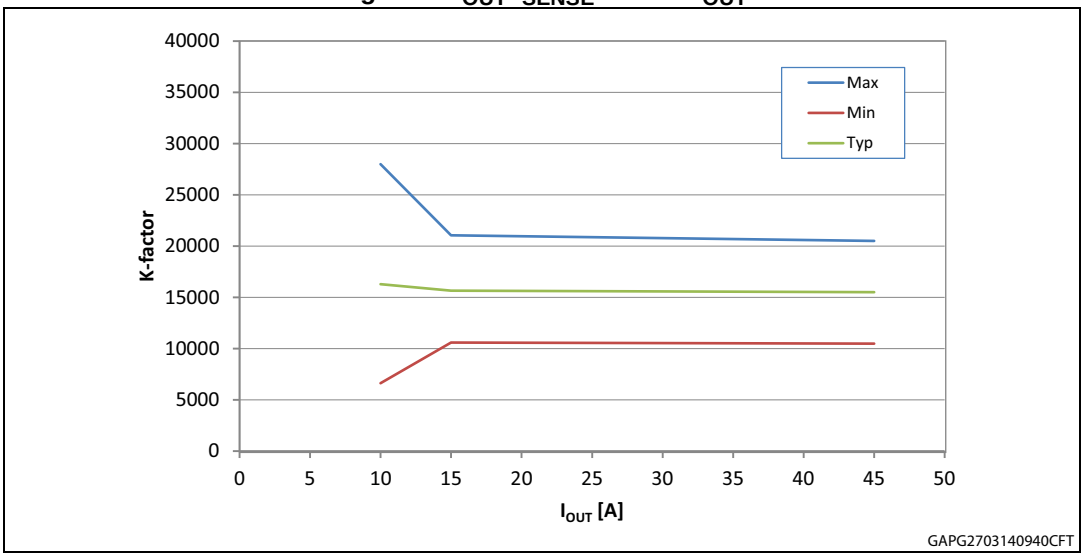


Figure 5. Current sense precision vs. I_{OUT}

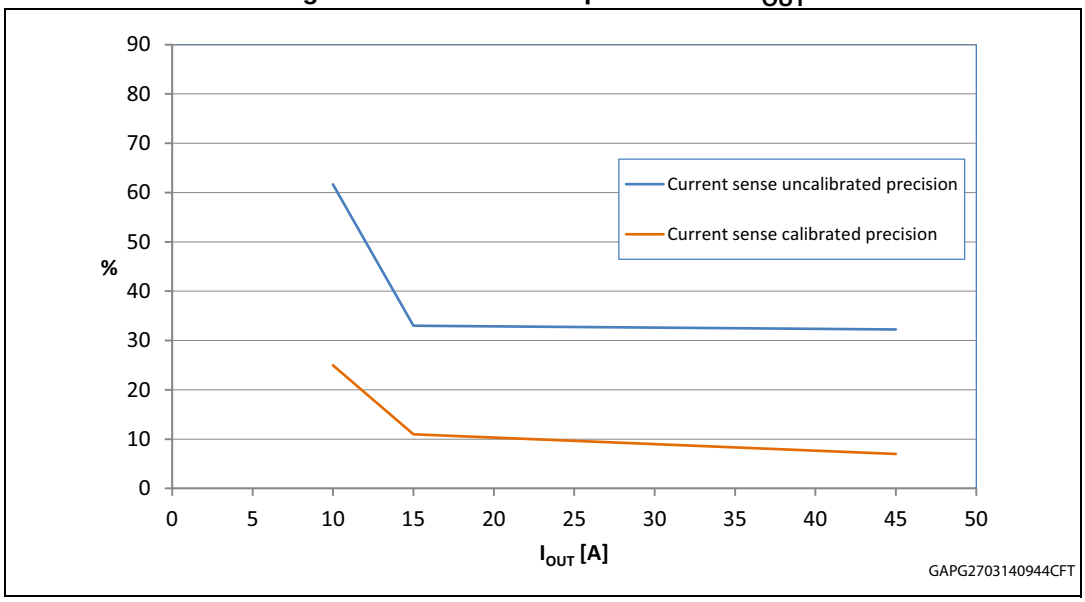


Figure 6. Switching times and Pulse skew

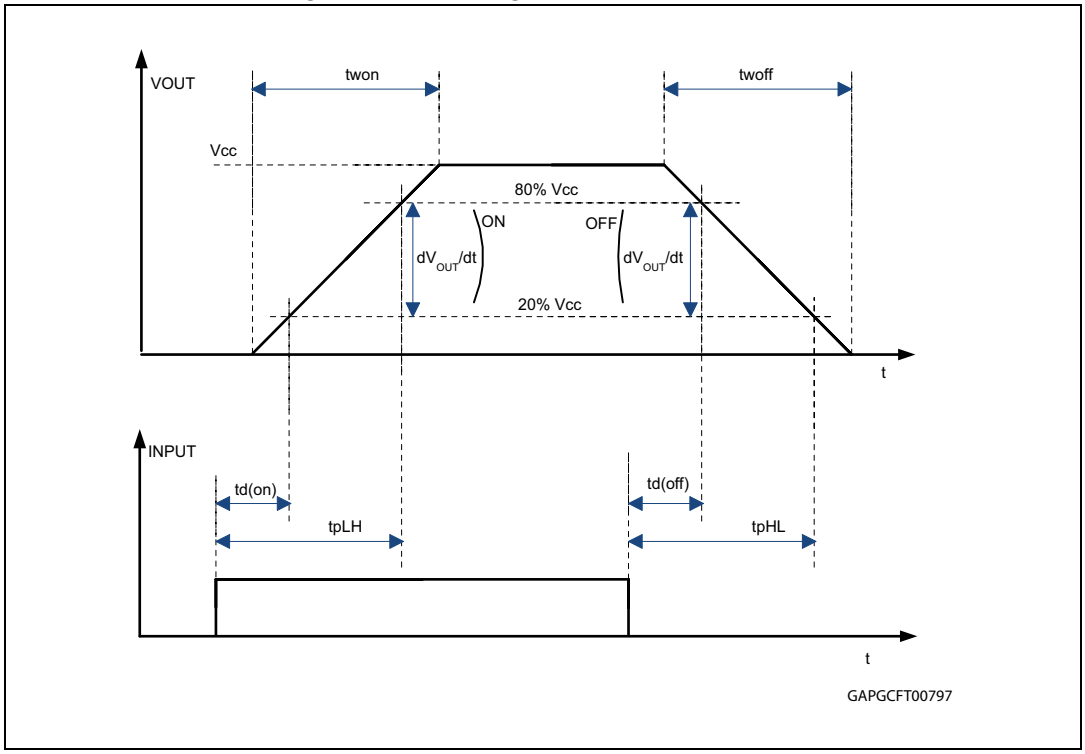


Figure 7. T_{DSTKON}

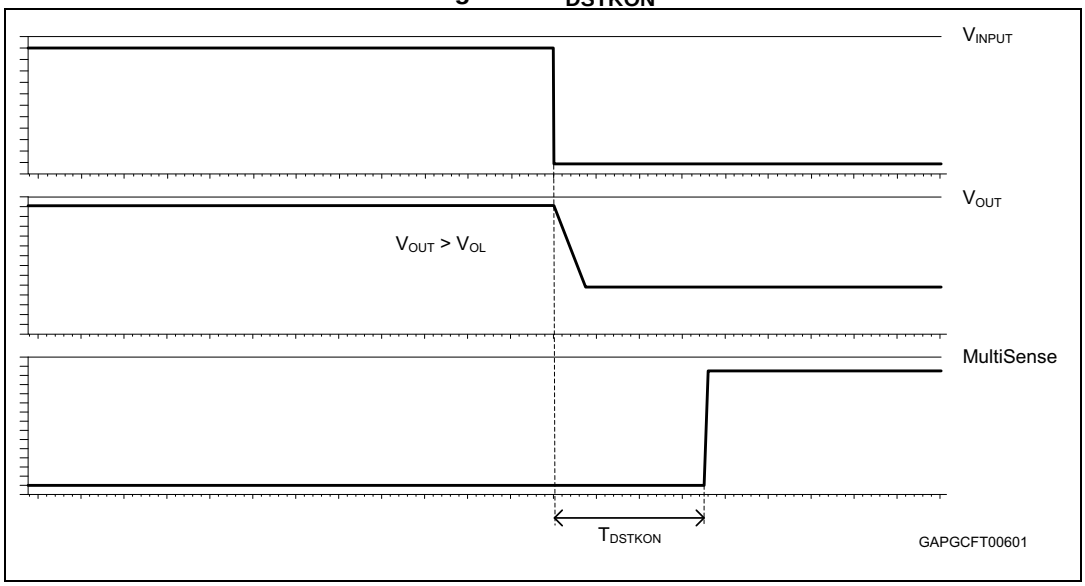
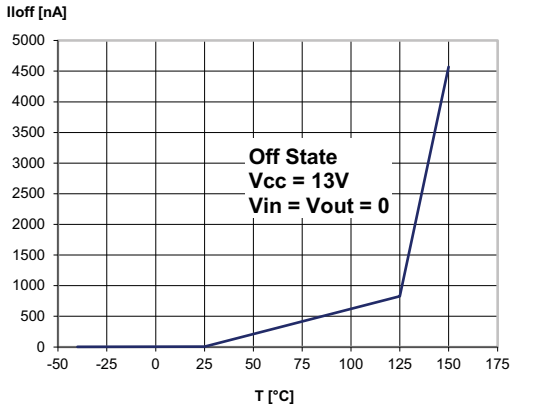


Table 11. Truth table

Mode	Conditions	IN_X	SEn	OUT_X	Current Sense	Comments
Stand by	All logic inputs low	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150°C	L	H	L	0	
		H	L	H	Hi-Z	
		H	H	H	I_{SENSE} = 1/K * I_{OUT}	
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$	H	L	H	Hi-Z	Output cycles with temperature hysteresis
		H	H	H	V_{SENSEH}	
Under-voltage	$V_{CC} < V_{USD}$ (falling)	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	H	H	V_{SENSEH}	
	Open-load	L	H	H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	< 0 V	0	

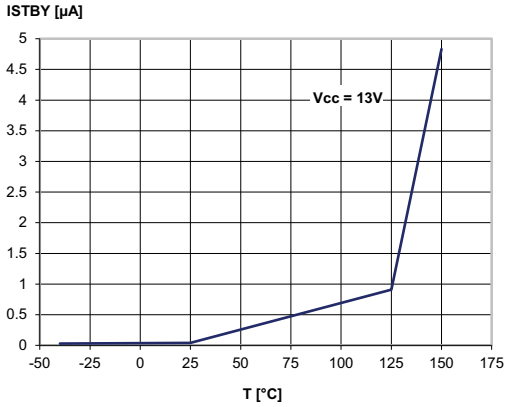
2.4 Electrical characteristics curves

Figure 8. OFF-state output current



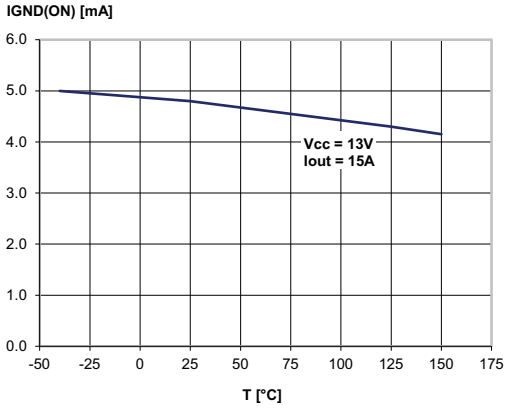
GAPG0603141513CFT

Figure 9. Standby current



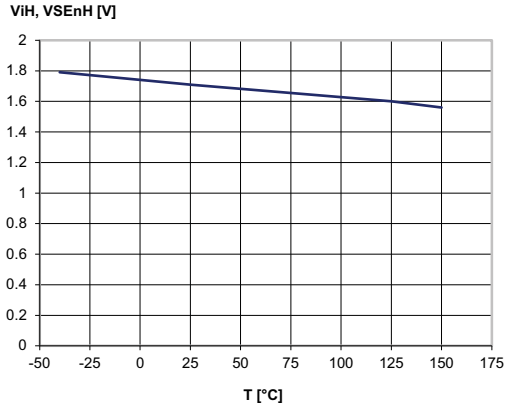
GAPG0603141519CFT

Figure 10. $I_{GND(ON)}$ vs. I_{out}



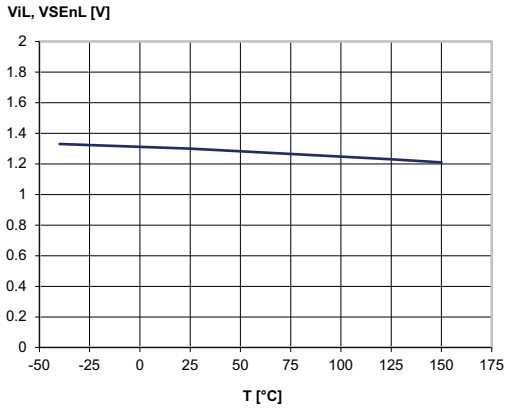
GAPG0603141520CFT

Figure 11. Logic input high level voltage



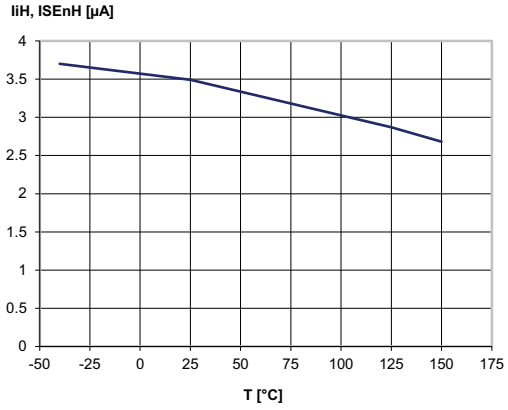
GAPG0603141522CFT

Figure 12. Logic input low level voltage



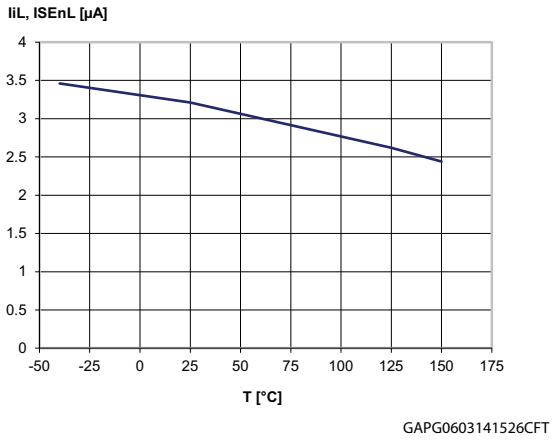
GAPG0603141523CFT

Figure 13. High level logic input current



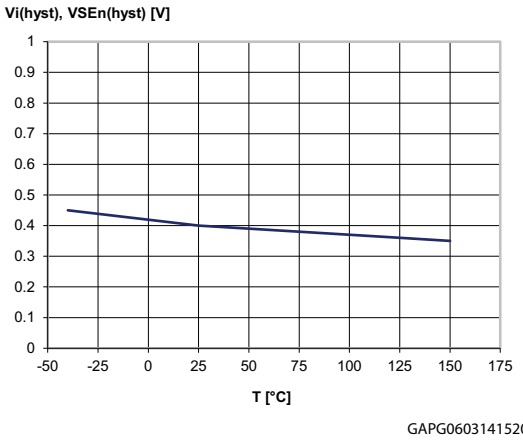
GAPG0603141524CFT

Figure 14. Low level logic input current



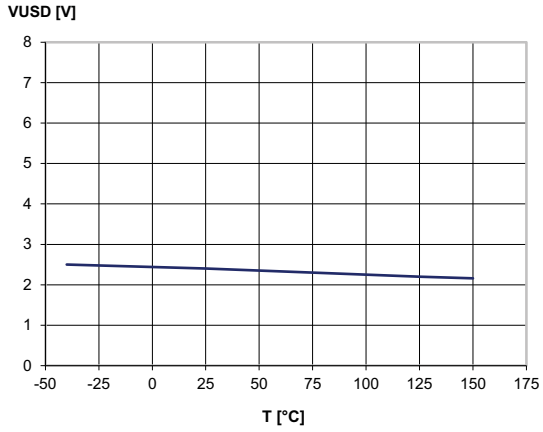
GAPG0603141526CFT

Figure 15. Logic Input hysteresis voltage



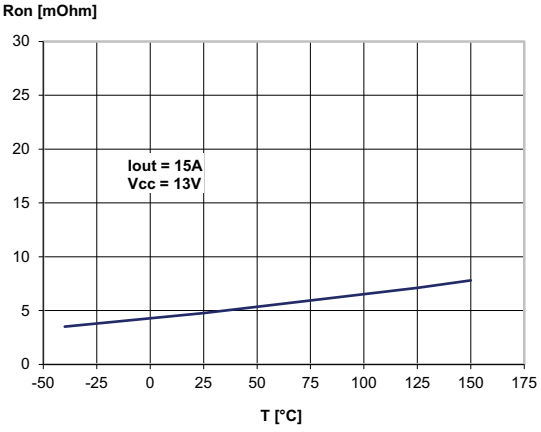
GAPG0603141520CFT

Figure 16. Undervoltage shutdown



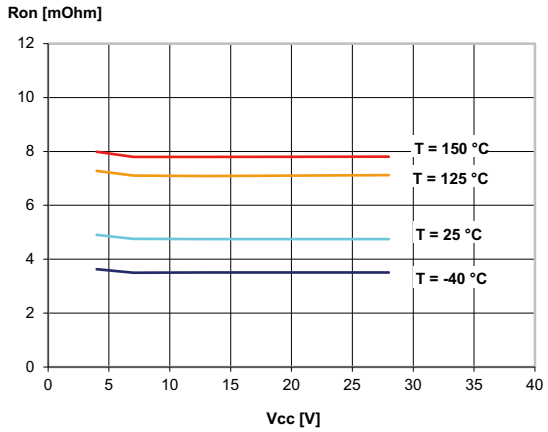
GAPG0603141541CFT

Figure 17. On-state resistance vs. T_{case}



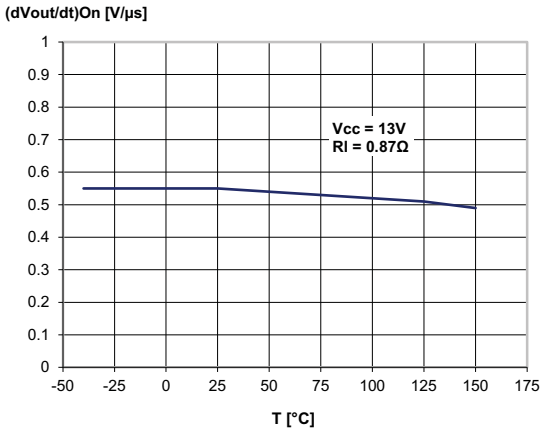
GAPG0603141542CFT

Figure 18. On-state resistance vs. V_{CC}



GAPG0603141543CFT

Figure 19. Turn-on voltage slope



GAPG0603141544CFT

Figure 20. Turn-off voltage slope

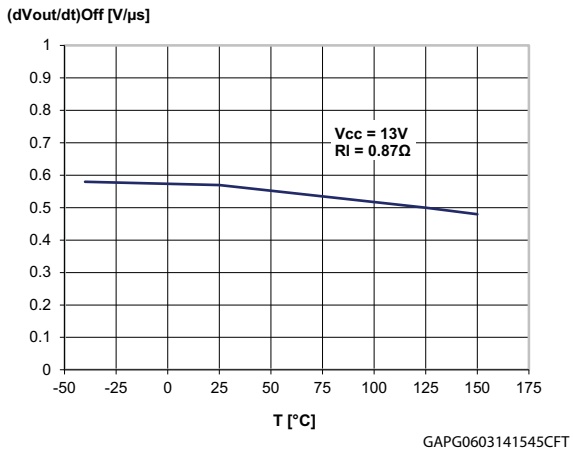


Figure 21. Won vs. T_{case}

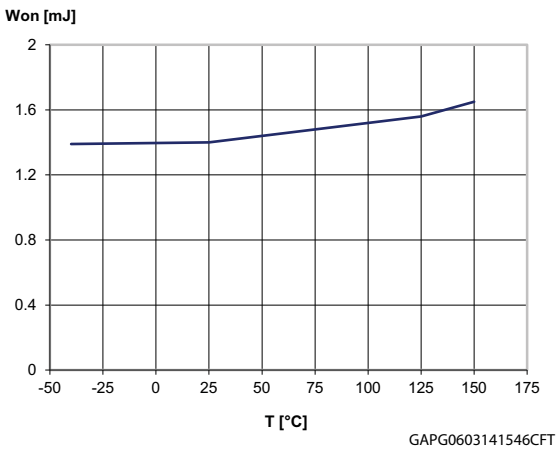


Figure 22. Woff vs. T_{case}

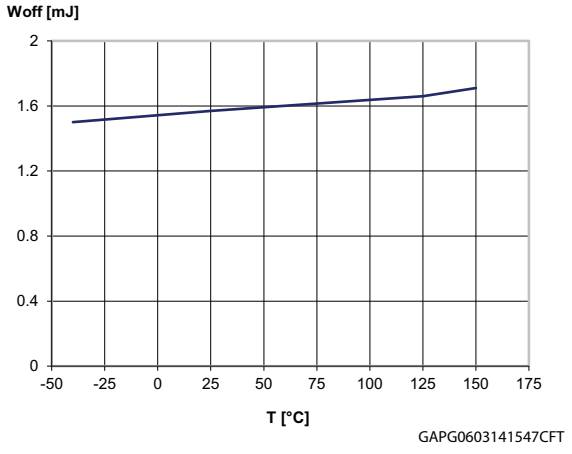


Figure 23. I_{LIMH} vs. T_{case}

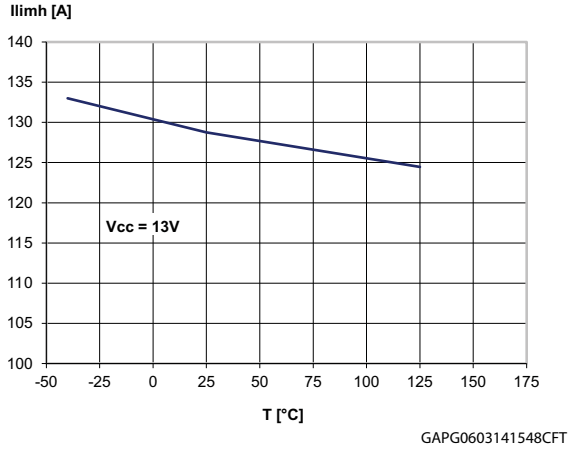


Figure 24. OFF-state open-load voltage detection threshold

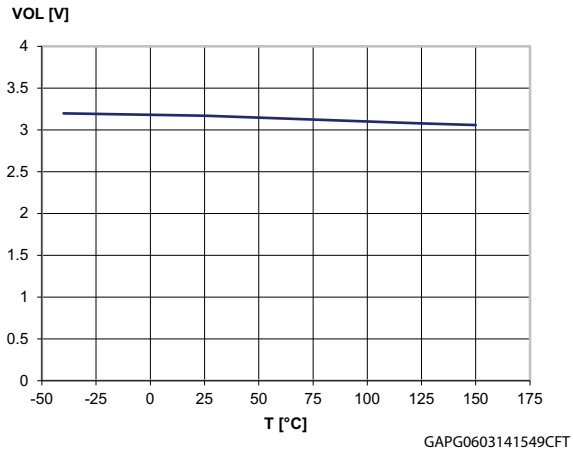


Figure 25. V_{sense} clamp vs. T_{case}

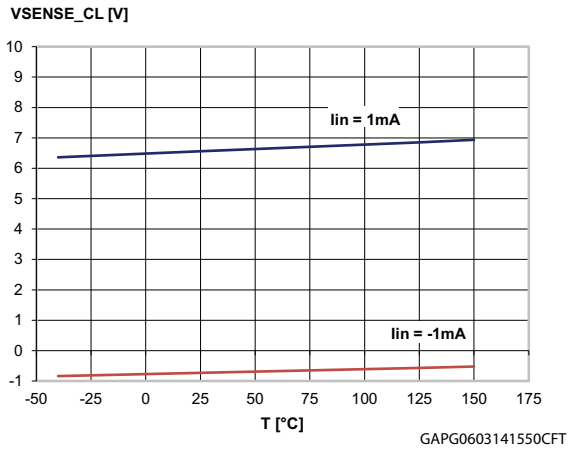
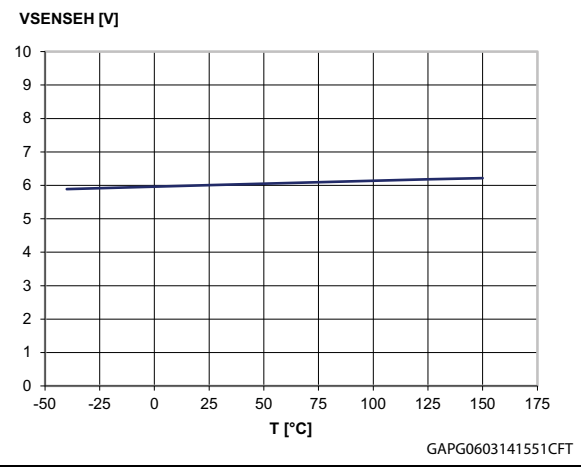


Figure 26. V_{senseh} vs. T_{case}



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. The device switches on again as soon as its junction temperature drops to T_R (see *Table 9*).

3.3 Current limitation

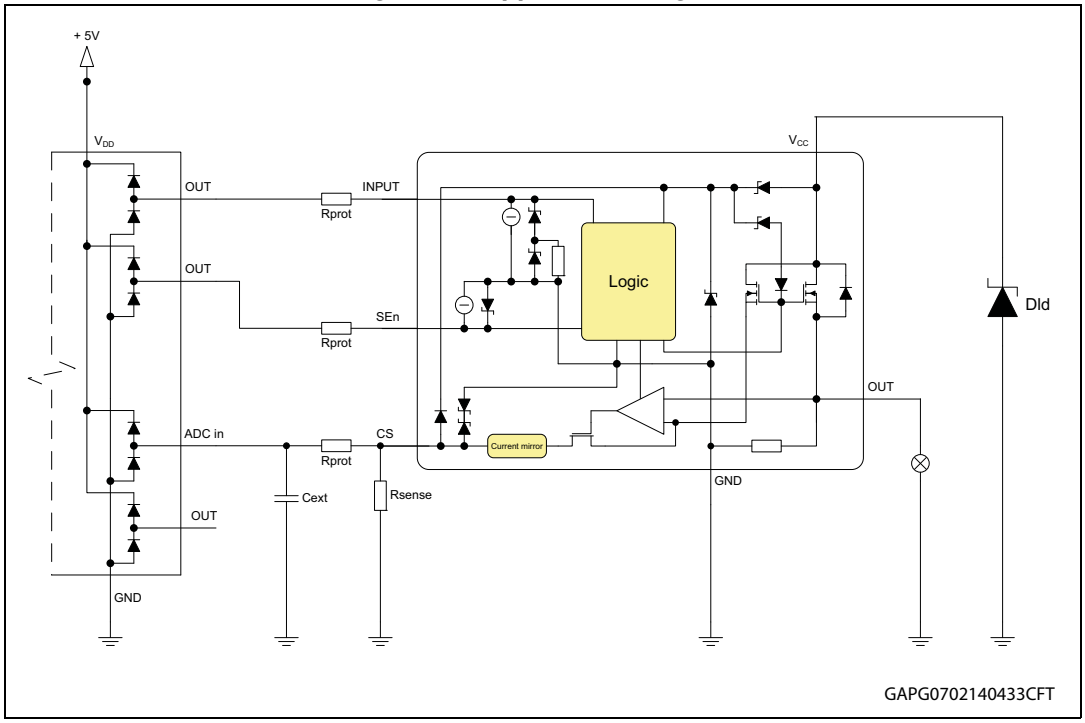
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} (see *Table 9*), allowing the inductor energy to be dissipated without damaging the device.

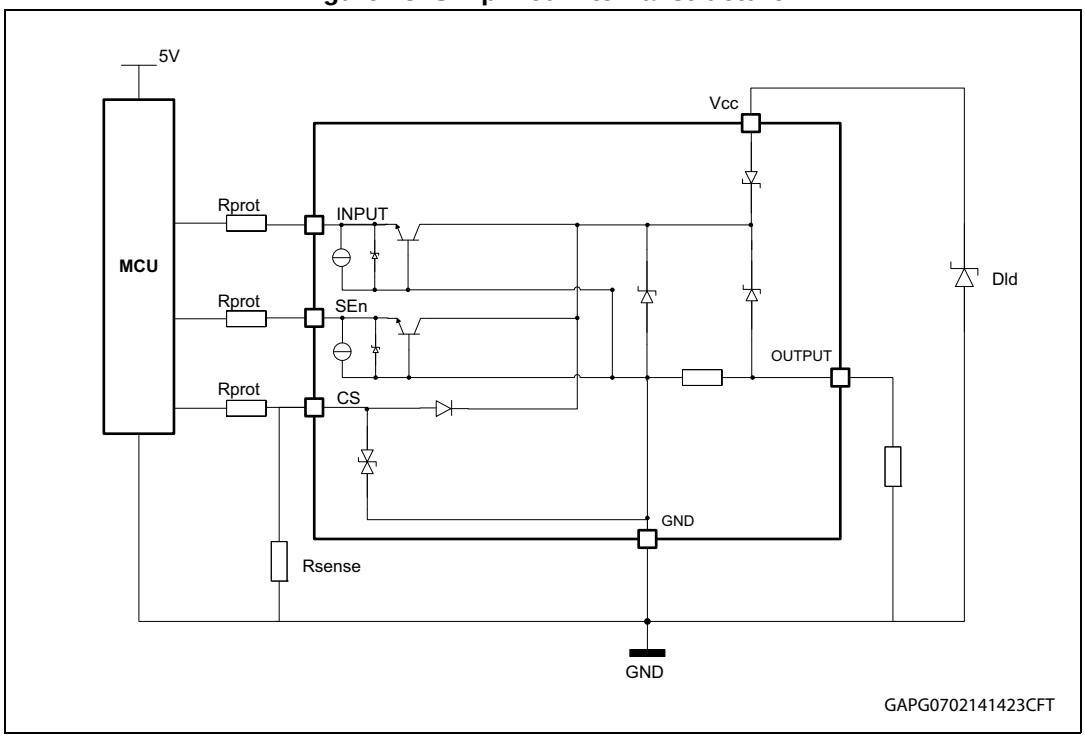
4 Application information

Figure 27. Application diagram



4.1 Protection against reverse battery

Figure 28. Simplified internal structure



The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 12*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 12. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S(1)		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50µs, 2Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1µs, 50Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1µs, 50Ω
4(2)	IV	-7V	1 pulse			100ms, 0.01Ω
Load dump according to ISO 16750-2:2010						
Test B(3)		40V	5 pulse	1 min		400ms, 2Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.
2. Test pulse from ISO 7637-2:2004(E).
3. With 40 V external suppressor referred to ground (-40°C < T_j < 150°C).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

$$7.5\ k\Omega \leq R_{prot} \leq 140\ k\Omega.$$

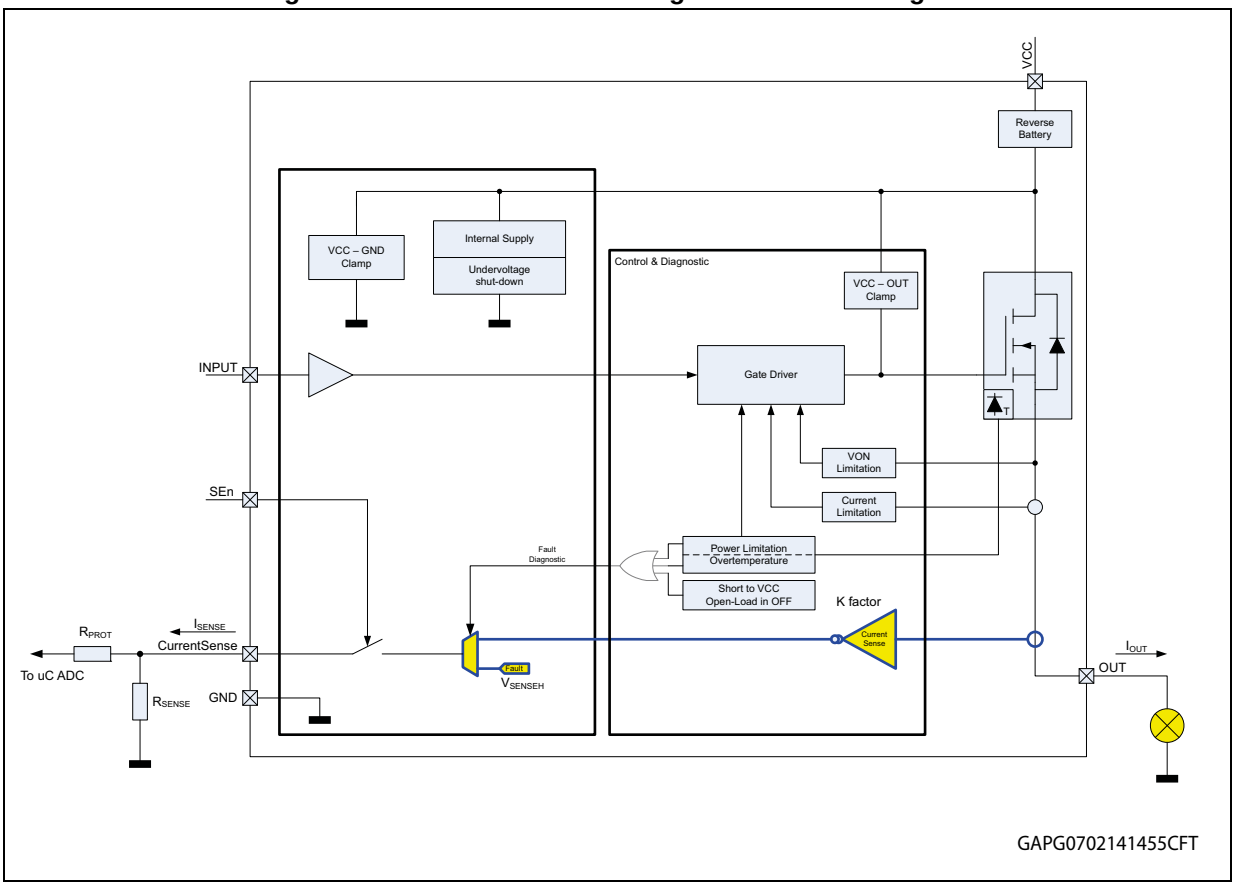
Recommended values: R_{prot} = 15 kΩ

4.4 CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signal:

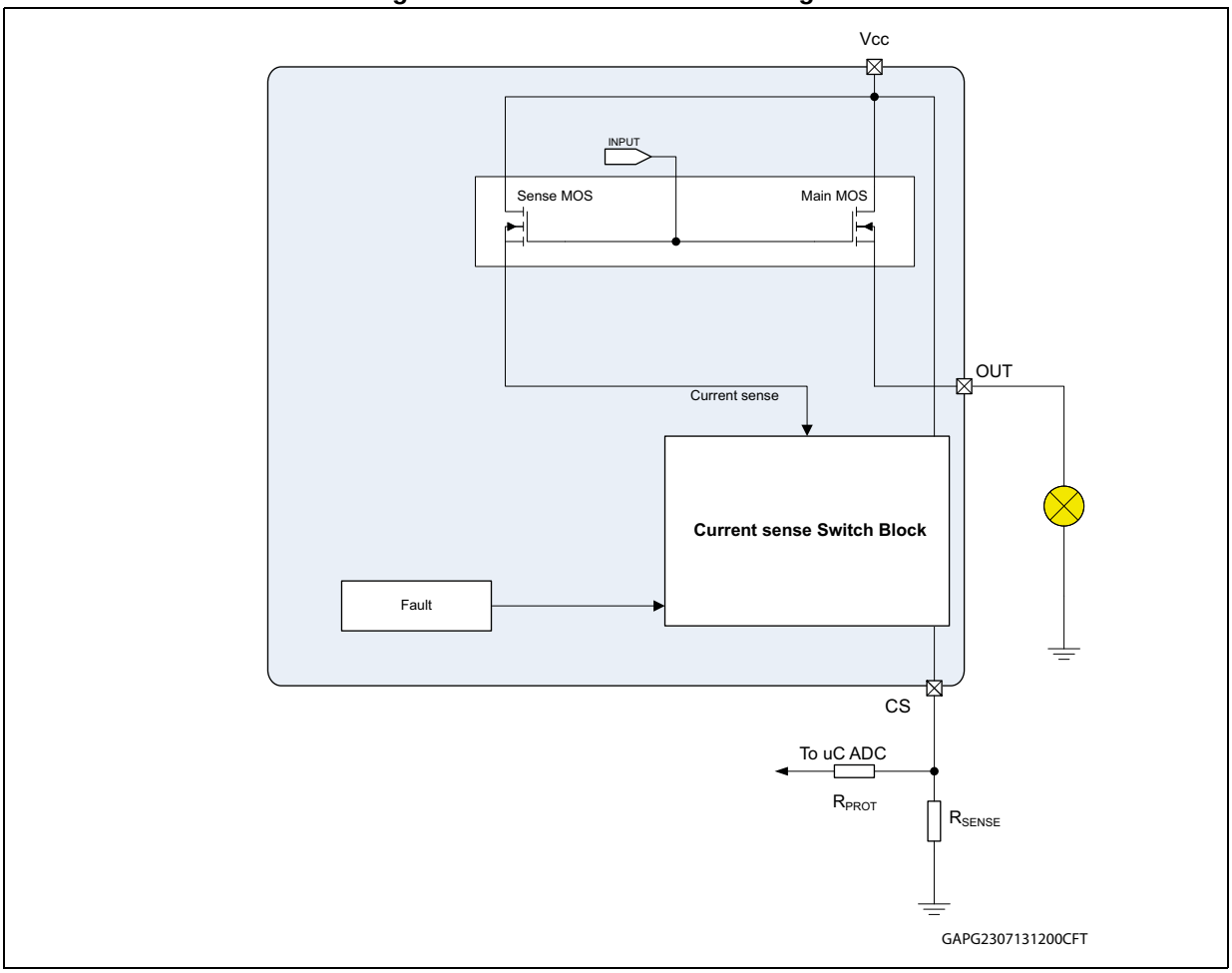
- Current monitor: current minitor of channel output current

Figure 29. CurrentSense and diagnostic – block diagram



4.4.1 Principle of CurrentSense signal generation

Figure 30. CurrentSense block diagram



Current sense

This output is capable of providing:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CurrentSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where :

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from CS pin in current output mode
- I_{OUT} is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a “current limited” voltage source, V_{SENSEH} (see *Table 10*).

In any case, the current sourced by the CS in this condition is limited to I_{SENSEH} (see *Table 10*).

Figure 31. Analogue HSD – open-load detection in off-state

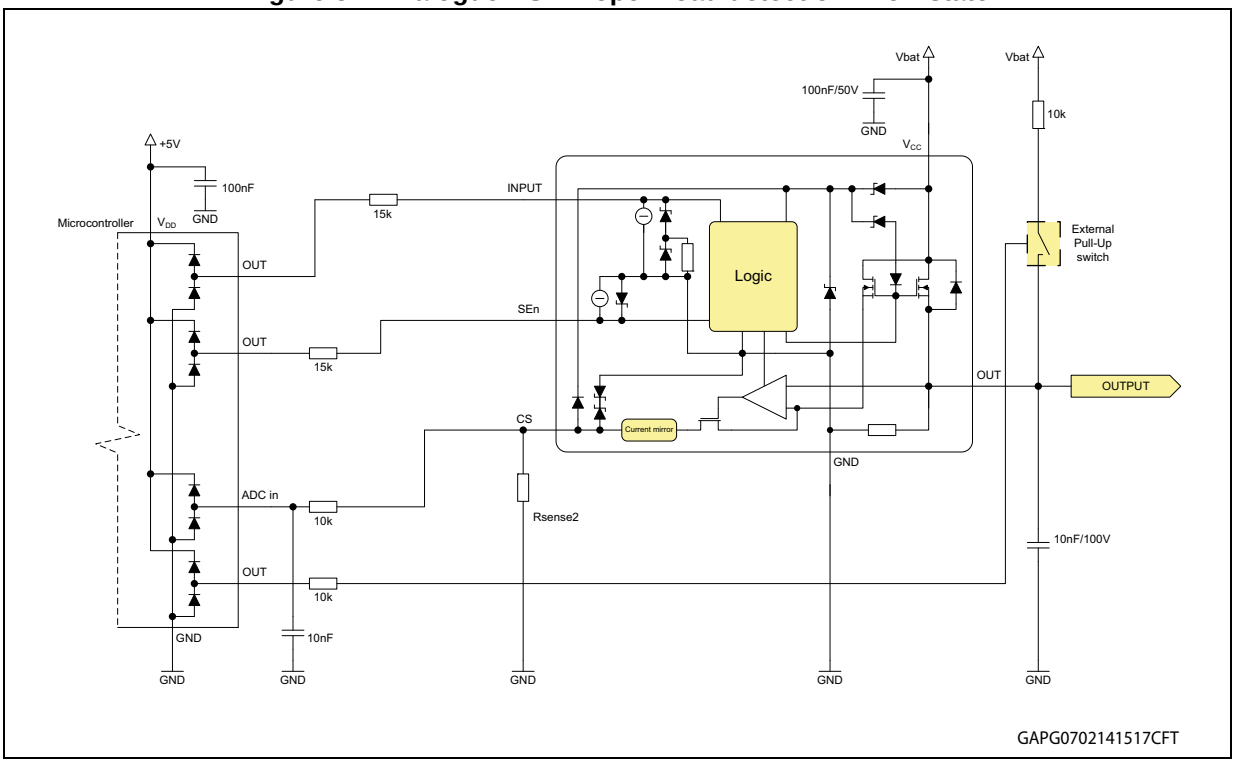


Figure 32. Open-load / short to V_{CC} condition

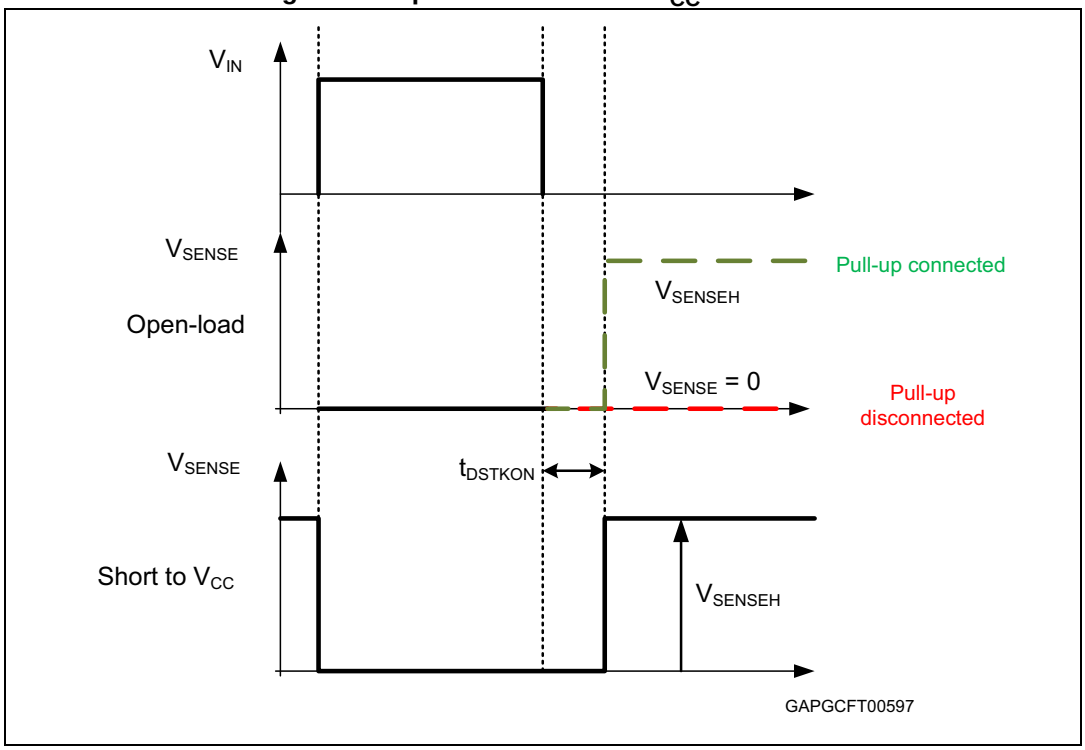


Table 13. CurrentSense pin levels in off-state

Condition	Output	CurrentSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

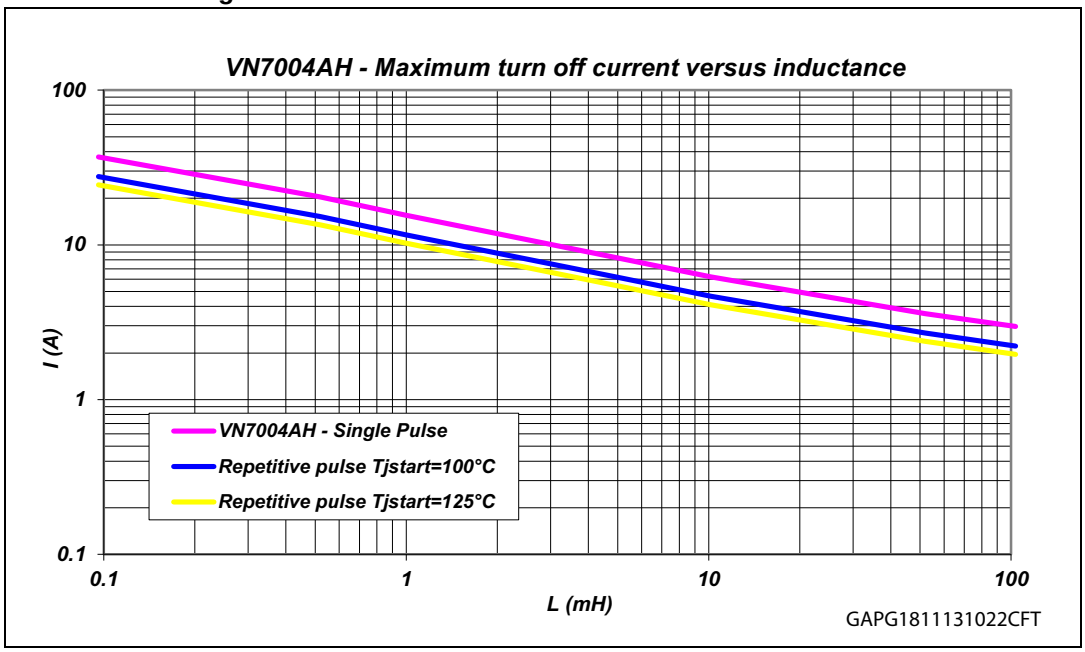
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation 2

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

4.5 Maximum demagnetization energy (V_{CC} = 16 V)

Figure 33. Maximum turn off current versus inductance



1. Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Package and PCB thermal data

5.1 Octapak thermal data

Figure 34. Octapak on two-layers PCB (2s0p to JEDEC JESD 51-5)

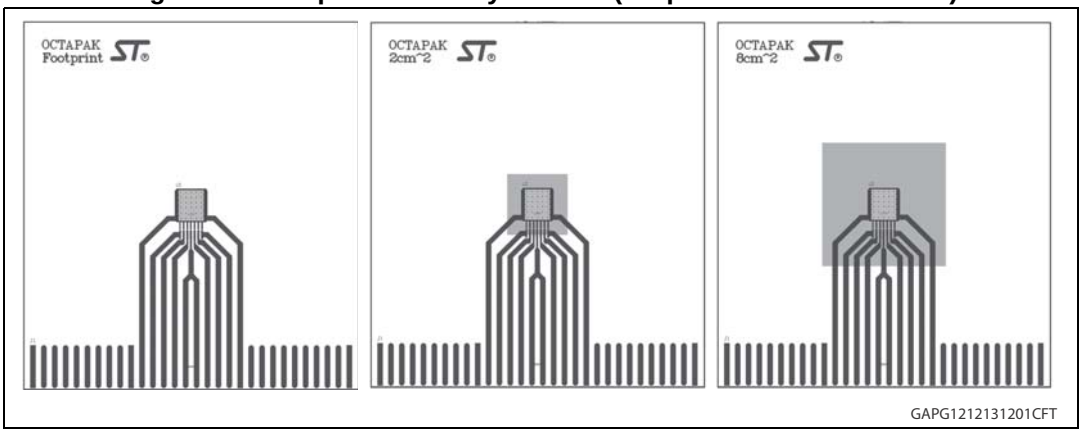


Figure 35. Octapak on four-layers PCB (2s2p to JEDEC JESD 51-7)

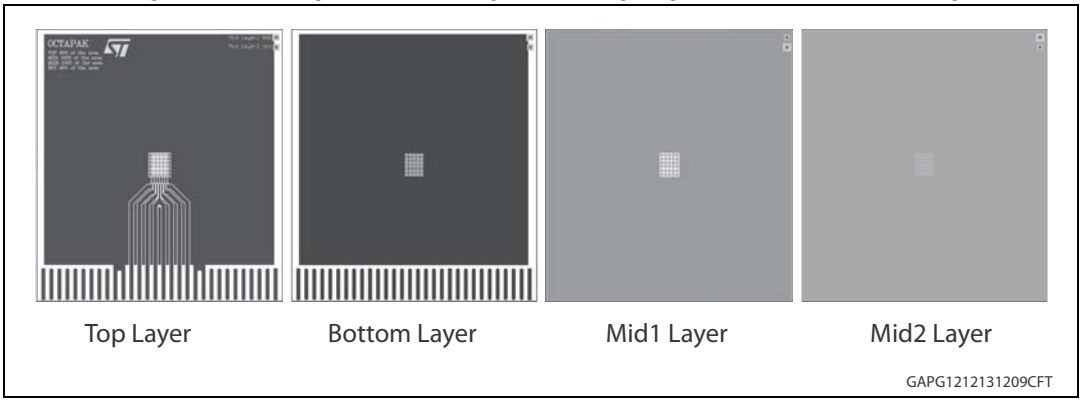


Table 14. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	6.4 mm x 7mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air conditions

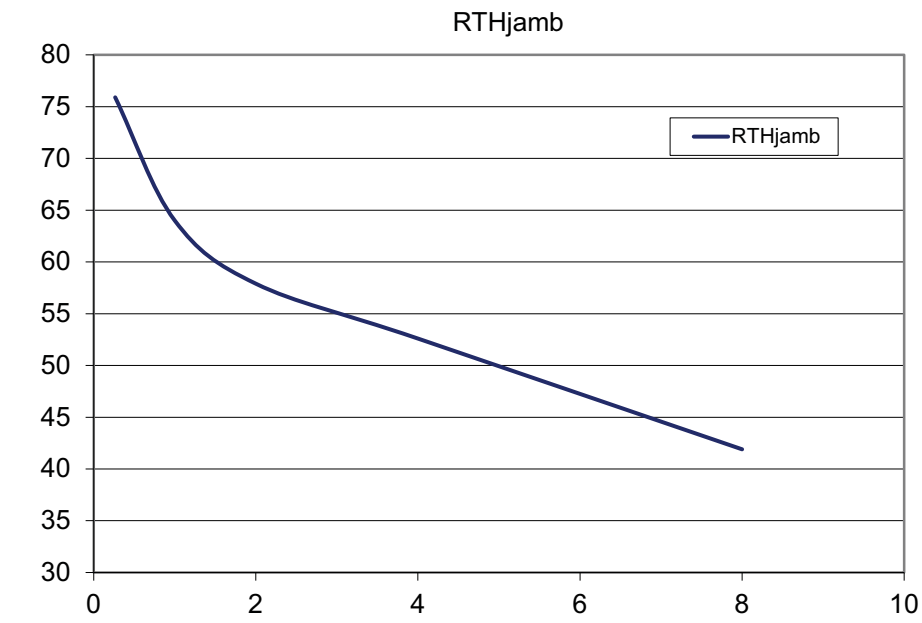
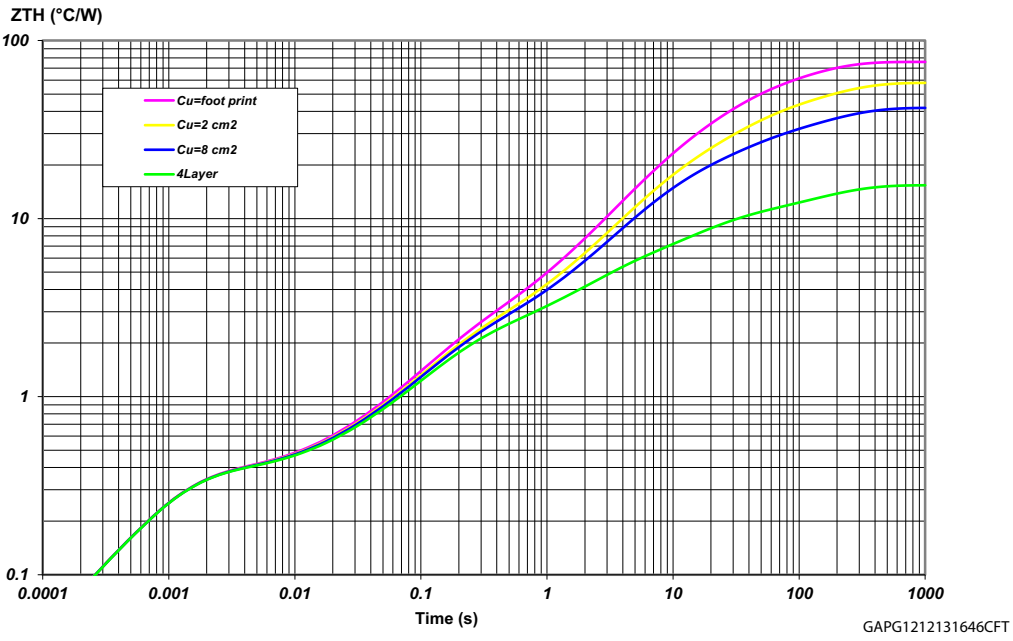


Figure 37. Octapak thermal impedance junction ambient single pulse

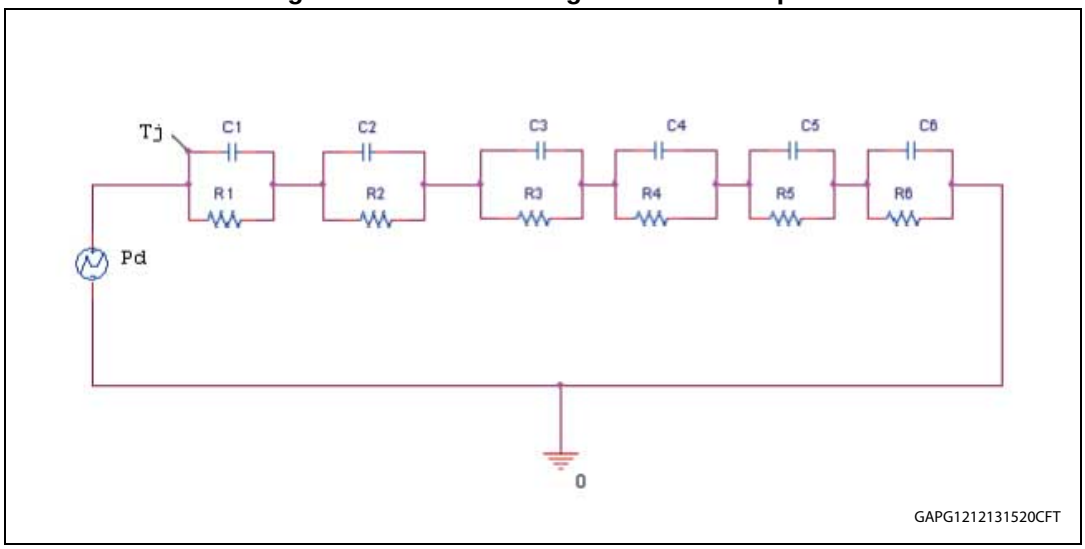


Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 38. Thermal fitting model for Octapak



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	0.005	0.005	0.005	0.005
R2 (°C/W)	0.35	0.35	0.35	0.35
R3 (°C/W)	1.54	1.54	1.54	1.54
R4 (°C/W)	10	10	10	2.5
R5 (°C/W)	28	20	12	5
R6 (°C/W)	36	26	18	6
C1 (W.s/°C)	0.002	0.002	0.002	0.002
C2 (W.s/°C)	0.0025	0.0025	0.0025	0.0025
C3 (W.s/°C)	0.1	0.1	0.1	0.1
C4 (W.s/°C)	0.6	0.6	0.6	0.8
C5 (W.s/°C)	0.8	1.4	2.2	3
C6 (W.s/°C)	3	6	9	25

6 Package information

6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 Octapak package information

Figure 39. Octapak package dimensions

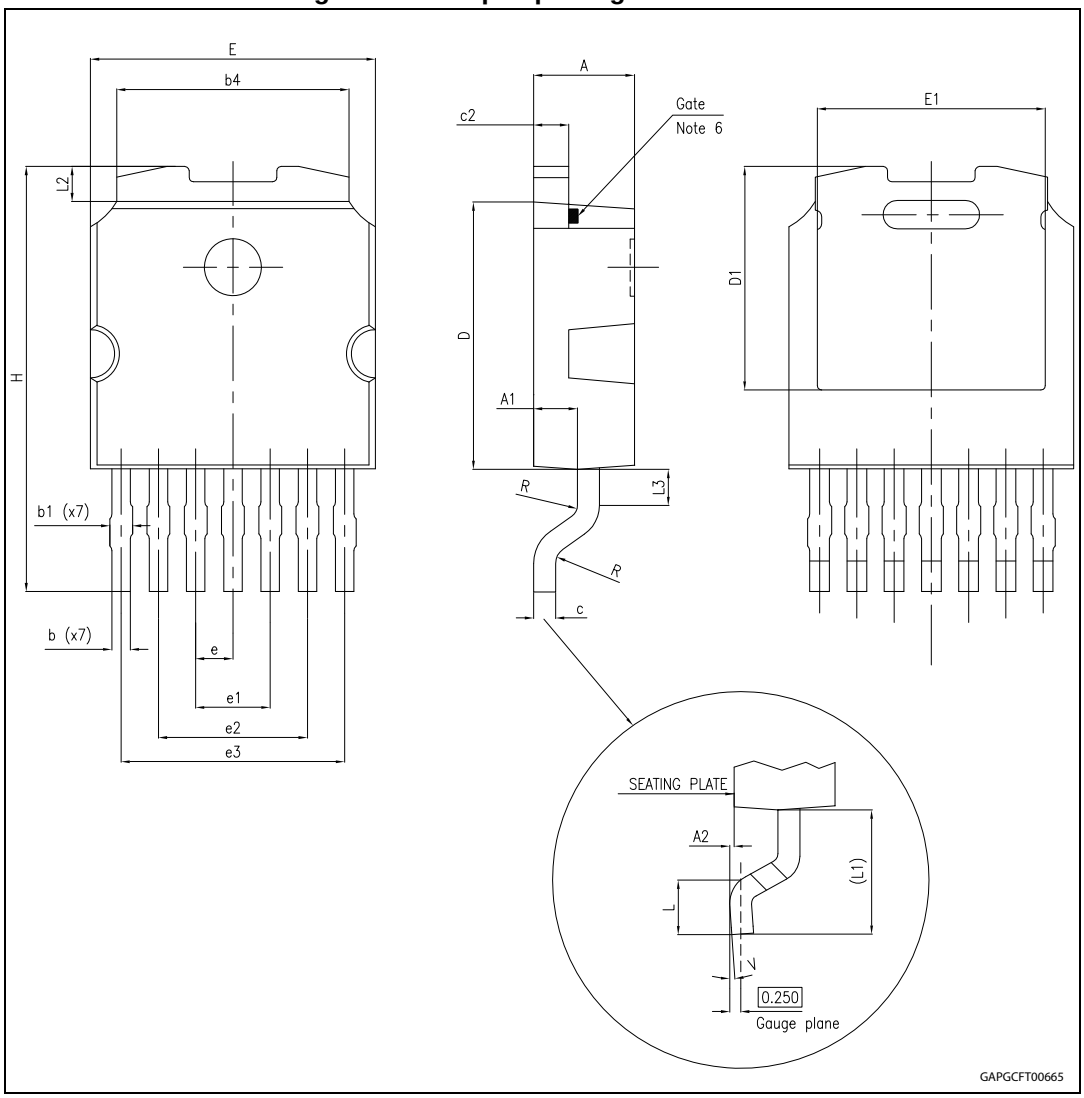


Table 16. Octapak mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.90	1.00	1.10
A2	0.03		0.15
b	0.38	0.45	0.52
b1			0.70
b4	5.20	5.30	5.40
c	0.45	0.50	0.60
c2	0.75	0.80	0.90
D	6.00	6.10	6.20
D1		5.15	
E	6.40	6.50	6.60
E1		5.30	
e		0.85 BSC	
e1	1.60	1.70	1.80
e2	3.30	3.40	3.50
e3	5.00	5.10	5.20
H	9.35	9.70	10.10
L	1.00		
(L1)		2.80	
L2		0.80	
L3		0.85	
R	0.40 BSC		
V2	0°		8°

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
26-Jul-2012	1	Initial release
20-Mar-2013	2	Updated *Features* list *Table 2: Pin functions*: – GND, INPUT, SEn: updated functions Updated *Table 3: Suggested connections for unused and not connected pins* *Table 4: Absolute maximum ratings*: – V_{CC}, $-I_{OUT}$: updated value – V_{CCJS}: added row – V_{CCPK}, I_{SENSE}, V_{ESD}: updated parameter and value – $-V_{SENSE}$: removed row *Table 5: Thermal data*: – $R_{thj\text{-}case}$: removed row – $R_{thj\text{-}board}$: added row *Table 6: Power section*: – $V_{USDReset}$, R_{ON_Rev}, $I_{GND(ON)}$: added row – V_{clamp}: added test conditions and value – I_{STBY}, $I_{L(OFF)}$: updated parameter definition – $I_{S(ON)}$: updated values Updated *Table 7: Switching (V_{CC} = 13 V; -40 ºC < T_j < 150 °C, unless otherwise specified)* *Table 8: Logic Inputs (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C)*: – V_{ICL}, V_{SEnCL}: updated values *Table 9: Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*: – I_{LIMH}: updated test conditions and values – I_{LIML}: updated value *Table 10: CurrentSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*: – V_{SENSE_CL}, K_0, dK_0/K_0, K_1, dK_1/K_1, K_2, dK_2/K_2, K_3, dK_3/K_3, $t_{DSENSE1L}$, $t_{DSENSE2H}$, $\Delta t_{DSENSE2H}$, $t_{DSENSE2L}$: updated test conditions – I_{SENSE0}: added test condition, updated values – V_{OUT_CSD}, V_{SENSE_SAT}, I_{SENSE_SAT}, I_{OUT_SAT}, $t_{D_OL_V}$: added rows – $I_{L(off2)}$, V_{SENSEH}, $t_{DSENSE1H}$: updated test conditions and values – I_{SENSEH}: updated value Removed *Figure: Switching times* and *Figure: Pulse skew* Added *Figure 6: Switching times and Pulse skew* and *Figure 7: T_{DSTKON}* *Table 11: Truth table*: – Overload: updated conditions
18-Sep-2013	3	Updated disclaimer.

Table 17. Document revision history (continued)

Date	Revision	Changes
27-Mar-2014	4	Updated *Features* list. Updated *Figure 2: Configuration diagram (top view)* *Table 4: Absolute maximum ratings*: – E_{MAX}: updated parameter and value Updated *Table 5: Thermal data* *Table 6: Power section*: – R_{ON}, R_{ON_Rev}: updated values *Table 7: Switching (V_{CC} = 13 V; -40 ºC < T_j < 150 °C, unless otherwise specified)*: – W_{on}, W_{off}, $(dV_{OUT}/dt)_{on}$, $(dV_{OUT}/dt)_{off}$: updated values – t_{SKEW}: updated values *Table 9: Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*: – I_{LIMH}: updated values; added note – T_{RS}: updated test conditions *Table 10: CurrentSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*: – K_0, dK_0/K_0: removed rows – K_1, dK_1/K_1: updated test conditions and values – K_2, dK_2/K_2, K_3, dK_3/K_3, $t_{DSENSE2H}$, $\Delta t_{DSENSE2H}$: updated values – $t_{D_OL_V}$: updated test conditions *Table 11: Truth table* Removed *Table : Electrical transient requirements (part 1/3)*, *Table : Electrical transient requirements (part 2/3)* and *Table : Electrical transient requirements (part 3/3)* Added *Figure 4: I_{OUT}/I_{SENSE} versus I_{OUT}* and *Figure 5: Current sense precision vs. I_{OUT}* Added *Section 2.4: Electrical characteristics curves* Added *Section 3: Protections*, *Chapter 4: Application information* and *Chapter 5: Package and PCB thermal data*
05-May-2014	5	Updated *Figure 37: Octapak thermal impedance junction ambient single pulse* Updated *Table 15: Thermal parameters*
26-Aug-2014	6	*Table 4: Absolute maximum ratings*: – V_{CCJS}: removed parameter – V_{CC_LSC}: added parameter *Table 9: Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)*: – I_{LIMH}: updated test conditions
10-Sep-2014	7	*Table 9: Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)* – V_{DS}: updated test conditions
17-Oct-2014	8	Updated *Table 16: Octapak mechanical data*.

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