LF411QML Low Offset, Low Drift JFET Input Operational Amplifier

Check for Samples: LF411QML-SP

FEATURES

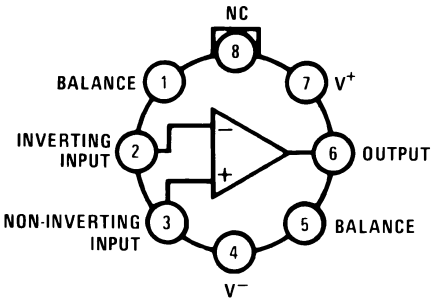
- **Available with Radiation Specification**
  - **ELDRS FREE 100 krad(Si)**
- **Internally Trimmed Offset Voltage: 0.5 mV(Typ)**
- **Input Offset Voltage Drift: 10 µV/°C**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 3 MHz**
- **High Slew Rate: 10V/µs**
- **Low Supply Current: 1.8 mA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion: A_V = 10, R_L = 10KΩ, V_O = 20V_{P-P}, BW = 20Hz - 20KHz <0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 µs**

DESCRIPTION

This device is a low cost, high speed, JFET input operational amplifier with very low input offset voltage and ensured input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411QML is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

This amplifier may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Connection Diagram



Pin 4 connected to case.

Figure 1. SDIP Package

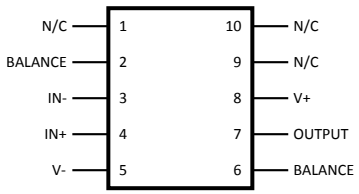


Figure 2. 10LD CLGA Package

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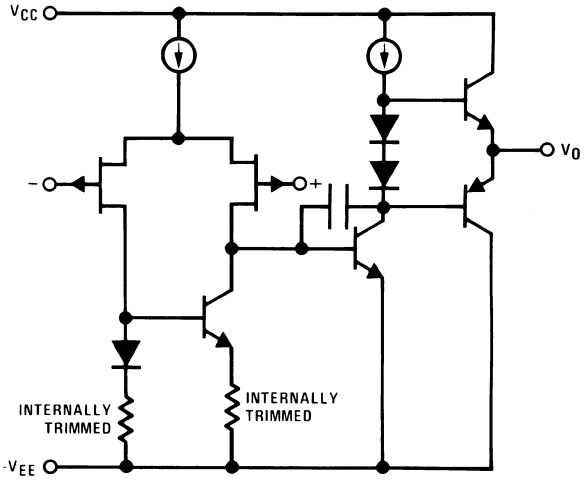
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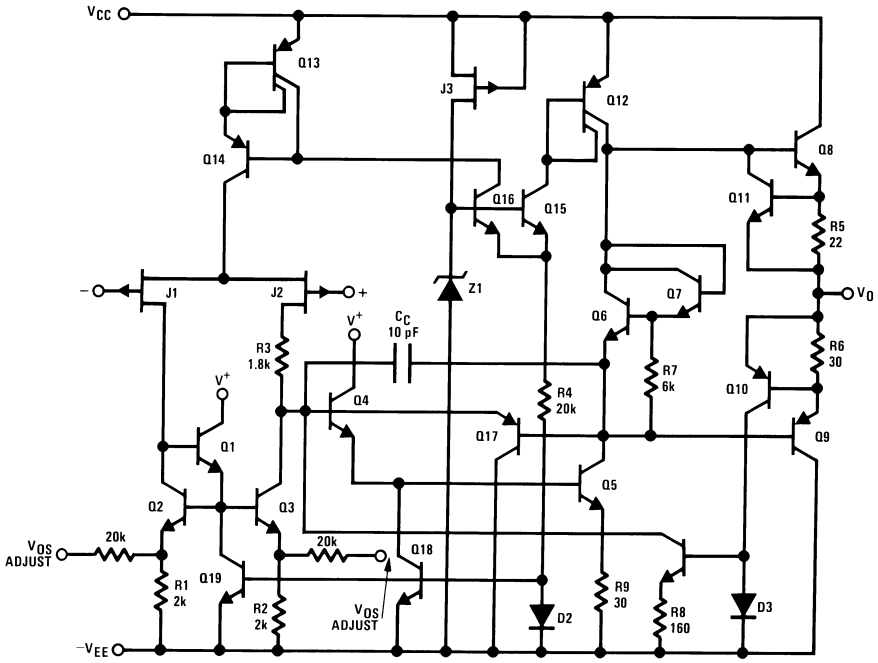
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Simplified Schematic



Detailed Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)

Supply Voltage			±18V
Differential Input Voltage			±30V
Input Voltage Range(2)			±15V
Output Short Circuit Duration			Continuous
Power Dissipation(3)(4)		SDIP Package	670mW
		CLGA Package	670mW
T_{Jmax}	H Package		150°C
	WG Package		150°C
Thermal Resistance	θ_{JA}	SDIP Package Still Air	162°C/W
		SDIP Package 500LF/Min Air Flow	65°C/W
		CLGA Package Still Air	170°C/W
		CLGA Package 500LF/Min Air Flow	120°C/W
	θ_{JC}	SDIP Package	20°C/W
		CLGA Package	26°C/W
Operating Temperature Range			$-55°C \le T_A \le 125°C$
Storage Temperature Range			$-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 seconds)			260°C
Package Weight (Typical)		SDIP Package	TBD
		CLGA Package	220mg
ESD Tolerance (5)			750V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(4) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside ensured limits.

(5) Human body model, 100pF discharged through 1.5KΩ.

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Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

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LF411 883 Electrical Characteristics
DC Parameters

The following conditions apply, unless otherwise specified.
DC: V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	R_S = 10KΩ		-2.0	2.0	mV	1
				-3.7	3.7	mV	2
				-3.3	3.3	mV	3
I_{IO}	Input Offset Current			-0.1	0.1	nA	1
			See (1)	-25	25	nA	2
$±I_{IB}$	Input Bias Current			-0.2	0.2	nA	1
			See (1)	-50	50	nA	2
V_{CM}	Input Common Mode Voltage Range		See (2)	±9.0		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	R_S ≤ 10KΩ, V_{CM} = ±9V		70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	+V_{CC} = 6V, -V_{CC} = -15V		70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	+V_{CC} = 15V, -V_{CC} = -6V		70		dB	1, 2, 3
I_S	Supply Current				3.4	mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	+V_I = -11V, -V_I = 11V, R_S = 10KΩ		13	50	mA	1
				6.0	60	mA	2, 3
$+I_{OS}$	Output Short Circuit Current	+V_I = 11V, -V_I = -11V, R_S = 10KΩ		-50	-13	mA	1
				-60	-6.0	mA	2, 3
$+V_{IO\ Adj}$	Input Offset Voltage Adjustment			8.0		mV	1
$-V_{IO\ Adj}$	Input Offset Voltage Adjustment				-8.0	mV	1
$+A_{VS}$	Large Signal Voltage Gain	V_O = 0 to 10V, R_L = 2KΩ	See (3)	25		V/mV	4
		V_O = 0 to 10V, R_L = 2KΩ	See (3)	15		V/mV	5, 6
$-A_{VS}$	Large Signal Voltage Gain	V_O = 0 to -10V, R_L = 2KΩ	See (3)	25		V/mV	4
		V_O = 0 to -10V, R_L = 2KΩ	See (3)	15		V/mV	5, 6
V_O+	Output Voltage Swing	R_L = 10KΩ, +V_I = 11V, -V_I = -11V, R_S = 10KΩ		12		V	4, 5, 6
V_O-	Output Voltage Swing	R_L = 10KΩ, +V_I = -11V, -V_I = 11V, R_S = 10KΩ			-12	V	4, 5, 6

(1) R_S = 10KΩ @ +125°C.
(2) Parameters specified by CMRR test.
(3) Datalog in K = V/mV.

AC Parameters

The following conditions apply, unless otherwise specified.
AC: V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR+	Slew Rate	V_O = -5V to 5V		8.0		V/µS	7
SR-	Slew Rate	V_O = 5V to -5V		8.0		V/µS	7
GBW	Gain Bandwidth Product			2.7		MHz	7

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Space Level Electrical Characteristics
DC Parameters

The following conditions apply, unless otherwise specified.
DC: V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	R_S = 10KΩ		-2.0	2.0	mV	1
				-3.7	3.7	mV	2
				-3.3	3.3	mV	3
I_{IO}	Input Offset Current			-0.1	0.1	nA	1
			See (1)	-25	25	nA	2
$±I_{IB}$	Input Bias Current			-0.2	0.2	nA	1
			See (1)	-50	50	nA	2
V_{CM}	Input Common Mode Voltage Range		See (2)	±9.0		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	R_S ≤ 10KΩ, V_{CM} = ±9V		70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	+V_{CC} = 6V, -V_{CC} = -15V		70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	+V_{CC} = 15V, -V_{CC} = -6V		70		dB	1, 2, 3
I_S	Supply Current				3.4	mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	+V_I = -11V, -V_I = 11V, R_S = 10KΩ		13	50	mA	1
				6.0	60	mA	2, 3
$+I_{OS}$	Output Short Circuit Current	+V_I = 11V, -V_I = -11V, R_S = 10KΩ		-50	-13	mA	1
				-60	-6.0	mA	2, 3
$+V_{IO\ Adj}$	Input Offset Voltage Adjustment			8.0		mV	1
$-V_{IO\ Adj}$	Input Offset Voltage Adjustment				-8.0	mV	1
$+A_{VS}$	Large Signal Voltage Gain	V_O = 0 to 10V, R_L = 2KΩ	See (3)	25		V/mV	4
		V_O = 0 to 10V, R_L = 2KΩ	See (3)	15		V/mV	5, 6
$-A_{VS}$	Large Signal Voltage Gain	V_O = 0 to -10V, R_L = 2KΩ	See (3)	25		V/mV	4
		V_O = 0 to -10V, R_L = 2KΩ	See (3)	15		V/mV	5, 6
V_O+	Output Voltage Swing	R_L = 10KΩ, +V_I = 11V, -V_I = -11V, R_S = 10KΩ		12		V	4, 5, 6
V_O-	Output Voltage Swing	R_L = 10KΩ, +V_I = -11V, -V_I = 11V, R_S = 10KΩ			-12	V	4, 5, 6

(1) R_S = 10KΩ @ +125°C.
(2) Parameters specified by CMRR test.
(3) Datalog in K = V/mV.

AC Parameters

The following conditions apply, unless otherwise specified.
AC: V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR+	Slew Rate	V_O = -5V to 5V		8.0		V/µS	7
SR-	Slew Rate	V_O = 5V to -5V		8.0		V/µS	7
GBW	Gain Bandwidth Product			2.7		MHz	7

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Space Level Electrical Characteristics (Continued)
DC Parameters - Drift Values

The following conditions apply, unless otherwise specified.
DC: V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω "Delta calculations performed on Space Level devices at Group B Subgroup 5 ONLY"

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			−1	1	mV	1
$+I_{IB}$	Input Bias Current			−0.1	0.1	nA	1
$-I_{IB}$	Input Bias Current			−0.1	0.1	nA	1

LF411–MLS 50k Radiation Electrical Characteristics
DC Parameters - Post Radiation Limits(1)

The following conditions apply, unless otherwise specified.
DC: V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω Post Radiation Limits +25°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{IO}	Input Offset Current			−0.25	0.25	nA	1
I_{IB+}	Input Bias Current			−1.0	1.0	nA	1
I_{IB-}	Input Bias Current			−1.0	1.0	nA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, Method 1019

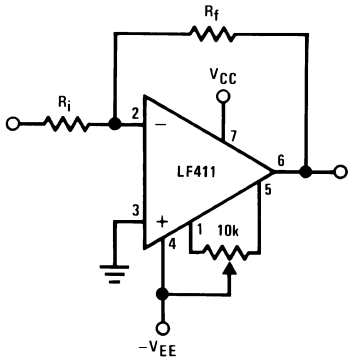
LF411MWGRLQMLV 100k Radiation Electrical Characteristics — ELDRS Free Only SMD# 5962R1122201
DC Parameters - Post Radiation Limits(1)

The following conditions apply, unless otherwise specified.
DC: V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω Post Radiation Limits +25°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{IO}	Input Offset Current			−1.0	1.0	nA	1
I_{IB+}	Input Bias Current			−0.20	6.0	nA	1
I_{IB-}	Input Bias Current			−0.20	6.0	nA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose rate environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

Typical Connection



Typical Performance Characteristics

Input Bias Current

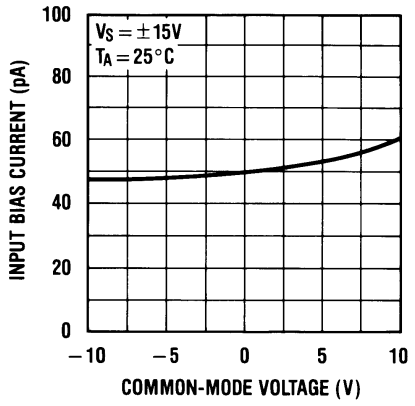


Figure 3.

Input Bias Current

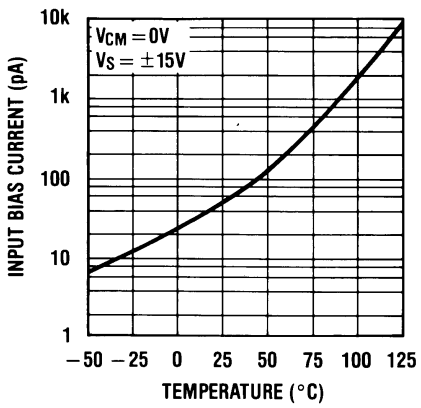


Figure 4.

Supply Current

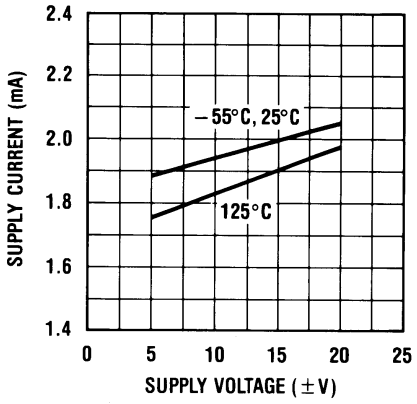


Figure 5.

Positive Common-Mode Input Voltage Limit

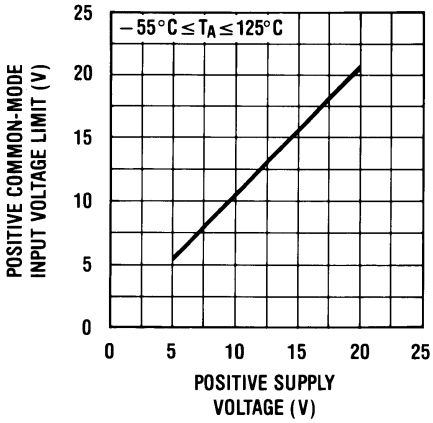


Figure 6.

Negative Common-Mode Input Voltage Limit

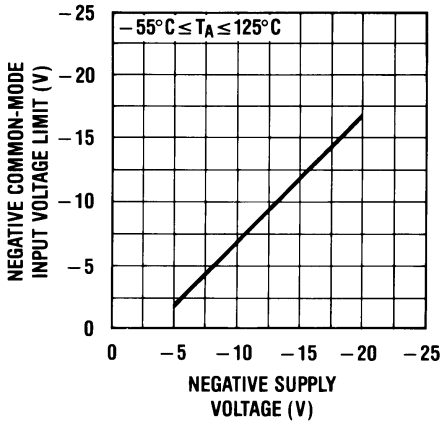


Figure 7.

Positive Current Limit

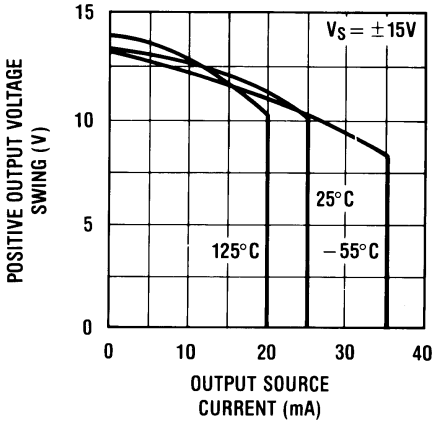


Figure 8.

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Typical Performance Characteristics (continued)

Negative Current Limit

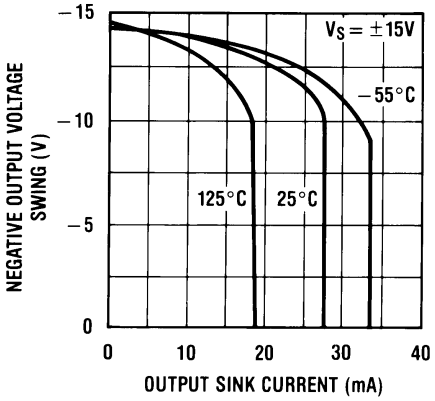


Figure 9.

Output Voltage Swing

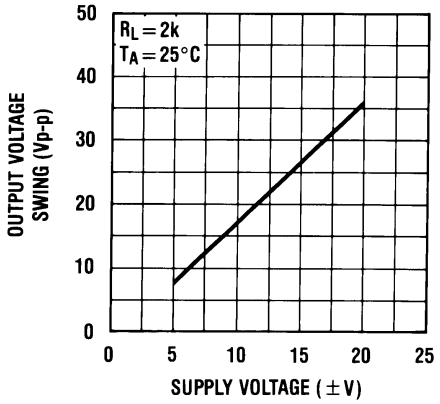


Figure 10.

Output Voltage Swing

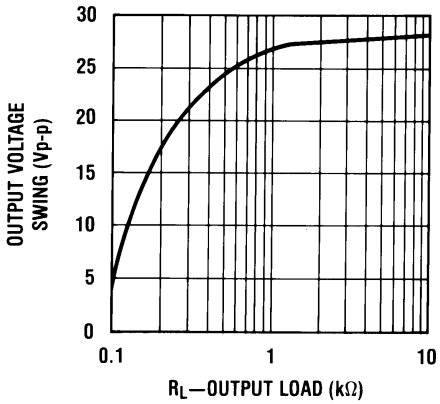


Figure 11.

Gain Bandwidth

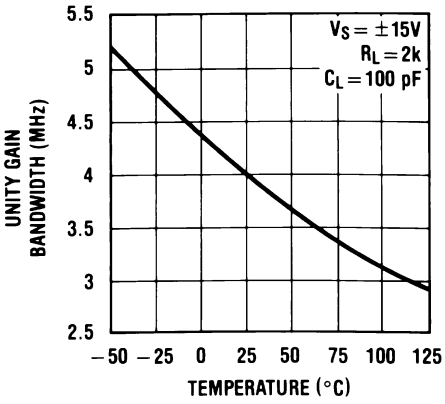


Figure 12.

Bode Plot

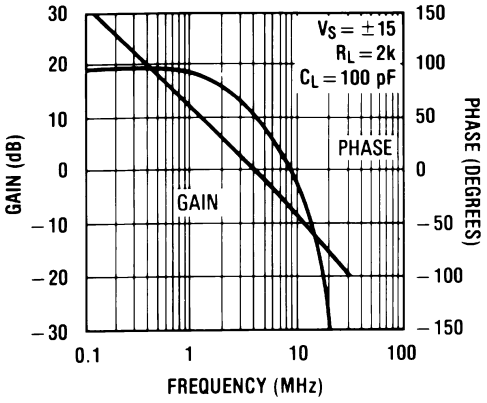


Figure 13.

Slew Rate

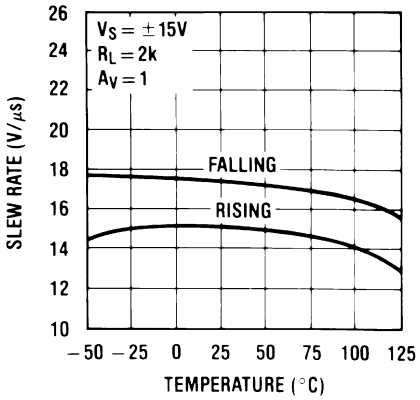


Figure 14.

Typical Performance Characteristics (continued)

Distortion vs Frequency

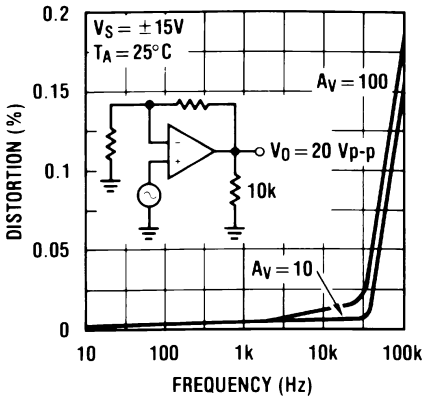


Figure 15.

Undistorted Output Voltage Swing

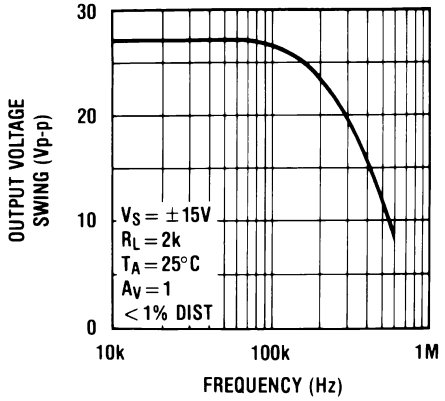


Figure 16.

Open Loop Frequency Response

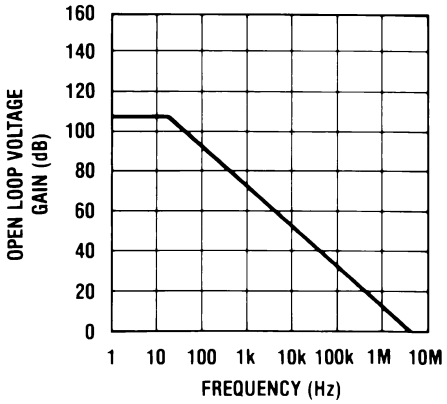


Figure 17.

Common-Mode Rejection Ratio

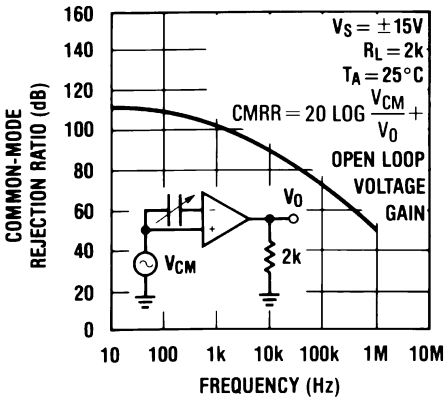


Figure 18.

Power Supply Rejection Ratio

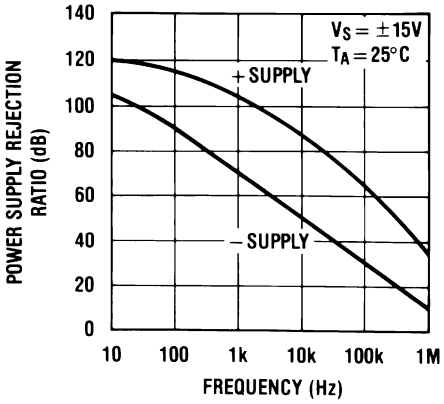


Figure 19.

Equivalent Input Noise Voltage

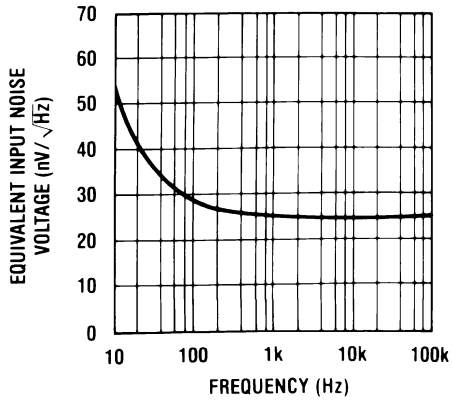


Figure 20.

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Typical Performance Characteristics (continued)

Open Loop Voltage Gain

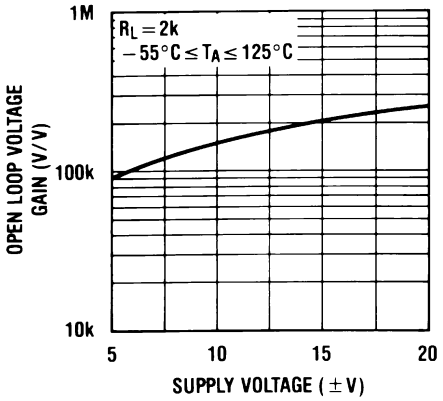


Figure 21.

Output Impedance

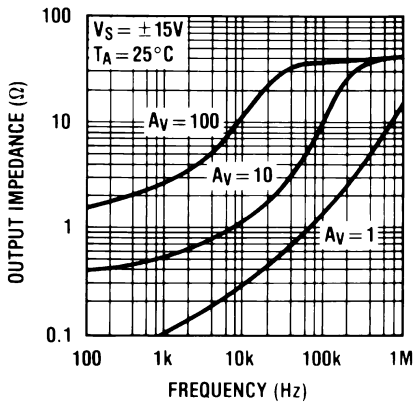


Figure 22.

Inverter Settling Time

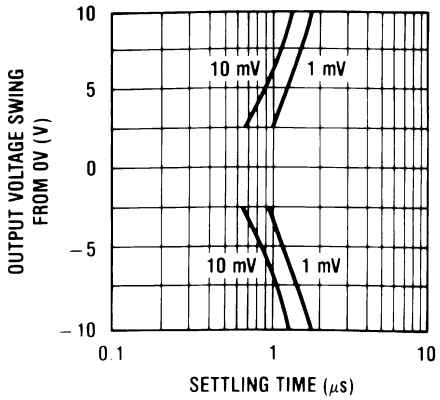
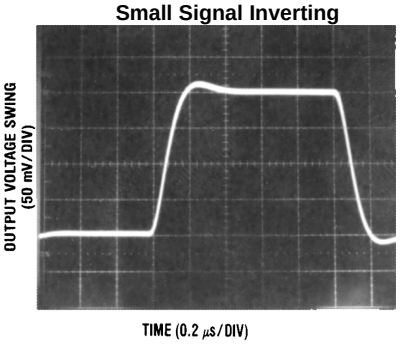


Figure 23.

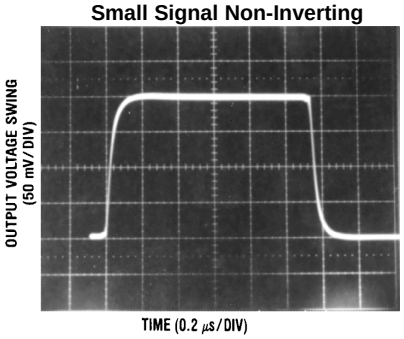
Pulse Response

R_L=2 kΩ, C_L10 pF

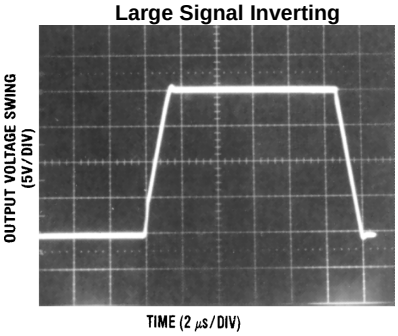
Small Signal Inverting



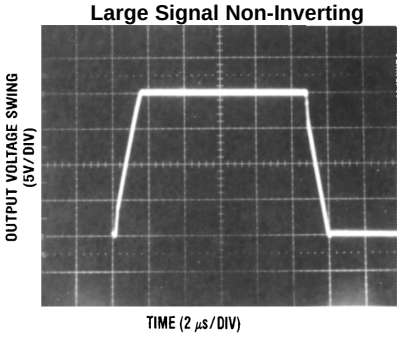
Small Signal Non-Inverting



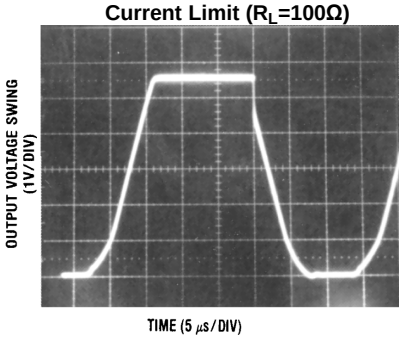
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L=100Ω)



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APPLICATION HINTS

The LF411QML series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and ensured input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411QML is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411QML will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

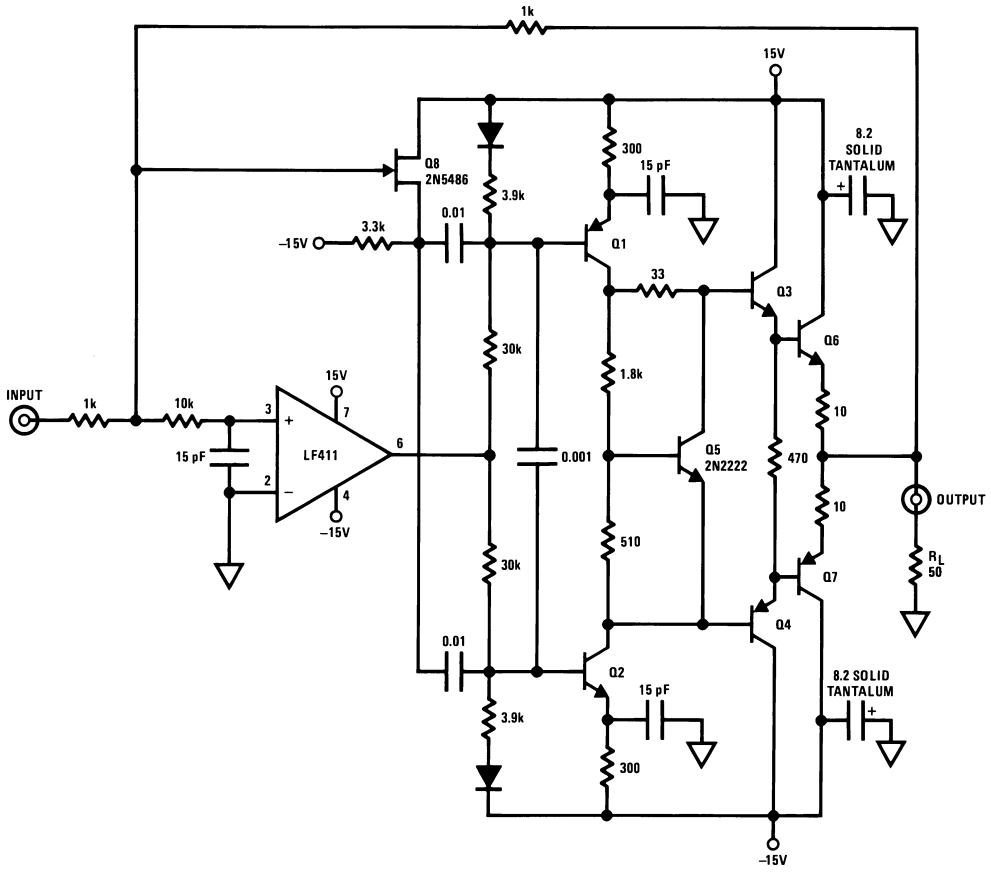
As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

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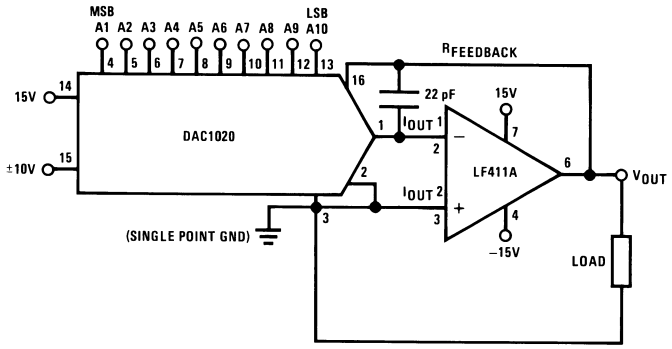
Typical Applications

Figure 24. High Speed Current Booster



PNP=2N2905
NPN=2N2219 unless noted
TO-5 heat sinks for Q6-Q7

Figure 25. 10-Bit Linear DAC with No V_{OS} Adjust



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le -\frac{1023}{1024}V_{REF}$$

where A_N=1 if the A_N digital input is high
A_N=0 if the A_N digital input is low

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Figure 26. Single Supply Analog Switch with Buffered Output

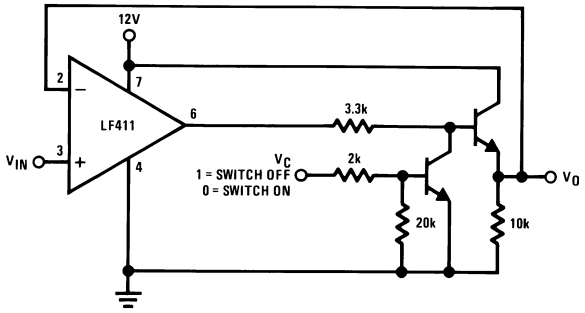


Table 2. Revision History

Date Released	Revision	Section	Originator	Changes
10/11/05	A	New Release to corporate format	L. Lytle	1 MDS data sheet was converted into the corporate data sheet format. MDS MNLF411M-X Rev 2A2 will be archived.
05/07/07	B	Features, Ordering Information Table, LF411-MLS Electricals	L. McGee	Added reference to Radiation and Radiation Electricals for LF411-MLS device. Revision A will be archived.
06/30/11	C	Features, Ordering Information Table, LF411-MLS 50k Post Radiation Electricals, LF411MWGRLQMLV Post Radiation Electricals	L. McGee & K.Kruckmeyer	Added LF411MWGRLQMLV to Ordering Info and modified Radiation Electricals to “Radiation” devices. Added 50k and 100k Post Radiation DC parameter tables. Revision B will be archived.
03/26/2013	C	All Sections		Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962R1122201VZA	ACTIVE	CFP	NAC	10	54	TBD	Call TI	Call TI	-55 to 125	LF411MWG RLQMLV Q 5962R11222 01VZA ACO 01VZA >T	Samples
LF411MWGRLQMLV	ACTIVE	CFP	NAC	10	54	TBD	Call TI	Call TI	-55 to 125	LF411MWG RLQMLV Q 5962R11222 01VZA ACO 01VZA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

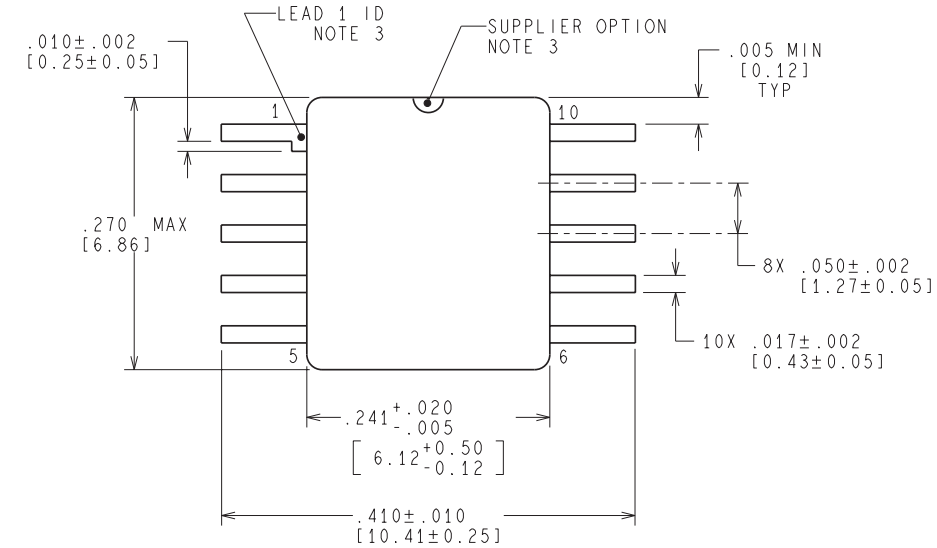
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

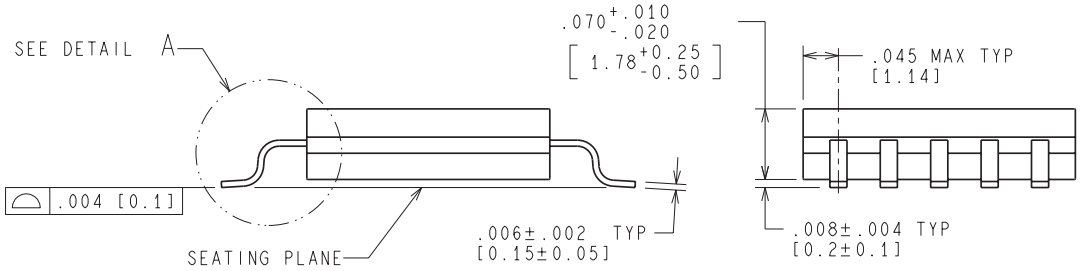
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

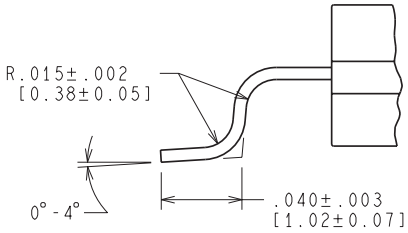
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NAC0010A







DETAIL A
TYPICAL

MIL-PRF-38535
CONFIGURATION CONTROL

WG10A (Rev H)

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