VIPer53EDIP - E
VIPer53ESP - E

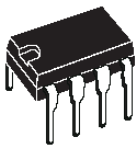
OFF-line Primary Switch

Features

- Switching frequency up to 300kHz
- Current mode control with adjustable limitation
- Soft start and shut-down control
- Automatic burst mode in standby condition ("Blue Angel" compliant)
- Undervoltage lockout with Hysteresis
- Integrated start-up current source
- Over-temperature protection
- Overload and short-circuit control
- Overvoltage protection
- In compliance with the 2002/95/EC European Directive



PowerSO-10



DIP-8

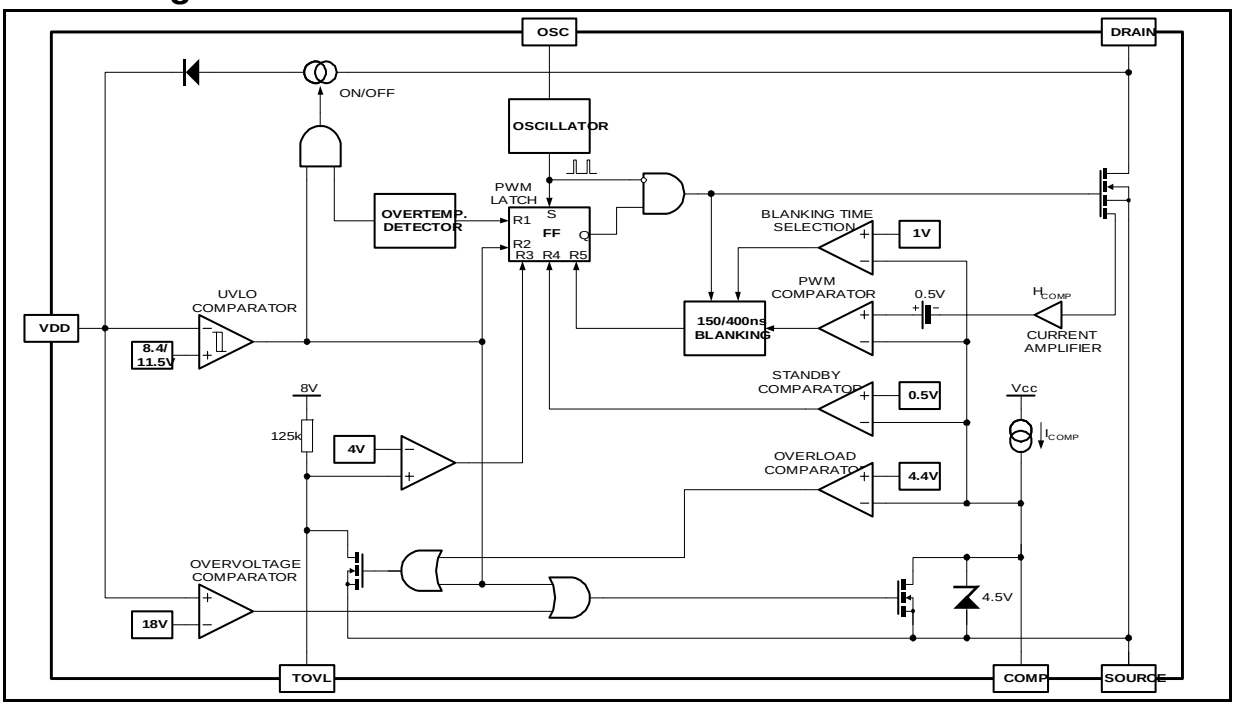
Description

The VIPer53E combines an enhanced current mode PWM controller with a high voltage MDMesh Power MOSFET in the same package.

Typical applications cover offline power supplies with a secondary power capability ranging up to 30W in wide range input voltage, or 50W in single European voltage range and DIP-8 package and 40W in wide range input voltage, or 65W in single European voltage range and PowerSO-10 package, with the following benefits:

- Overload and short-circuit events controlled by feedback monitoring and delayed device reset;
- Efficient standby mode by enhanced pulse skipping.
- Integrated start-up current source is disabled during normal operation to reduce the input power.

Block diagram



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1 Electrical data

1.1 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{DS}	Continuous Drain Source Voltage (T_J= 25 ... 125°C) (1)	-0.3 ... 620	V
I_D	Continuous Drain Current	Internally limited	A
V_{DD}	Supply Voltage	0 ... 19	V
V_{OSC}	OSC Input Voltage Range	0 ... V_{DD}	V
I_{COMP} I_{TOVL}	COMP and TOVL Input Current Range (1)	-2 ... 2	mA
V_{ESD}	Electrostatic Discharge: Machine Model (R = 0Ω; C = 200pF) Charged Device Model	 200 1.5	 V kV
T_J	Junction Operating Temperature	Internally limited	°C
T_C	Case Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	°C

1. In order to improve the ruggedness of the device versus eventual drain overvoltages, a resistance of 1kΩ should be inserted in series with the TOVL pin.\

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter		PowerSO-10 (1)	DIP-8 (2)	Unit
R_{thJC}	Thermal Resistance Junction-case	Max	2	20	°C/W
R_{thJA}	Thermal Resistance Ambient-case	Max	60	80	°C/W

1. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 mm thick) connected to the DRAIN pin.
2. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 mm thick) connected to the device tab.

2 Electrical characteristics

T_J = 25°C, V_{DD} = 13V, unless otherwise specified

Table 3. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Voltage	I_D = 1mA; V_{COMP} = 0V	620			V
I_{DSS}	Off State Drain Current	V_{DS} = 500V; V_{COMP} = 0V; T_j = 125°C			150	µA
$R_{DS(on)}$	Static Drain-Source On State Resistance	I_D = 1A; V_{COMP} = 4.5V; V_{TOVL} = 0V T_J = 25°C T_J = 100°C		0.9	1 1.7	Ω Ω
t_{fv}	Fall Time	I_D = 0.2A; V_{IN} = 300V (1)		100		ns
t_{rv}	Rise Time	I_D = 1A; V_{IN} = 300V (1)		50		ns
C_{oss}	Drain Capacitance	V_{DS} = 25V		170		pF
C_{Eon}	Effective Output Capacitance	200V < V_{DSon} < 400V (2)		60		pF

1. On clamped inductive load
2. This parameter can be used to compute the energy dissipated at turn on E_{ton} according to the initial drain to source voltage V_{DSon} and the following formula:

$$E_{ton} = \frac{1}{2} \cdot C_{Eon} \cdot 300^2 \cdot \left(\frac{V_{DSon}}{300}\right)^{1.5}$$

Table 4. Oscillator Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{OSC1}	Oscillator Frequency Initial Accuracy	R_T = 8kΩ; C_T = 2.2nF *Figure 15 on page 23*	95	100	105	kHz
F_{OSC2}	Oscillator Frequency Total Variation	R_T = 8kΩ; C_T = 2.2nF *Figure 17 on page 24* V_{DD} = V_{DDon} ... V_{DDovp}; T_J = 0 ... 100°C	93	100	107	kHz
V_{OSChi}	Oscillator Peak Voltage			9		V
V_{OSClo}	Oscillator Valley Voltage			4		V

Table 5. Supply Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DSstart}$	Drain Voltage Starting Threshold	V_{DD} = 5V; I_{DD} = 0mA		34	50	V
I_{DDch1}	Startup Charging Current	V_{DD} = 0 ... 5V; V_{DS} = 100V *Figure 9 on page 22*		-12		mA
I_{DDch2}	Startup Charging Current	V_{DD} = 10V; V_{DS} = 100V *Figure 9.*		-2		mA
$I_{DDchoff}$	Startup Charging Current in Thermal Shutdown	V_{DD} = 5V; V_{DS} = 100V *Figure 11.* $T_J > T_{SD} - T_{HYST}$	0			mA
I_{DD0}	Operating Supply Current Not Switching	F_{sw} = 0kHz; V_{COMP} = 0V		8	11	mA
I_{DD1}	Operating Supply Current Switching	F_{sw}=100kHz		9		mA
V_{DDoff}	V_{DD} Undervoltage Shutdown Threshold	*Figure 9 on page 22*	7.5	8.4	9.3	V
V_{DDon}	V_{DD} Startup Threshold	*Figure 9.*	10.2	11.5	12.8	V
V_{DDhyst}	V_{DD} Threshold Hysteresis	*Figure 9.*	2.6	3.1		V
V_{DDovp}	V_{DD} Overvoltage Shutdown Threshold	*Figure 9.*	17	18	19	V

Table 6. Pwm Comparator Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
H_{COMP}	ΔV_{COMP} / ΔI_{DPEAK}	V_{COMP} = 1 ... 4 V *Figure 14.* dI_D/dt = 0	1.7	2	2.3	V/A
V_{COMPos}	V_{COMP} Offset	dI_D/dt = 0 *Figure 14.*		0.5		V
I_{Dlim}	Peak Drain Current Limitation	I_{COMP} = 0mA; V_{TOVL} = 0V *Figure 14.* dI_D/dt = 0	1.7	2	2.3	A
I_{Dmax}	Drain Current Capability	V_{COMP} = $V_{COMPovl}$; V_{TOVL} = 0V dI_D/dt = 0	1.6	1.9	2.3	A
t_d	Current Sense Delay to Turn-Off	I_D = 1A		250		ns
V_{COMPbl}	V_{COMP} Blanking Time Change Threshold	*Figure 10 on page 22*		1		V
t_{b1}	Blanking Time	V_{COMP} < V_{COMPBL} *Figure 10.*	300	400	500	ns
t_{b2}	Blanking Time	V_{COMP} > V_{COMPBL} *Figure 10.*	100	150	200	ns
t_{ONmin1}	Minimum On Time	V_{COMP} < V_{COMPBL}	450	600	750	ns

Table 6. Pwm Comparator Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{ONmin2}	Minimum On Time	$V_{COMP} > V_{COMPBL}$	250	350	450	ns
$V_{COMPoff}$	V_{COMP} Shutdown Threshold	*Figure 13 on page 23*		0.5		V
V_{COMPhi}	V_{COMP} High Level	I_{COMP}=0mA (1)		4.5		V
I_{COMP}	COMP Pull Up Current	V_{COMP}= 2.5V		0.6		mA

1. In order to ensure a correct stability of the internal current source, a 10nF capacitor (minimum value 8nF) should always be present on the COMP pin.

Table 7. Overload Protection Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{COMPovl}$	V_{COMP} Overload Threshold	I_{TOVL} = 0mA *Figure 7 on page 20* (1)		4.35		V
$V_{DIFFovl}$	V_{COMPhi} to $V_{COMPovl}$ Voltage Difference	$V_{DD} = V_{DDoff} \ldots V_{DDreg}$; I_{TOVL}= 0mA *Figure 7.* (1)	50	150	250	mV
V_{OVLth}	V_{TOVL} Overload Threshold	*Figure 7.*		4		V
t_{OVL}	Overload Delay	C_{OVL} = 100nF *Figure 7.*		8		ms

1. $V_{COMPovl}$ is always lower than V_{COMPhi}

Table 8. Over temperature Protection Section

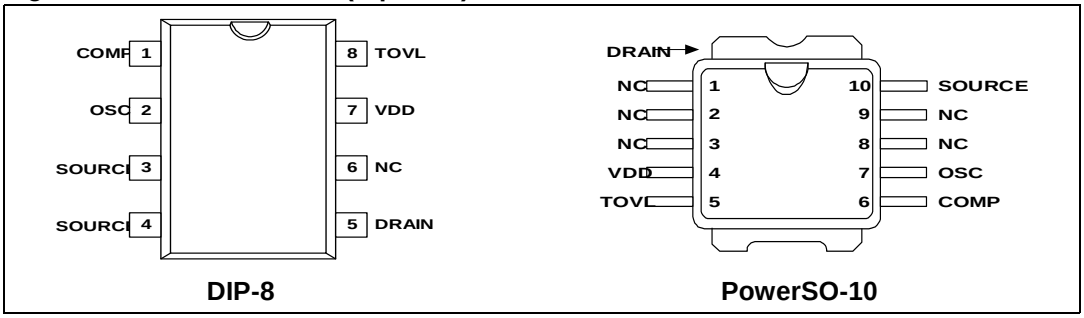
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{SD}	Thermal Shutdown Temperature	*Figure 11 on page 22*	140	160		°C
T_{HYST}	Thermal Shutdown Hysteresis	*Figure 11 on page 22*		40		°C

Table 9. Typical Output Power Capability

Type	European (195 - 265Vac)	US / Wide range (85 - 265Vac)
VIPer53EDIP-E	50W	30W
VIPer53ESP-E	65W	40W

3 Pin connections and function

Figure 1. Pin connection (top view)



DIP-8 PowerSO-10

Figure 2. Current and voltage conventions

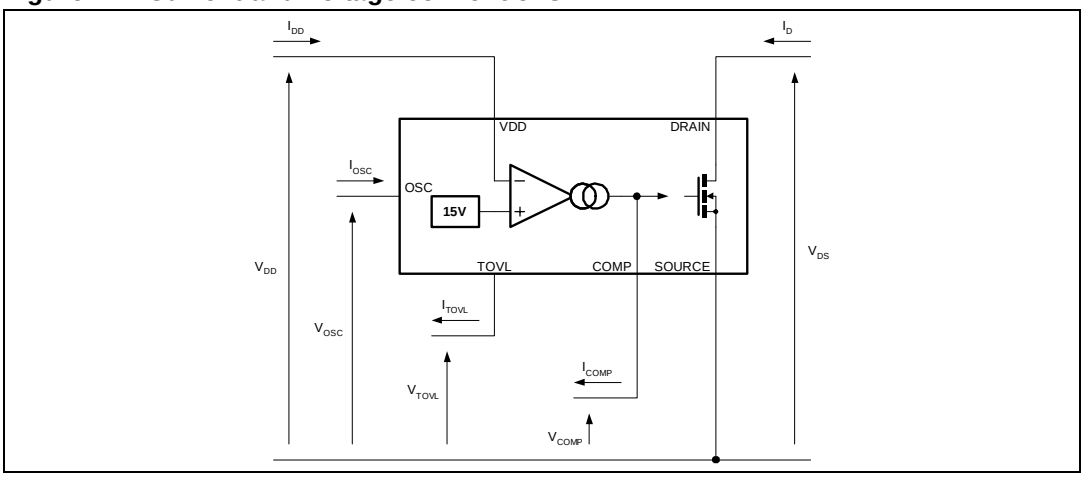
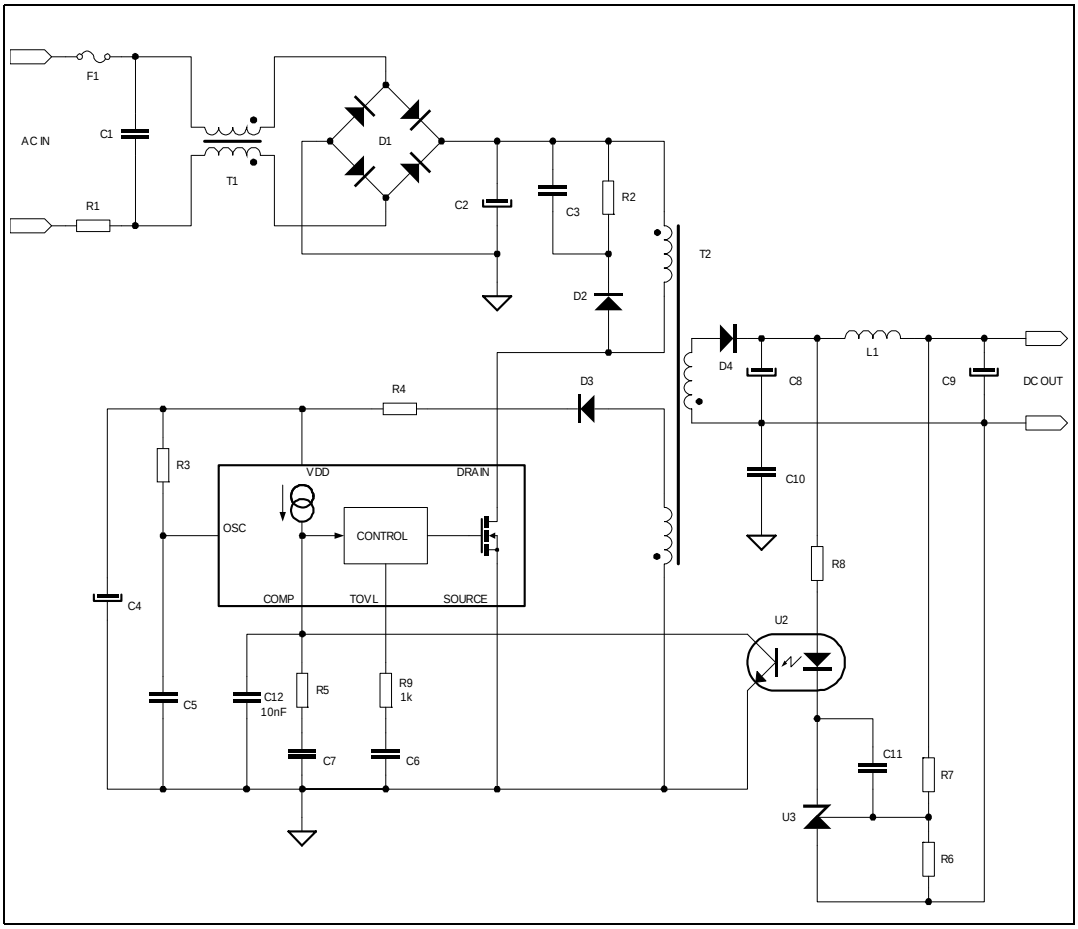


Table 10. Pin function

Pin Name	Pin Function
V_{DD}	Power supply of the control circuits. Also provides the charging current of the external capacitor during start-up. The functions of this pin are managed by four threshold voltages: - VDDon: Voltage value at which the device starts switching (Typically 11.5 V). - VDDoff: Voltage value at which the device stops switching (Typically 8.4 V). - VDDovp: Triggering voltage of the overvoltage protection (Trimmed to 18 V).
SOURCE	Power MOSFET source and circuit ground reference.
DRAIN	Power MOSFET drain. Also used by the internal high voltage current source during the start-up phase, to charge the external V_{DD} capacitor.
COMP	Allows the setting of the dynamic characteristic of the converter through an external passive network. The useful voltage range extends from 0.5V to 4.5V. The Power MOSFET is always off below 0.5V, and the overload protection is triggered if the voltage exceeds 4.35V. This action is delayed by the timing capacitor connected to the TOVL pin.
TOVL	Allows the connection of an external capacitor for delaying the overload protection, which is triggered by a voltage on the COMP pin higher than 4.4V.
OSC	Allows the setting of the switching frequency through an external Rt-Ct network.

4 Rectangular U-I Output characteristics

Figure 3. Off Line Power Supply With Optocoupler Feedback



5 Secondary Feedback Configuration Example

The secondary feedback is implemented through an optocoupler driven by a programmable zener diode (TL431 type) as shown in *Figure 3 on page 8*

The optocoupler is connected in parallel with the compensation network on the COMP pin which delivers a constant biasing current of 0.6mA to the optotransistor. This current does not depend on the compensation voltage, and so it does not depend on the output load either. Consequently, the gain of the optocoupler ensures a constant biasing of the TL431 device (U3), which is responsible for secondary regulation. If the optocoupler gain is sufficiently low, no additional components are required to a minimum current biasing of U3. Additionally, the low biasing current protects the optocoupler from premature failure.

The constant current biasing can be used to simplify the secondary circuit: instead of a TL431, a simple zener and resistance network in series with the optocoupler diode can insure a good secondary regulation. Current flowing in this branch remains constant just as it does by using a TL431, so typical load regulation of 1% can be achieved from zero to full output current with this simple configuration.

Since the dynamic characteristics of the converter are set on the secondary side through components associated to U3, the compensation network has only a role of gain stabilization for the optocoupler, and its value can be freely chosen. R5 can be set to a fixed value of 2.2kΩ, offering the possibility of using C7 as a soft start capacitor: When starting up the converter, the VIPer53E device delivers a constant current of 0.6mA on the COMP pin, creating a constant voltage of 1.3V in R5 and a rising slope across C7. This voltage shape, together with the operating range of 0.5V to 4.5V provides a soft startup of the converter. The rising speed of the output voltage can be set through the value of C7. The C4 and C6 values must be adjusted accordingly in order to ensure a correct startup.

6 Current Mode Topology

The VIPer53E implements the conventional current mode control method for regulating the output voltage. This kind of feedback includes two nested regulation loops:

The inner loop controls the peak primary current cycle by cycle. When the Power MOSFET output transistor is on, the inductor current (primary side of the transformer) is monitored with a SenseFET technique and converted into a voltage. When Vs reaches V_{COMP}, the power switch is turned off. This structure is completely integrated as shown on the Block Diagram of *Figure on page 1*, with the current amplifier, the PWM comparator, the blanking time function and the PWM latch. The following formula gives the peak current in the Power MOSFET according to the compensation voltage:

$$I_{Dpeak} = \frac{V_{COMP} - V_{COMPos}}{H_{COMP}}$$

The outer loop defines the level at which the inner loop regulates peak current in the power switch. For this purpose, V_{COMP} is driven by the feedback network (TL431 through an optocoupler in secondary feedback configuration, see *Figure 3 on page 8*) and is sets accordingly the peak drain current for each switching cycle.

As the inner loop regulates the peak primary current in the primary side of the transformer, all input voltage changes are compensated for before impacting the output voltage. This results in an improved line regulation, instantaneous correction to line changes, and better stability for the voltage regulation loop.

Current mode topology also provides a good converter start-up control. The compensation voltage can be controlled to increase slowly during the start-up phase, so the peak primary current will follow this soft voltage slope to provide a smooth output voltage rise, without any overshoot. The simpler voltage mode structure which only controls the duty cycle, leads generally to high current at start-up with the risk of transformer saturation.

An integrated blanking filter inhibits the PWM comparator output for a short time after the integrated Power MOSFET is switched on. This function prevents anomalous or premature termination of the switching pulse in the case of current spikes caused by primary side transformer capacitance or secondary side rectifier reverse recovery time when working in continuous mode.

7 Standby Mode

The device offers a special feature to address the low load condition. The corresponding function described hereafter consists of reducing the switching frequency by going into burst mode, with the following benefits:

– It reduces the switching losses, thus providing low consumption on the mains lines. The device is compliant with “Blue Angel” and other similar standards, requiring less than 0.5 W of input power when in standby.
– It allows the regulation of the output voltage, even if the load corresponds to a duty cycle that the device is not able to generate because of the internal blanking time, and associated minimum turn on.

For this purpose, a comparator monitores the COMP pin voltage, and maintains the PWM latch and the Power MOSFET in the Off state as long as V_{COMP} remains below 0.5V (See Block Diagram on page 2). If the output load requires a duty cycle below the one defined by the minimum turn on of the device, the V_{COMP} net decreases its voltage until it reaches this 0.5V threshold ($V_{COMPoff}$). The Power MOSFET can be completely Off for some cycles, and resumes normal operation as soon as V_{COMP} is higher than 0.5V. The output voltage is regulated in burst mode. The corresponding ripple is not higher than the nominal one at full load.

In addition, the minimum turn on time which defines the frontier between normal operation and burst mode changes according to V_{COMP} value. Below 1.0V (V_{COMPbl}), the blanking time increases to 400ns, whereas for higher voltages, it is 150ns *Figure 10 on page 22* The minimum turn on times resulting from these values are respectively 600 ns and 350 ns, when taking into account internal propagation time. This brutal change induces an hysteresis between normal operation and burst mode as shown on *Figure 10 on page 22*

When the output power decreases, the system reaches point 2 where V_{COMP} equals V_{COMPbl}. The minimum turn-on time passes immediately from 350ns to 600ns, exceeding the effective turn-on time that should be needed at this output power level. Therefore the regulation loop will quickly drive V_{COMP} to $V_{COMPoff}$ (Point 3) in order to pass into burst mode and to control the output voltage. The corresponding hysteresis can be seen on the switching frequency which passes from F_{SWnom} which is the normal switching frequency set by the components connected to the OSC pin and to FSWstby. Note: This frequency is actually an equivalent number of switching pulses per second, rather than a fixed switching frequency since the device is working in burst mode.

As long as the power remains below P_{RST} the output of the regulation loop remains stuck at V_{COMPsd} and the converter works in burst mode. Its “density” increases (i.e. the number of missing cycles decreases) as the power approaches P_{RST} and finally resumes normal operation at point 1. The hysteresis cannot be seen on the switching frequency, but it can be seen in the sudden surge of the COMP pin voltage from point 3 to point 1 at that power level.

The power points value P_{RST} and P_{STBY} are defined by the following formulas:

$$P_{RST} = \frac{1}{2} \bullet F_{SWnom} \bullet (tb_1 + td)^2 \bullet V^2IN \bullet \frac{1}{Lp}$$

$$P_{STBY} = \frac{1}{2} \bullet F_{SWnom} \bullet Ip^2(V_{COMPbl}) \bullet Lp$$

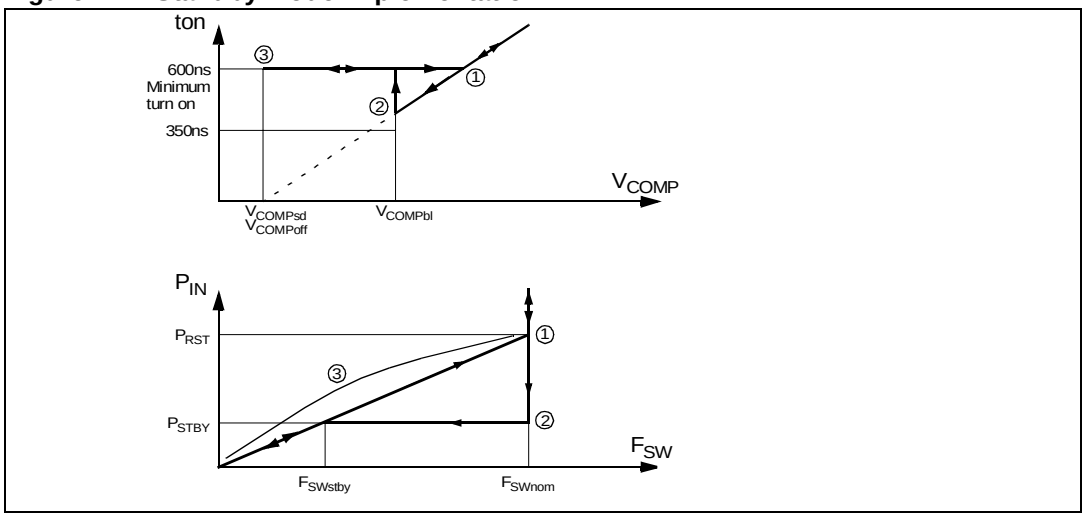
Where Ip($V_{COMPbl2}$) is the peak Power MOSFET current corresponding to a compensation voltage of V_{COMPbl} (1V). Note: The power point PSTBY where the converter is going into burst mode does not depend on the input voltage.

The standby frequency F_{SWstby} is given by:

$$P_{SWstby} = \frac{P_{STBY}}{P_{RST}} \bullet F_{SWnom}$$

The ratio between the nominal and standby switching frequencies can be as high as 4, depending on the Lp value and input voltage.

Figure 4. .Standby Mode Implementation



8 High Voltage Start-up Current Source

An integrated high voltage current source provides a bias current from the DRAIN pin during the start-up phase. This current is partially absorbed by internal control circuits in standby mode with reduced consumption, and also supplies the external capacitor connected to the V_{DD} pin. As soon as the voltage on this pin reaches the high voltage threshold V_{DDon} of the UVLO logic, the device turns into active mode and starts switching. The start-up current generator is switched off, and the converter should normally provide the needed current on the V_{DD} pin through the auxiliary winding of the transformer, as shown on *Figure 3 on page 8*.

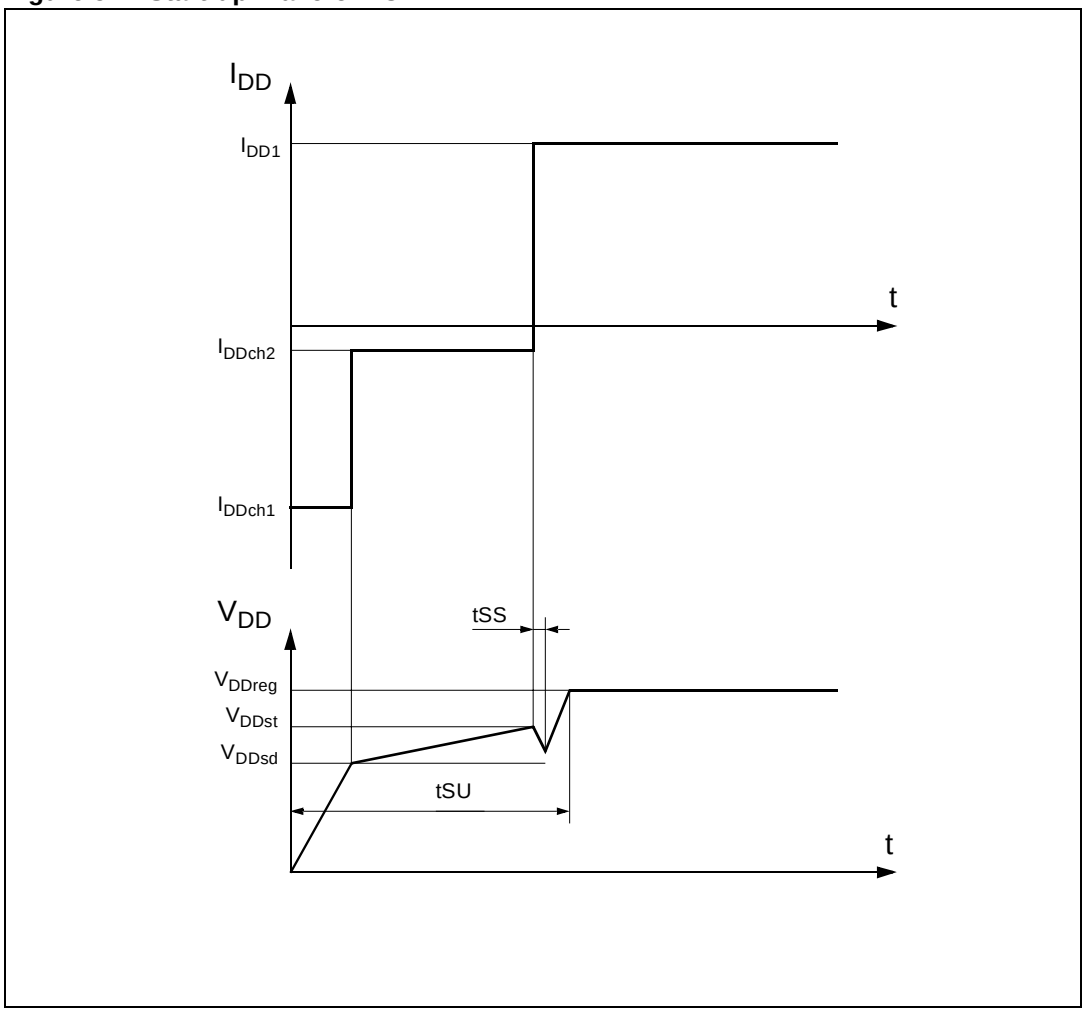
The external capacitor C_{VDD} on the V_{DD} pin must be sized according to the time needed by the converter to start-up, when the device starts switching. This time tss depends on many parameters, including transformer design, output capacitors, soft start feature, and compensation network implemented on the COMP pin and possible secondary feedback circuit. The following formula can be used for defining the minimum capacitor needed:

$$C_{VDD} > \frac{I_{DD1} \cdot tss}{V_{DDhyst}}$$

Figure 9 on page 22 shows a typical start-up event. V_{DD} starts from 0V with a charging current I_{DDch1} at about 9 mA. When about V_{DDoff} is reached, the charging current is reduced down to I_{DDch2} which is about 0.6mA. This lower current leads to a slope change on the V_{DD} rise. Device starts switching for V_{DD} equal to V_{DDon}, and the auxiliary winding delivers some energy to V_{DD} capacitor after the start-up time tss.

The charging current change at V_{DDoff} allows a fast complete start-up time t_{SDU}, and maintains a low restart duty cycle. This is especially useful for short circuits and overloads conditions, as described in the following section.

Figure 5. Start-up Waveforms



9 Short-Circuit and Overload Protection

A $V_{COMPovl}$ threshold of about 4.4V has been implemented on the COMP pin. When V_{COMP} goes above this level, the capacitor connected on the TOVL pin begins to charge. When reaching typically V_{OVLth} (4V), the internal MOSFET driver is disabled and the device stops switching. This state is latched because of to the regulation loop which maintains the COMP pin voltage above the $V_{COMPovl}$ threshold. Since the V_{DD} pin does not receive any more energy from the auxiliary winding, its voltage drops down until it reaches V_{DD}off and the device is reset, recharging the V_{DD} capacitor for a new restart cycle. Note: If VCOMP drops below the VCOMPovl threshold for any reason during the VDD drop, the device resumes switching immediately.

The device enters an endless restart sequence if the overload or short circuit condition is maintained. The restart duty cycle D_{RST} is defined as the time ratio for which the device tries to restart, thus delivering its full power capability to the output. In order to keep the whole converter in a safe state during this event, D_{RST} must be kept as low as possible, without compromising the real start-up of the converter. A typical value of about 10% is generally sufficient. For this purpose, both V_{DD} and TOVL capacitors can be used to satisfy the following conditions:

$$C_{OVL} > 12.5 \cdot 10^{-6} \cdot tss$$

$$C_{VDD} > 8 \cdot 10^{4} \cdot \left(\frac{1}{D_{RST}} - 1\right) \cdot \frac{C_{OVL} \cdot I_{DDch2}}{V_{DDhyst}}$$

Refer to the previous start-up section for the definition of tss, and C_{VDD} must also be checked against the limit given in this section. The maximum value of the two calculus will be adopted.

All this behavior can be observed on *Figure 2 on page 7*. In *Figure 7 on page 20* the value of the drain current Id for $V_{COMP} = V_{COMPovl}$ is shown. The corresponding parameter I_{Dmax} is the drain current to take into account for design purposes. Since I_{Dmax} represents the maximum value for which the overload protection is not triggered, it defines the power capability of the power supply.

10 Regulation Loop Stability

The complete converter open loop transfer function can be built from both power cell and the feedback network transfer functions. A theoretical example can be seen in *Figure 11 on page 22* for a discontinuous mode flyback loaded by a simple resistor.

A typical schematic corresponding to this situation can be seen on *Figure 3 on page 8*. The transfer function of the power cell is represented as G(s) in .*Figure 11 on page 22* It exhibits a pole which depends on the output load and on the output capacitor value. As the load of a converter may change, two curves are shown for two different values of output resistance value, R_{L1} and R_{L2}. A zero at higher frequency values then appears, due to the output capacitor ESR. Note: The overall transfer function does not depend on the input voltage because of the current mode control. A typical regulation loop is shown on *Figure 3 on page 8* and has a fixed behavior represented by F(s) on *Figure 11 on page 22*. A double zero due to the R_1-C_1 network on the COMP pin and to the integrator built around the TL431 and R_2-C_2 is set at the same value as the maximum load R_{L2} pole.

The total transfer function is shown as F(s). G(s) at the bottom of *Figure 11 on page 22*. For maximum load (plain line), the load pole begins exactly where the zeros of the COMP pin and the TL431 stop, and this results in a first order decreasing slope until it reaches the zero of the output capacitor ESR. The point where the complete transfer function has a unity gain is known as the regulation bandwidth and has a double interest:

- The higher it is, the faster the reaction will be to an eventual load change, and the smaller the output voltage change will be.
- The phase shift in the complete system at this point has to be less than 135° to ensure good stability. Generally, a first-order slope gives 90° of phase shift, and a second-order gives 180°.

In *Figure 3 on page 8*, the unity gain is reached in a first order slope, so the stability is ensured.

The dynamic load regulation is improved by increasing the regulation bandwidth, but some limitations have to be respected:

1. As the transfer function above zero due the ESR capacitor is not reliable (the ESR itself is not well specified, and other parasitic effects may take place), the bandwidth should always be lower than the minimum of FC and ESR zero
2. As the highest bandwidth is obtained with the highest output power (plain line with RL2 load in *Figure 3*, the above criteria will be checked for this condition and allows the value of R4 if R1 is set to a fixed value (e.g., (2.2kΩ).

As the highest bandwidth is obtained with the highest output power (Plain line with R_{L2} load in *Figure 3*), the above criteria will be checked for this condition and allows to define the value of R_4, if R1 is set fixed (2.2kΩ, for instance). The following formula can be derived:

$$R_4 = \sqrt{\frac{P_{MAX}}{P_{OUT2}}} \cdot \frac{G_O \cdot R_1}{F_{BW2} \cdot R_{L2} \cdot C_{OUT}}$$

with: $$P_{OUT2} = \frac{V_{OUT}^2}{R_{L2}}$$

and: $$P_{MAX} = \frac{1}{2} \cdot L_P \cdot I_{LIM}^2 \cdot F_{SW}$$

Go is the current transfer ratio of the optocoupler.

The lowest load gives another condition for stability: The frequency F_{BW1} must not encounter the third order slope generated by the load pole, the R1-C1 network on the COMP pin and the R2-C2 network at the level of the TL431 on secondary side. This condition can be met by adjusting both C_1 and C2 values:

$$C_1 > \frac{R_{L1} \cdot C_{OUT}}{6.3 \cdot \frac{G_O}{R_4} \cdot R_1^2} \cdot \sqrt{\frac{P_{OUT1}}{P_{MAX}}}$$

$$C_2 > \frac{R_{L1} \cdot C_{OUT}}{6.3 \cdot \frac{G_O}{R_4} \cdot R_1 \cdot R_2} \cdot \sqrt{\frac{P_{OUT1}}{P_{MAX}}}$$

with: $P_{OUT1} = \frac{V_{OUT}^2}{R_{L1}}$

The above formula gives a minimum value for C1. It can be then increased to provide a natural soft start function as this capacitor is charged by the current I_{COMP} at start-up.

11 Special Recommendations

10nF capacitor (minimum value: 8nF) should always be connected to the COMP pin to ensure correct stability of the internal current source *Figure 12 on page 22*.

In order to improve the ruggedness of the device versus eventual drain overvoltages, a resistance of 1kΩ should be inserted in series with the TOVL pin, as shown on *Figure 12 on page 22*

Note: This resistance does not impact the overload delay, as its value is negligible prior to the internal pull-up resistance (about 125kΩ).

12 Software Implementation

All the above considerations and some others are included included in ST design software which provides all of the needed components around the VIPer device for specified output configurations, and is available on www.st.com.

13 Operation pictures

Figure 6. Rise and Fall time

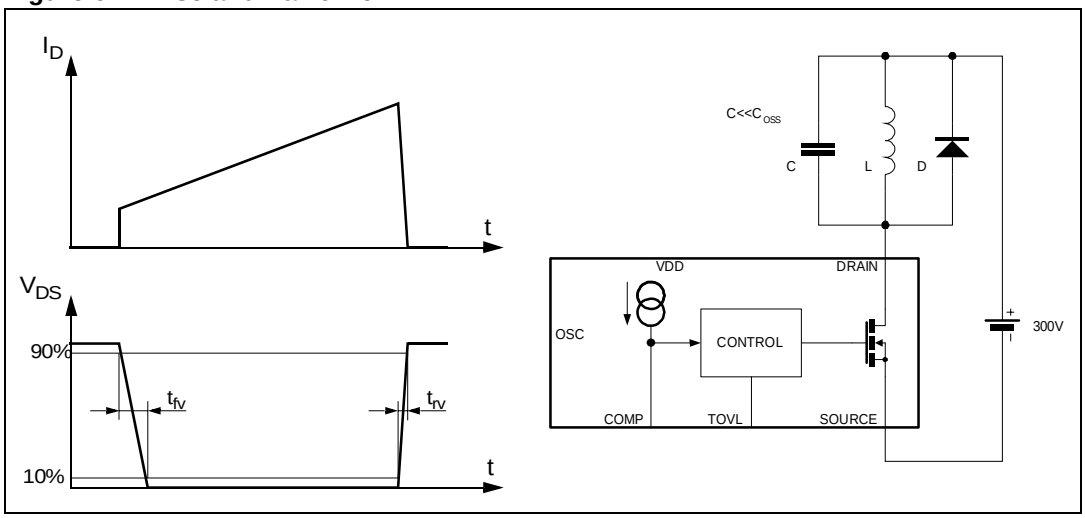


Figure 7. Overloaded Event

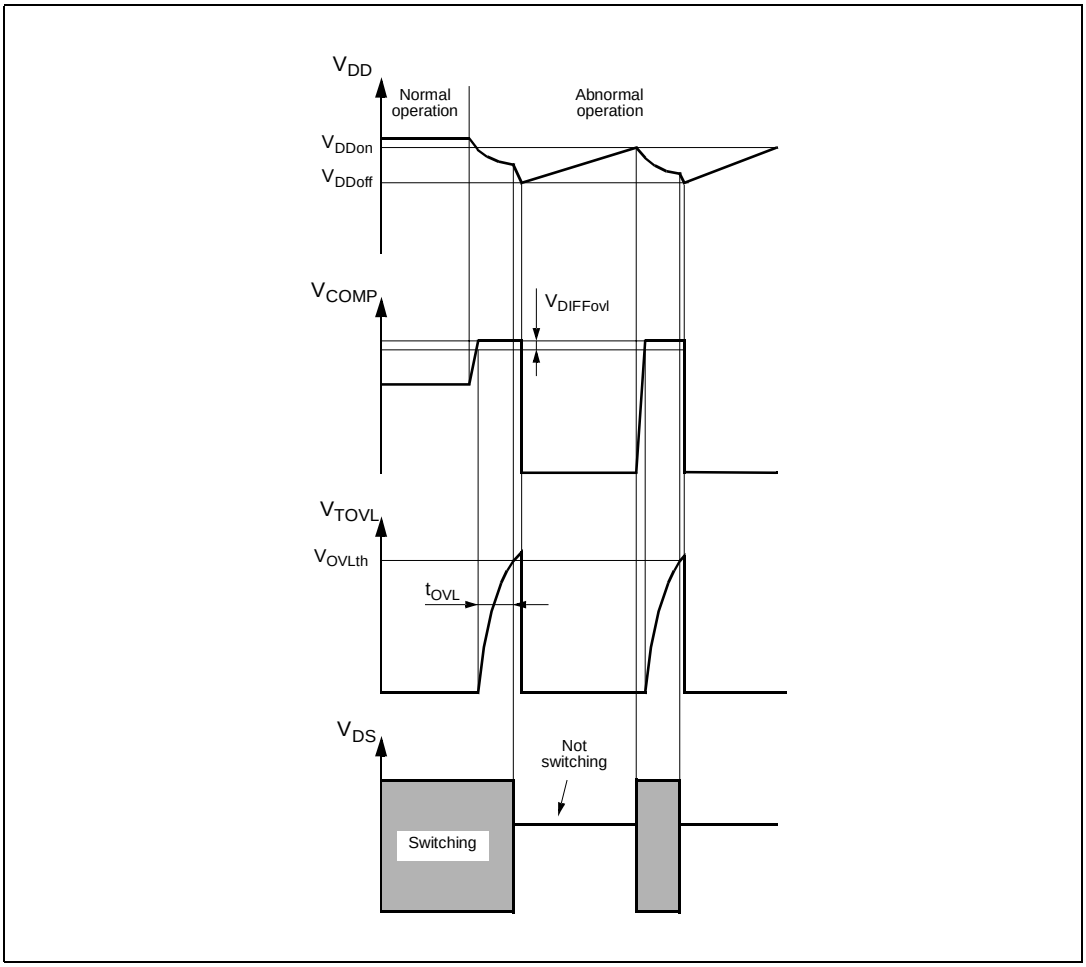


Figure 8. Complete Converter Transfer Function

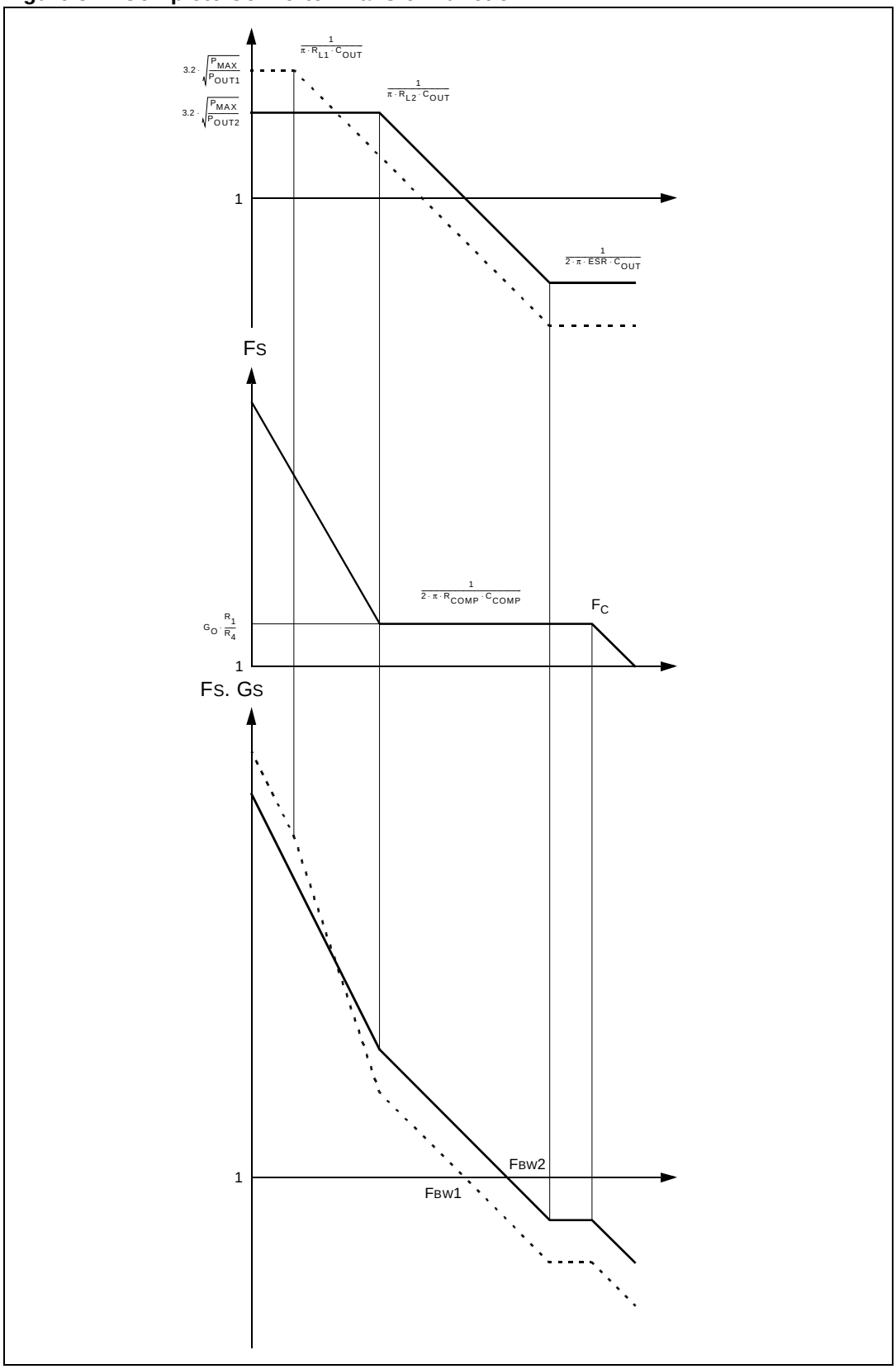


Figure 9. Start-up V_{DD} current

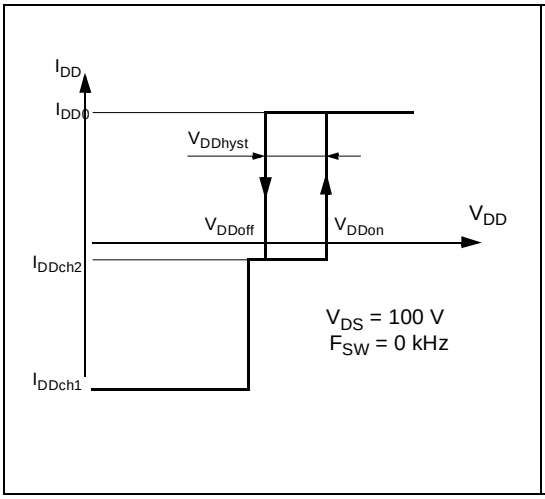


Figure 10. Blanking Time

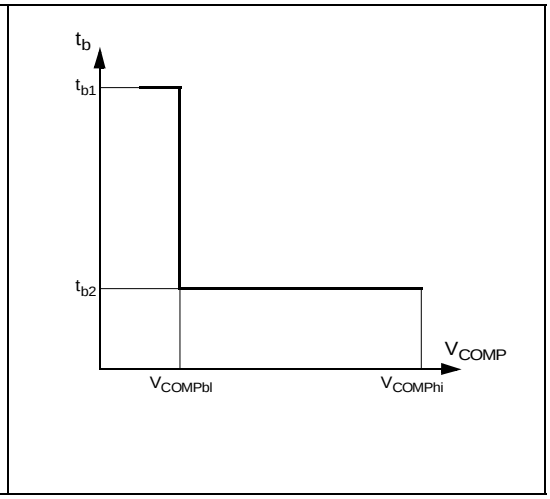


Figure 11. Thermal Shutdown

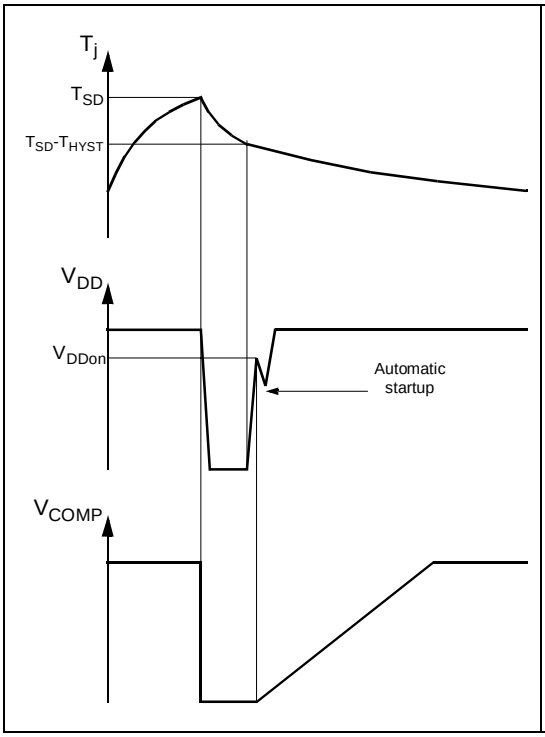


Figure 12. Overvoltage Event

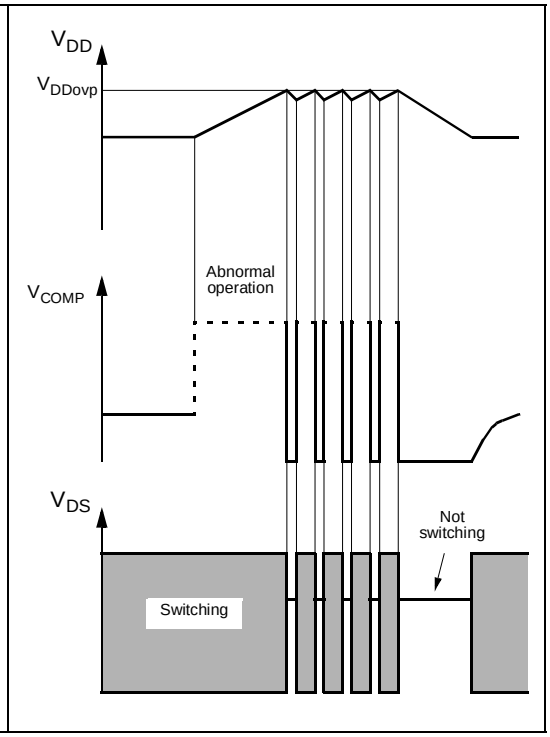


Figure 13. Shutdown Action

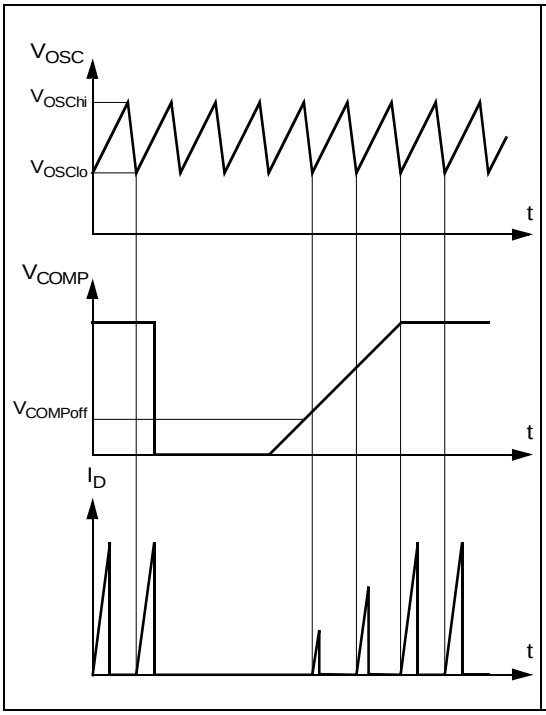


Figure 14. Comp Pin Gain and Offset

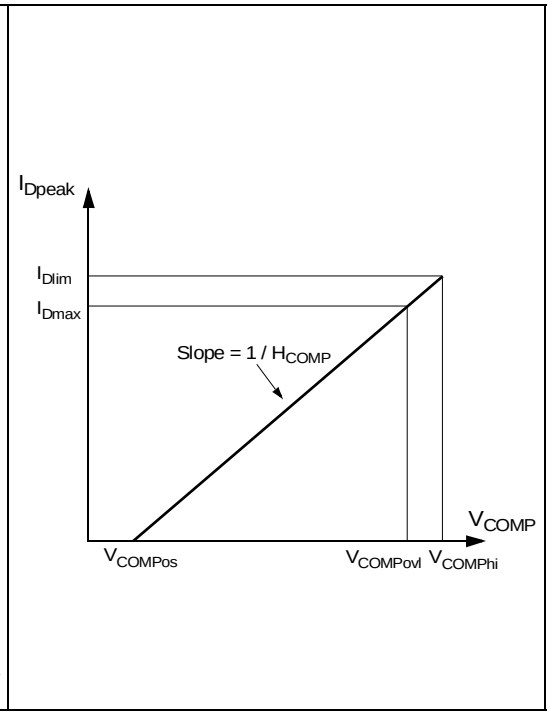
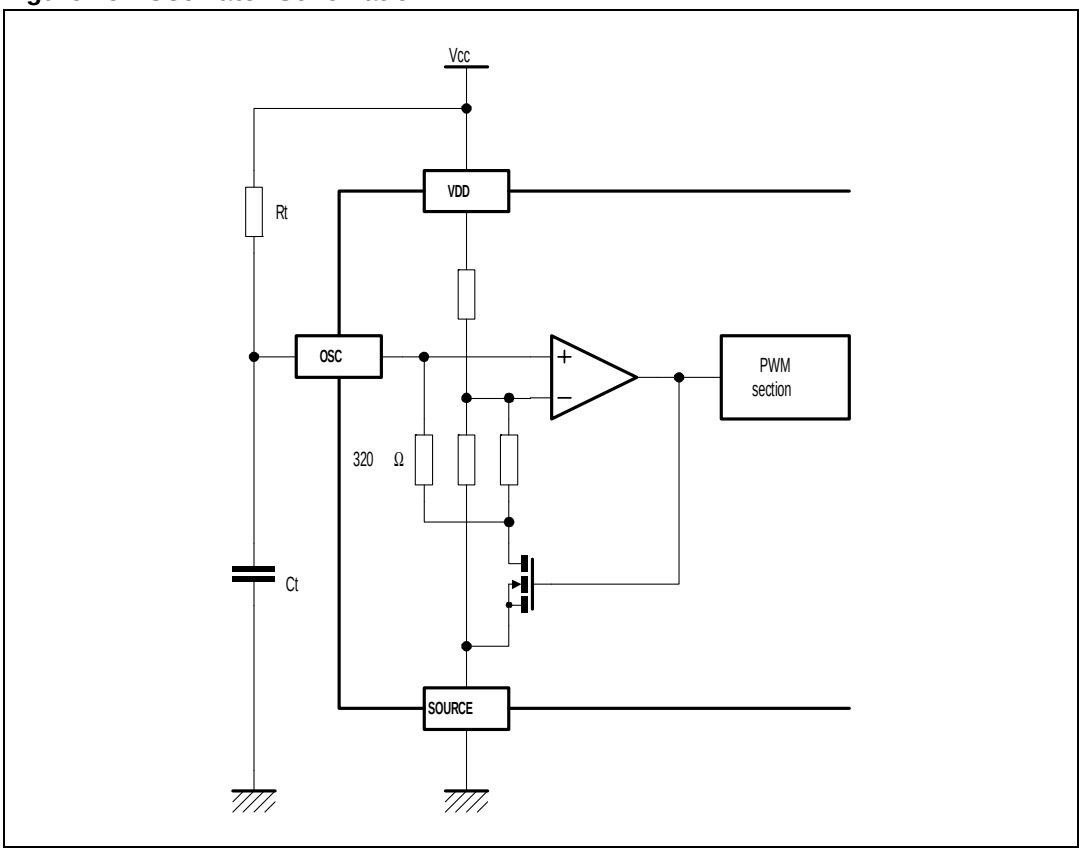


Figure 15. Oscillator Schematic



The switching frequency settings shown on the graphic here below is valid within the following boundaries:

$R_t > 2k\Omega$

$F_{SW} = 300kHz$

Figure 16. Oscillator Settings

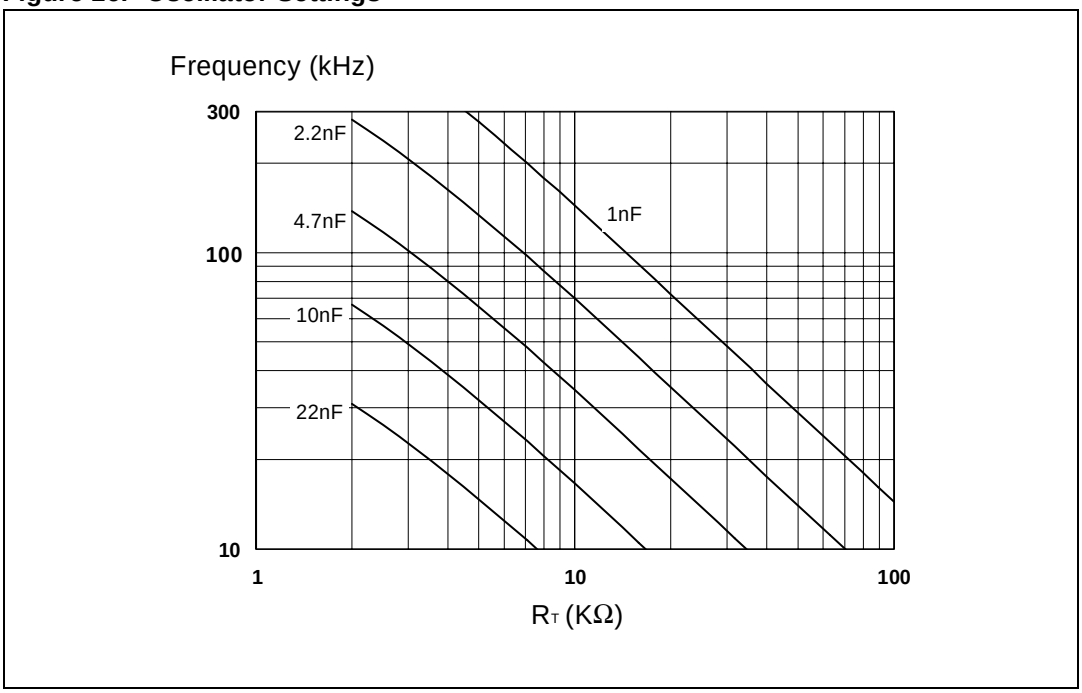


Figure 17. Typical Frequency Variation vs. Junction Temperature

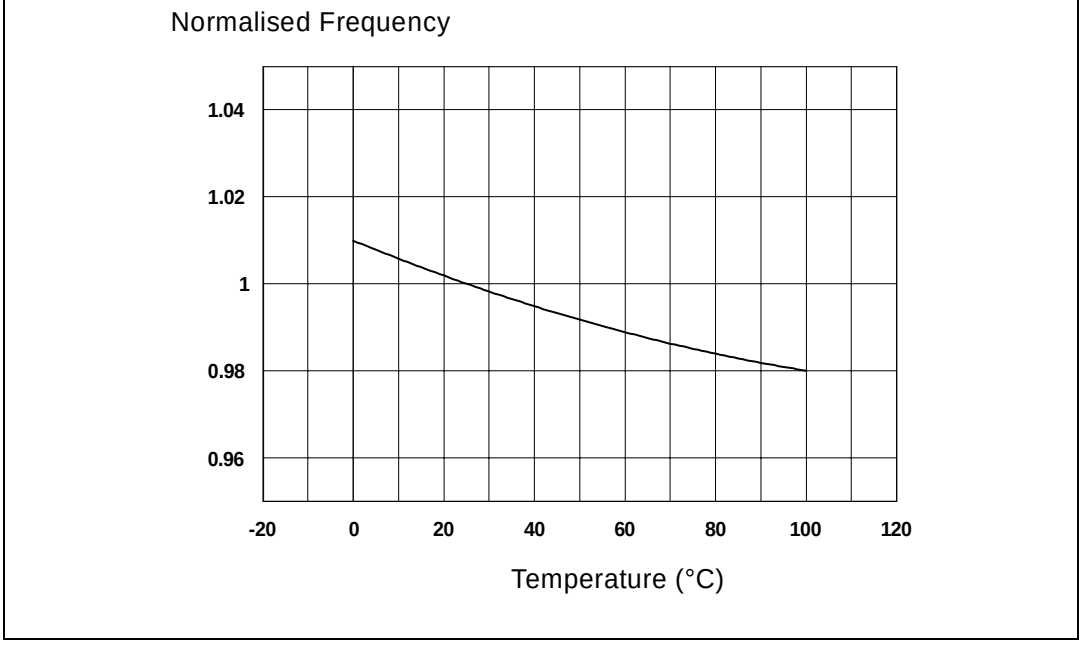
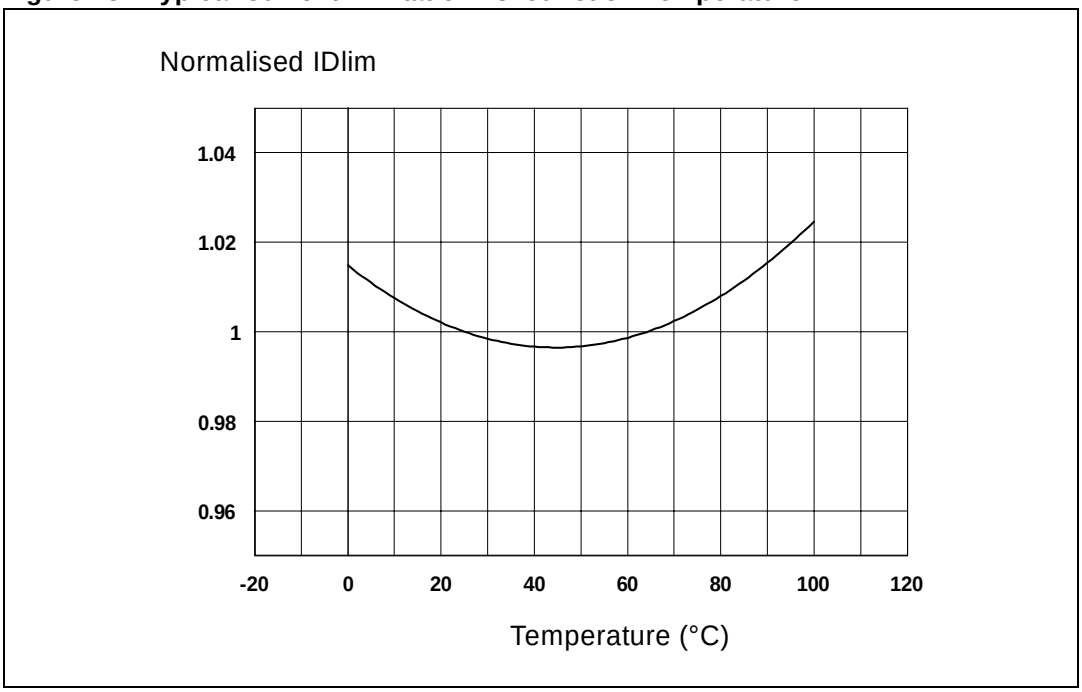


Figure 18. Typical Current Limitation vs. Junction Temperature



14 Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 11. DIP8 Mechanical Data

Dimensions			
Ref.	Databook (mm)		
	Nom.	Min	Max
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.26
E1	6.10	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81
Package Weight	Gr. 470		

Figure 19. Package Dimensions

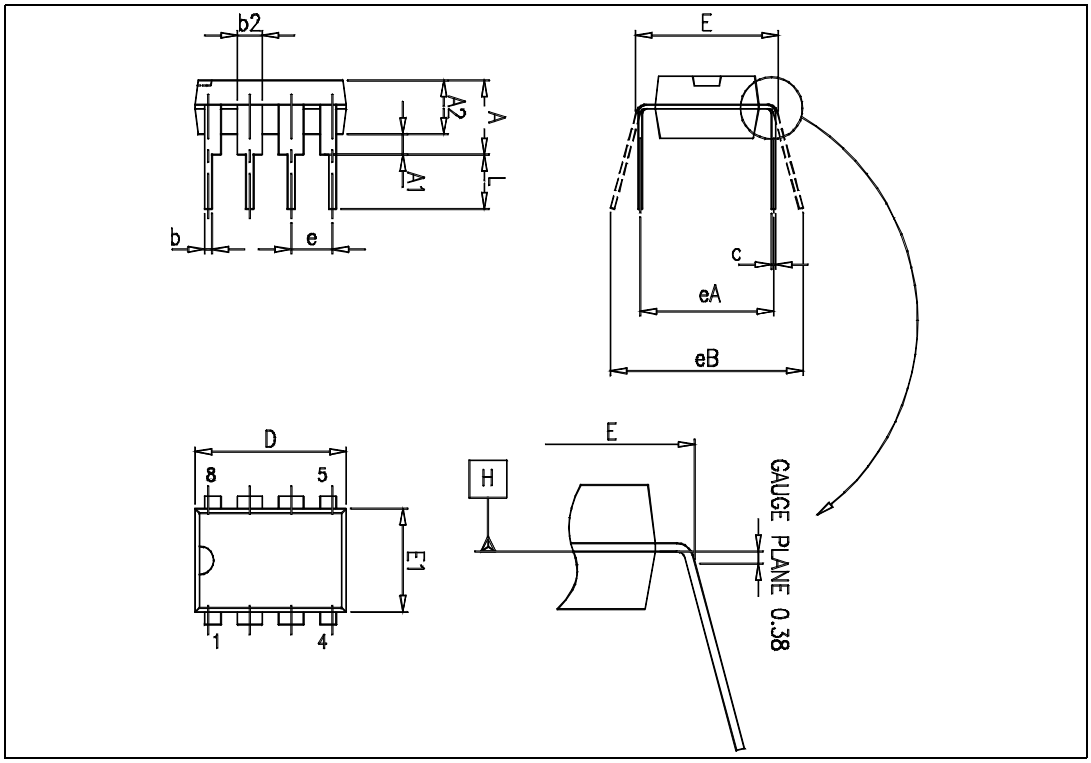
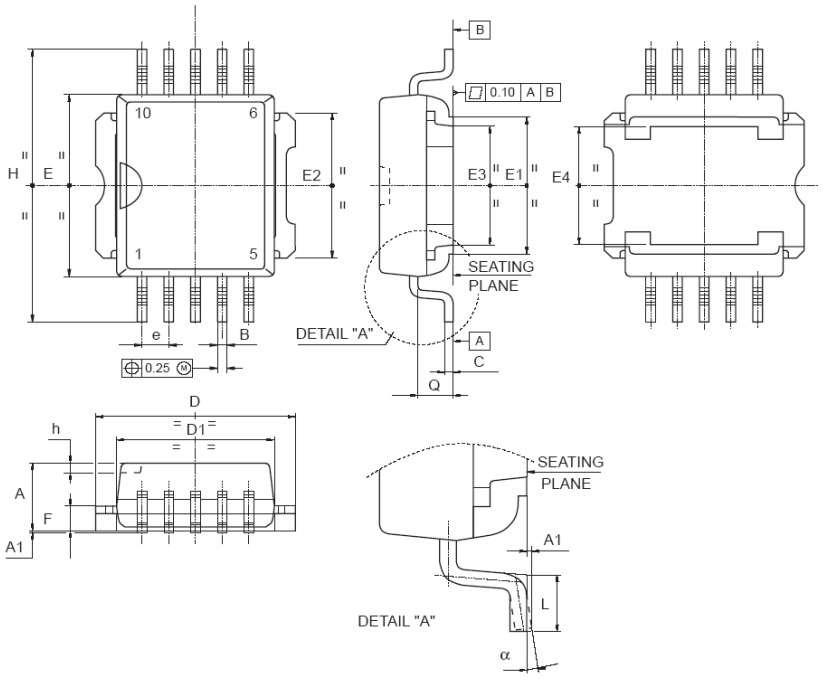


Table 12. PowerSO-10 Mechanical Data

Dimensions			
Ref.	Databook (mm)		
	Nom.	Min	Max
A	3.35		3.65
A1	0.00		0.10
B	0.40		0.60
c	0.35		0.55
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E1	7.20		7.40
E2	7.20		7.60
E3	6.10		6.35
E4	5.90		6.10
e		1.27	
F	1.25		1.35
H	13.80		14.40
h		0.50	
L	1.20		1.80
q		1.70	
α	0°		8°

Figure 20. Package Dimensions



15 Order codes

Table 13. Order codes

Part Number	Package	Shipment
VIPer53ESPTR - E	PowerSO-10	Tape and reel
VIPer53ESP - E	PowerSO-10	Tube
VIPer53EDIP - E	DIP-8	Tube

16 Revision history

Table 14. Document revision history

Date	Revision	Changes
12-Jan-2006	1	Initial release.

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