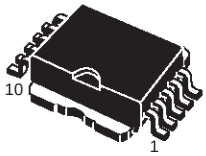
SGS-THOMSON MICROELECTRONICS

VIPer31SP

BATTERY CHARGER PRIMARY I.C.

ADVANCE DATA

TYPE	V_{DSS}	I_n	$R_{DS(on)}$
VIPer31SP	600 V	1 A	6.5 Ω



Power SO-10

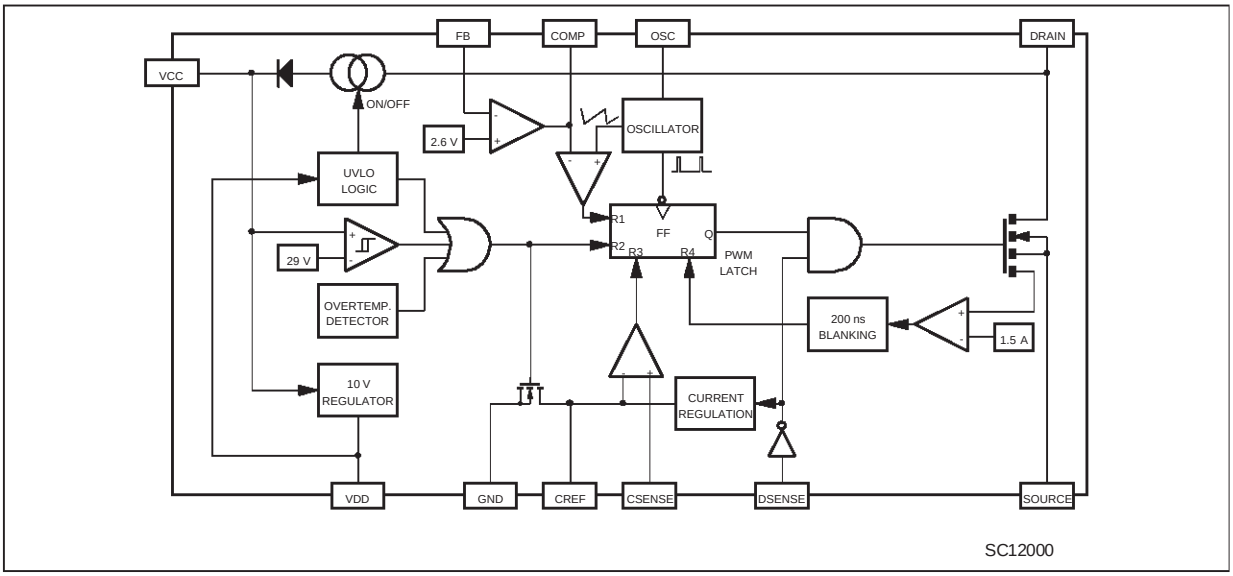
FEATURE

- RECTANGULAR CHARACTERISTIC, WITHOUT OPTOCOUPLER
- INTERNALLY TRIMMED CURRENT REFERENCE
- FIXED SWITCHING FREQUENCY, ADJUSTABLE UP TO 150 KHZ
- AUXILIARY VOLTAGE REGULATOR
- SOFT START AND SHUT DOWN CONTROL
- AUTOMATIC BURST MODE OPERATION IN STAND-BY CONDITION ABLE TO MEET "BLUE ANGEL" NORM (<1W TOTAL POWER CONSUMPTION)
- UNDERVOLTAGE LOCK-OUT WITH HYSTERESIS
- INTEGRATED START UP SUPPLY
- AVALANCHE RUGGED
- OVERVOLTAGE PROTECTION
- OVERTEMPERATURE PROTECTION
- CYCLE BY CYCLE CURRENT LIMITATION
- DEMAGNETISATION CONTROL

DESCRIPTION

VIPer31SP combines on the same silicon chip a PWM control dedicated to output current regulation together with an optimised high voltage avalanche rugged vertical power MOSFET (600V/1A). Typical applications cover battery chargers with constant current and constant voltage output characteristics, without any optocoupler between primary and secondary sections. Typical output power capability is 15 W in wide range condition and 30 W in single range or with doubler configuration. Burst mode operation is an additional feature of this device, offering the possibility to operate in no load condition with an input power as low as 1W. This feature insures the compliance towards "Blue Angel" norm and other similar ones.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

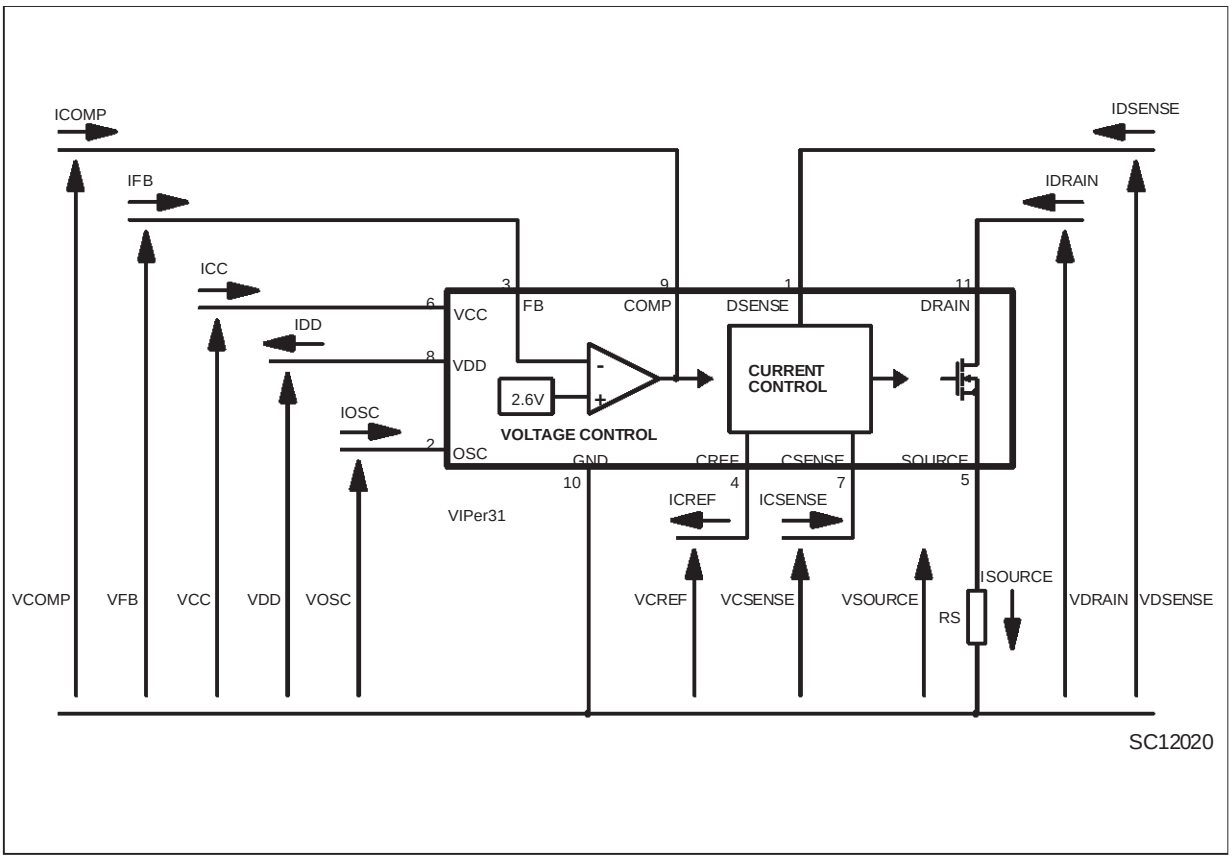
Symbol	Parameter	Value	Unit
V_{DS}	Continuous Drain-Source Voltage (Tj = 25 to 125°C)	600	V
I_D	Maximum DC Drain Current	Internally Limited	A
I_{DREV}	Reverse DC Drain Current	-2.5	A
V_{CC}	Supply Voltage	0 to 35	V
V_X	Voltage Range Input (CSENSE, COMP, FB, OSC, CREF)	-03 to V_{DD}	V
I_X	Current Input (CSENSE, COMP, FB, OSC, CREF	10	mA
I_{DSENSE}	Current Range Input (DSENSE)	-10 to +10	mA
V_{esd}	Electrostatic Discharge (R = 1.5 KΩ C = 100pF)	2000	V
$I_{D(AV)}$	Avalanche Drain-Source Current, Repetitive or Not-Repetitive (T_C = 100 °C, Pulse Width Limited by T_J max)	TBD	A
$E_{D(AV)}$	Avalanche Drain-Source Energy, Repetitive or Not-Repetitive (T_C = 25 °C, Pulse Width Limited by T_J max)	TBD	mJ
P_{tot}	Power Dissipation at T_C = 25°C	62	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-65 to 150	°C

THERMAL DATA

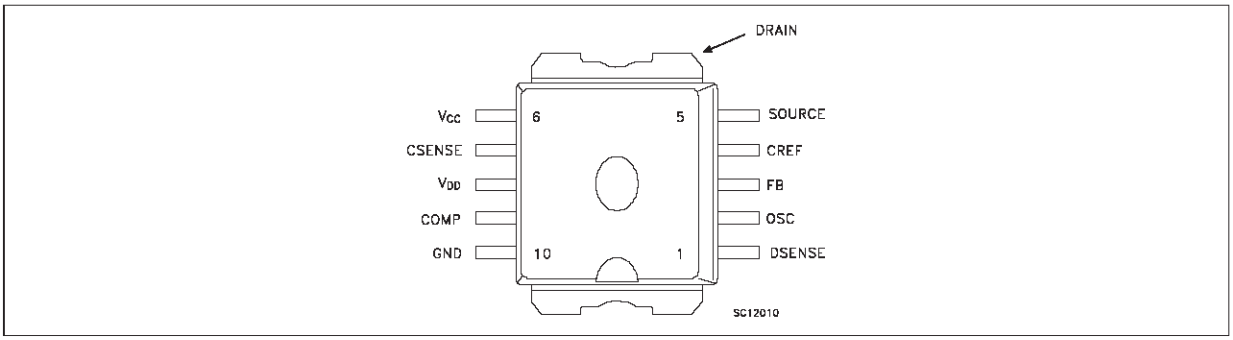
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.0	°C/W
$R_{thj\text{-}amb.}$	Thermal Resistance Junction-ambient (Note1)	Max	50	°C/W

Note 1 : This thermal resistance corresponds to the standard mounting on a FR4 type printed circuit board.

CURRENT AND VOLTAGE CONVENTIONS



CONNECTION DIAGRAMS (top View)



PINS FUNCTIONAL DESCRIPTION

DRAIN PIN:
Integrated power MOSFET drain pin. It provides internal bias current during start-up via an integrated high voltage current source which is switched off during normal operation. The device is able to handle an unclamped current during its normal operation, assuring self protection against voltage surges, PCB stray inductance, and allowing a snubberless operation for low output power.

SOURCE PIN:
Integrated power MOSFET source pin. To be connected to an external current sense resistance which defines the output current value.

GND
Used as the signal reference for all low level signals. To be connected to the cold point of the current sense resistance.

V_{DD} PIN:
It corresponds to the low voltage supply of the control part of the circuit. If Vdd goes below 6V, the circuit is shut down and the start-up current source is activated. The circuit resumes normal operation when the V_{DD} voltage reaches 8V. An internal low drop linear regulator generates the V_{DD} voltage from the V_{CC} one, thus limiting its value at 10V.

V_{CC} PIN:
This pin receives the auxiliary unregulated voltage from the main transformer, which can range from 7V up to 27V during normal operation. It delivers a start up current of 1.5mA during the shut down phase. The V_{CC} pin is also connected to an internal 10V low drop regulator which provides the V_{DD} voltage.

C_{SENSE} PIN:
Receives the voltage of the current sense resistor, representative from the power MOSFET drain current.

C_{REF} PIN:
Serves as a reference for the peak power MOSFET drain current. It is also the output of the curent regulation function, which adjusts this reference voltage to keep the average output current constant. To be connected to an external filtering capacitor.

D_{SENSE} PIN:
Detects the full demagnetisation of the main transformer, in order to drive the current regulation function. Refer to the application part for further details. It is also used to prevent any new turn on of the power MOSFET during the demagnetisation phase.

FB PIN:
This is the inverting input of the voltage mode error amplifier. This error amplifier is in charge of the limitation of the V_{CC} voltage when the output current is lower than the nominal regulated one.

COMP PIN:
This is the output of the voltage mode error amplifier. An external R-C network connected between this pin and the FB pin defines the bandwidth of the voltage regulation loop, and insures the stability of the converter.

OSC PIN:
An RT-CT network must be connected on that pin to define the switching frequency. Note that despite the connection of RT to V_{DD}, no significant frequency change occurs for V_{DD} varying from 7V to 10V. It provides also a synchronisation capability, when connected to an external frequency source.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, V_{CC} = 12 V, unless otherwise specified)

POWER SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Voltage	I_D = 1 mA V_{COMP} = 0 V	600			V
I_{DSS}	Off-State Drain Current	V_{DS} = 500 V V_{COMP} = 0 V			1	mA
$R_{DS(on)}$	Static Drain Source on Resistance	I_D = 0.3 A V_{SENSE} = 0 V T_J = 25 °C T_J = 100 °C			 6.5 10	 Ω Ω
t_f	Fall Time	ID = 0.3 A V_{in} = 300 V (1) (see fig. 1)		250		ns
t_r	Rise Time	I_D = 0.3 A V_{in} = 300 V (1) (see fig. 1)		TBD		ns
C_{OSS}	Output Capacitance	V_{DS} = 25 V		TBD		pF

(1) On Inductive Load, Clamped.

SUPPLY SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CCch}	Start-up Charging Current	V_{DD} = 0 to V_{DDon} V_{DS} = 250 V (see fig. 2)		-1.5		mA
I_{CC0}	Operating Supply Current	F_{SW} = 0 KHz (see fig. 2)		10		mA
I_{CC1}	Operating Supply Current	F_{SW} = 100 KHz		TBD		mA
I_{CC2}	Operating Supply Current	F_{SW} = 200 KHz		TBD		mA
V_{DDoff}	Undervoltage Shutdown	(see fig. 2)		6		V
V_{DDon}	Undervoltage Reset	(see fig. 2)		8		V
V_{DDhyst}	Hysteresis Start-up	(see fig. 2)	TBD	2		V
V_{DDreg}	Output Voltage	(see fig. 2)	TBD		TBD	V
V_{DO}	Drop Out Voltage	V_{CC} = 9 V I_{DD} = TBD mA (see fig. 2)			TBD	mV
I_{DDsc}	Short Circuit Current	V_{DD} = 0 V			TBD	mA

OSCILLATOR SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{SW1}	Oscillator Frequency Initial Accuracy	R_T = 8.2 KΩ C_T = 3300 pF T_J = 25 °C (see fig.3)	TBD	50	TBD	KHz
F_{SW2}	Oscillator Frequency Total Variation	R_T = 8.2 KΩ C_T = 3300 pF V_{DD} = 7 to10 V	TBD	50	TBD	KHz
$V_{OSC\ HI}$	Oscillator Peak Voltage	(1)		6.2		V
$V_{OSC\ LO}$	Oscillator Valley Voltage	(1)		2.5		V

(1) The peak and valley voltages are used internally by the voltage mode PWM. The sawtooth generated by the oscillator is compared to the COMP pin voltage to limit the duty cycle of the power mosfet switch. See block diagram on page 1.

ELECTRICAL CHARACTERISTICS (continued)

ERROR AMPLIFIER SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage	I_{COMP} = 0 mA T_J = 25 °C	TBD	2.6	TBD	V
ΔV_{REF}	Temperaure Variation			TBD	TBD	%
GBW	Unity Gain Bandwidth	(see fig. 4)		400		KHz
A_{VOL}	Open Loop Voltage Gain	(see fig. 4)	TBD	50		dB
I_{FB}	Input Bias Current	V_{FB} = 5 V		2.5	5	µA
$V_{COMP\ LO}$	Output Low Level	I_{COMP} = -100 µA V_{FB} = 5 V		1		V
$V_{COMP\ HI}$	Output High Level	I_{COMP} = 100 µA V_{FB} = 0 V		9		V
$I_{COMP\ LO}$	Output Low Current Capability	V_{COMP} = 5 V V_{FB} = 5 V		3.5		mA
$I_{COMP\ HI}$	Output High Current Capability	V_{COMP} = 5 V V_{FB} = 0 V		-3.5		mA

CURRENT REGULATION SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REG}	Reference Voltage	(see fig. 5)	320	350	380	mV
t_d	Current Sense Delay to Turn-off	(See fig 1)			350	ns
$V_{DSENSEth}$	Demagnetization Detector Threshold Voltage	(see fig. 6)		2.6		V
$V_{DSENSEcl}$	Demagnetization Detector Clamping Voltage	I_{DSENSE} = 10 mA (see fig. 6)		6		V

PROTECTION SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{Dlim}	Peak Drain Current Limitation	R_S = 0 (see fig. 9)	1		2.5	A
t_b	Current Limitation Blanking Time	R_S = 0 (see fig. 9)		1.2		µs
V_{CClim}	V_{CC} Overvoltage Threshold	V_{FB} = 0 V (see fig. 7)	26		35	V
V_{CChyst}	V_{CC} Overvoltage Hysteresis	V_{FB} = 0 V (see fig. 7)		2		V
T_{SD}	Thermal Shutdown Temperature	(see fig. 8)	150			°C
T_{SDhyst}	Thermal Shutdown Hysteresis	(see fig. 8)		TBD		°C

Figure 1: Switching Times

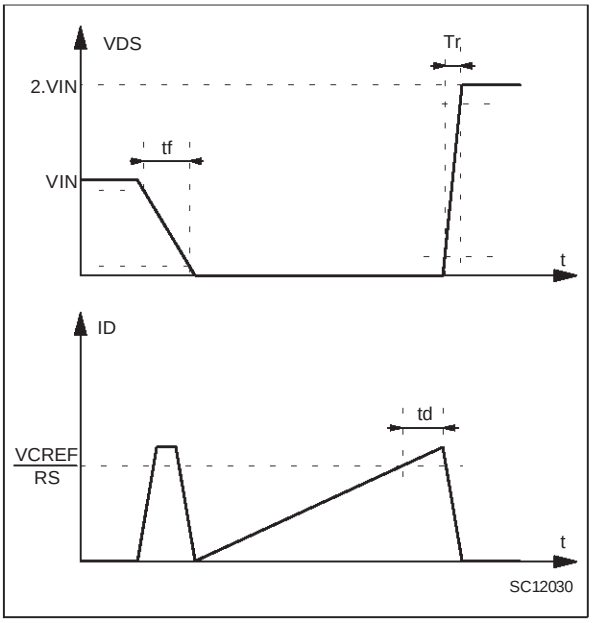


Figure 2: UVLO Logic Behaviour

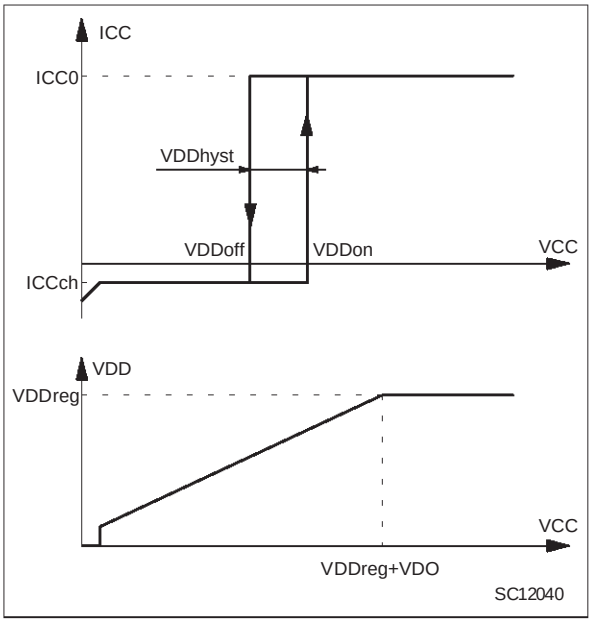
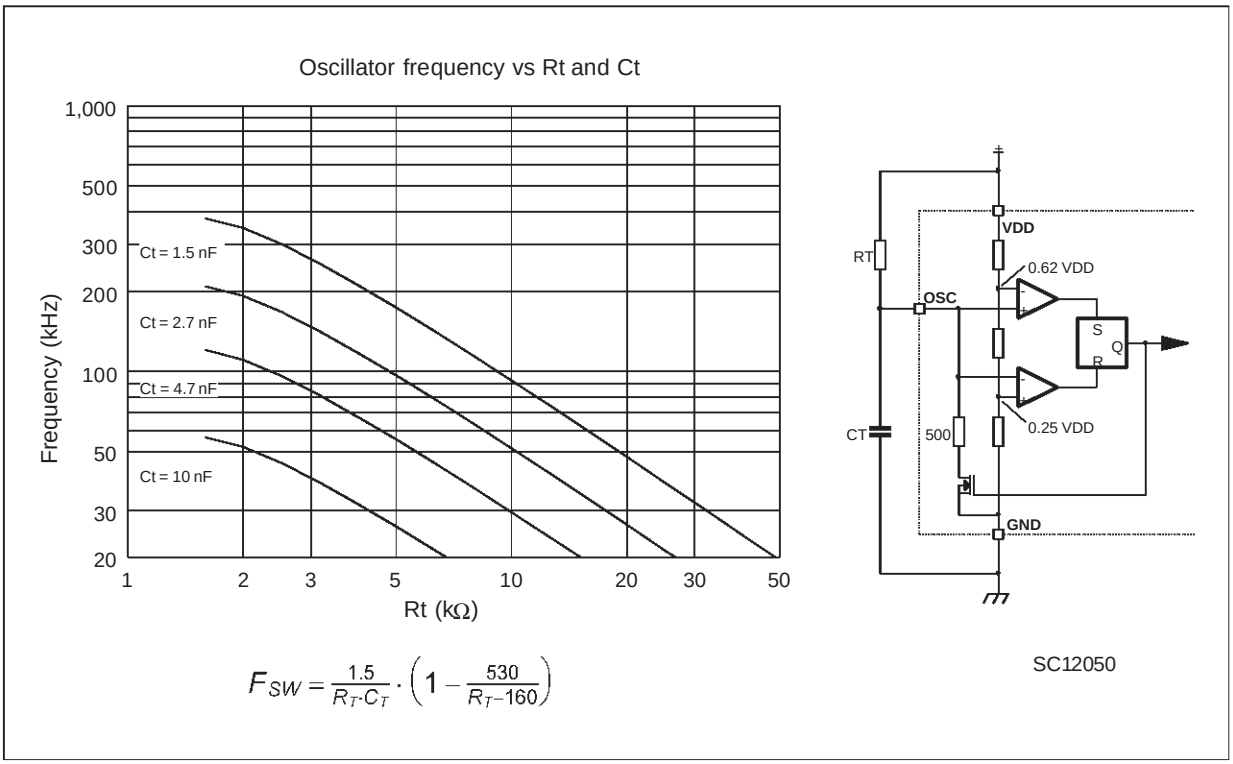


Figure 3: Switching Frequency Setting



$$F_{SW} = \frac{1.5}{R_T \cdot C_T} \cdot \left(1 - \frac{530}{R_T - 160}\right)$$

Figure 4: Error Amplifier Phase and Gain

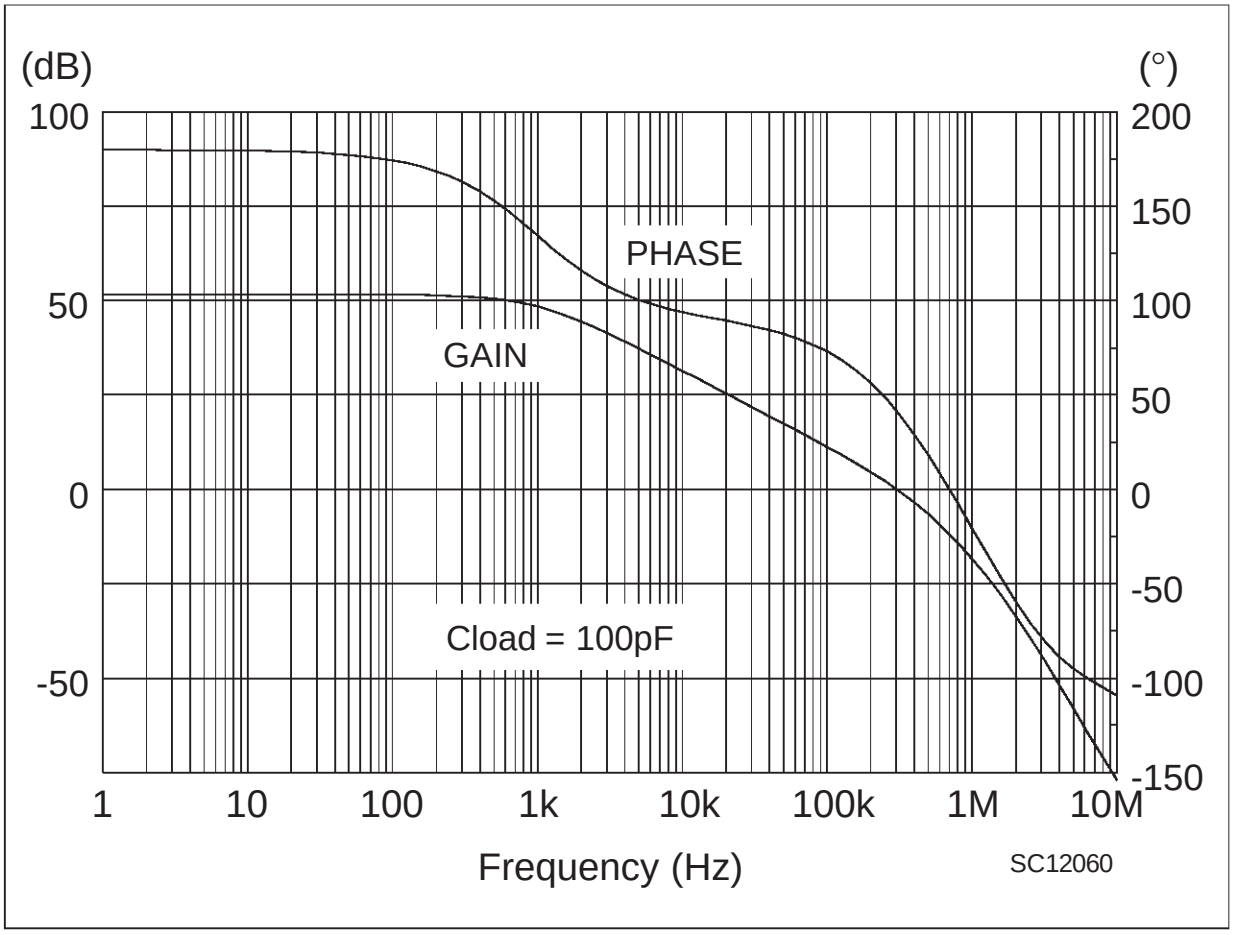


Figure 5: Reference Voltage Measurement

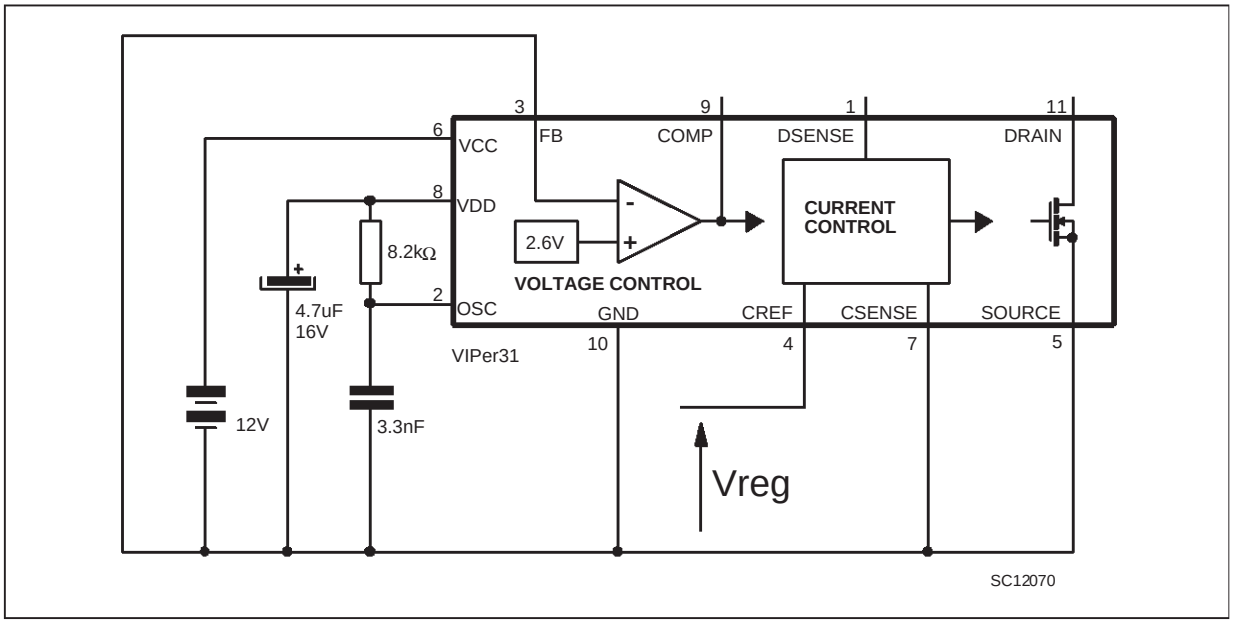


Figure 6: Demagnetisation Control Logic

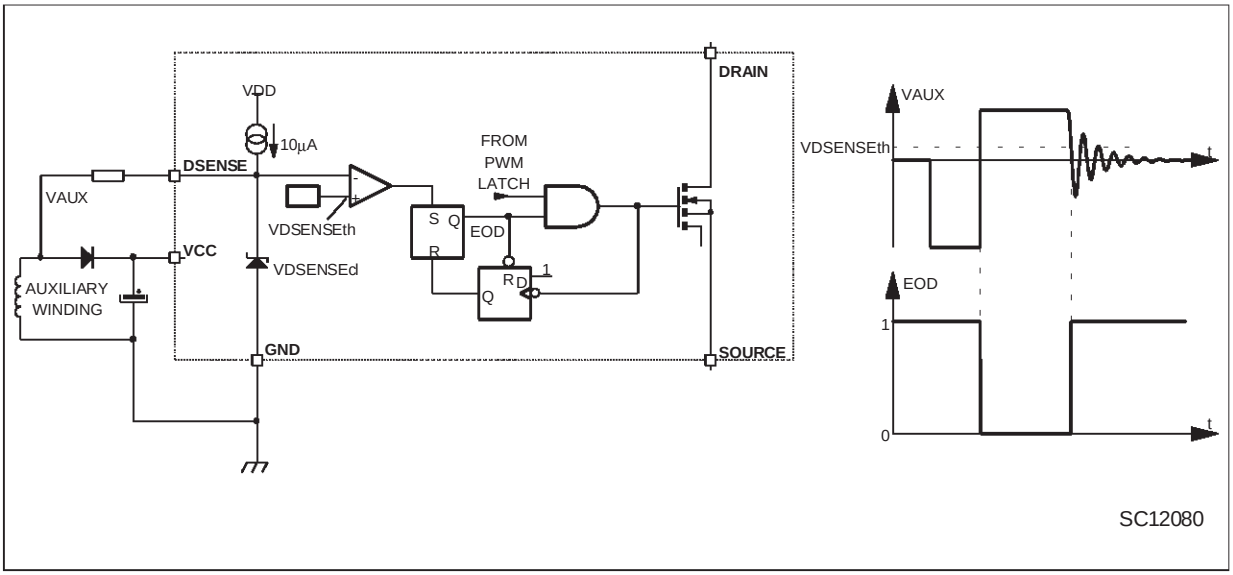


Figure 7: Overvoltage Protection

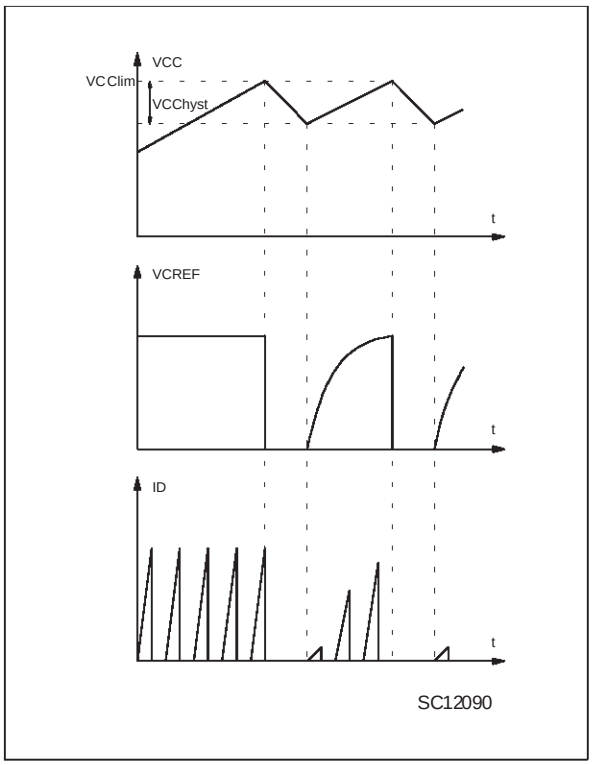


Figure 8: Overtemperature Protection

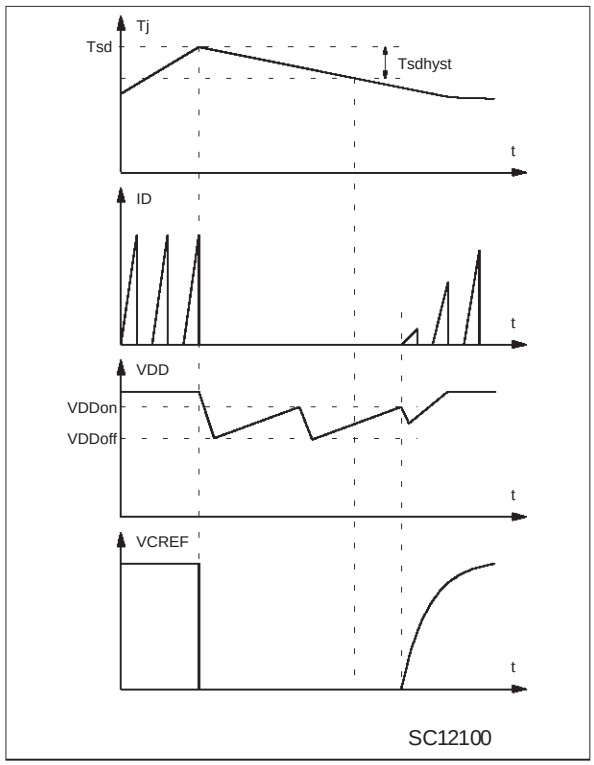


Figure 9: Blanking Time and Current Limitation

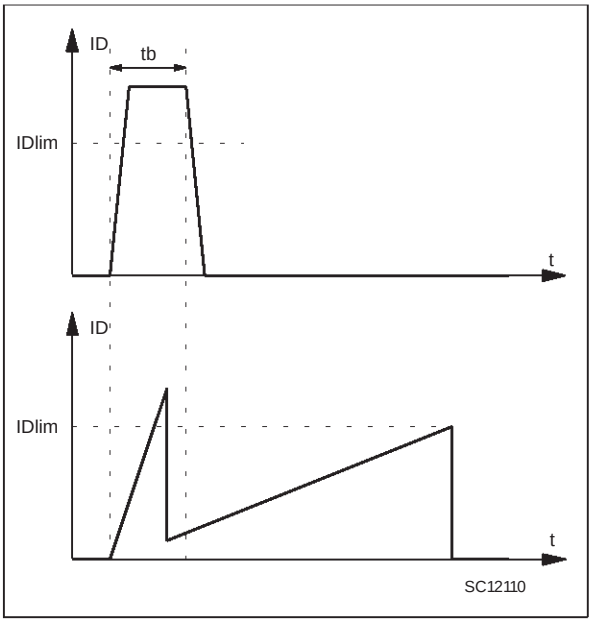


Figure 11: Typical Output Characteristics

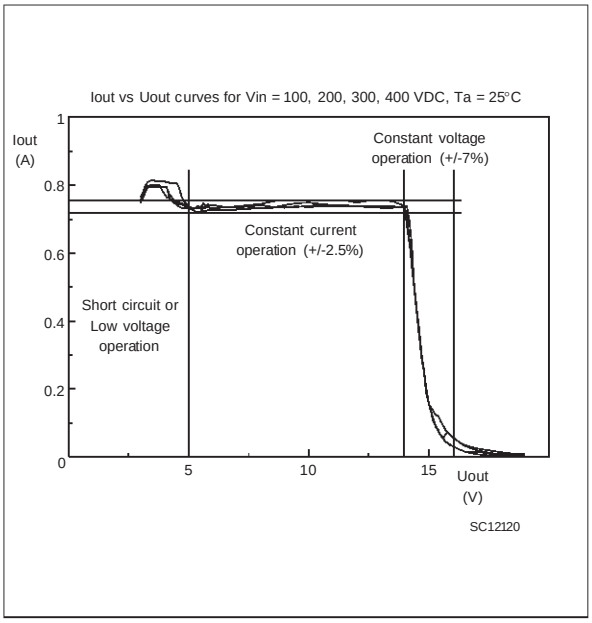
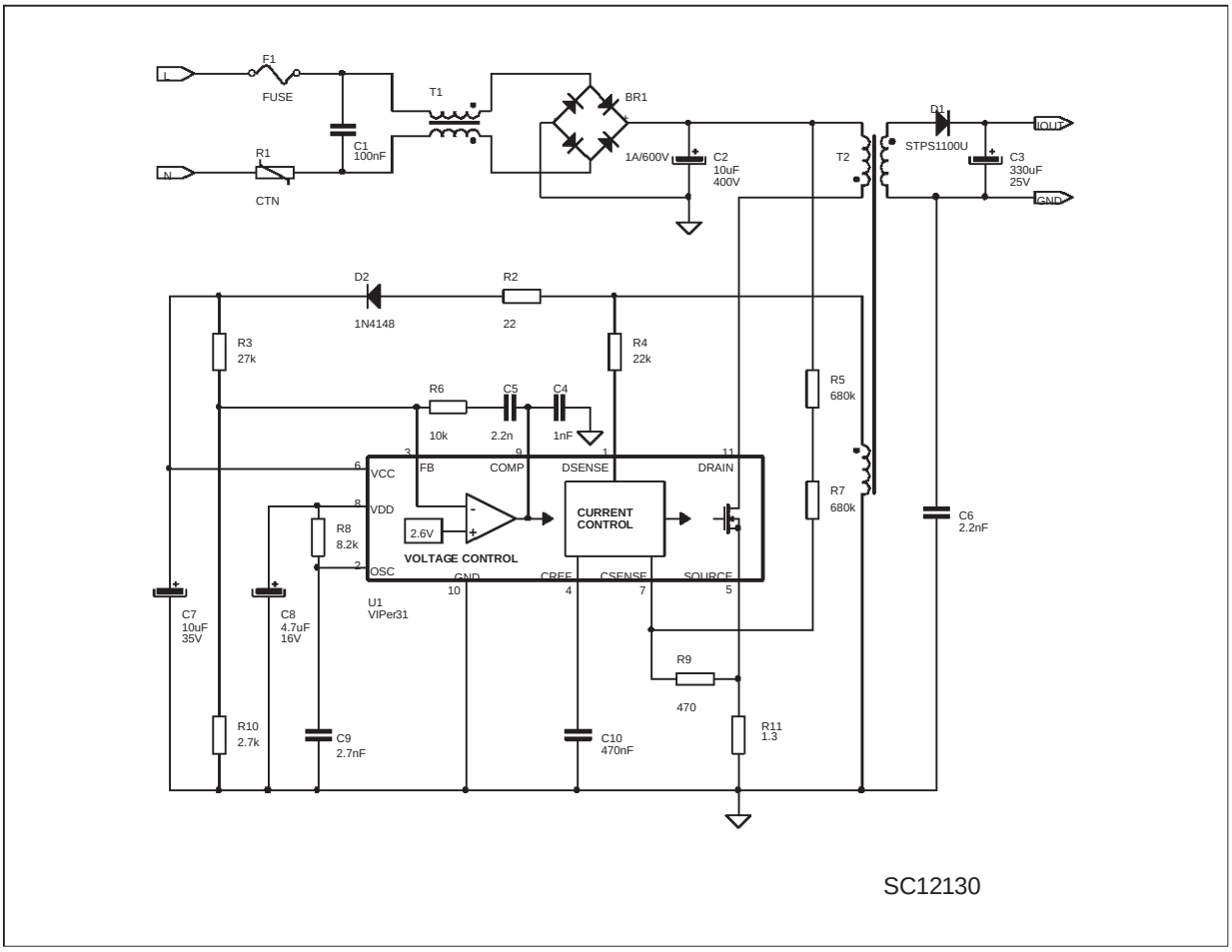


Figure 10: Typical AC/DC Adapter



OPERATION DESCRIPTION :

This device is intended to be used in off line AC/DC adapter where the desired output characteristic must present a rectangular characteristic. For output voltage values lower than a fixed value, the average output current must be constant, whatever are the input or output voltages. If the output current consumed by the load is lower than the previous constant current value, the output voltage value must be limited. In addition, the device provides protection against output short circuits and overtemperature events.

The two modes of operation are described in the following paragraphs. Figure 10 presents a typical application of which the output characteristic can be seen on figure 11.

CONSTANT OUTPUT CURRENT

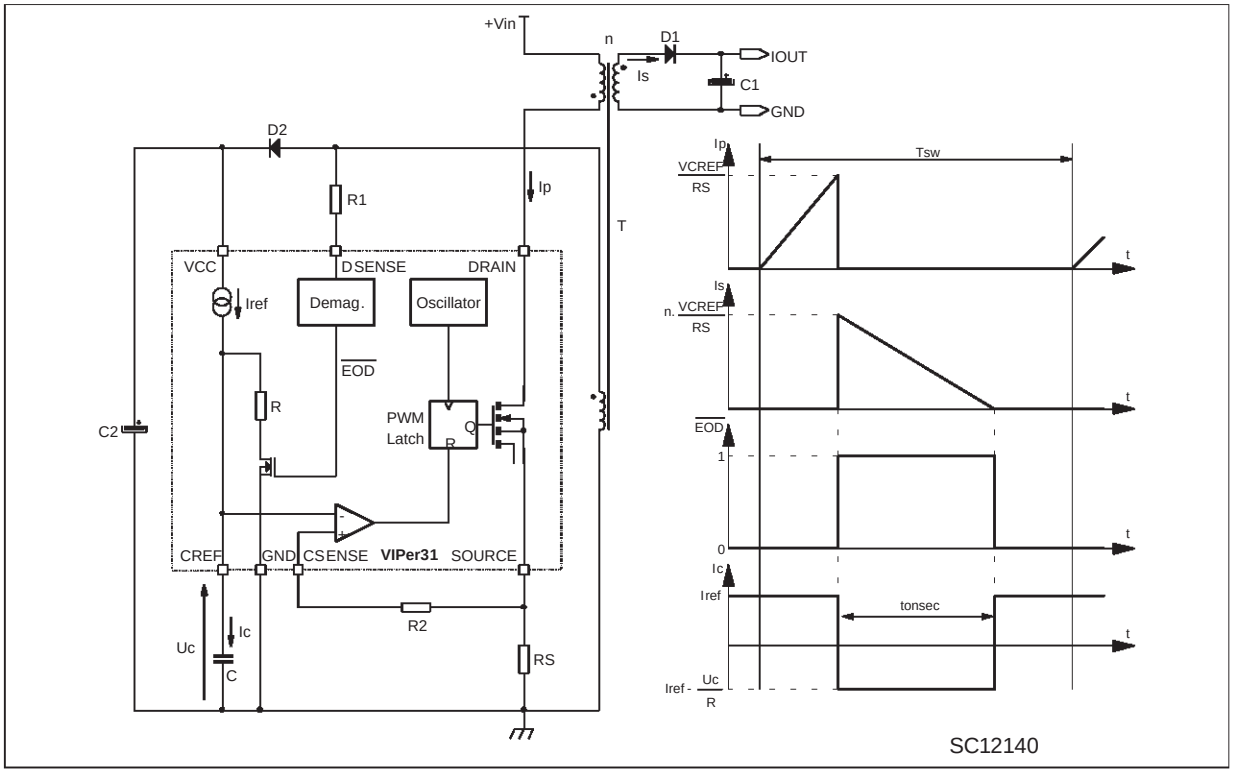
The power topology to be used with this device is a simple discontinuous flyback, as shown on figure 10. The average output current of such a topology cannot be easily kept constant, as it depends on the output voltage. Actually, if the peak primary current is fixed, the converter behaves as a constant power generator.

Therefore, a modulation of the peak primary current versus output voltage must be done in order to get the constant output current characteristic. A conventional way consists to use an optocoupler between primary and secondary, with additional circuitry on secondary side (Reference, error amplifier and current sense resistor).

This device avoids the use of all the secondary circuitry by controlling from primary side the secondary average output current. Figure 12 presents the internal constitution of the current control function. It is built around a constant current source Iref, and a mosfet switch driven with the complemented signal EOD, in series with a resistance R. The middle point of these elements is available on the CREF pin.

The EOD signal is generated by the demagnetisation function, which is monitoring the voltage of the main transformer auxiliary winding.

Figure 12: Constant Current Operation



An external resistance R_1 is needed to withstand the negative voltage generated by the winding. As long as the transformer is delivering some energy on secondary side, the negated EOD signal remains in the high state and the mosfet switch Q is on. The duration of this state is noted tonsec and corresponds to the time where the secondary current is flowing through D_1. For details about the demagnetisation function, refer to figure 6.

The average output current can be expressed as:

$$I_{OUT} = \frac{I_S}{2} X \frac{t_{ONSEC}}{T_{SW}} \quad (1)$$

Where :

I_S is the peak secondary current.

t_{ONSEC} is the conduction time on secondary side.

T_{SW} is the switching period.

Taking into account the transformer ratio n between primary and secondary side, I_S can also be expressed versus primary peak current I_P :

$$I_S = n \times I_P \quad (2)$$

The value of the capacitor C is sufficiently high to consider the voltage Uc as constant. This capacitor is submitted to a charging current and discharging current at the rhythm of the switching frequency. As these currents are in the range of a few mA (Iref is typically 1 mA), a 470 nF is a suited value for a switching frequency of 60 kHz. In steady state, it can be written that the charge is equal to the discharge :

$$I_{REF} \times (T_{SW} - t_{ONSEC}) = (\frac{U_C}{R} - I_{REF}) \times t_{ONSEC}$$

It comes :

$$U_C = R \times I_{REF} \times \frac{T_{SW}}{t_{ONSEC}} \quad (3)$$

As U_C can be considered as a constant voltage, can be also expressed as :

$$I_P = \frac{U_C}{R_S} \quad (4)$$

Combining (1), (2), (3) and (4) :

$$I_{OUT} = \frac{n}{2} \times \frac{R \times I_{REF}}{R_S}$$

This last expression shows that the average output current doesn't depend any more neither on the output voltage, nor on the duty cycle, nor on the input voltage. The only parameters which are setting its value are :

The transformer ratio n.

The sense resistor value R_S

The product $R \times I_{REF}$

This product corresponds to a voltage which is noted Vreg in the specification tables. Figure 5 shows the test fixture for measuring it : The DSENSE pin is held in the high state (In fact, it is left open, as an internal pull up current source is internally connected on this pin) and the mosfet switch Q is always in the high state. In this case, the voltage on the CREF pin establishes at $R \times I_{REF}$.

Note that the oscillator must be running for the demagnetisation block to sample correctly the DSENSE pin.

As V_{reg} has a typical value of 350 mV, the output current can be finally written as :

$$I_{OUT} = n \times \frac{0.175}{R_S}$$

A sense resistor of 1.3 Ω with a transformer ratio of 6 gives a typical output current of about 800 mA.

The schematics of figure 10 shows a compensation on the CSENSE pin with the two resistances R5 and R7. These resistances are connected on the Vin input voltage and are providing an offset on the current sense pin. The higher is the input voltage, and the higher is this offset current. The purpose of this compensation is to cancel the effect of the current control propagation time td, which induces an extra current on top of the theoretical peak current Ip given by (4).

The output current obtained with this compensation can be seen on figure 11. The typical "flatness" is about +/-2.5 %, including the input voltage variation from 100 VDC to 400 VDC. If less accuracy is needed, these two resistances can be omitted.

CONSTANT VOLTAGE OPERATION

An another part of the circuit is in charge of the regulation of the output voltage, and generates the vertical characteristic of figure 11. It consists of a primary feedback regulation, with a conventional voltage mode control : An operational amplifier with an internal voltage reference of 2.6 V is configured in error amplifier and defines the duty cycle of the power mosfet switch by comparison with the oscillator sawtooth (See block diagram on page 1).

As it is a primary feedback, the accuracy of the output voltage depends closely on the transformer coupling quality. This is especially

true for low output current where the output voltage can reach high values, as shown on figure 11 : 20 V can be reached for a nominal regulated one of 14.5 V, with a typical transformer. But a simple clamping zener can limit it to about 17 V with a reasonable dissipated power. The 10 % to 100 % output load regulation is better than +/-7 %.

COMPONENTS SIZING

The following procedure defines the value of essential parameters for the transformer and the sensing resistance in a typical application. The user can adapt by himself the final design, according to specific needs, if any.

- 1. Define the maximum output voltage V_{OUT}^{MAX} for which the converter has still to operate in constant current mode.
- 2. Check that the ratio between the minimum operating output voltage V_{OUT}^{MIN} and V_{OUT}^{MAX} is lower than 2.5. This ratio is limited by the overvoltage protection value (Typically 29 V) and V_{DDreg} (Typically 10 V) and their tolerances.
- 3. Compute the transformer turn ratio n from primary to secondary with the formula :

$$n = \frac{100}{V_{OUT}^{MAX}} = \frac{n_p}{n_s}$$

- 4. Compute the sense resistance value with the formula :

$$R_S = n \times \frac{0.175}{I_{OUT}}$$

- 5. Compute the transformer turn ratio n_{AUX} from auxiliary to secondary with the formula :

$$n_{AUX} = \frac{25}{V_{OUT}^{MAX}} = \frac{n_a}{n_s}$$

- 6. The current control function requires the converter to work in discontinuous mode. The primary inductance value L_P of the transformer can be computed by respecting this constraint in all conditions, or by using the following formula : $L_P = \frac{n}{10} \times \frac{V_{IN}^{MIN} \times T_{SW}}{I_{OUT}}$ where :

  V_{IN}^{MIN} is the minimum input rectified DC voltage from the mains.

  T_{SW} is the switching period.

START UP SEQUENCE

An integrated high voltage current source provides a bias current from the DRAIN pin during the start-up phase. This current is partially absorbed by internal control circuits which are placed into a standby mode with reduced consumption and also provided to the external capacitors connected to the V_{DD} and V_{CC} pins. As soon as the voltage on this pin reaches the high voltage threshold V_{DDon} of the UVLO logic, the device turns into active mode and starts switching. The start up current generator is switched off, and the converter should normally provide the needed current on the VDD pin through the auxiliary winding of the transformer, as shown on figure 13.

The sum of the external capacitors C_{START} on the V_{DD} and V_{CC} pins must be sized according to the time needed by the converter to start up, when the device starts switching. This time t_{SS} depends on many parameters, among which transformer design, output capacitors, capacitor value implemented on the CREF pin (See soft start consideration here after). The following formula can be used for defining the minimum capacitor needed :

$$C_{START} > \frac{I_{DD} \times t_{SS}}{V_{DDhyst}}$$ where :

I_{DD} is the consumption current on the V_{DD} pin when switching. Refer to specified I_{DD1} and I_{DD2} values.

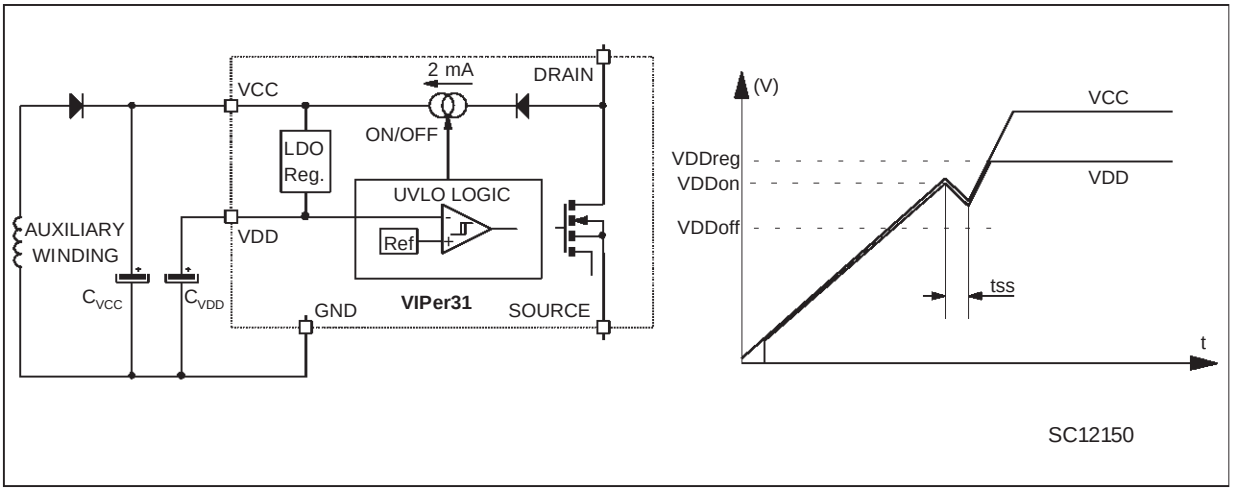
t_{SS} is the start up time of the converter when the device begins to switch. Worst case is generally at full load.

V_{DDhyst} is the voltage hysteresis of the UVLO logic. Refer to the minimum specified value.

$C_{START} = C_{VDD} + C_{VCC}$ is the sum of both capacitors on V_{DD} and V_{CC} pins. Once is defined, allot a standard 4.7 µF / 16 V on the V_{DD} pin, and the rest on the V_{CC} pin. The V_{DD} capacitor insures a correct decoupling of the internal serial regulator between V_{CC} and V_{DD}.

Soft start feature is implemented through the CREF capacitor which is also filtering the CREF voltage. The minimum value of this capacitor has to be set according to the switching frequency, in order to filter the charging and discharging current issued from the CREF pin (Refer to the current control description part). It can be increased from

Figure 13: Start Up Circuit and Sequence



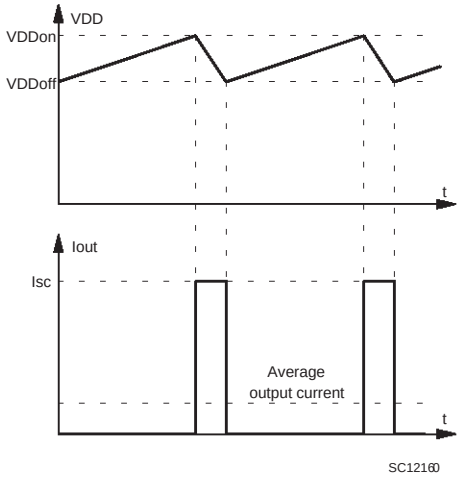
this value to provide a soft start feature, of which the duration depends on some circuit parameters, like transformer ratio, sense resistor, output capacitors and load. The user will define the best appropriate value by experiments.

SHORT CIRCUIT OPERATION

In case of abnormal condition where the auxiliary winding is unable to provide the low voltage supply current to the V_{CC} pin (i.e. short circuit on the output of the converter), the external capacitors discharge themselves down to the low threshold voltage V_{DD}off of the UVLO logic, and the device get back to the inactive state where the internal circuits are in standby mode and the start up current source is activated. The converter enters a endless start up cycle, with a start-up duty cycle defined by the ratio of charging current towards discharging when the VIPer31 tries to start. This ratio is fixed by design to 1.5 to 12, which gives a 11% start up duty cycle, while the power dissipation at start up is approximately 0.6 W, for a 230 Vrms input voltage.

The average output short circuit current is the product of the start up duty cycle by the output current flowing during the active phase of the device (See figure 14). This output current is limited by either the CREF pin voltage, or the internal current limitation of 1.3 A. These values together with the low value of start-up duty cycle prevents the stress of the output rectifiers and of the transformer when in short circuit.

Figure 14 : Short circuit operation



OVERVOLTAGE PROTECTION

If the output voltage accuracy is not a concern, but only a limitation is desired, the internal overvoltage protection can be used. In this case, five components can be taken out from the schematics of figure 10 (R3-R10-R6-C4-C5) and the input pin FB of the error amplifier is simply grounded. The internal overvoltage protection will act as soon as the V_{CC} voltage reaches typically 29 V, by turning off the power mosfet switch. An hysteresis of about 3 V will enable again the switching of the device at a lower voltage level on the V_{CC} pin. This results in an efficient voltage limitation, in a burst mode operation type, with some ripple on the output. Case by case experiments will define the correct value of output capacitor C3, according to the loading current in low output power condition.

STANDBY MODE

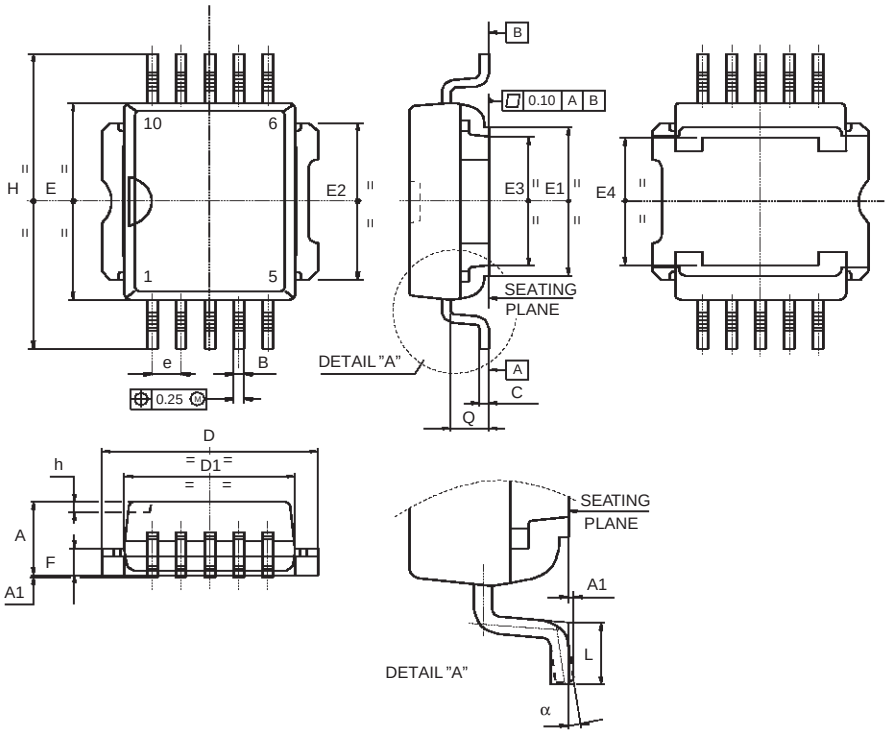
The standby mode is represented by a very low output current, corresponding to a full loaded battery in a battery charger application. The output voltage is limited by either the overvoltage protection or the error amplifier, according to the design. This results into different situations :

- In case the overvoltage protection is used, the burst mode operation as described previously takes place, governed by the hysteresis of the overvoltage comparator.
- If the error amplifier is used, many situation can occur, depending on the compensation network foreseen by the designer. These situations can range from a normal continuous operation, to burst mode. In any case, the output voltage will be regulated to the desired value.

Note that the burst operation is providing a very low input power consumption, because it reduces the switching frequency, and thus commutation losses. Less than 1 W of input power can be observed in this operative mode, with a few hundreds of mW delivered to the secondary load. This is far compliant with standby standards, like the ”Blue Angel” one.

Power SO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0^o		8^o			



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