UM1985
User manual

VIP-M07-ADIS

Introduction

This document describes the specifications for the 12 V M0-7 discovery board that is able to work connected to SPC560B-DIS discovery board to create a complete solution for a specific 12 V BCM (Body Control Module) system.

In a typical car body application it is necessary to connect a microcontroller to drive several loads (bulb lamps, led lamps, electrical motors, and so on). When using a bulb lamp, to increase its lifetime and avoid flickering, it is necessary to shift PWM signals and adapt the duty cycle to battery voltage.

The M0-7 expansion board provides diagnostics feedback and current consumptions to operating close loop for each single load synchronized with the PWM signals. SPC560B-DIS is the core hardware to generate shifted PWM signals and synchronize ADC conversion.

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1 Overview

VIP-M07-ADIS is an easy-to-use board offered at budget price. Together with a dedicated GUI and firmware (STSW-M07-ADIS) and in combination with SPC560B-DIS board, it becomes a tool to evaluate M0-7 high-side drivers.

1.1 Getting started

Follow the sequence below to configure the system and launch the application:

1. Check jumper position in the SPC560B-DIS board:
   - J14,J13,J12,J7,J6,J11,J5,J4 removed
   - S1,S2,J10,J9,J2,J1,J3 inserted
2. Connect the SPC560B-DIS board to a PC with a USB cable ‘type A to mini-B’
3. Download firmware STSW-M07-ADIS and program board as described on *www.st.com*
4. Disconnect USB cable
5. Plug VIP-M07-ADIS board and connect 12 V power supply on J30
6. Install GUI on your PC as described on *www.st.com*
7. Connect loads to the outputs
8. Check jumper position in the VIP-M07-ADIS:
   - J1,J7,J8,J29 – pin 2 connected to pin 1
   - J2 inserted
9. Connect USB cable to PC
10. Execute GUI (*www.st.com*)

1.2 Hardware, schematic and layout

Figure 1. VIP-M07-ADIS schematic

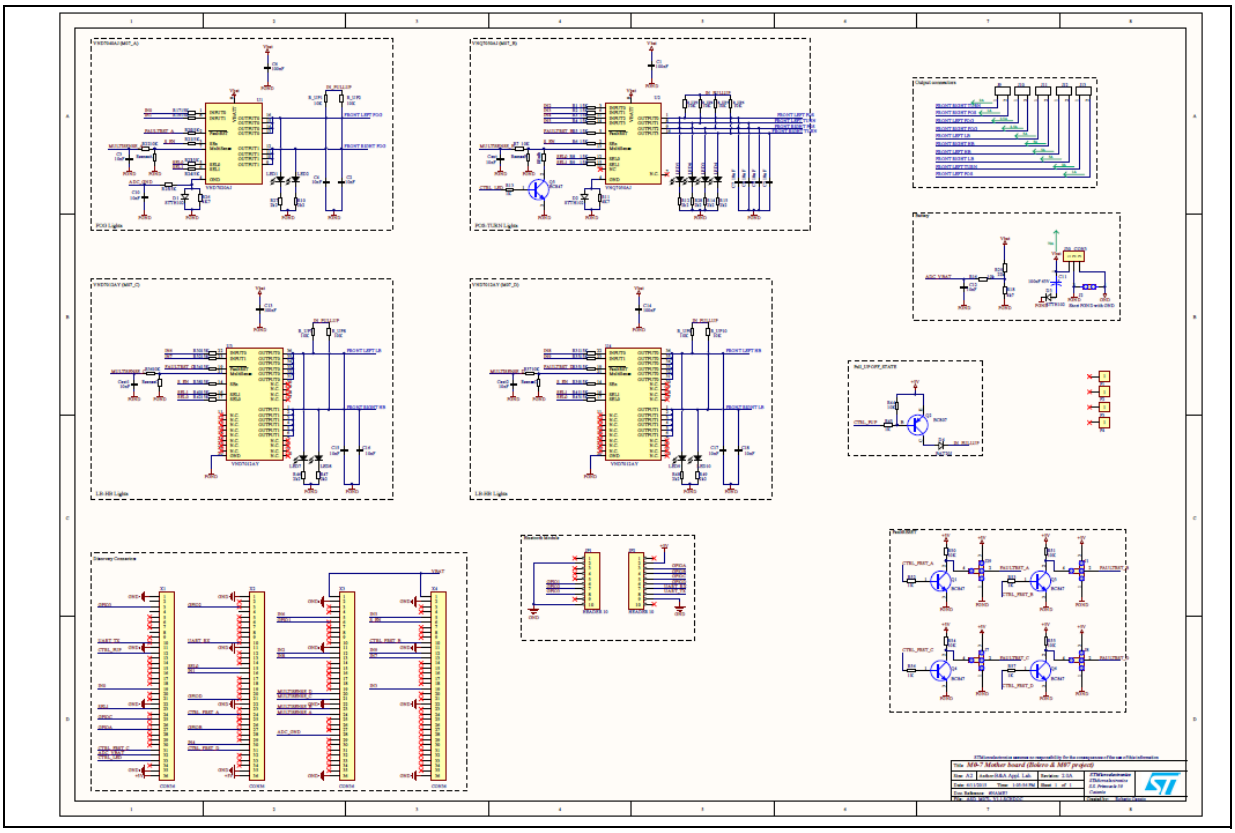


Figure 2. VIP-M07-ADIS top layer

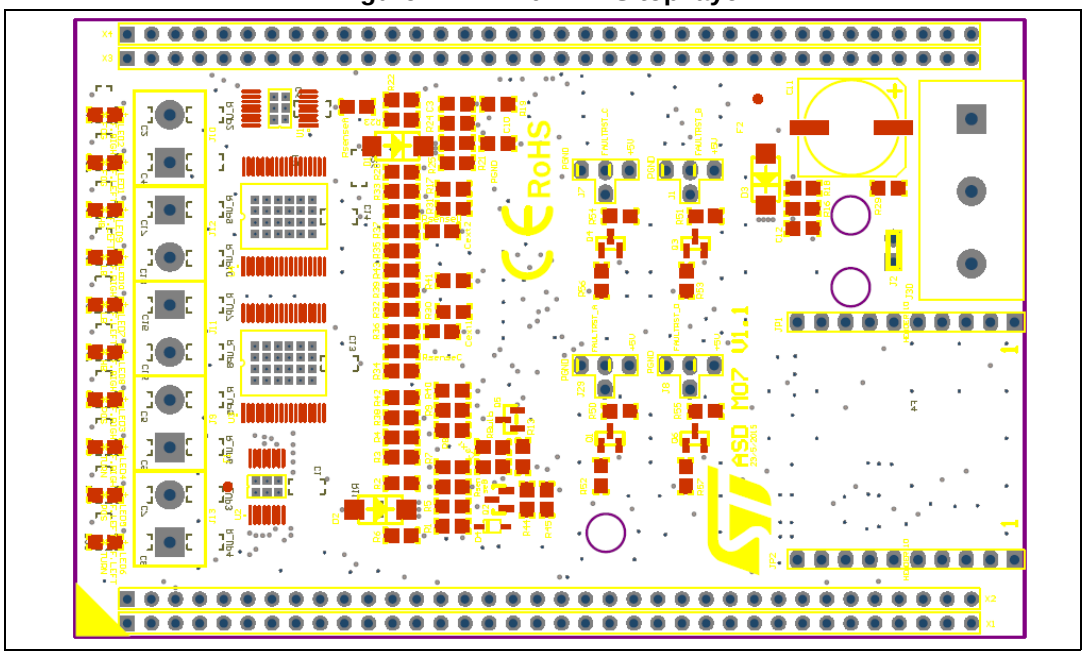
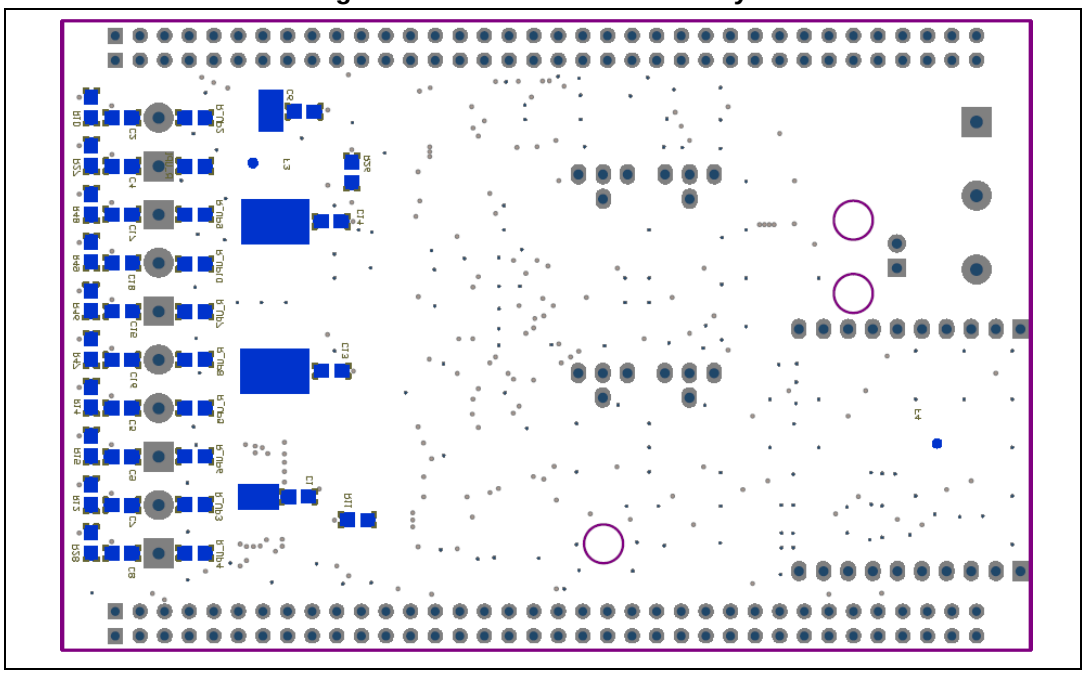


Figure 3. VIP-M07-ADIS bottom layer



1.3 M0-7 devices

These devices are manufactured using ST proprietary VIPower M0-7 technology and are designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and off-state open-load.

Here below a short description of the most important features of M0-7 devices:

- General
  - Smart high-side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - Off-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/ disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with a dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery through self turn-on
  - Electrostatic discharge protection

The VIP-M07-ADIS is equipped with 4 M0-7 high-side drivers:

- **M0-7_ A** is a VND7020AJ quad channels in PowerSSO-16 package with 22 mΩ of R_{ON}
- **M0-7_ B** is a VNQ7050AJ quad channels in PowerSSO-16 package with 50 mΩ of R_{ON}
- **M0-7_ C** and **M0-7_D** is a VND7012AY dual channels in PowerSSO-36 package with 12 mΩ of R_{ON}

The suggested configuration to drive front lights is illustrated in *Table 1*:

Table 1. Loads configuration

Light		Load (W)	Part number	Device	Channel
Front Left	Position	W5W/H7	VNQ7050AJ	M0-7_B	0
	Low Beam	H3/H15	VND7012AY	M0-7_C	0
	High Beam	H7	VND7012AY	M0-7_D	0
	Fog	21W	VND7020AJ	M0-7_A	0
	Turn	W16W	VNQ7050AJ	M0-7_B	1
Front Right	Position	W5W/H7	VNQ7050AJ	M0-7_B	2
	Low Beam	H3/H15	VND7012AY	M0-7_D	1
	High Beam	H7	VND7012AY	M0-7_C	1
	Fog	21W	VND7020AJ	M0-7_A	1
	Turn	W16W	VNQ7050AJ	M0-7_B	3

1.4 Power supply

The power supply is provided through J30 connectors and current capability that must be adequate to the loads.

1.5 LEDs

LED *x*: indicates the status of the correspondent output *x* (each output has a LED connected to indicate its status).

1.6 Jumpers

A FaultRST pin is an active low compatible with 3 V and 5 V CMOS outputs and unlatches the output in case of fault or disables the latch-off functionality.

J1,7,8,29 are multi positions and they allow three different configurations:

1. Pin 2 connected with pin 1, FaultRST is forced to GND setting the outputs in auto-restart mode
2. Pin 2 connected with pin 3, FaultRST is forced to 5 V so unlatches the output in case of fault
3. Pin 2 connected with pin 4, FaultRST is driven by microcontroller output

J2 connects signal ground and powers ground at the same time.

1.7 Extension connectors

The male headers X1,X2,X3 and X4 are two strip lines connectors of 2 x 36 each and they are used to allow the access to all the SPC560B54L5 MCU pins with exception of JTAG, TCK, TMS, TDI, TDO, XTAL, EXTAL and VDD_LV. The pins used in this M0-7 application

are described in *Table 2*.

Table 2. Extension connectors pins used

Discovery Connector X1		ASD_M0-7Ls	Discovery Connector X2		ASD_M0-7Ls	Discovery Connector X3		ASD_M0-7Ls	Discovery Connector X4		ASD_M0-7Ls
1	GND		1	GND		1	Batt		1	Batt	
2	PE[2]		2	PE[3]		2	GND		2	GND	
3	PC[5] (CSN)	GPIO3	3	PC[4]	GPIO2	3	TCK		3	TDI	
4	PE[4]		4	PE[5]		4	TDO		4	TMS	
5	PH[4]		5	PH[5]		5	PA[6]	IN6	5	PA[5]	IN5
6	PH[6]		6	PH[7]		6	PC[2]	GPIO1	6	PC[3]	S_EN
7	PH[8]		7	PE[6]		7	PG[11]		7	PG[10]	
8	PE[7]		8	PC[12]		8	PE[15]		8	PE[14]	
9	PC[13]		9	PB[1] (RxDC)		9	PG[15]		9	PG[14]	
10	PB[2]		10	PB[3]		10	PE[12]		10	PA[11]	CTRL_ FRST_ B
11	GND		11	GND		11	GND		11	GND	
12	PB[0] (TxDC)	CTRL_ PUP	12	PC[14]		12	PA[10]	IN2	12	PA[9]	IN9
13	PC[15]		13	PG[5]		13	PA[8]	IN8	13	PA[7]	IN7
14	PG[4]		14	PG[3]		14	PE[13]		14	PF[14]	
15	PG[2]		15	PA[2]	SEL0	15	PF[15]		15	PG[0]	
16	PE[0]		16	PA[1]	IN1	16	PG[1]		16	PH[3]	
17	PE[1]		17	PE[8]		17	PH[2]		17	PH[1]	
18	PE[9]		18	PE[10]		18	PH[0]		18	PG[12]	
19	PA[0]	IN0	19	PE[11]		19	PG[13]		19	PA[3]	IN3
20	RESET _ASD		20	PG[9]		20	PB[15]	MultiSE NSE_D	20	PD[15]	
21	PG[8]		21	PC[11]	GPIOD	21	PB[14]	MultiSE NSE_C	21	PD[14]	
22	GND		22	GND		22	GND		22	GND	
23	PC[10]	SEL1	23	PG[7]		23	PB[13]	MultiSE NSE_B	23	PD[13]	
24	PG[6]		24	PC[9]	CTRL_ FRST_ A	24	PB[12]	MultiSE NSE_A	24	PD[12]	

Table 2. Extension connectors pins used (continued)

Discovery Connector X1		ASD_M0-7Ls	Discovery Connector X2		ASD_M0-7Ls	Discovery Connector X3		ASD_M0-7Ls	Discovery Connector X4		ASD_M0-7Ls
25	PC[8]	GPIOC	25	PF[9]		25	PB[11]		25	PD[11]	
26	PF[8]		26	PF[12]		26	PD[10]		26	PD[9]	
27	PC[6] (TxDL)	GPIOA	27	PC[7] (RxDL)	GPIOB	27	PB[7]		27	PB[6]	
28	PF[10]		28	PF[11]		28	PB[5]	ADC_GND	28	PB[4]	
29	PA[15]		29	PF[13]		29	PD[8]		29	PD[7]	
30	PA[14] (CLK)		30	PA[4]	IN4	30	PD[6]		30	PD[5]	
31	PA[12] (MISO)	CTRL_FRST_C	31	PA[13] (MOSI)	CTRL_FRST_D	31	PD[4]		31	PD[3]	
32	PB[9]	ADC_Vbat	32	PB[8]		32	PD[2]		32	PD[1]	
33	PB[10]	CTRL_Led	33	PF[0]		33	PD[0]		33	PF[7]	
34	PF[1]		34	PF[2]		34	PF[6]		34	PF[5]	
35	GND		35	GND		35	PF[4]		35	PF[3]	
36	5V		36	5V		36	GND		36	GND	

1.8 R_{sense} configuration

In normal operating conditions, *Equation 1* describes relation between I_{out} and V_{sense}

Equation 1

$$V_{SENSE} = R_{SENSE} \times I_{SENSE} = R_{SENSE} \times (I_{out}/k)$$

Design value of Sense Resistor can be calculated from the above equation given the intended voltage at the ADC with the nominal load current and the typical K factor of the device.

The calculated sense resistor implies following considerations that have to be taken into account:

a) In normal operating conditions, in order not to reach MultiSense voltage saturation V_{SENSE_SAT}, with the maximum load current that can be read I_{OUT_MAX}, the R_{SENSE} has to fulfill in *Equation 2*:

Equation 2

$$R_{SENSE} < K_{MIN} \times (V_{SENSE} / I_{OUT\ MAX})$$

MultiSense is guaranteed within this maximum current linearity. If a lower maximum load current needs to be read, like for example in case a LED string, the R_{SENSE} value must be increased.

b) In normal operating conditions, the maximum sense voltage that can be read with the given R_{SENSE} must be higher than a certain ADC threshold. This can be expressed by *Equation 3*:

Equation 3

$$R_{SENSE} > V_{SENSEMAX} / I_{SENSE\ SAT\ MIN}$$

$V_{SENSEMAX}$ is the maximum voltage that the ADC has to read at the maximum monitored load current. This value can be below or equal 5 V which normally is the maximum operating range of the ADC.

c) In fault conditions (overload, short-circuit to GND that causes Power Limitation or Thermal Shutdown and in open-load/short to battery in OFF state), in order to be able to differentiate a normal operating condition from a Fault condition, the MultiSense pin must be capable to develop a voltage above the V_{SENSEH} (Value given in the datasheet, V_{SENSEH} = 6 V typically). Therefore the following condition must be fulfilled:

Equation 4

$$R_{SENSE} > V_{SENSE_MIN} / I_{SENSE_H_MIN}$$

d) Finally the current sense resistor is necessary to protect the MultiSense pin in case of reverse battery. During this event, for monolithic devices an intrinsic diode between MultiSense and V_{CC} pins is forward biased and the resulting current must be limited (in the datasheet the maximum MultiSense current that can flow in reverse battery condition is indicated in the absolute maximum rating table). This value is given in the Absolute Maximum Ratings section of M0-7 datasheet

(I_{SENSE} value, in case of VND7020AJ this is 20 mA), therefore the minimum R_{SENSE} to protect the MultiSense pin in case of reverse battery (supposing a static condition of V_{CC} = -16 V) is.

Equation 5

$$R_{SENSE} > (-V_{CC} - V_F)/I_{SENSE_rev_max} = (16V = 0.7V)/20mA = 765\Omega$$

In conclusion the R_{SENSE} value must fulfill two opposite conditions to have linearity in normal operating condition: one is avoiding MultiSense pin current saturation (increase R_{SENSE}) and the other is avoiding MultiSense pin voltage saturation (decrease of R_{SENSE}). Moreover the R_{SENSE} value has to be dimensioned in order to distinguish a normal operating condition (linear mode V_{SENSE} proportional to load current) from a Fault condition (Constant Voltage Generator developing V_{SENSE_H} across the R_{SENSE}).

In the board there are 4 M0-7 with 4 R_{SENSE} selected in order to have V_{SENSE} = 2 V and I_{OUT} depending of the devices:

- VNQ7050AJ is a 50mΩ, in order to have V_{SENSE} = 2 V at I_{OUT} = 2A
  R_{SENSE} = K x (V_{SENSE}/I_{OUT}) = 1120 x (2 V / 2 A) = 1120 Ω -> 1.1 k Ω
- VNQ7012AY is a 12mΩ, in order to have V_{SENSE} = 2V at I_{OUT} = 7A
  R_{SENSE} = K x (V_{SENSE}/I_{OUT}) = 4280 x (2 V / 7 A) = 1222 Ω -> 1.2 k Ω
- VND7020AJ is a 20mΩ, in order to have V_{SENSE} = 2V at I_{OUT} = 3A
  R_{SENSE} = K x (V_{SENSE}/I_{OUT}) = 2755 x (2 V / 3 A) = 1836 Ω -> 2.2 k Ω

2 Graphical User Interface

The Graphical User Interface STSW-M07-ADIS is available on *www.st.com*.

3 Revision history

Table 3. Document revision history

Date	Revision	Changes
17-Nov-2015	1	Initial release.
13-Apr-2016	2	Updated *Introduction*. Updated: - *Section 1: Overview* - *Section 1.1: Getting started* - *Section 1.5: LEDs* - *Section 1.6: Jumpers* - *Section 1.7: Extension connectors* Updated: *Section 2: Graphical User Interface* Deleted Appendix.

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