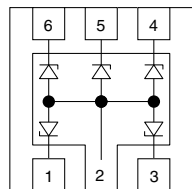
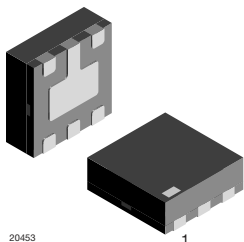


5-Line ESD-Protection Diode Array in LLP75



19956



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1

MARKING (example only)



Dot = Pin 1 marking

XX = Date code

YY = Type code (see table below)

FEATURES

- Ultra compact LLP75-6L package
- Low profile < 0.6 mm
- 5-line ESD-protection
- Low leakage current $I_R < 0.1 \mu A$
- Low load capacitance $C_D = 13 \text{ pF}$
- ESD-protection acc. IEC 61000-4-2
± 15 kV contact discharge
± 15 kV air discharge
- Working voltage range $V_{RWM} = 5 \text{ V}$
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Compliant to RoHS Directive 2002/95/EC and in accordance to WEEE 2002/96/EC


RoHS
COMPLIANT

GREEN
[5-2008]**

ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VESD05A5A-HSF	VESD05A5A-HSF-GS08	3000	15 000

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VESD05A5A-HSF	LLP75-6L	AR	4.2 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

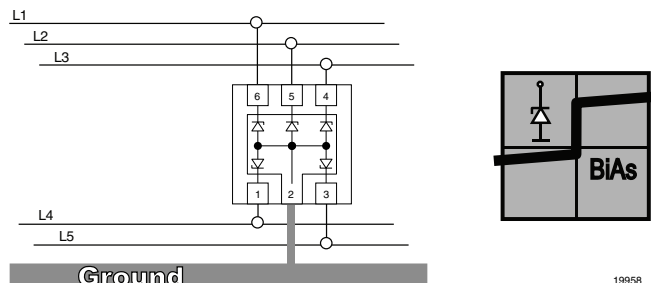
ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	BiAs-Mode: each input (pin 1 - pin 6) to ground (pin 2); acc. IEC 61000-4-5; $t_p = 8/20 \text{ } \mu\text{s}$; single shot	I_{PPM}	2.5	A
	BiSy-mode: each input (pin 1 - pin 6) to any other input pin. Pin 2 not connected. Acc. IEC 61000-4-5; $t_p = 8/20 \text{ } \mu\text{s}$; single shot	I_{PPM}	2.5	A
Peak pulse power	BiAs-mode: each input (pin 1 - pin 6) to ground (pin 2); acc. IEC 61000-4-5; $t_p = 8/20 \text{ } \mu\text{s}$; single shot	P_{PP}	33	W
	BiSy-mode: each input (pin 1 - pin 6) to any other input pin. Pin 2 not connected. Acc. IEC 61000-4-5; $t_p = 8/20 \text{ } \mu\text{s}$; single shot	P_{PP}	43	W
ESD immunity	acc. IEC61000-4-2; 10 pulses BiAs-mode: each input (pin 1 - pin 6) to ground (pin 2)	Contact discharge	V_{ESD}	± 15 kV
		Air discharge	V_{ESD}	± 15 kV
ESD immunity	acc. IEC 61000-4-2 ; 10 pulses BiSy-mode: each input (pin 1 - pin 6) to any other input pin. Pin 2 not connected.	Contact discharge	V_{ESD}	± 10 kV
		Air discharge	V_{ESD}	± 10 kV
Operating temperature	Junction temperature	T_J	- 40 to + 125	°C
Storage temperature		T_{STG}	- 55 to + 150	°C

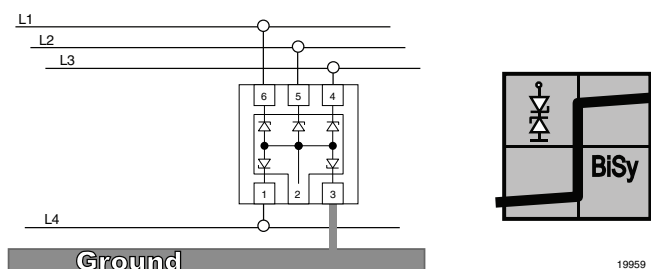
** Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

APPLICATION NOTE:

- a. With the VESD05A5A-HSF 5 different signal or data lines can be clamped to ground. Due to the different clamping levels in forward and reverse direction the VESD05A5A-HSF clamping behavior is Bidirectional and Asymmetrical (BiAs).



- b. If symmetrical clamping behaviour is required the VESD05A5A-HSF can also be used as a Bidirectional Symmetrical protection device protecting up to 4 lines. In this case pin no. 2 must not be connected.



ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	N_{lines}	-	-	5	lines
Reverse working voltage	at $I_R = 0.1\text{ }\mu\text{A}$	V_{RWM}	5	-	-	V
Max. reverse current	at $V_R = 5\text{ V}$	I_R	-	< 0.01	0.1	μA
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	V_{BR}	6	6.7	7.5	V
Reverse clamping voltage	at $I_{PP} = 1\text{ A}$	V_C	-	9	10	V
	at $I_{PP} = I_{PPM} = 2.5\text{ A}$	V_C	-	12	13	V
Forward clamping voltage	at $I_{PP} = 1\text{ A}$	V_F	-	2	2.5	V
	at $I_{PP} = I_{PPM} = 2.5\text{ A}$	V_F	-	3.2	4	V
Line capacitance	at $V_R = 0\text{ V}$; $f = 1\text{ MHz}$	C_D	-	13	15	pF
	at $V_R = 2.5\text{ V}$; $f = 1\text{ MHz}$	C_D	-	8	-	pF

Note

- BiAs mode (between pin 1, 3, 4, 5 or 6 and pin 2)

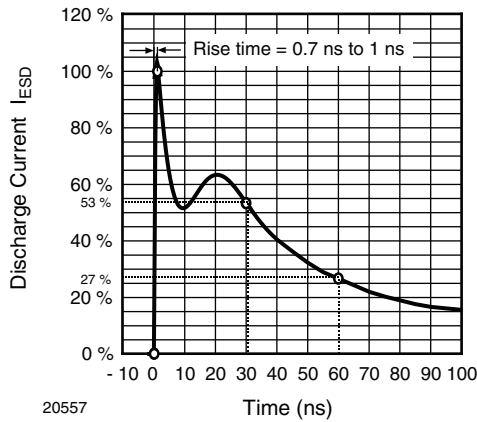
TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)


Fig. 1 - ESD Discharge Current Wave Form
acc. IEC 61000-4-2 (330 Ω /150 pF)

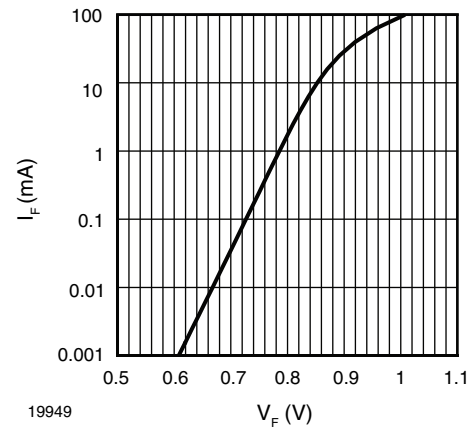


Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F

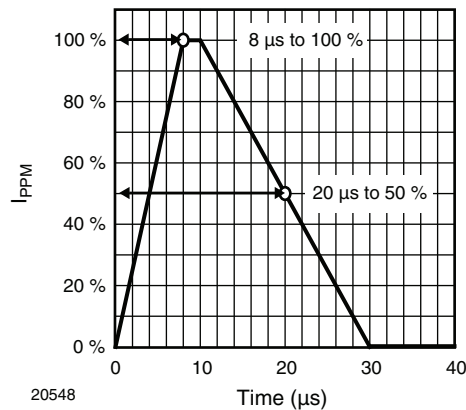


Fig. 2 - 8/20 μ s Peak Pulse Current Wave Form
acc. IEC 61000-4-5

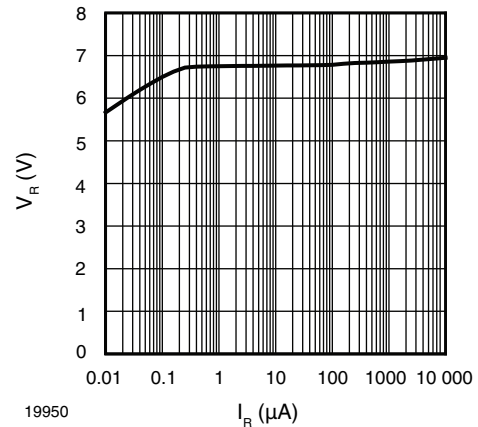


Fig. 5 - Typical Reverse Voltage V_R vs. Reverse Current I_R

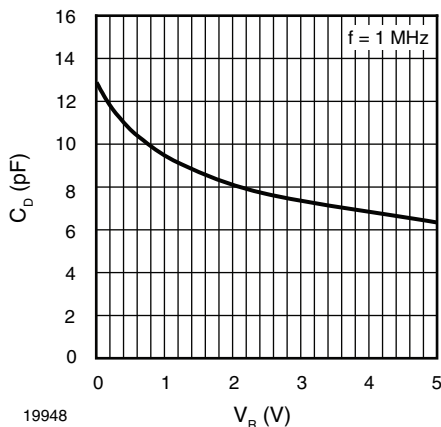


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

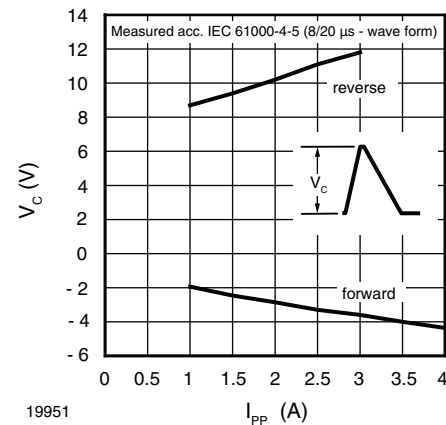


Fig. 6 - Typical Peak Clamping Voltage V_C vs.
Peak Pulse Current I_{PP}

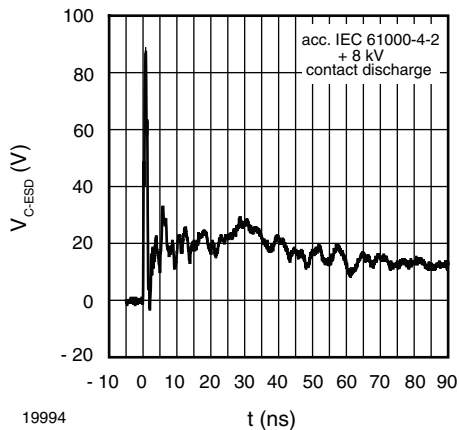


Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

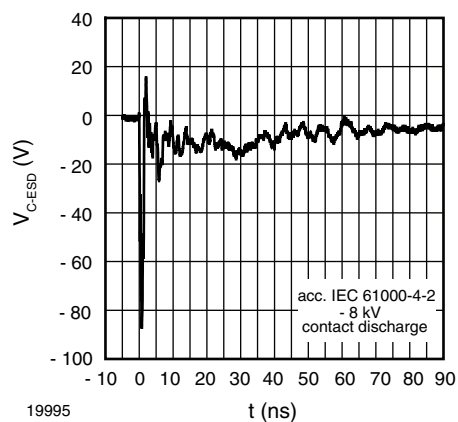


Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

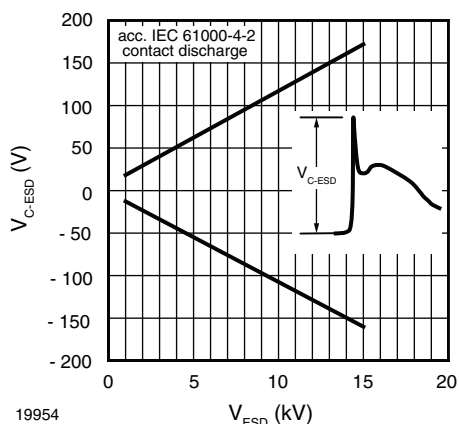
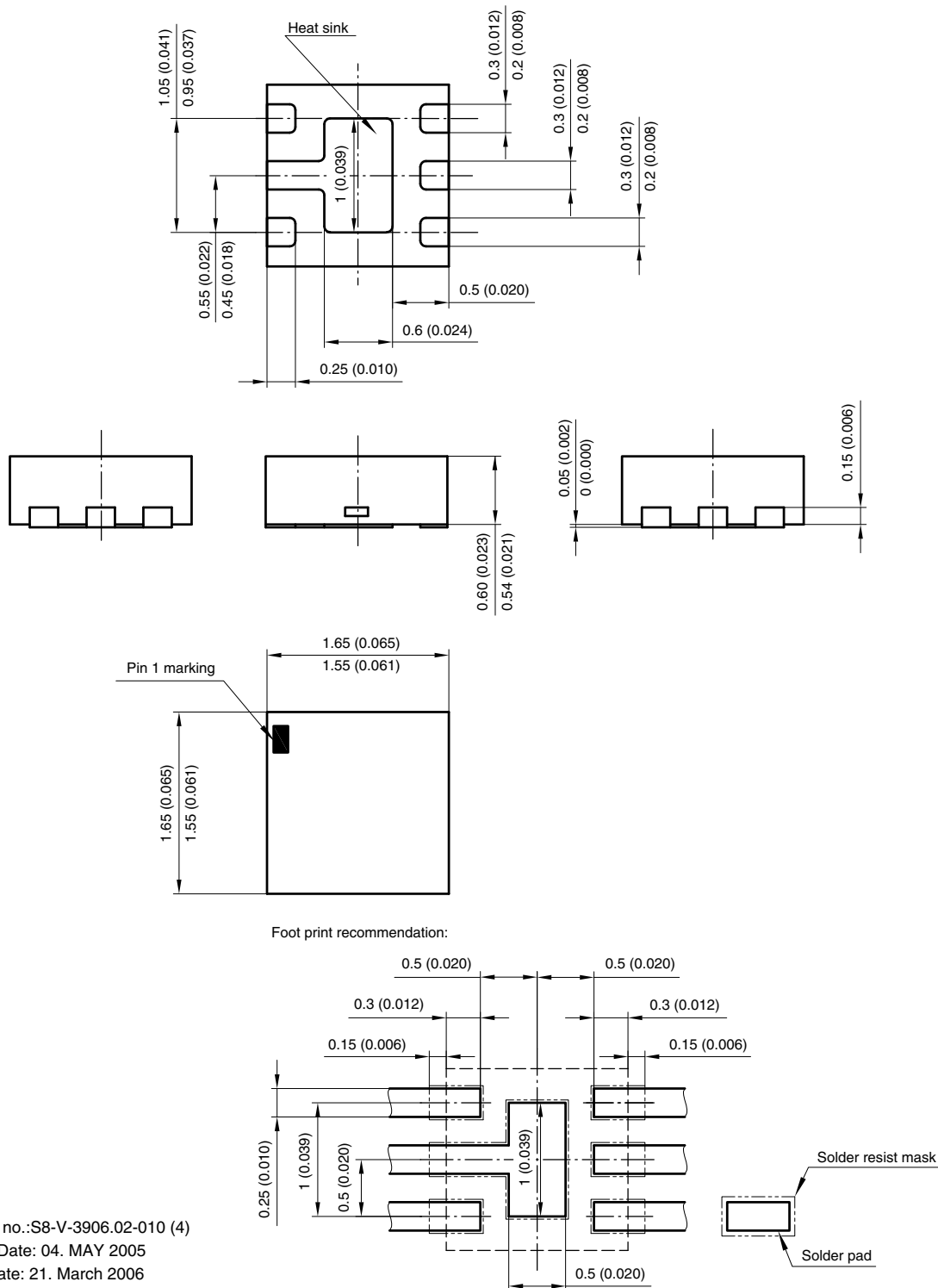


Fig. 9 - Typical max. Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

PACKAGE DIMENSIONS in millimeters (inches): **LLP75-6L**


Document no.: S8-V-3906.02-010 (4)
Created - Date: 04. MAY 2005
Rev. 4 - Date: 21. March 2006
20454



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