Reference Manual

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VCM-DAS-3

Analog Output & Digital I/O
Module for the PC/104 Bus





VERSALOGIC
CORPORATION



WWW.VERSALOGIC.COM

3888 Stewart Road
Eugene, OR 97402
(541) 485-8575
Fax (541) 485-5712

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MVCMDAS3

Product Release Notes

Rev 2 Release

Production release.

Rev 1 Release

Alpha. No customer release.

Support Page

The VCM-DAS-3 support page, at **http://www.VersaLogic.com/private/vcmdas3support.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

Note: This is a private page for VCM-DAS-3 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

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Introduction 1

Description

The VCM-DAS-3 is a PC/104-format data acquisition board that provides analog outputs and digital I/O for process control and other applications. Its features include:

- 16 analog voltage outputs with 12-bit resolution
- Multiple output ranges
- Software adjustable output ranges per channel
- Simultaneous or individual DAC update
- Power-up ranges set by jumpers in groups of eight, reset per channel by software
- Software calibration
- 16-bit or 8-bit ISA modes
- Read-back of DAC and SPAN codes
- Reset/power up to 0V outputs for all ranges
- External trigger
- +5V operation
- 24-channel digital I/O

The VCM-DAS-3 module provides 16 single-ended analog outputs and 24 digital I/O channels. Fully compatible at the register and connector level with the Diamond Systems Ruby-MM DAC board, VCM-DAS-3 also provides enhanced mode operation that extends its capabilities. In enhanced mode:

- Analog output ranges can be set for individual channels through software.
- Analog output and ranges can be read from individual channels.
- Specific analog channels can be placed into sleep mode to conserve power.
- Individual channels can be updated and read.
- Calibration can be performed with software.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 3.55" x 3.775" (PC/104 standard)

Storage Temperature:
-40° C to +85° C

Operating Temperature:
-40° C to +85° C

Power Requirements:
5V ± 10%

Analog Output:

Channels:	16 outputs
Resolution:	12 bits
Output Ranges:	Bipolar: ±10V, ±5V, ±2.5V, -2.5V to 7.5V Unipolar: 0 - 10V, 0 - 5V
Output Current:	±5 mA max per channel
Settling Time:	8 uS Typ. (±10V Range, 20V Step to ±1LSB)
Accuracy:	±1 LSB
Integral Nonlinearity:	±1 LSB
Differential Nonlinearity:	±1 LSB
Calibration:	One gain and one zero adjustment for all channels
Gain Temp. Coefficient:	±2 ppm/° C
Update Method:	Simultaneous, individual, or external trigger
Reset:	Outputs reset to 0V when board is jumpered for Enhanced Mode, mid-scale otherwise

Digital I/O:

Channels:	24
Compatibility:	CMOS / TTL, 82C55 Mode 0 only
Low Input Voltage:	-0.3V min., 0.8V max
High Input Voltage:	2.0V min., 5.5V max.
Low Output Voltage:	0.4V max.
High Output Voltage:	3.0V max.
Output Current:	+4 mA / -8 mA max.
Pull-up Resistor:	10 K Ohm
Reset:	All channels set to input mode

Software:

Operating Systems:	Compatible with most X86 operating systems including Windows 95/85/NT/CE/XP, QNX, VxWorks, and Linux
Driver Support:	No native drivers. Fully compatible with Diamond Systems drivers.

Compatibility:
PC/104 – Full compliance, 8-bit and 16-bit

Weight:
0.152 lbs (0.069 kg)

Specifications are subject to change without notice.

RoHS Compliance

The VCM-DAS-3 is RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Technical Support

If you are unable to solve a problem after reading this manual please visit the VCM-DAS-3 Product Support web page at **http://www.VersaLogic.com/private/vcmdas3support.asp**. If you have further questions, contact VersaLogic technical support at (541) 485-8575. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

VCM-DAS-3 Support Website

http://www.VersaLogic.com/private/vcmdas3support.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575.

Please provide the following information:

- Your name, the name of your company and your phone number
- The name of a technician or engineer that can be contacted if any questions arise.
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning.

Dimensions

The VCM-DAS-3 complies with all PC/104 standards. Dimensions are given below to help with pre-production planning and layout.

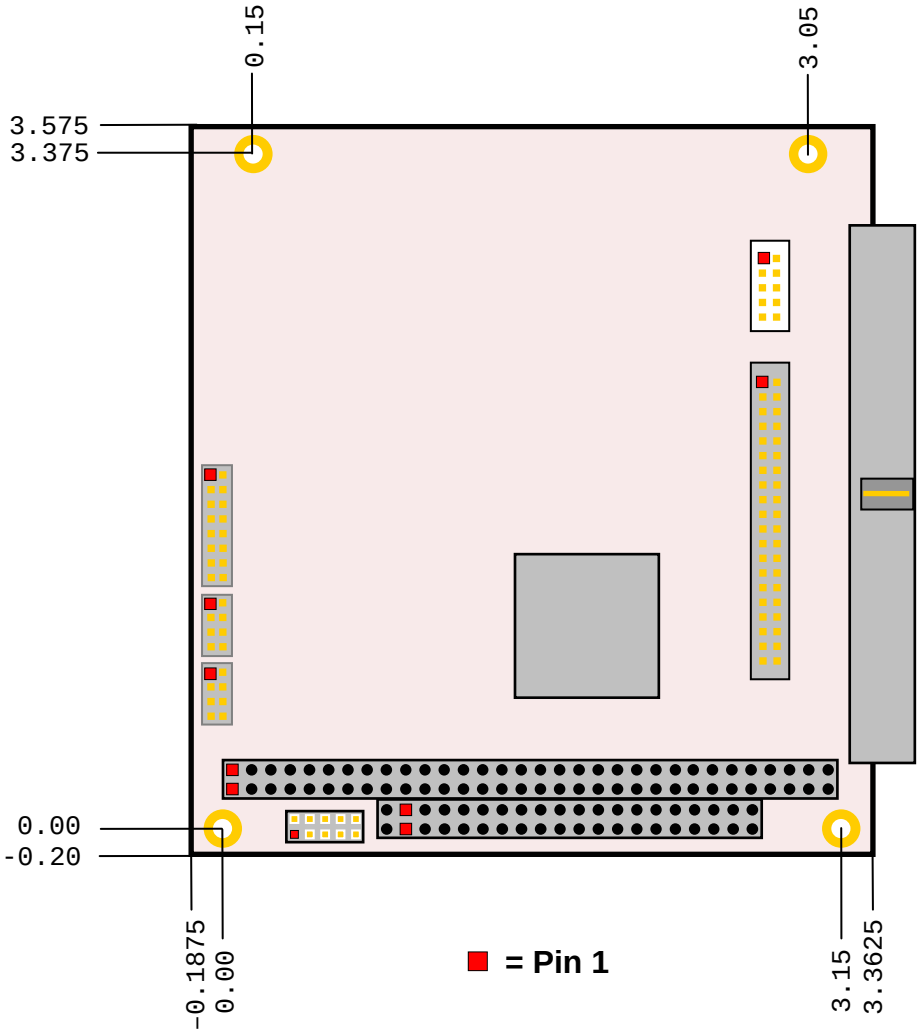


Figure 1. Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

SIDE PROFILE

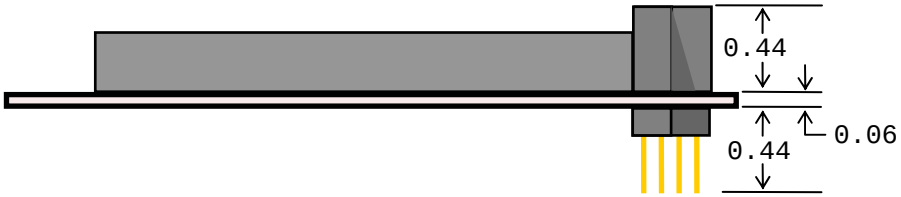


Figure 2. Side Profile
(Not to scale. All dimensions in inches.)

External Connectors

CONNECTOR LOCATIONS

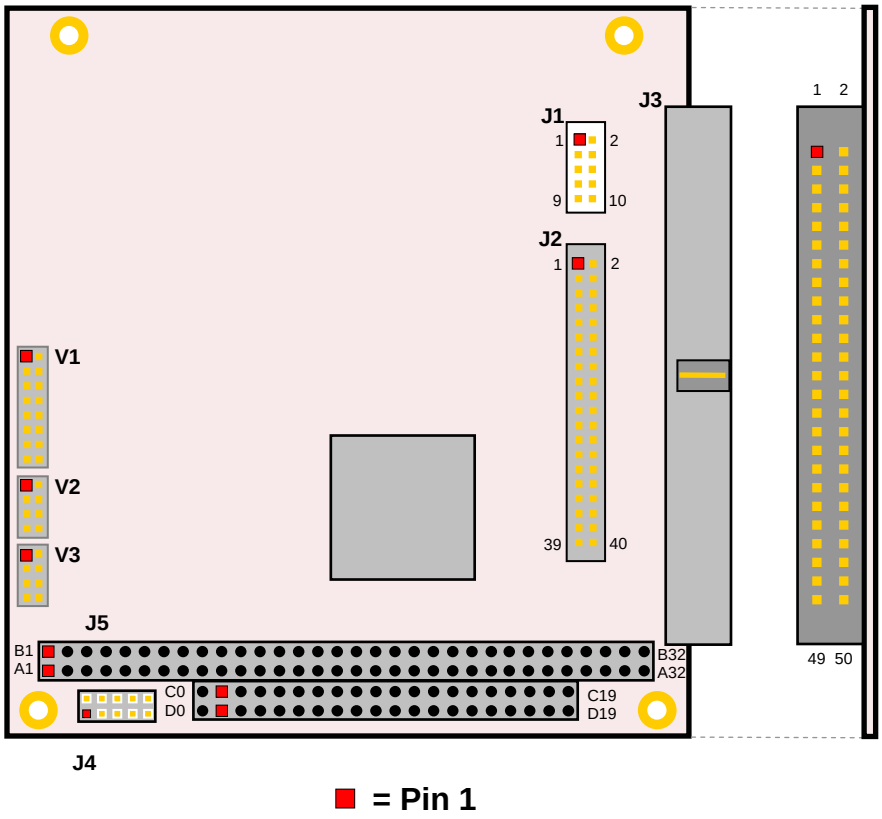


Figure 3. Connector Locations (Top)
(Not to scale.)

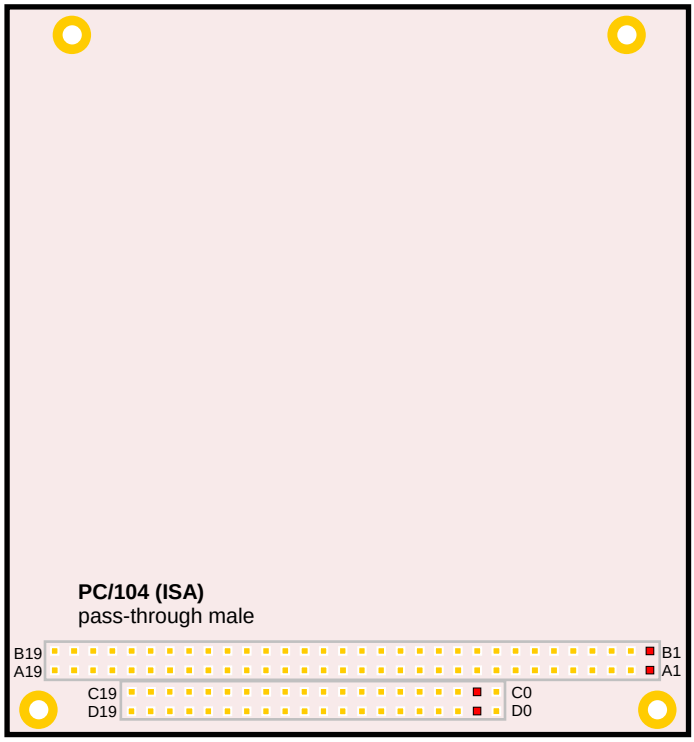


Figure 4. Connector Locations (Bottom)
(Not to scale.)

CONNECTOR FUNCTIONS AND INTERFACE CABLES

Table 1 provides information about the function, mating connectors, and transition cables for VCM-DAS-3 connectors. Page numbers indicate where a detailed pinout is available.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Page
J1	Digital I/O (A0-A7)	FCI 89361-710LF	–	2mm 10-pin IDC	8
J2	Analog Outputs, Digital I/O (B0-C7)	FCI 89361-740LF	CBR-4004A	12” 2mm 40-pin to 40-pin IDC to screw terminal board CBR-4004B	9
J3	Analog Outputs, Digital I/O	Standard 0.1” 50-pin cable-mount IDC	Diamond Systems C-50-18	Data acquisition, 50 conductor 0.1" ribbon cable	10
J4	Factory use only	–	–	–	–
J5	PC/104	AMP 1375795-2	–	–	–

J1 I/O CONNECTOR

The J1 I/O connector incorporates digital I/O signals A0 through A7. The pinout of the connector is shown in Table 2.

Table 2 J1 I/O Connector Pinout

J1 Pin	Signal Name	Function
1	Ground	Ground
2	DIO A7	Digital I/O A7
3	DIO A6	Digital I/O A6
4	DIO A5	Digital I/O A5
5	DIO A4	Digital I/O A4
6	DIO A3	Digital I/O A3
7	DIO A2	Digital I/O A2
8	DIO A1	Digital I/O A1
9	DIO A0	Digital I/O A0
10	Ground	Ground

J2 I/O CONNECTOR

The J2 I/O connector incorporates analog voltage outputs 0 through 15 and digital I/O channels B0 through C7. Table 3 illustrates the function of each pin and the pinout assignments to connectors on the CBR-4004 I/O board.

Table 3: J2 I/O Connector Pinout

J2 Pin	Signal Name	Function	CBR-4004 Connector	CBR-4004 Pin (Label)
1	VOUT 00	Analog Out Ch 0	**J1**	5 (IO1)
2	VOUT 01	Analog Out Ch 1	**Analog**	4 (IO2)
3	VOUT 02	Analog Out Ch 2	**Output**	3 (IO3)
4	VOUT 03	Analog Out Ch 3		2 (IO4)
5	Ground	Ground		1 (GND1)
6	VOUT 04	Analog Out Ch 4	**J2**	5 (IO5)
7	VOUT 05	Analog Out Ch 5	**Analog**	4 (IO6)
8	VOUT 06	Analog Out Ch 6	**Output**	3 (IO7)
9	VOUT 07	Analog Out Ch 7		2 (IO8)
10	Ground	Ground		1 (GND1)
11	VOUT 08	Analog Out Ch 8	**J3**	5 (IO9)
12	VOUT 09	Analog Out Ch 9	**Analog**	4 (IO10)
13	VOUT 10	Analog Out Ch 10	**Output**	3 (IO11)
14	VOUT 11	Analog Out Ch 11		2 (IO12)
15	Ground	Ground		1 (GND2)
16	VOUT 12	Analog Out Ch 12	**J4**	5 (IO13)
17	VOUT 13	Analog Out Ch 13	**Analog**	4 (IO14)
18	VOUT 14	Analog Out Ch 14	**Output**	3 (IO15)
19	VOUT 15	Analog Out Ch 15		2 (IO16)
20	Ground	Ground		1 (GND2)
21	DIO B7	Digital I/O B7	**J6**	5 (IO17)
22	DIO B6	Digital I/O B6	**Digital I/O B**	4 (IO18)
23	DIO B5	Digital I/O B5		3 (IO19)
24	DIO B4	Digital I/O B4		2 (IO20)
25	Ground	Ground		1 (GND3/PBRST#)
26	DIO B3	Digital I/O B3	**J7**	5 (IO21)
27	DIO B2	Digital I/O B2	**Digital I/O B**	4 (IO22)
28	DIO B1	Digital I/O B1		3 (IO23)
29	DIO B0	Digital I/O B0		2 (IO24)
30	Ground	Ground		1 (GND3)
31	DIO C7	Digital I/O C7	**J8**	5 (IO25)
32	DIO C6	Digital I/O C6	**Digital I/O C**	4 (IO26)
33	DIO C5	Digital I/O C5		3 (IO27)
34	DIO C4	Digital I/O C4		2 (I028)
35	Ground	Ground		1 (GND4)
36	DIO C3	Digital I/O C3	**J9**	5 (IO29)
37	DIO C2	Digital I/O C2	**Digital I/O C**	4 (IO30)
38	DIO C1	Digital I/O C1		3 (IO31)
39	DIO C0	Digital I/O C0*		2 (IO32)
40	Ground	Ground		1 (GND4)

* Pin 39 can also used as an external trigger for updating DAC channels. See External Trigger Update.

J3 I/O CONNECTOR

The J3 I/O connector incorporates analog voltage outputs 0 through 15 and digital I/O channels A0 through C7. The pinout of the connector is shown in Table 4.

Note This connector is compatible with Diamond Systems' cable C-50-18. Any standard 0.1" 50-pin cable-mount IDC connector will mate with this connector.

Table 4: J3 I/O Connector Pinout

J3 Pin	Signal Name	Function	J3 Pin	Signal Name	Function
1	Ground	Ground	26	DIO A6	Digital I/O A6
2	VOUT 00	Analog Output 0	27	DIO A5	Digital I/O A5
3	Ground	Ground	28	DIO A4	Digital I/O A4
4	VOUT 01	Analog Output 1	29	DIO A3	Digital I/O A3
5	Ground	Ground	30	DIO A2	Digital I/O A2
6	VOUT 02	Analog Output 2	31	DIO A1	Digital I/O A1
7	Ground	Ground	32	DIO A0	Digital I/O A0
8	VOUT 03	Analog Output 3	33	DIO B7	Digital I/O B7
9	Ground	Ground	34	DIO B6	Digital I/O B6
10	VOUT 04	Analog Output 4	35	DIO B5	Digital I/O B5
11	Ground	Ground	36	DIO B4	Digital I/OB4
12	VOUT 05	Analog Output 5	37	DIO B3	Digital I/O B3
13	Ground	Ground	38	DIO B2	Digital I/O B2
14	VOUT 06	Analog Output 6	39	DIO B1	Digital I/O B1
15	Ground	Ground	40	DIO B0	Digital I/O B0
16	VOUT 07	Analog Output 7	41	DIO C7	Digital I/O C7
17	VOUT 08	Analog Output 8	42	DIO C6	Digital I/O C6
18	VOUT 09	Analog Output 9	43	DIO C5	Digital I/O C5
19	VOUT 10	Analog Output 10	44	DIO C4	Digital I/O C4
20	VOUT 11	Analog Output 11	45	DIO C3	Digital I/O C3
21	VOUT 12	Analog Output 12	46	DIO C2	Digital I/O C2
22	VOUT 13	Analog Output 13	47	DIO C1	Digital I/O C1
23	VOUT 14	Analog Output 14	48	DIO C0	Digital I/O C0*
24	VOUT 15	Analog Output 15	49	V5_0	Protected +5.0 Volts
25	DIO A7	Digital I/O A7	50	Ground	Ground

* Pin 48 can also used as an external trigger for updating DAC channels. See External Trigger Update.

Installation

HARDWARE ASSEMBLY

The VCM-DAS-3 uses pass-through PC/104 (ISA) connectors so that expansion modules can be added to the top or bottom of the stack. PC/104 modules must not be positioned between the CPU board and any PC/104-*Plus* (PCI) modules on the stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Standoffs are secured to the top circuit board using four pan head screws. Standoffs and screws are available as part number VL-HDW-101.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack. Use caution when using the extractor tool not to damage any board components.

STACK ARRANGEMENT EXAMPLE

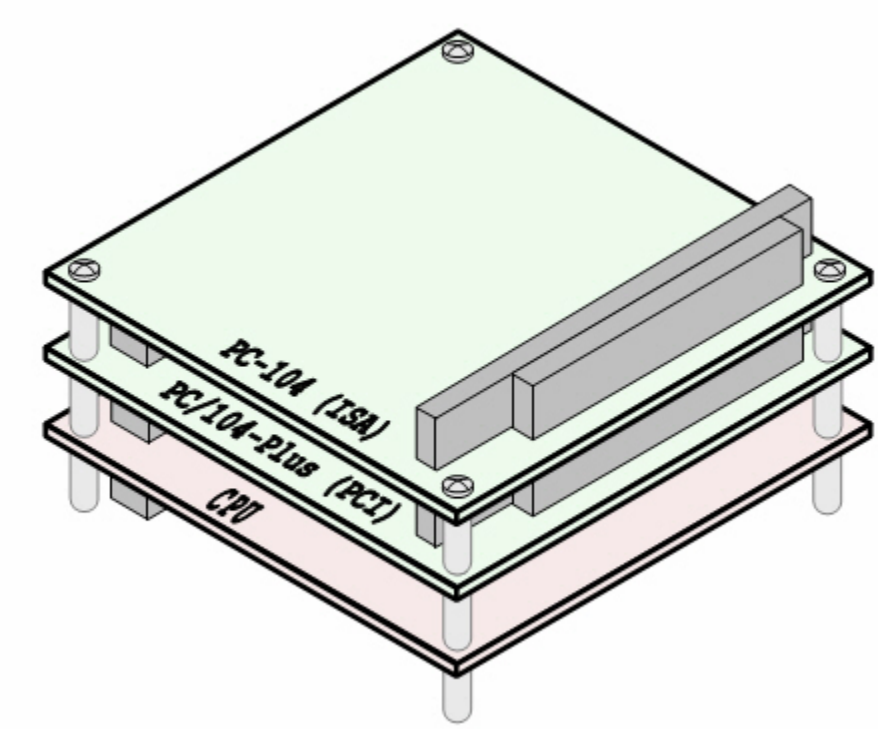


Figure 5. Stack Arrangement

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION

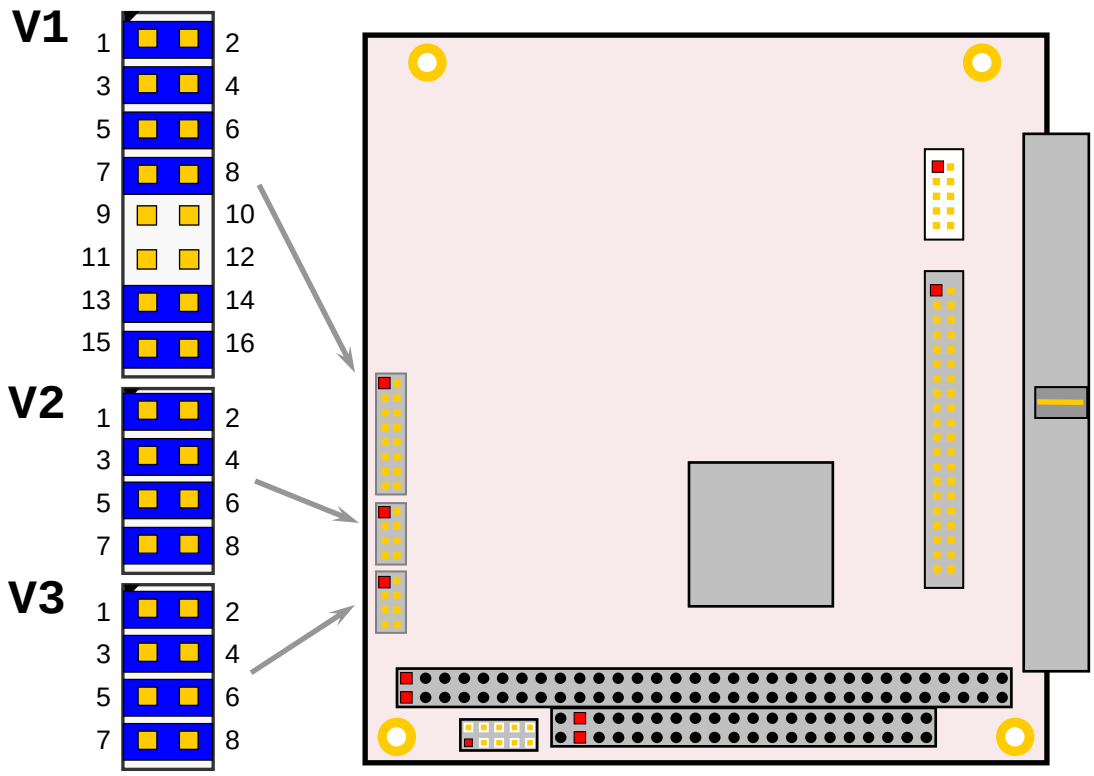


Figure 6. Jumper Block Locations

JUMPER SUMMARY

Table 5: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[15-16]	**Bit Mode Selector** In = 16-bit ISA Transactions Out = 8-bit ISA Transactions 8-bit mode forces the VCM-DAS-3 to respond with 8-bit transactions. This mode is required when using the board on an 8-bit bus. The 16-bit mode allows both 8 and 16-bit transactions.	In	15
V1[13-14]	**Enhanced/Compatible Mode Selector** In = Enhanced Mode Out = Compatible Mode Enhanced mode provides extra DAC functions, which should operate properly in applications designed for the Diamond Systems Ruby-MM board.	In	15
V1 [11-12] to [1-2]	**Base Address Selector** – A base address of 0x000 to 0x3F0 can be selected. The last digit is always 0. First Digit [11-12] 9-10] 0 In Out 1 Out In 2 Out In 3 Out Out Second Digit [7-8] [5-6] [3-4] [1-2] 0 In In In In 1 In In In Out 2 In In Out In 3 In In Out Out 4 In Out In In 5 In Out In Out 6 In Out Out In 7 In Out Out Out 8 Out In In In 9 Out In In Out A Out In Out In B Out In Out Out C Out Out In In D Out Out In Out E Out Out Out In F Out Out Out Out	Out, Out, In, In, In, In, (0x300)	15
V2	**A/D Channel 0-7 Span Range Selector** [7-8] [5-6] [3-4] [1-2] 0V to +5V In In In In 0V to +10V In In In Out -5V to +5V In In Out In -10V to +10V In In Out Out -2.5V to +2.5V In Out In In -2.5V to +7.5V In Out In Out These jumpers set the initial power up span ranges for A/D channels 0-7.	In, In, In, In (0V to +5V)	26
V3	**A/D Channel 8-16 Span Range Selector** [7-8] [5-6] [3-4] [1-2] 0V to +5V In In In In 0V to +10V In In In Out -5V to +5V In In Out In -10V to +10V In In Out Out -2.5V to +2.5V In Out In In -2.5V to +7.5V In Out In Out These jumpers set the initial power up span ranges for A/D channels 8-16.	In, In, In, In (0V to +5V)	26

Base Address Configuration

As shipped, the VCM-DAS-3 is configured for a base address of 0x300. The card occupies up to 16 consecutive I/O addresses in enhanced mode (only eight I/O addresses in compatible mode). Jumper block V1[11-12] through V1[1-2] is used set the base address.

The base address can be configured from 0x000 to 0x3F0 on any 10h address boundary. Figure 7 shows how to set the address selector jumpers for the appropriate upper and middle hex digits of the three digit base address (for example, the “3” and “1” of base address 0x310).

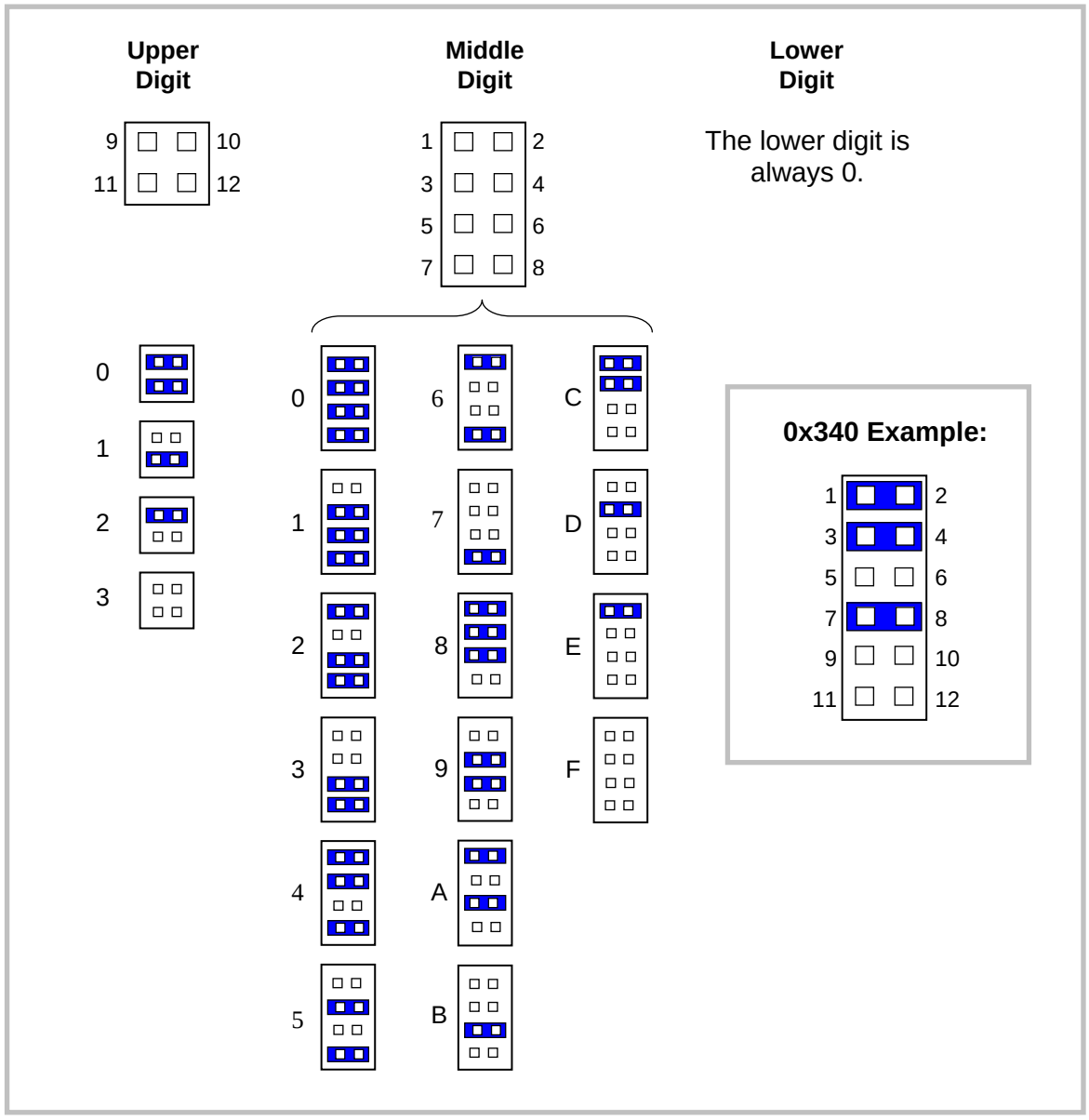


Figure 7. Base Address Jumpers

Bit Mode Configuration

The VCM-DAS-3 can operate using 8-bit or16-bit ISA transactions. For compatibility with 8-bit ISA buses, you must set the VCM-DAS-3 to use 8-bit ISA transactions.

Jumper V1[15-16] selects the bit mode. When a jumper is present, the board will operate on either 16-bit or 8-bit ISA bus. When the jumper is removed, the board is forced to perform only 8-bit ISA transactions. The default setting is jumper installed.

Enhanced Mode Configuration

Jumper V1[13-14] enables you to select between compatible or enhanced modes. A jumper installed on V1[13-14] sets the VCM-DAS-3 to enhanced mode. When no jumper is installed, the board operates in compatible mode. The default mode is enhanced.

In compatible mode, eight registers are decoded for use, including all the registers needed for DAC and DIO operations and control. These registers are identical to those provided by the Diamond Systems Ruby-MM, and enable full compatibility in applications designed with that board. In this mode, analog output ranges are determined by jumper settings (in two banks of eight registers) and are not software programmable.

Enhanced mode provides three additional registers for more specific control of DAC operations. The ENH_CON register enables you to set spans for specific DAC channels, read DAC data and spans, set DAC channels to sleep mode for power savings, and set and read the gain for all channels.

Power-up Span Range Configuration

Jumper block V2 sets the initial span range for A/D channels 7-0. Jumper block V3 sets the initial span range for A/D channels 15-8. (See Table 5 for a list of settings.) The span range can be set differently for each 8-channel bank. Within each bank, all channels will have the same initial span range; however, in enhanced mode, ranges can be set individually for each channel via software.

Two unipolar output ranges (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and –2.5V to 7.5V) are available.

I/O Port Mapping

In enhanced mode, the VCM-DAS-3 operates occupies 16 ports in the I/O map. Eleven ports are mapped to functional registers, and the remaining five ports are decoded by the board and cannot be used by other PC/104 modules.

Table 6: Enhanced Mode I/O Port Addresses

Write Register	Read Register	I/O Port Address	As Shipped Address
–	PLDVER	Base Address + F	0x30F
–	–	Base Address + E	0x30E
–	–	Base Address + D	0x30D
–	–	Base Address + C	0x30C
–	–	Base Address + B	0x30B
ENCTRL	ENCTRL	Base Address + A	0x30A
ENDATHI	ENDATHI	Base Address + 9	0x309
ENDATLO	ENDATLO	Base Address + 8	0x308
DIOCTRL	DIOCTRL	Base Address + 7	0x307
DIOC	DIOC	Base Address + 6	0x306
DIOB	DIOB	Base Address + 5	0x305
DIOA	DIOA	Base Address + 4	0x304
EXTRIG	EXTRIG	Base Address + 3	0x303
DACSEL	–	Base Address + 2	0x302
DACHI	DACALL1	Base Address + 1	0x301
DACLO	DACALL0	Base Address + 0	0x300

In compatible mode, the VCM-DAS-3 operates occupies eight ports in the I/O map, all of which are functional.

Table 7: Compatible Mode I/O Port Addresses

Write Register	Read Register	I/O Port Address	As Shipped Address
DIOCTRL	DIOCTRL	Base Address + 7	0x307
DIOC	DIOC	Base Address + 6	0x306
DIOB	DIOB	Base Address + 5	0x305
DIOA	DIOA	Base Address + 4	0x304
EXTRIG	EXTRIG	Base Address + 3	0x303
DACSEL	–	Base Address + 2	0x302
DACHI	DACALL1	Base Address + 1	0x301
DACLO	DACALL0	Base Address + 0	0x300

I/O PORT REGISTER FUNCTIONS

The following table lists the functions assigned to each read and write I/O port register.

Table 8: Register Functions

Write Register	Description	Page
ENCTRL	Enhanced control	18
ENDATHI	Enhanced Data MSB	19
ENDATLO	Enhanced Data LSB	19
DIOCTRL	Digital I/O control register	20
DIOC	Digital I/O port C data	22
DIOB	Digital I/O port B data	22
DIOA	Digital I/O port A data	22
EXTRIG	External trigger enable	23
DACSEL	DAC channel register	24
DACHI	Analog output most significant data byte (MSB).	25
DACLO	Analog output least significant data byte (LSB).	25

Read Register	Description	Page
ENCTRL	Enhanced control	18
ENDATHI	Enhanced Data MSB	19
ENDATLO	Enhanced Data LSB	19
DIOCTRL	Digital I/O control register	20
DIOC	Digital I/O port C data	21
DIOB	Digital I/O port B data	21
DIOA	Digital I/O port A data	21
EXTRIG	External trigger enable	23
DACALL1	Update all DACs simultaneously	25
DACALL0	Update all DACs simultaneously	25

Enhanced Mode Registers

Setting the VCM-DAS-3 to enhanced mode enables three additional functional registers. To enable enhanced mode, install a jumper on pins V1[13-14].

ENHANCED CONTROL REGISTER

ENCTRL (Write) 030Ah

7	6	5	4	3	2	1	0
CTRL3	CTRL2	CTRL1	CTRL0	SEL3	SEL2	SEL1	SEL0

Table 9: Register Bit Assignments

Bit	Mnemonic	Description
7-4	CTRL	**Enhanced DAC Control** – These bits select operations to be performed on specific DAC channels. **CTRL3 CTRL2 CTRL1 CTRL0 Function** 0 0 0 0 Set Span: 0V to +5V 0 0 0 1 Set Span: 0V to +10V 0 0 1 0 Set Span: -5V to +5V 0 0 1 1 Set Span: -10V to +10V 0 1 0 0 Set Span: -2.5V to +2.5V 0 1 0 1 Set Span: -2.5V to +7.5V 0 1 1 0 (Reserved. Do not use.) 0 1 1 1 (Reserved. Do not use.) 1 0 0 0 Read DAC 1 0 0 1 Read Span 1 0 1 0 Load DAC (LDAC) 1 0 1 1 DAC Sleep 1 1 0 0 (Reserved. Do not use.) 1 1 0 1 (Reserved. Do not use.) 1 1 1 0 Set Gain 1 1 1 1 Read Gain
3-0	SEL	**Channel Selection** – These bits select the DAC channel for the operation. **SEL3 SEL2 SEL1 SEL0 Channel** 0 0 0 0 0 0 0 0 1 1 0 0 1 0 2 0 0 1 1 3 0 1 0 0 4 0 1 0 1 5 0 1 1 0 6 0 1 1 1 7 1 0 0 0 8 1 0 0 1 9 1 0 1 0 10 1 0 1 1 11 1 1 0 0 12 1 1 0 1 13 1 1 1 0 14 1 1 1 1 15

ENCTRL (Read) 030Ah

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	READY

Table 10: Register Bit Assignments

Bit	Mnemonic	Description
7-1	–	Enhanced DAC Control
0	Ready	**Ready** – Factory use only. 0 = SPI transaction in progress 1 = SPI transaction complete The internal logic of the SPI state machine is much faster than the ISA bus speed, which limits the usefulness of his bit for anything other than factory debugging of the design.

ENHANCED MODE DATA REGISTERS

ENDATHI MSB (Read) 0309h

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8

ENDATLO LSB (Read/Write) 0308h

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The data format of these registers depends on the operation executed in the ENCTRL register. See the sections listed below for information on data formats for specific operations.

Operation	CTRL Code (ENCTRL)	Page
Read DAC	08h	34
Read Span	09h	34
Set Gain	0Eh	33
Read Gain	0Fh	33

Digital I/O Control Register

DIOCTRL (Read/Write) 0307h

7	6	5	4	3	2	1	0
–	–	–	DIRA	DIRCHI	–	DIRB	DIRCLO

Table 11: DIOCTRL Bit Assignments

Bit	Mnemonic	Description
7-5	–	Unused. These bits have no function.
4	DIRA	**DIO Port A Direction** – These bits control the direction of DIO port A (A7-A0). 0 = Output 1 = Input
3	DIRCHI	**DIO Port C MSB Direction** – These bits control the direction of the upper half of DIO port C (C7-C4). 0 = Output 1 = Input
2	–	Unused. This bit has no function.
1	DIRB	**DIO Port B Direction** – These bits control the direction of DIO port B (B7-B0). 0 = Output 1 = Input
0	DIRCLO	**DIO Port C LSB Direction** – These bits control the direction of the lower half of DIO port C (C3-C0). 0 = Output 1 = Input

Digital I/O Data Registers

DIGITAL INPUT REGISTERS

DIOA (Read) 0304h

D7	D6	D5	D4	D3	D2	D1	D0
DIO A7	DIO A6	DIO A5	DIO A4	DIO A3	DIO A2	DIO A1	DIO A0

DIOB (Read) 0305h

D7	D6	D5	D4	D3	D2	D1	D0
DIO B7	DIO B6	DIO B5	DIO B4	DIO B3	DIO B2	DIO B1	DIO B0

DIOC (Read) 0306h

D7	D6	D5	D4	D3	D2	D1	D0
DIO C7	DIO C6	DIO C5	DIO C4	DIO C3	DIO C2	DIO C1	DIO C0

Table 12: Digital Input Data Bit Assignments

Bit	Mnemonic	Description
7-0	DIO A7-A0 DIO B7-B0 DIO C7-C0	**Digital Input Data** – Data read from these registers returns the current input state of the digital port signals on connectors J1 and J2. Data is not inverted. When a signal line is high, the bit reads as 1; when a signal line is low, the bit reads as 0. To operate a port in input mode, you must first set the direction of the port to input by setting the appropriate bit in the DIOCTRL register. If a port is operated in output mode, the registers can be used to read back the logic state of the output lines. Normally, the data read would be the same as the data written to the output registers; however, if an output line is stuck high or shorted to ground, the fault will be reflected in the feedback data.

DIGITAL OUTPUT REGISTERS

DIOC (Write) 0306h

D7	D6	D5	D4	D3	D2	D1	D0
DIO C7	DIO C6	DIO C5	DIO C4	DIO C3	DIO C2	DIO C1	DIO C0

DIOB (Write) 0305h

D7	D6	D5	D4	D3	D2	D1	D0
DIO B7	DIO B6	DIO B5	DIO B4	DIO B3	DIO B2	DIO B1	DIO B0

DIOA (Write) 0304h

D7	D6	D5	D4	D3	D2	D1	D0
DIO A7	DIO A6	DIO A5	DIO A4	DIO A3	DIO A2	DIO A1	DIO A0

Table 13: Digital Output Data Bit Assignments

Bit	Mnemonic	Description
D7-D0	DIO A7-A0 DIO B7-B0 DIO C7-C0	**Digital Output Data** – Data written to these registers is driven onto the digital port signals on connectors J1 and J2. Data is not inverted. When a bit is set to 1, the signal line is driven high; when a bit is reset to 0, the signal line is driven low. To operate a port in output mode, you must first set the direction of the port to output by clearing the appropriate bit in the DIOCTRL register.

External Trigger Enable Register

EXTRIG (Read/Write) 0303h

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	TRIGEN

Table 14: EXTRIG Bit Assignments

Bit	Mnemonic	Description
7-1	–	Unused. These bits have no function.
0	TRIGEN	**Trigger Enable** – When the external trigger is enabled, digital I/O line C0 will update all DACs simultaneously when it is brought low. This can be done either by an external signal, when C0 is in input mode, or in software, when C0 is in output mode. If using an external trigger, make sure that the lower half of Port C is in input mode. 1 = Enable 0 = Disable

Analog Output Data Registers

DAC CHANNEL SELECT REGISTER

DACSEL (Write) 0302h

7	6	5	4	3	2	1	0
–	–	–	–	SEL3	SEL2	SEL1	SEL0

Table 15: DACSEL Bit Assignments

Bit	Mnemonic	Description
7-4	–	Unused. These bits have no function.
3-0	SEL	**Channel Selection** – These bits select the DAC channel upon which digital output functions will be performed.

SEL3	SEL2	SEL1	SEL0	Selected Channel
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

DAC WRITE REGISTERS

DACHI (Write) 0301h

7	6	5	4	3	2	1	0
–	–	–	–	DA11	DA10	DA9	DA8

DACLO (Write) 0300h

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA4	DA1	DA0

Table 16: DACHI Bit Assignments

Bit	Mnemonic	Description
7-4	–	Unused. These bits have no function.
3-0	DACHI	**Analog Output Data MSB** – Digital-to-analog data bits DA11-DA8. DA11 is the most significant bit. This register is used with the DACLO register to form the 12-bit analog output value.

Table 17: DACLO Bit Assignments

Bit	Mnemonic	Description
7-0	DACLO	**Analog Output DATA LSB** – Digital-to-analog data bits DA7-DA0. DA0 is the least significant bit. This register is used with the DACHI register to form the 12-bit analog output value.

DAC READ REGISTERS

DACALL1 (Read) 0301h

7	6	5	4	3	2	1	0
–	–	–	–	DA11	DA10	DA9	DA8

DACALL0 (Read) 0300h

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA4	DA1	DA0

Reading from these locations updates all DACs to the values written to them. Only DACs with new data written to them will change. The remaining channels will retain their current values.

Analog Output Ranges and Resolution

VCM-DAS-3 provides six different analog output ranges (shown in Table 18), including four bipolar ranges and two unipolar ranges. One of the bipolar ranges (-2.5 to +7.5V) is asymmetrical. Power-up ranges are determined by jumper settings (see Power-up Span Range Configuration). Ranges for individual channels can be set by software using the Set Span command, available in enhanced mode.

The resolution for any output range is equal to the maximum possible range of output voltages divided by the maximum number of possible steps. For a 12-bit D/A converter, the maximum number of steps is 4096. The actual output codes range from 0 to 4095, which is the full range of possible 12-bit binary numbers. (See Analog Output Data Representation.)

The table below shows the analog output ranges and resolutions available on the VCM-DAS-3. Negative full scale refers to the output voltage for a code of 0, and positive full scale refers to the output voltage for a code of 4095.

Table 18: Analog Output Ranges and Resolution

Full-Scale Voltage	Bipolar or Unipolar	Range Name	Negative Full Scale	Positive Full Scale	Resolution (1 LSB)
10V	Bipolar	±10V	-10V	+9.9951V	4.88mV
5V	Bipolar	±5V	-5V	+4.9963V	2.44mV
2.5V	Bipolar	±2.5V	-2.5V	+2.4988V	1.22mV
7.5V	Bipolar	-2.5 to +7.5V	-2.5V	+7.4963V	2.44mV
10V	Unipolar	0-10V	0V	+9.9976V	2.44mV
5V	Unipolar	0-5V	0V	+4.9988V	1.22mV

SETTING A SPAN RANGE

Power-up span ranges are determined for blocks of channels by jumper settings (see Power-up Span Range Configuration); however, in enhanced mode, you can set the span range for any individual channel. To perform a Set Span operation:

1. Write the appropriate Set Span code (see Enhanced Control Register) to the CTRL field of the ENCTRL register at I/O port 0x30A, combined with the channel number in the SEL bits of the same register.
2. Perform an LDAC operation by writing Ah to the CTRL field of the ENCTRL register, combined with the channel number in the SEL field of the same register.

Analog Output Data Representation

Two different digital coding schemes are used for analog output operations.

- For unipolar output ranges (positive voltages only), straight binary coding is used.
- For bipolar output ranges (both positive and negative voltages), offset binary coding is used.

STRAIGHT BINARY CODING

The formulas for calculating analog or straight binary digital values are given by:

$$\text{Digital} = \frac{\text{Analog}}{\text{Step}} \qquad \text{Analog} = \text{Step} \times \text{Digital}$$

Where:

Analog = Applied voltage

Digital = A/D conversion data

Step = 0.00244140625 for 0-10V range
0.00122070313 for 0-5V range
0.0006103515625 for 0-2.5V range

Table 19: Straight Binary Data Format

0-2.5V Range	0-5V Range	0-10V Range	Hex	Decimal	Comment
+2.5000	+5.0000	+10.0000	–	–	Out of range
+2.4993	+4.9987	+9.9975	FFFh	4095	Maximum positive voltage
+1.2500	+2.5000	+5.0000	800h	2048	Positive half scale
+0.6250	+1.2500	+2.5000	400h	1024	Positive quarter scale
+0.00061	+0.00122	+0.00244	001h	1	Positive 1 LSB
0.0000	0.0000	0.0000	000h	0	Zero (ground output)

OFFSET BINARY CODING

The formulas for calculating analog or straight binary digital values are given by:

$$\text{Digital} = \left[\frac{\text{Analog}}{\text{Step}} \right] + \text{Offset}_1 \qquad \text{Analog} = (\text{Step} \times \text{Digital}) - \text{Offset}_2$$

Where:

Analog = Applied voltage

Digital = A/D conversion data

Offset_1 = 2048 for symmetrical ranges
1024 for asymmetrical range

Step = 0.00122070313 for ±2.5V range
0.00244140625 for ±5V and -2.5 to +7.5 ranges
0.0048828125 for ±10V range

Offset_2 = 2.5 for ±2.5V and -2.5 to +7.5 ranges
5 for ±5V
10 for ±10V range

Table 20: Offset Binary Data Format – Symmetrical Ranges

±2.5V Output Voltage	±5V Output Voltage	±10V Output Voltage	Hex	Decimal	Comment
+2.5000	+5.0000	+10.0000	–	–	Out of range
+2.4987	+4.9975	+9.9951	FFFh	4095	Maximum positive voltage
+1.2500	+2.5000	+5.0000	C00h	3072	Positive half scale
+0.6250	+1.2500	+2.5000	A00h	2560	Positive quarter scale
+0.00122	+0.00244	+0.00488	801h	2049	Positive 1 LSB
0.0000	0.0000	0.0000	800h	2048	Zero (ground voltage)
-0.00122	-0.00244	-0.00488	7FFh	2047	Negative 1 LSB
-0.6250	-1.2500	-2.5000	600h	1536	Negative quarter scale
-1.2500	-2.5000	-5.0000	400h	1024	Negative half scale
-2.5000	-5.0000	-10.0000	000h	0	Maximum negative voltage

Table 21: Offset Binary Data Format – Asymmetrical Range

-2.5 to +7.5 Output Voltage	Hex	Decimal	Comment
+7.5000	–	–	Out of range
+7.4975	FFFh	4095	Maximum positive voltage
+3.7500	A00h	2560	Positive half scale
+1.8750	700h	1792	Positive quarter scale
+0.00244	401h	1025	Positive 1 LSB
0.0000	400h	1024	Zero (ground voltage)
-0.00244	3FFh	1023	Negative 1 LSB
-0.6250	300h	768	Negative quarter scale
-1.2500	200h	512	Negative half scale
-2.5000	000h	0	Maximum negative voltage

Analog Output Programming

Analog output voltages can be programmed either directly or with the use of a driver. This section describes how to modify analog output voltages directly.

VCM-DAS-3 analog outputs have a resolution of 12 bits. Data is written to the board in 8-bit bytes, so two bytes must be used to write a single analog output value. These bytes are referred to as the least significant byte (LSB) and the most significant byte (MSB).

When modifying analog outputs, one or multiple channels can be updated simultaneously. For this reason, the update operation is separate from the data write operation.

To change an analog output on one or more channels:

1. Write the channel number to the DACSEL register at I/O port 0x302.
2. Write the LSB to the DACLO register at I/O port 0x300.
3. Write the MSB to the DACHI register at I/O port 0x301.
4. Repeat steps 1-3 for each channel to be changed.
5. Finally, update all channels simultaneously by reading the DACLO register.

External Trigger Update

An external trigger is enabled by setting the TRIGEN bit in the EXTRIG register at I/O port 0x303. When the external trigger is enabled, digital I/O line C0 will update all DACs simultaneously when it is brought low. This can be done either by an external signal, when C0 is in input mode, or in software, when C0 is in output mode. If using an external trigger, make sure that the lower half of Port C is in input mode.

When the trigger signal is low, DACs are updated as soon as new data is written to them. When the trigger signal is high, the DAC voltage outputs remain fixed, unless updated in software.

Load DAC Operation

The Load DAC (LDAC) operation provides a method for updating a single DAC channel. To perform the LDAC operation, write Ah to the CTRL field of the ENCTRL register at I/O port 0x30A, combined with the channel number in the SEL field of the same register.

To change an analog output a single channel using the LDAC operation:

1. Write the channel number to the DACSEL register at I/O port 0x302.
2. Write the LSB to the DACLO register at I/O port 0x300.
3. Write the MSB to the DACHI register at I/O port 0x301.
4. Perform the LDAC operation for the selected channel.

Analog Output Code Example

The following Visual BASIC code illustrates how to operate the analog output feature of the VCM-DAS-3.

```
FUNCTION LIB_das3aout (BYVAL channel, BYVAL range, BYVAL voltage)
'
'Description:   This function performs an
'               analog output operation to the
'               specified channel.
'
'Entry:         channel: analog output channel (0 to 15)
'               range:   0=5V, 1=10V, 2=+/-5V, 3=+/-10V
'                        4=2.5V, 5=-2.5V/+7.5V
'               voltage: analog output voltage (within range)
'
'Returns:       0 if no errors
'               1 if timeout occurs
'
'Examples:      'Output +5.000V on channel 0
'               x = LIB_das3aout (0,1,5.000)
'
'               'Output -7.500V on channel 1
'               x = LIB_das3aou (1, 3, -7.500)
'
'Enhanced Control Register (BASE + 0xA)
'                  D7   D6   D5   D5   D3   D2   D1   D0
'                  EC3  EC2  EC1  EC0  ---DAC CHANNEL---
'                  ====================================
'   0V to +5V      0    0    0    0
'   0V to +10V     0    0    0    1
'  -5V to +5V      0    0    1    0
' -10V to +10V     0    0    1    1
'-2.5V to +2.5V    0    1    0    0
'-2.5V to +7.5V    0    1    0    1

DIM value AS INTEGER
DIM hidac AS INTEGER
DIM lodac AS INTEGER
DIM done AS INTEGER
DIM y AS INTEGER
DIM x AS INTEGER
DIM bipolar AS INTEGER
DIM fullscale AS SINGLE

SELECT CASE range
       CASE 0    '+5V
            bipolar = 0
            fullscale = 5
       CASE 1   '+10V
            bipolar = 0
            fullscale = 10
       CASE 2   '+/-5V
            bipolar = 1
            fullscale = 5
```

```
        CASE 3   '+/-10V
             bipolar = 1
             fullscale = 10
        CASE 4   '+/-2.5V
             bipolar = 1
             fullscale = 2.5
        CASE 5   '+7.5/-2.5V
             bipolar = 2
             fullscale = 7.5
END SELECT

IF bipolar = 1 THEN
   'offset binary coding (symetrical ratio)
   value = INT((voltage / fullscale) * 2048 + 2048)
ELSEIF bipolar = 2 THEN  'offset binary coding (asymetrical ratio)
   value = INT((voltage / fullscale) * 3072 + 1024)
ELSE 'Unipolar
   'straight binary coding
   value = INT((voltage / fullscale) * 4096)
END IF

'Limit excursion
IF value > 4095 THEN
  value = 4095
END IF

'Separate low byte from high nibble
lodac = value AND &HFF
hidac = (value AND &HF00) / 256

'Set selected DAC channel to the desired range
'(ENHANCED MODE REGISTER)
OUT BASE + &HA, ((range * 16) + channel)

'Set selected DAC channel to desired voltage
OUT BASE, lodac
OUT BASE + 2, channel
OUT BASE + 1, hidac

'A single read updates all outputs
x = INP(BASE)

'Wait for DONE or timeout before returning
done = 0
y = 0
WHILE NOT done
      y = y + 1
      IF y < 2000 THEN   'timeout
         done = INP(BASE + &HA) AND &H01 '(ENHANCED MODE REGISTER)
      ELSE
         LIB_das3aout = 1
         EXIT FUNCTION
      END IF
WEND

LIB_das3aout = 0

END FUNCTION
```

Calibration

Calibration, if desired, is accomplished by mathematical transformation in software. Gain for the board (not individual channels) can be adjusted using the ENCTRL register. Offset adjustments are not currently implemented on the board.

An SPI transaction to the gain pot will take less than 10 us. However, the Gain pot takes up to 20 ms to update its EEPROM when written to. During calibration, you need to wait 2 ms after the write command before measuring the voltage of the DAC output.

SETTING THE GAIN

The range of gain adjustment is 24 mV. The gain is encoded using the eight bits of the ENDATLO register, so each step equals 0.094 mV. To perform the Set Gain command, write E0h to the ENCTRL register at I/O port 0x30A, and then write the gain value to the ENDATLO register at I/O port 0x308. The following procedure is recommended for setting the gain:

1. Select channel 0 by writing 0h to the DACSEL register at I/O port 0x302.
2. Output the code for 0V by writing 0h to both the DACHI and DACLO registers.
3. Using high-precision volt meter (VOM), read the voltage on channel 0. The voltage read is the offset.
4. Output the code for known voltage minus the offset to channel 0.
5. Using the VOM, read voltage on channel 0. The difference between the VOM reading and the known voltage applied in step 4 is the gain error.
6. Adjust gain pot up or down to reduce the gain error to the lowest possible amount.

Note that there is no adjustment for offset error. You must accommodate for offset with software. The gain value you set is non-volatile.

READING THE GAIN

To perform the Read Gain operation, write F0h to the ENCTRL register at I/O port 0x30A, and then read the value of the ENDATLO register at I/O port 0x308.

Enhanced Mode Operations

The VCM-DAS-3 must be in enhanced mode to perform enhanced mode operations.

READING DAC DATA

Reading a DAC using the Read DAC operation does not cause the DAC to be updated, as reading the DACALL0 register does. Performing a Read DAC operation loads the DAC voltage code in the ENDATHI and ENDATLO registers. To read the voltage of a DAC:

1. Perform a Read DAC operation by writing 8h to the CTRL field of the ENCTRL register at I/O port 0x30A, combined with the channel number in the SEL field of the same register.
2. Read the ENDATHI register and then the ENDATLO register. The 12 bits of the output voltage code are offset toward the MSB, as shown below.

ENDATHI MSB (Read) 0309h

7	6	5	4	3	2	1	0
D11	D10	D9	D8	D7	D6	D5	D4

ENDATLO LSB (Read) 0308h

7	6	5	4	3	2	1	0
D3	D2	D1	D0	0	0	0	0

READING THE SPAN OF A CHANNEL

To read the span of a channel:

1. Perform a Read Span operation by writing 9h to the CTRL field of the ENCTRL register at I/O port 0x30A, combined with the channel number in the SEL field of the same register.
2. Read the span code from bits 3-0 of the ENDATLO register at I/O port 0x308, as shown below.

ENDATLO LSB (Read) 0308h

7	6	5	4	3	2	1	0
–	–	–	–	D3	D2	D1	D0

SETTING A CHANNEL TO SLEEP MODE

To set a DAC to sleep mode, perform a Sleep DAC operation by writing Bh to the CTRL field of the ENCTRL register at I/O port 0x30A, combined with the channel number in the SEL field of the same register. The channel remains in sleep mode until a voltage output code is written to it.

READING THE SLEEP STATUS OF A CHANNEL

To read the sleep status of a channel:

1. Perform a Read Span operation by writing 9h to the CTRL field of the ENCTRL register at I/O port 0x30A, combined with the channel number in the SEL field of the same register.
2. Read the SLEEPSTAT bit (bit 4) of the ENDATLO register at I/O port 0x308, as shown below. A value of 0 = awake. A value of 1 = sleep mode.

ENDATLO LSB (Read) 0308h

7	6	5	4	3	2	1	0
–	–	–	SLEEPSTAT	–	–	–	–

Signal Direction

The 24 digital I/O port signals on the VCM-DAS-3 can be configured as inputs or outputs, in groups of eight or, in the case of port DIOC, in groups of four. Signal direction is set by manipulating the bits in the DIOCTRL register. The logic level on any digital I/O channel can be set by writing a 1 or 0 to the appropriate bit. The digital I/O interface of the VCM-DAS-3 are 82C55 Mode 0 compatibly only.

Signal Polarity

All digital I/O circuits on the VCM-DAS-3 are non-inverted, true logic. A high logic level is represented by a 1 in the digital I/O data registers, and a low logic level is represented by a 0.

Since Opto 22 modules invert the logic sense of signals passed through them, the register-to-module interface is negative logic. The resulting data interface levels between the VCM-DAS-3 and I/O rack modules are shown below.

Data Written	I/O Pin	Output Modules	Input Modules	I/O Pin	Data Read
0	(Low)	Power On	Voltage Present	(Low)	0
1	(High)	Power Off	Voltage Absent	(High)	1

Digital Input

The logic state of the digital input channels can be read at any time by reading the DIOA, DIOB, or DIOC registers. Simply choose the correct register and read it as an 8-bit quantity.

Digital Output

The logic state of any digital output channel can be manipulated at any time by writing to the DIOA, DIOB, or DIOC registers. Simply choose the correct register and write the digital value as an 8-bit quantity.

References



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