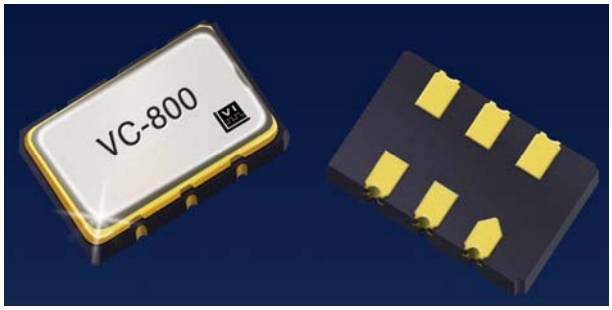
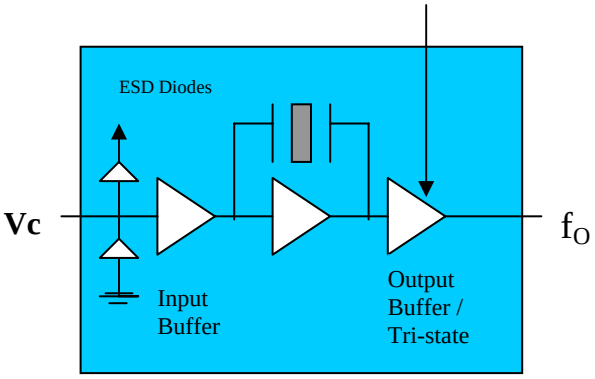
VC-800

Voltage Controlled Crystal Oscillator



The VC-800 Voltage Controlled Crystal Oscillator



Features

- **Worlds Smallest VCXO, 5.0 X 3.2 X 1.5 mm**
- High Frequencies to 74.250 MHz
- 5.0 or 3.3 V operation
- Linearity ≤ 10%
- Tri-State Output
- Low jitter < 6ps rms
- VCXO with CMOS outputs
- 0/70 or –40/85 °C temperature range
- Hermetically sealed ceramic SMD package

Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- SONET/SDH
- DWDM
- xDSL/PCMCIA cards
- Digital Video

Description

Vectron's VC-800 Voltage Controlled Crystal Oscillator (VCXO) is a quartz stabilized square wave generator with a CMOS output and is tested at CMOS and TTL (5.0 volt operation) logic levels.

The VC-800 is the smallest available VCXO making it ideally suitable for PCMCIA applications as well as any other where size is limited but performance is required.

Performance Characteristics

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	f_O	1.544		75.000	MHz
Supply Voltage [1] (+3.3 V) (+5.0 V)	V_{DD}	2.97 4.5	3.3 5.0	3.63 5.5	V
Supply Current	I_{DD}		12	25	mA
Output Logic Levels Output Logic High[2] Output Logic Low[2]	 V_{OH} V_{OL}	 0.9*V_{DD}		 0.1V_{DD}	 V V
Transition Times Rise Time[2] Fall Time[2]	 t_R t_F		 1 1	 3 3	 ns ns
Tristate Output Enabled Output Disabled	 V_{IN} V_{IL}	 2.5		 0.7	 V V
Symmetry or Duty Cycle[3] (ordering option)	SYM	40	50	60	%
Operating temperature (*ordering option*)		0/70 or –40/85			°C
Test Conditions for APR (+5V option)	V_C	0.5		4.5	V
Test Conditions for APR (+3.3V option)	V_C	0.3		3.0	V
Absolute Pull Range (*ordering option*)	APR	±50 ±70 ±80			ppm
Gain Transfer (See Figure 3)		Positive			ppm/V
Control Voltage Leakage Current	I_{VCXO}			±1	uA
Control Voltage Bandwidth (-3dB)	BW	10			kHz
Phase Noise 10 Hz Offset 100 Hz Offset 1 KHz Offset 10 KHz Offset 100 KHz Offset 1 MHz Offset			 -58 -88 -118 -143 -151 -151		 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Package Size		5.0 x 3.2 x 1.5			mm

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the equivalent five gate TTL load and operating conditions under which these parameters are tested and specified.
3. Symmetry is defined as (ON TIME/PERIOD with Vs= 1.4 V for TTL and Vs=2.5 V for CMOS, 5 volt operation, and Vs=1.65V for 3.3 Volt operation.

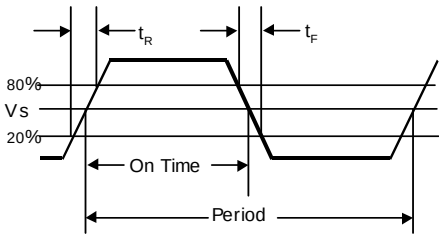


Figure 1. Output Waveform

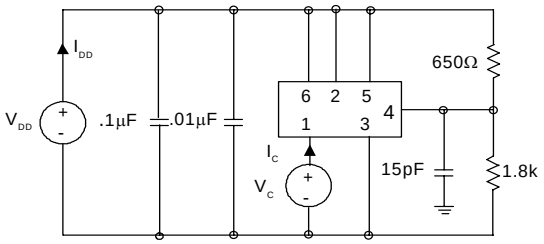
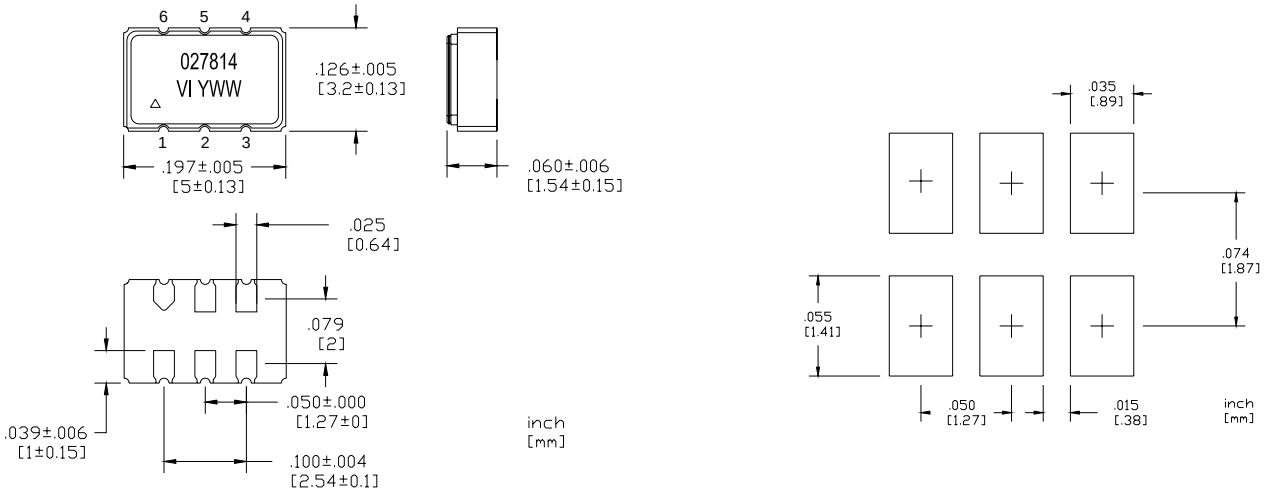


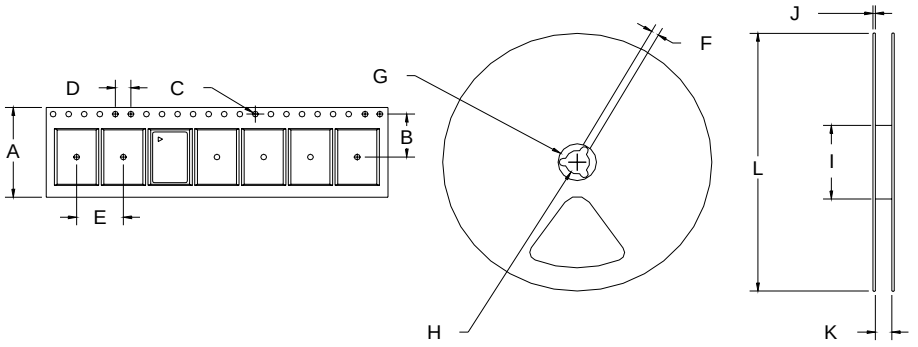
Figure 2. Typical Output Test Conditions (25±5°C)

Outline Diagram, Pad Layout and Pin Out



Pin #	Symbol	Function
1	V_C	Control Voltage
2	Tri-state	Logic low disables output Logic high or no connection enables output waveform
3	GND	Ground
4	f_O	Output Frequency
5	CMOS/TTL	Logic low for CMOS optimized symmetry Logic high or no connection for TTL optimized symmetry
6	V_{DD}	Supply Voltage

Tape and Reel



Tape and Reel Dimensions (mm)													
Tape Dimensions						Reel Dimensions							# Per
Product	A	B	C	D	E	F	G	H	I	J	K	L	Reel
VC-800	12	5.5	1.5	4	8	1.78	20.6	13	55	6	12.4	178	500

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	6	Vdc
Storage Temperature	Tstorage	-55/125	°C
Voltage Control Range	V_C	0 to V_{DD}	V

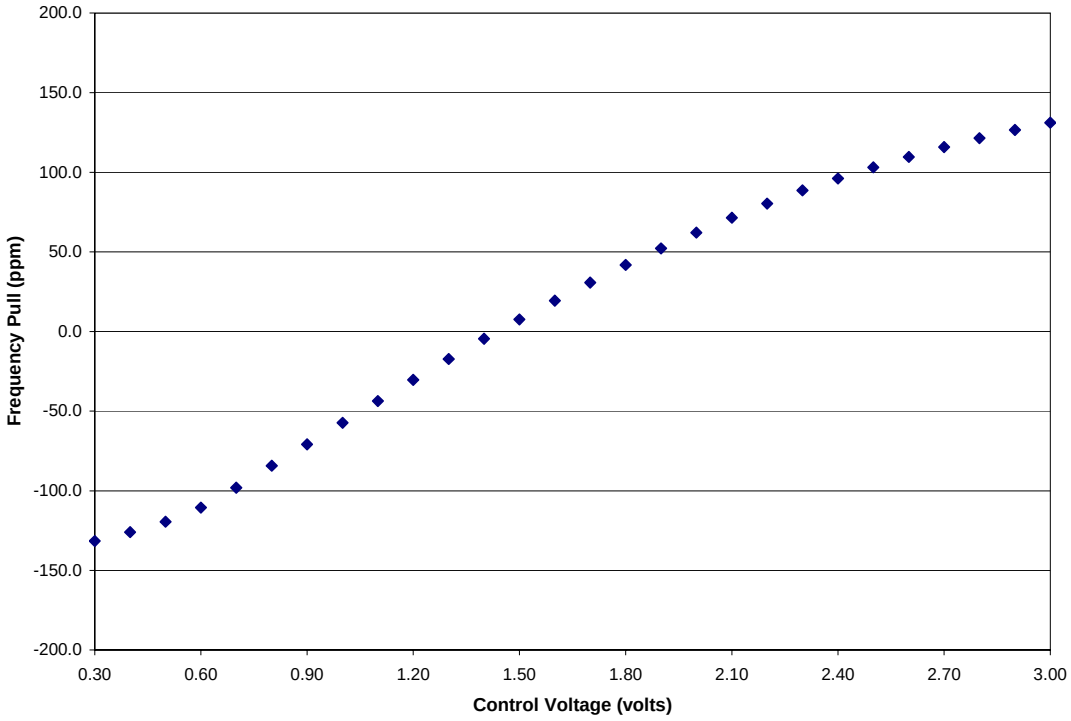


Figure 3. Typical Frequency Pull Versus Control Voltage, 35.328MHz Output, 3.3 Volt Supply

Reliability

The VC-800 is capable of meeting the following qualification tests.

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Solderability	MIL-STD-883 Method 2003
Gross and Fine Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the the VC-800, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

Table 4. ESD Ratings

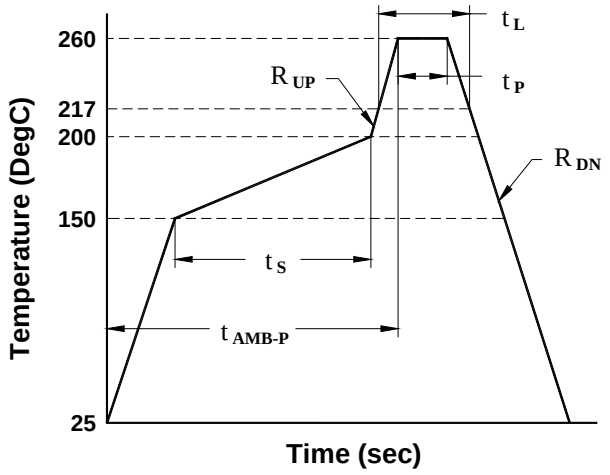
Model	Minimum	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

The VC-800 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements and parameters are listed in the table below. The contact pads are gold over nickel so lower IR reflow temperatures such as 220°C can be used (device is backwards compatible with a lead solder assembly).

The VC-800 is hermetically sealed so an aqueous wash is not an issue.

Table 5. Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max



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Standard Frequencies (MHz)

3.600	4.096	8.192	10.000	12.960
13.500	16.384	19.440	27.000	28.375
32.768	34.560	38.785	44.736	51.840
74.1758	74.250			

Other frequencies may be available upon request

Ordering Information

VC - 800 - K A C - G T J – XX.XX

Product Family
VC = VCXO

Package
800= 5.0x3.2x1.5 mm

Input
K = 5.0 Vdc ± 10%
L = 3.3 Vdc ± 10%

Output
A = CMOS

Operating Temperature
C = 0°C to 70°C
F = -40°C to 85°C

Absolute Pull Range
G = ± 50 ppm minimum
M = ± 70 ppm minimum
N = ± 80 ppm minimum

Tristate
T = Pin 2: Enable High (or Float) / Disable Low

Symmetry
J = 50±5%
K= 50±10%

Frequency (MHz)

NOTE: Not all combinations of options are available.

For Additional Information, Please Contact:

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