

VINCULUM

BINDING USB TECHNOLOGIES

Future Technology Devices International Ltd.

V2DIP2-64

VNCL2-64Q Development Module Datasheet

Document Reference No.: FT_000166

Version 1.01

Issue Date: 2010-05-06

Future Technology Devices International Ltd (FTDI)

Unit 1, 2 Seaward Place, Centurion Business Park, Glasgow, G41 1HH, United Kingdom

Tel.: +44 (0) 141 429 2777 Fax: + 44 (0) 141 429 2758

E-Mail (Support): support1@ftdichip.com

Web: http://www.vinculum.com

Neither the whole nor any part of the information contained in, or the product described in this manual, may be adapted or reproduced in any material or electronic form without the prior written consent of the copyright holder. This product and its documentation are supplied on an as-is basis and no warranty as to their suitability for any particular purpose is either made or implied. Future Technology Devices International Ltd will not accept any claim for damages howsoever arising as a result of use or failure of this product. Your statutory rights are not affected. This product or any variant of it is not intended for use in any medical appliance, device or system in which the failure of the product might reasonably be expected to result in personal injury. This document provides preliminary information that may be subject to change without notice. No freedom to use patents or other intellectual property rights is implied by the publication of this document. Future Technology Devices International Ltd, Unit 1, 2 Seaward Place, Centurion Business Park, Glasgow, G41 1HH, United Kingdom. Scotland Registered Number: SC136640

Copyright © 2010 Future Technology Devices International Limited

1 Introduction

V2DIP2-64 module is designed to allow rapid development of designs using the VNC2-64Q IC. The V2DIP2-64 is supplied as a PCB designed to fit into a 60 pin 0.8" wide, 0.1" pitch DIP socket.The module provides access to the UART, parallel FIFO, and SPI interface pins of the VNC2-64Q device, via its IO bus pins. Two USB ports are accessed via type A USB connectors.

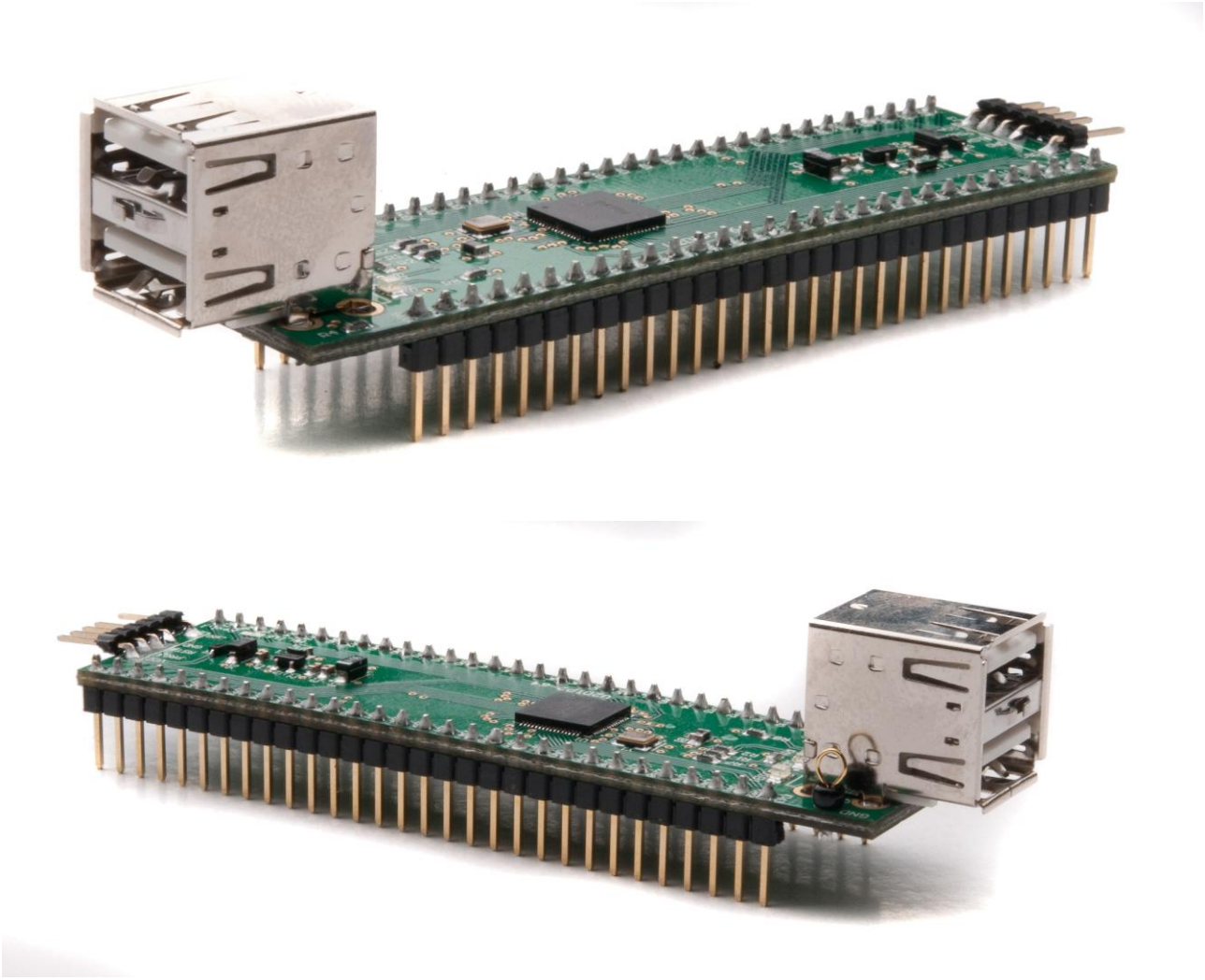


Figure 1.1 - V2DIP2-64

The VNC2 is one of the family of Vinculum devices from FTDI : the second of FTDI's Vinculum family of Embedded dual USB host controller integrated circuit devices. The device is capable of handling the USB Host Interface for a variety of different USB device classes, e.g. BOMS (bulk only mass storage), Printer, HID (human interface device) etc. When interfacing to mass storage devices such as USB Flash drives, VNC2 also transparently handles the FAT File structure.

Communication with non USB devices such as a low cost microcontroller is accomplished via either UART, SPI or parallel FIFO interfaces using a simple to implement command set. VNC2 provides a new cost effective solution for providing USB Host capability into products that previously did not have the hardware resources available.

The device comes with a Debugger interface with bus master functionality and suite of tools which allows customers to create their own firmware (Compiler – Linker – Debugger – Assembler–IDE).

The Vinculum-II VNC2 family of devices are available in Pb-free (RoHS compliant) 32-lead LQFP, 32-lead QFN, 48-lead LQFP, 48-lead QFN, 64-Lead lQFP and 64-lead QFN packages

Copyright © 2010 Future Technology Devices International Limited

Table of Contents

1 Introduction 1
2 Features 3
3 Pin Out and Signal Description 4
3.1 Module Pin Out 4
3.2 Pin Signal Description 6
3.3 Default Interface I/O Pin Configuration 8
3.4 UART Interface 10
3.4.1 Signal Description – UART Interface 10
3.5 Serial Peripheral Interface (SPI) 11
3.5.1 Signal Description - SPI Slave 11
3.5.2 Signal Description - SPI Master 11
3.6 Parallel FIFO Interface-Asynchronous Mode 12
3.6.1 Signal Description - Parallel FIFO Interface 12
3.6.2 Timing Diagram – Asynchronous FIFO Mode Read and Write Cycle 13
3.7 Parallel FIFO Interface-Synchronous Mode 14
3.7.1 Timing Diagram – Synchronous FIFO Mode Read and Write Cycle 14
3.8 Debugger Interface 16
3.8.1 Signal Description - Debugger Interface 16
4 Firmware 17
4.1 Firmware Support 17
4.2 Available Firmware 17
4.3 Firmware Upgrades 17
5 Mechanical Dimensions 18
6 Schematic Diagram 19
7 Contact Information 20
Appendix A – References 21
Appendix B – List of Figures and Tables 22
List of Figures 22
List of Tables 22
Appendix C – Revision History 23

Copyright © 2010 Future Technology Devices International Limited

2 Features

The V2DIP2-64 incorporates the following features:

- Uses FTDI's VNC2-64Q embedded USB host controller IC device
- Two USB 'A' type socket to interface with USB peripheral devices
- UART, parallel FIFO and SPI interfaces can be programmed to a choice of available I/O pins
- Single 5V supply input from DIL connectors or 5V supplied via USB VBUS slave interface or debugger module.
- Auxiliary 3.3 V / 200 mA power output to external logic
- All VNC2 signals available on 0.8" wide, 0.1" pitch DIL male connectors.
- Power and traffic indicator LED's
- Debugger interface pin available on DIL pins or via 6 way male header which interfaces to separate debugger module
- Firmware upgrades via UART or debugger interface pin header
- V2DIP2-64 is a Pb-free, RoHS complaint development module
- FOC software development suite of tools to create customised firmware includes a Compiler, Linker,Debugger and Assembler all wrapped up in an easy to use Integrated Design Environment GUI.

Copyright © 2010 Future Technology Devices International Limited

3 Pin Out and Signal Description

3.1 Module Pin Out

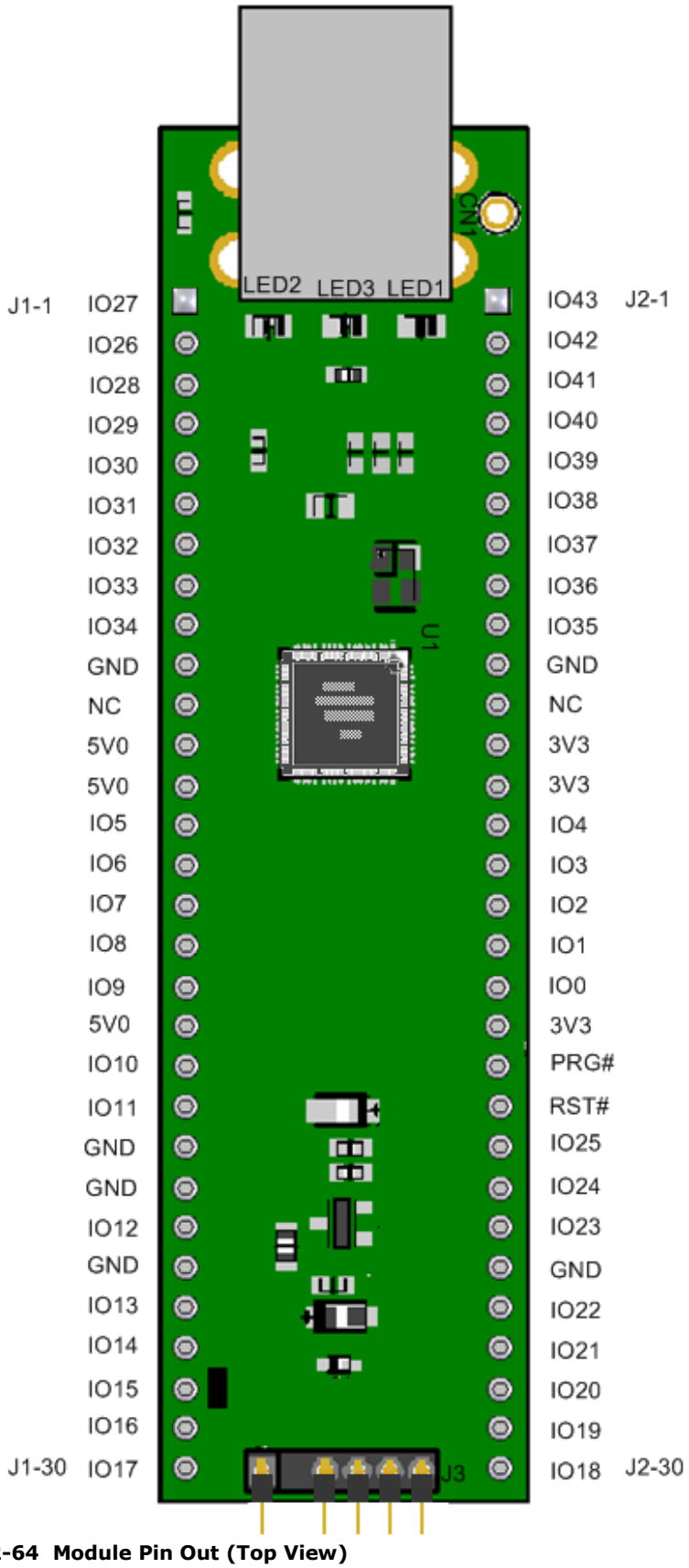


Figure 3.1 - V2DIP2-64 Module Pin Out (Top View)

Copyright © 2010 Future Technology Devices International Limited

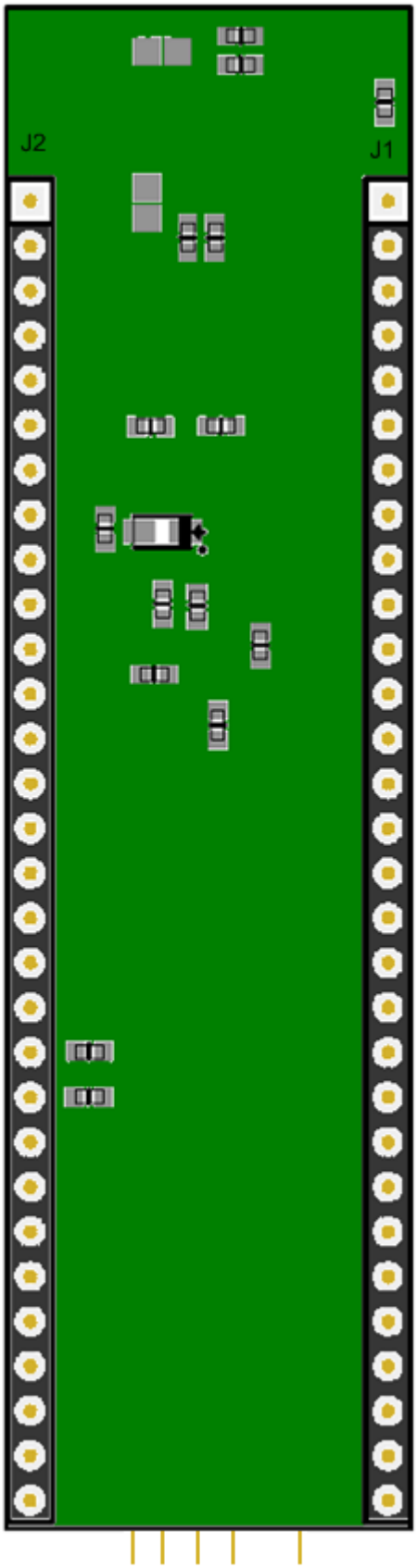


Figure 3.2 - V2DIP2-64 Module Pin Out (Bottom View)

Copyright © 2010 Future Technology Devices International Limited

3.2 Pin Signal Description

Pin No.	Name	Pin Name on PCB	Type	Description
J1-1	IOBUS26	IO26	I/O	5V safe bidirectional data / control bus bit 26
J1-2	IOBUS27	IO27	I/O	5V safe bidirectional data / control bus bit 27
J1-3	IOBUS28	IO28	I/O	5V safe bidirectional data / control bus bit 28
J1-4	IOBUS29	IO29	I/O	5V safe bidirectional data / control bus bit 29
J1-5	IOBUS30	IO30	I/O	5V safe bidirectional data / control bus bit 30
J1-6	IOBUS31	IO31	I/O	5V safe bidirectional data / control bus bit 31
J1-7	IOBUS32	IO32	I/O	5V safe bidirectional data / control bus bit 32
J1-8	IOBUS33	IO33	I/O	5V safe bidirectional data / control bus bit 33
J1-9	IOBUS34	IO34	I/O	5V safe bidirectional data / control bus bit 34
J1-10	GND	GND	PWR	Module ground supply pin
J1-11	-	-	-	Not connected
J1-12	5V0	5V0	PWR Input	5.0V module supply pin. This pin can be used to provide the 5.0V input to the V2DIP2-64 when the V2DIP2-64 is not powered from the USB connector (VBUS) or the debugger interface. Also connected to DIL connector pins pins J1-12, J1-13, J1-19 and J3-6.
J1-13	5V0	5V0	PWR Input	5.0V module supply pin. This pin can be used to provide the 5.0V input to the V2DIP2-64 when the V2DIP2-64 is not powered from the USB connector (VBUS) or the debugger interface. Also connected to DIL connector pins pins J1-12, J1-13, J1-19 and J3-6.
J1-14	IOBUS5	IO5	I/O	5V safe bidirectional data / control bus bit 5
J1-15	IOBUS6	IO6	I/O	5V safe bidirectional data / control bus bit 6
J1-16	IOBUS7	IO7	I/O	5V safe bidirectional data / control bus bit 7
J1-17	IOBUS8	IO8	I/O	5V safe bidirectional data / control bus bit 8
J1-18	IOBUS9	IO9	I/O	5V safe bidirectional data / control bus bit 9
J1-19	5V0	5V0	PWR Input	5.0V module supply pin. This pin can be used to provide the 5.0V input to the V2DIP2-64 when the V2DIP2-64 is not powered from the USB connector (VBUS) or the debugger interface. Also connected to DIL connector pins pins J1-12, J1-13, J1-19 and J3-6.
J1-20	IOBUS10	IO10	I/O	5V safe bidirectional data / control bus bit 10
J1-21	IOBUS11	IO11	I/O	5V safe bidirectional data / control bus bit 11
J1-22	GND	GND	PWR	Module ground supply pin
J1-23	GND	GND	PWR	Module ground supply pin
J1-24	IOBUS12	IO12	I/O	5V safe bidirectional data / control bus bit 12
J1-25	GND	GND	PWR	Module ground supply pin
J1-26	IOBUS13	IO13	I/O	5V safe bidirectional data / control bus bit 13
J1-27	IOBUS14	IO14	I/O	5V safe bidirectional data / control bus bit 14
J1-28	IOBUS15	IO15	I/O	5V safe bidirectional data / control bus bit 15
J1-29	IOBUS16	IO16	I/O	5V safe bidirectional data / control bus bit 16
J1-30	IOBUS17	IO17	I/O	5V safe bidirectional data / control bus bit 17
J2-1	IOBUS43	IO26	I/O	5V safe bidirectional data / control bus bit 26
J2-2	IOBUS42	IO27	I/O	5V safe bidirectional data / control bus bit 27
J2-3	IOBUS41	IO28	I/O	5V safe bidirectional data / control bus bit 28
J2-4	IOBUS40	IO29	I/O	5V safe bidirectional data / control bus bit 29
J2-5	IOBUS39	IO30	I/O	5V safe bidirectional data / control bus bit 30
J2-6	IOBUS38	IO31	I/O	5V safe bidirectional data / control bus bit 31
J2-7	IOBUS37	IO32	I/O	5V safe bidirectional data / control bus bit 32
J2-8	IOBUS36	IO33	I/O	5V safe bidirectional data / control bus bit 33
J2-9	IOBUS35	IO34	I/O	5V safe bidirectional data / control bus bit 34
J2-10	GND	GND	PWR	Module ground supply pin
J2-11	-	-	-	Not connected

Table 3.1 - Pin Signal Descriptions

Copyright © 2010 Future Technology Devices International Limited

Pin No.	Name	Pin Name on PCB	Type	Description
J2-12	3V3	3V3	3.3V Output from V2DIP2's on board 3.3V L.D.O.	3.3V output from V2DIP2's on board 3.3V L.D.O.
J2-13	3V3	3V3	3.3V Output from V2DIP2's on board 3.3V L.D.O.	3.3V output from V2DIP2's on board 3.3V L.D.O.
J2-14	IOBUS4	IO4	I/O	5V safe bidirectional data / control bus bit 4
J2-15	IOBUS3	IO3	I/O	5V safe bidirectional data / control bus bit 3
J2-16	IOBUS2	IO2	I/O	5V safe bidirectional data / control bus bit 2
J2-17	IOBUS1	IO1	I/O	5V safe bidirectional data / control bus bit 1
J2-18	IOBUS0	IO0	I/O	5V safe bidirectional data / control bus bit 0
J2-19	3V3	3V3	3.3V Output from VDIP2's on board 3.3V L.D.O.	3.3V output from V2DIP2's on board 3.3V L.D.O.
J2-20	PROG#	PRG#	Input	This pin is used in combination with the RESET# pin and the UART interface to program firmware into the VNC2.
J2-21	RESET#	RST#	Input	Can be used by an external device to reset the VNC2. This pin is also used in combination with PROG# and the UART interface to program firmware into the VNC2
J2-22	IOBUS25	IO25	I/O	5V safe bidirectional data / control bus bit 25
J2-23	IOBUS24	IO24	I/O	5V safe bidirectional data / control bus bit 24
J2-24	IOBUS23	IO23	I/O	5V safe bidirectional data / control bus bit 23
J2-25	GND	GND	PWR	Module ground supply pin
J2-26	IOBUS22	IO22	I/O	5V safe bidirectional data / control bus bit 22
J2-27	IOBUS21	IO21	I/O	5V safe bidirectional data / control bus bit 21
J2-28	IOBUS20	IO20	I/O	5V safe bidirectional data / control bus bit 20
J2-29	IOBUS19	IO19	I/O	5V safe bidirectional data / control bus bit 19
J2-30	IOBUS18	IO18	I/O	5V safe bidirectional data / control bus bit 18

Table 3.1 - Pin Signal Descriptions

Copyright © 2010 Future Technology Devices International Limited

3.3 Default Interface I/O Pin Configuration

The VNC2-64Q device is delivered without any firmware pre-loaded. As such the IOMUX will provide a default pinout as shown in **Table 3.2**

Pin No.	*Pin Name on PCB*	*Type*	*Data and Control Bus Configuration Options*				
			UART Interface	*SPI Slave Interface*	*SPI Master Interface*	*Parallel FIFO Interface*	*Debugger Interface*
J2-18	IO0	I/O	NA	NA	NA	NA	Debug_if
J2-28	IO20	I/O	uart_txd	NA	NA	NA	NA
J2-27	IO21	I/O	uart_rxd	NA	NA	NA	NA
J2-26	IO22	I/O	uart_rts#	NA	NA	NA	NA
J2-24	IO23	I/O	uart_cts#	NA	NA	NA	NA
J2-23	IO24	I/O	uart_dtr#	NA	NA	NA	NA
J2-22	IO25	I/O	uart_dsr#	NA	NA	NA	NA
J1-1	IO26	I/O	uart_dcd#	NA	NA	NA	NA
J1-2	IO27	I/O	uart_ri#	NA	NA	NA	NA
J1-3	IO28	I/O	uart_tx_active	NA	NA	NA	NA
J1-7	IO32	I/O	NA	spi_s0_clk	NA	NA	NA
J1-8	IO33	I/O	NA	spi_s0_mosi	NA	NA	NA
J1-9	IO34	I/O	NA	spi_s0_miso	NA	NA	NA
J2-9	IO35	I/O	NA	spi_s0_cs#	NA	NA	NA
J2-8	IO36	I/O	NA	spi_s1_clk	NA	NA	NA
J2-7	IO37	I/O	NA	spi_s1_mosi	NA	NA	NA
J2-6	IO38	I/O	NA	spi_s1_miso	NA	NA	NA
J2-5	IO39	I/O	NA	spi_s1_cs#	NA	NA	NA
J2-4	IO40	I/O	NA	NA	spi_m_clk	NA	NA
J2-3	IO41	I/O	NA	NA	spi_m_mosi	NA	NA
J2-2	IO42	I/O	NA	NA	spi_m_miso	NA	NA
J2-1	IO43	I/O	NA	NA	spi_m_cs#	NA	NA
J2-14	IO4	I/O	NA	NA	NA	fifo_data[0]	NA
J1-14	IO5	I/O	NA	NA	NA	fifo_data[1]	NA
J1-15	IO6	I/O	NA	NA	NA	fifo_data[2]	NA

Table 3.2 - Default Interface I/O Pin Configuration

Copyright © 2010 Future Technology Devices International Limited

Pin No.	Pin Name on PCB	Type	Data and Control Bus Configuration Options				
			UART Interface	SPI Slave Interface	SPI Master Interface	Parallel FIFO Interface	Debugger Interface
J1-16	IO7	I/O	NA	NA	NA	fifo_data[3]	NA
J1-17	IO8	I/O	NA	NA	NA	fifo_data[4]	NA
J1-18	IO9	I/O	NA	NA	NA	fifo_data[5]	NA
J1-20	IO10	I/O	NA	NA	NA	fifo_data[6]	NA
J1-21	IO11	I/O	NA	NA	NA	fifo_data[7]	NA
J1-24	IO12	I/O	NA	NA	NA	fifo_rxf#	NA
J1-26	IO13	I/O	NA	NA	NA	fifo_txe#	NA
J1-27	IO14	I/O	NA	NA	NA	fifo_rd#	NA
J1-28	IO15	I/O	NA	NA	NA	fifo_wr#	NA
J1-29	IO16	I/O	NA	NA	NA	fifo_oe#	NA

Table 3.2 - Default Interface I/O Pin Configuration

Copyright © 2010 Future Technology Devices International Limited

3.4 UART Interface

When the data and control buses are configured in UART mode, the interface implements a standard asynchronous serial UART port with flow control. The UART can support baud rates from 300baud to 3Mbaud. The UART interface is described more fully in a Vinculum-II datasheet please refer to:- FTDI website

3.4.1 Signal Description – UART Interface

The UART signals can be programmed to a choice of available I/O pins. **Table 3.3** explains the available pins for each of the UART signals.

Available Pins	*Name*	*Type*	*Description*
J2-18, J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	uart_txd	Output	Transmit asynchronous data output
J2-17, J1-14, J1-18, J1-26, J1-30, J2-27, J2-22, J1-4, J1-8, J2-7, J2-3	uart_rxd	Input	Receive asynchronous data input
J2-16, J1-15, J1-20, J1-27, J2-30, J2-26, J1-1, J1-5, J1-9, J2-6, J2-2	uart_rts#	Output	Request To Send Control Output
J2-15, JI-16, J1-21, J1-28, J2-29, J2-24, J1-2, J1-6, J2-9, J2-5, J2-1	uart_cts#	Input	Clear To Send Control Input
J2-18, J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	uart_dtr#	Output	Data Acknowledge (Data Terminal Ready Control) Output
J2-17, J1-14, J1-18, J1-26, J1-30, J2-27, J2-22, J1-4, J1-8, J2-7, J2-3	uart_dsr#	Input	Data Request (Data Set Ready Control) Input
J2-16, J1-15, J1-20, J1-27, J2-30, J2-26, J1-1, J1-5, J1-9, J2-6, J2-2	uart_dcd#	Input	Data Carrier Detect Control Input
J2-15, JI-16, J1-21, J1-28, J2-29, J2-24, J1-2, J1-6, J2-9, J2-5, J2-1	uart_ri#	Input	Ring Indicator Control Input. RI# low can be used to resume the PC USB Host controller from suspend.
J2-18, J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	uart_tx_active	Output	Enable Transmit Data for RS485 designs. uart_tx_active may be used to signal that a transmit operation is in progress. The uart_tx_active signal will be set high one bit-time before data is transmitted and return low one bit time after the last bit of a data frame has been transmitted

Table 3.3 - Data and Control Bus Signal Mode Options – UART

Copyright © 2010 Future Technology Devices International Limited

3.5 Serial Peripheral Interface (SPI)

The VNC2-64Q has one master module and two slave modules. These modules are described more fully in a Vinculum-II datasheet please refer to:- FTDI website

3.5.1 Signal Description - SPI Slave

The SPI Slave signals can be programmed to a choice of available I/O pins. **Table 3.4** explains the available pins for each of the SPI Slave signals.

Available Pins	*Name*	*Type*	*Description*
J2-18, J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	spi_s0_clk spi_s1_clk	Input	Slave clock input
J2-17, J1-14, J1-18, J1-26, J1-30, J2-27, J2-22, J1-4, J1-8, J2-7, J2-3	spi_s0_mosi spi_s1_mosi	Input/Output	Master Out Slave In Synchronous data from master to slave
J2-16, J1-15, J1-20, J1-27, J2-30, J2-26, J1-1, J1-5, J1-9, J2-6, J2-2	spi_s0_miso spi_s1_miso	Output	Master In Slave Out Synchronous data from slave to master
J2-15, JI-16, J1-21, J1-28, J2-29, J2-24, J1-2, J1-6, J2-9, J2-5, J2-1	spi_s0_cs# spi_s1_cs#	Input	Slave chip select

Table 3.4 - Data and Control Bus Signal Mode Options – SPI Slave

3.5.2 Signal Description - SPI Master

The SPI Master signals can be programmed to a choice of available I/O pins. **Table 3.5** shows the SPI master signals and the available pins that they can be mapped.

Available Pins	*Name*	*Type*	*Description*
J2-18, J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	spi_m_clk	Output	SPI master clock input
J2-17, J1-14, J1-18, J1-26, J1-30, J2-27, J2-22, J1-4, J1-8, J2-7, J2-3	spi_m_mosi	Output	Master Out Slave In Synchronous data from master to slave
J2-16, J1-15, J1-20, J1-27, J2-30, J2-26, J1-1, J1-5, J1-9, J2-6, J2-2	spi_m_miso	Input	Master In Slave Out Synchronous data from slave to master
J2-15, JI-16, J1-21, J1-28, J2-29, J2-24, J1-2, J1-6, J2-9, J2-5, J2-1	spi_m_cs_0#	Output	Active low slave select 0 from master to slave 0
J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	spi_m_cs_1#	Output	Active low slave select 1 from master to slave 1

Table 3.5 - Data and Control Bus Signal Mode Options – SPI Master

Copyright © 2010 Future Technology Devices International Limited

3.6 Parallel FIFO Interface-Asynchronous Mode

The Parallel FIFO Asynchronous mode is functionally the same as the Parallel FIFO Interface present in VDIP2 has an eight bit data bus, individual read and write strobes and two hardware flow control signals.

3.6.1 Signal Description - Parallel FIFO Interface

The Parallel FIFO Interface signals can be programmed to a choice of available I/O pins. **Table 3.6** shows the Parallel FIFO Interface signals and the pins that they can be mapped.

Available Pins	*Name*	*Type*	*Description*
J2-18, J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	fifo_data[0]	I/O	FIFO data bus Bit 0
J2-17, J1-14, J1-18, J1-26, J1-30, J2-27, J2-22, J1-4, J1-8, J2-7, J2-3	fifo_data[1]	I/O	FIFO data bus Bit 1
J2-16, J1-15, J1-20, J1-27, J2-30, J2-26, J1-1, J1-5, J1-9, J2-6, J2-2	fifo_data[2]	I/O	FIFO data bus Bit 2
J2-15, JI-16, J1-21, J1-28, J2-29, J2-24, J1-2, J1-6, J2-9, J2-5, J2-1	fifo_data[3]	I/O	FIFO data bus Bit 3
J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	fifo_data[4]	I/O	FIFO data bus Bit 4
J2-17, J1-14, J1-18, J1-26, J1-30, J2-27, J2-22, J1-4, J1-8, J2-7, J2-3	fifo_data[5]	I/O	FIFO data bus Bit 5
J2-16, J1-15, J1-20, J1-27, J2-30, J2-26, J1-1, J1-5, J1-9, J2-6, J2-2	fifo_data[6]	I/O	FIFO data bus Bit 6
J2-15, JI-16, J1-21, J1-28, J2-29, J2-24, J1-2, J1-6, J2-9, J2-5, J2-1	fifo_data[7]	I/O	FIFO data bus Bit 7
J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	fifo_rxf#	Output	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high.
J2-17, J1-14, J1-18, J1-26, J1-30, J2-27, J2-22, J1-4, J1-8, J2-7, J2-3	fifo_txe#	Output	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing fifo_wr# high, then low.
J2-16, J1-15, J1-20, J1-27, J2-30, J2-26, J1-1, J1-5, J1-9, J2-6, J2-2	fifo_rd#	Input	Enables the current FIFO data byte on D0...D7 when low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when fifo_rd# goes from high to low
J2-15, JI-16, J1-21, J1-28, J2-29, J2-24, J1-2, J1-6, J2-9, J2-5, J2-1	fifo_wr#	Input	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when fifo_wr# goes from high to low.

Table 3.6 - Data and Control Bus Signal Mode Options – Parallel FIFO Interface

Copyright © 2010 Future Technology Devices International Limited

3.6.2 Timing Diagram – Asynchronous FIFO Mode Read and Write Cycle

When in Asynchronous FIFO interface mode, the timing of a read and write operation on the FIFO interface is shown in **Figure 3.3 and** Table 3.7

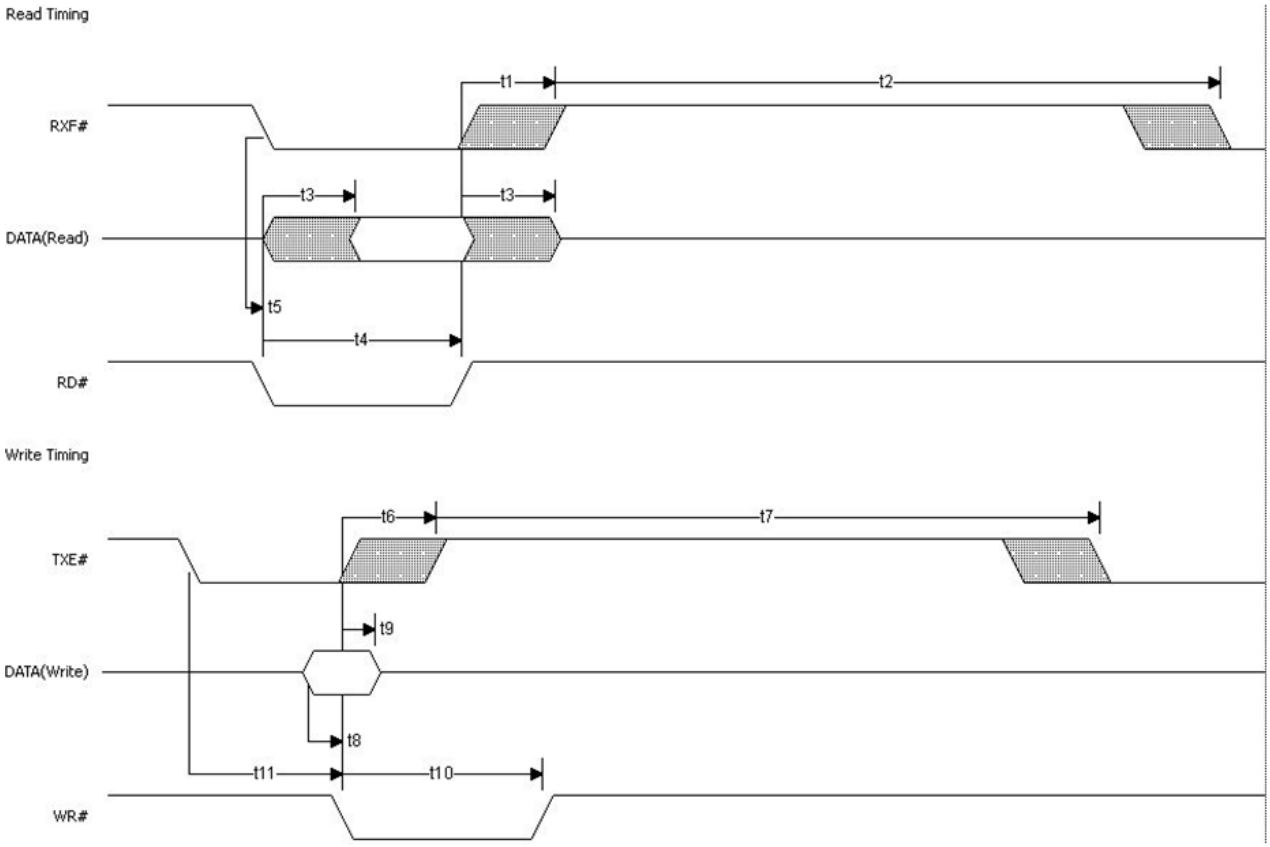


Figure 3.3 – Asynchronous FIFO Mode Read and Write Cycle.

Time	*Description*	*Min*	*Max*	*Unit*
t1	RD# inactive to RXF#	1	14	ns
t2	RXF# inactive after RD# cycle	100	-	ns
t3	RD# to Data	1	14	ns
t4	RD# active pulse width	30	-	ns
t5	RD# active after RXF#	0	-	ns
t6	WR# active to TXE# inactive	1	14	ns
t7	TXE# inactive after WR# cycle	100	-	ns
t8	DATA to TXE# active setup time	5	-	ns
t9	DATA hold time after WR# inactive	5	-	ns
t10	WR# active pulse width	30	-	ns
t11	WR# active after TXE#	0	-	ns

Table 3.7 Asynchronous FIFO Mode Read Cycle Timing

In asynchronous mode an external device can control data transfer driving FIFO_WR# and FIFO_RD# inputs. In contrast to synchronous mode, in asynchronous mode the 245 FIFO module generates the output enable EN# signal. EN# signal is effectively the read signal RD#.

Current byte is available to be read when FIFO_RD# goes low. When FIFO_RD# goes high, FIFO_RXF# output will also go high. It will only become low again when there is another byte to read.

When FIFO_WR# goes low FIFO_TXE# flag will always go high. FIFO_TXE# goes low again only when there is still space for data to be written in to the module.

Copyright © 2010 Future Technology Devices International Limited

3.7 Parallel FIFO Interface-Synchronous Mode

The Parallel FIFO Synchronous mode has an eight bit data bus, individual read and write strobes, two hardware flow control signals, an output enable and a clock out.

The synchronous FIFO mode uses the parallel FIFO interface signals detailed in **Table 3.6** and additional two signals detailed in **Table 3.8**.

Available Pins	*Name*	*Type*	*Description*
J2-18, J2-14, J1-17, J1-24, J1-29, J2-28, J2-23, J1-3, J1-7, J2-8, J2-4	fifo_oe#	Output	FIFO Output Enable
J2-17, J1-14, J1-18, J1-26, J1-30, J2-27, J2-22, J1-4, J1-8, J2-7, J2-3	fifo_clkout	Output	FIFO Output Enable

Table 3.8 - Data and Control Bus Signal Mode Options – Synchronous FIFO mode

3.7.1 Timing Diagram – Synchronous FIFO Mode Read and Write Cycle

When in Synchronous FIFO interface mode, the timing of a read and write operation on the FIFO interface are shown in **Figure 3.4** and **Table 3.9**

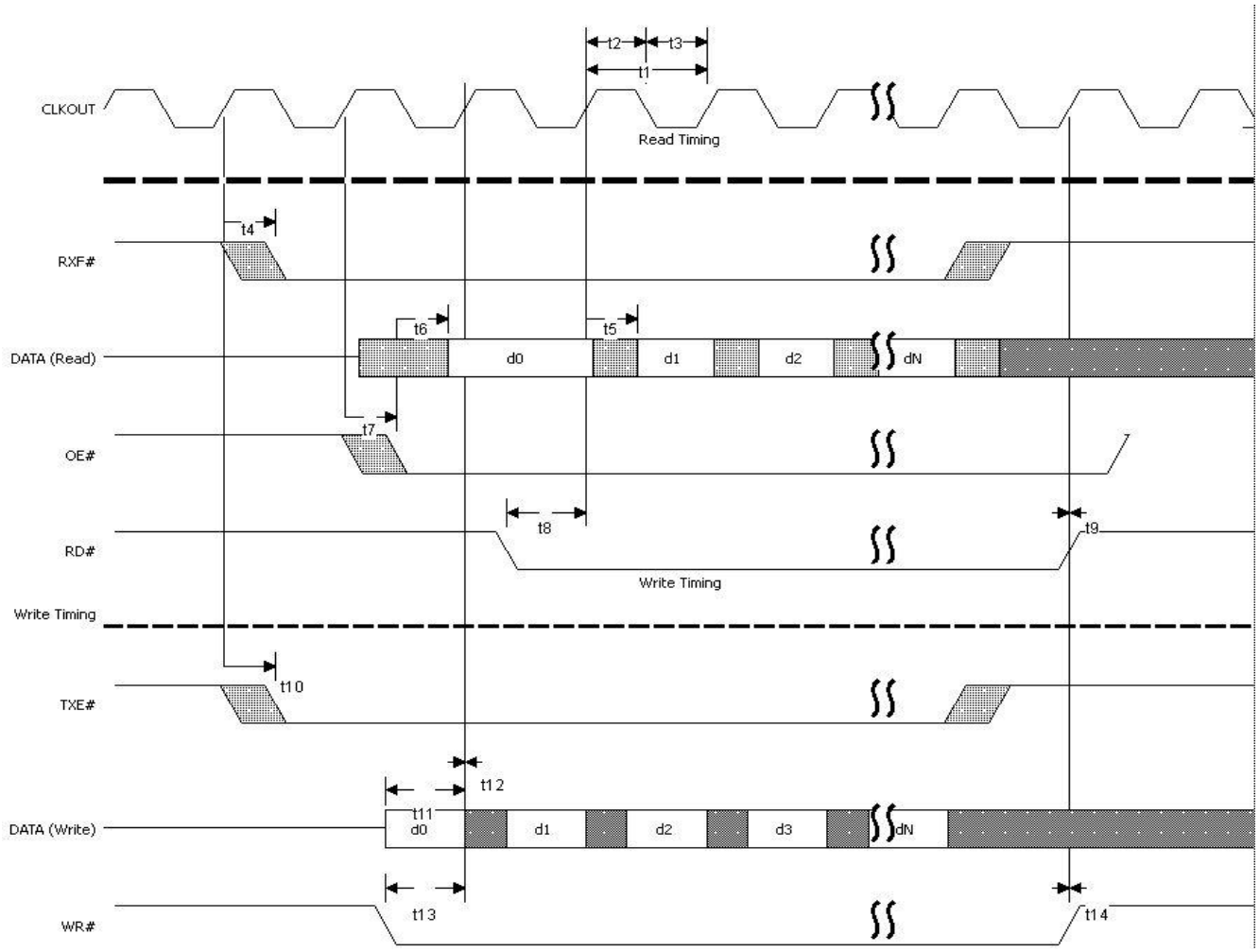


Figure 3.4 - Synchronous FIFO Mode Read and Write Cycle

Copyright © 2010 Future Technology Devices International Limited

Time	Description	Min	Typical	Max	Uni
t1	CLKOUT period	-	20.83	-	ns
t2	CLKOUT high period	9.38	10.42	11.46	ns
t3	CLKOUT low period	9.38	10.42	11.46	ns
t4	CLKOUT to RXF#	1	-	7.83	ns
t5	CLKOUT to read DATA valid	1	-	7.83	ns
t6	OE# to read DATA valid	1	-	7.83	ns
t7	CLKOUT to OE#	1	-	7.83	ns
t8	RD# setup time	12	-	-	ns
t9	RD# hold time	0	-	-	ns
t10	CLKOUT TO TXE#	1	-	-	ns
t11	Write DATA setup time	12	-	-	ns
t12	Write DATA hold time	0	-	-	ns
t13	WR# setup time	12	-	-	ns
t14	WR# hold time	0	-	-	ns

Table 3.9 - Synchronous FIFO Mode Read and Write Cycle Timing

In synchronous mode data can be transmitted to and from the FIFO module on each clock edge. An external device synchronises to the CLKOUT output and it also has access to the output enable OE# input to control data flow. An external device should drive output enable OE# low before pulling RD# line down.

When bursts of data are to be read from the module RD# should be kept low. RXF# remains low when there is still data to be read. Similarly when bursts of data are to be written to the module WR# should be kept low. TXE# remains low when there is still space available for the data to be written

Copyright © 2010 Future Technology Devices International Limited

3.8 Debugger Interface

The purpose of the debugger interface is to provide access to the VNC2 silicon/firmware debugger. The debug interface can be accessed via the appropriate pin on the DIL connector or more easily, it can be accessed by connecting a debug module to the J3 connector. This debug module will give access to the debugger through a USB connection to a PC via the Integrated Development Environment (IDE). The IDE is a graphical interface to the VNC2 software development tool-chain and gives the following debug capabilities through the debugger interface:

- Flash Erase, Write and Program.
- Application debug - application code can have breakpoints, be single stepped and can be halted. Detailed internal debug - memory and register read/write access.

The Debugger Interface, and how to use it, is further described in the following applications Note Vinculum-II Debug Interface Description

3.8.1 Signal Description - Debugger Interface

Table 3.10 shows the signals and pins description for the Debugger Interface pin header J3

Pin No.	*Name*	*Name On PCB*	*Type*	*Description*
J3-1	IO0	DBG	I/O	Debugger Interface
J3-2	-	[Key]	-	Not connected. Used to make sure that the debug module is connected correctly.
J3-3	GND	GND	PWR	Module ground supply pin
J3-4	RESET#	RST#	Input	Can be used by an external device to reset the VNCL2. This pin is also used in combination with PROG# and the UART interface to program firmware into the VNC2.
J3-5	PROG#	PRG#	Input	This pin is used in combination with the RESET# pin and the UART interface to program firmware into the VNC2.
J3-6	5V0	VCC	PWR Input	5.0V module supply pin. This pin can be used to provide the 5.0V input to the V2DIP2-64 from the debugger interface when the V2DIP2-64 is not powered from the USB connector (VBUS) or the DIL connector pins J1-12, J1-13, J1-19 and J3-6.

Table 3.10 - Signal Name and Description – Debugger Interface

Copyright © 2010 Future Technology Devices International Limited

4 Firmware

4.1 Firmware Support

The VNC2 on the V2DIP2-64 can be programmed with the customers own firmware created using the Vinculum II firmware development tool chain or with various pre-compiled firmware profiles to allow a designer to easily change the functionality of the chip. Please refer to:- FTDI website for full details on available pre-compiled firmware

4.2 Available Firmware

V2DAP firmware is currently available: USB Host for single Flash Disk and general purpose USB peripherals. Selectable UART, FIFO or SPI interface command monitor. please refer to:- FTDI website for full details.

4.3 Firmware Upgrades

Refer to the debugger interface section which can be used to update the firmware.

Copyright © 2010 Future Technology Devices International Limited

5 Mechanical Dimensions

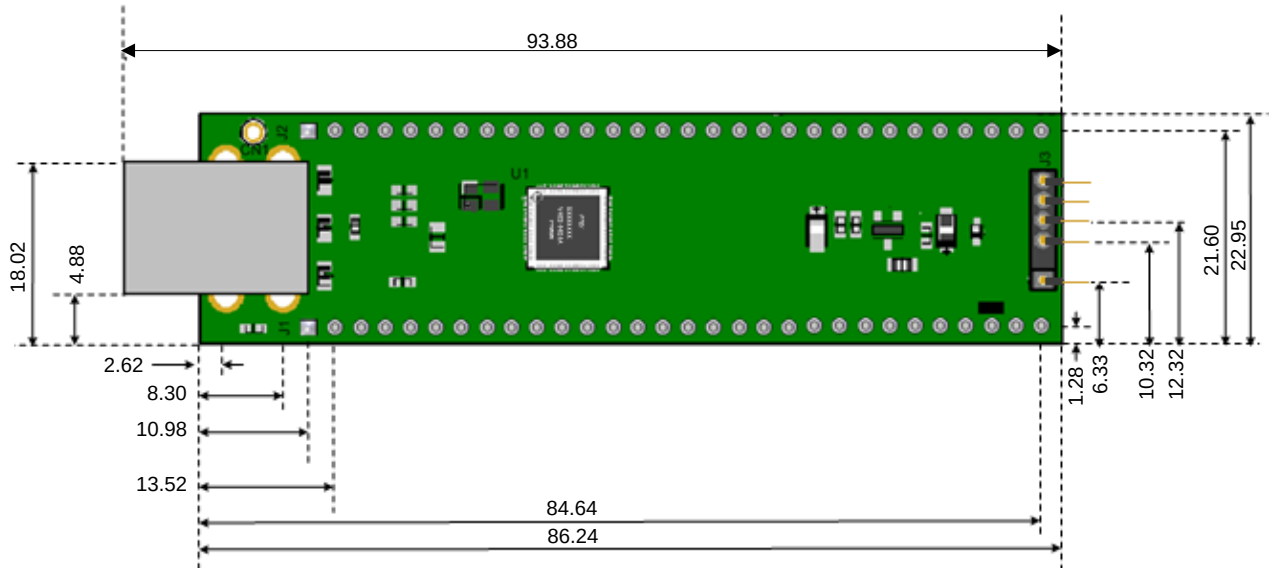


Figure 5.1 - V2DIP2 -64 Dimensions (Top View)

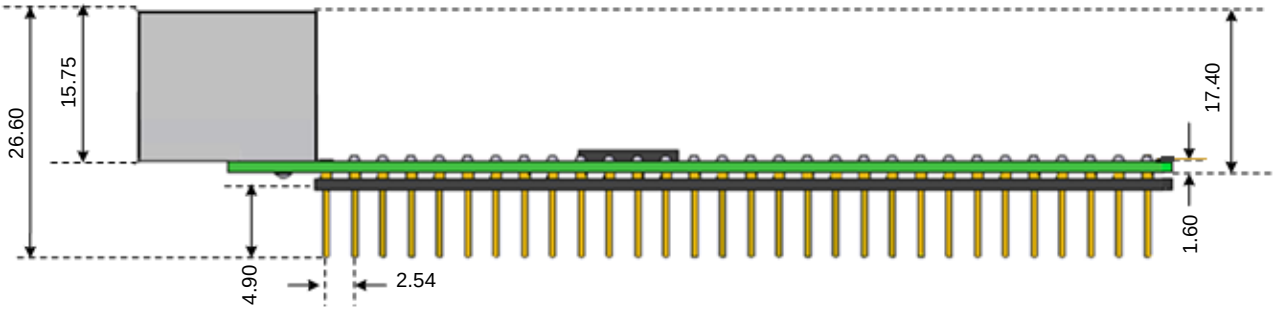


Figure 5.2 - V2DIP2 -64 Dimensions (Side View)

±0.20mm Tolerance (except pitch)

All dimensions are in mm

Copyright © 2010 Future Technology Devices International Limited

6 Schematic Diagram

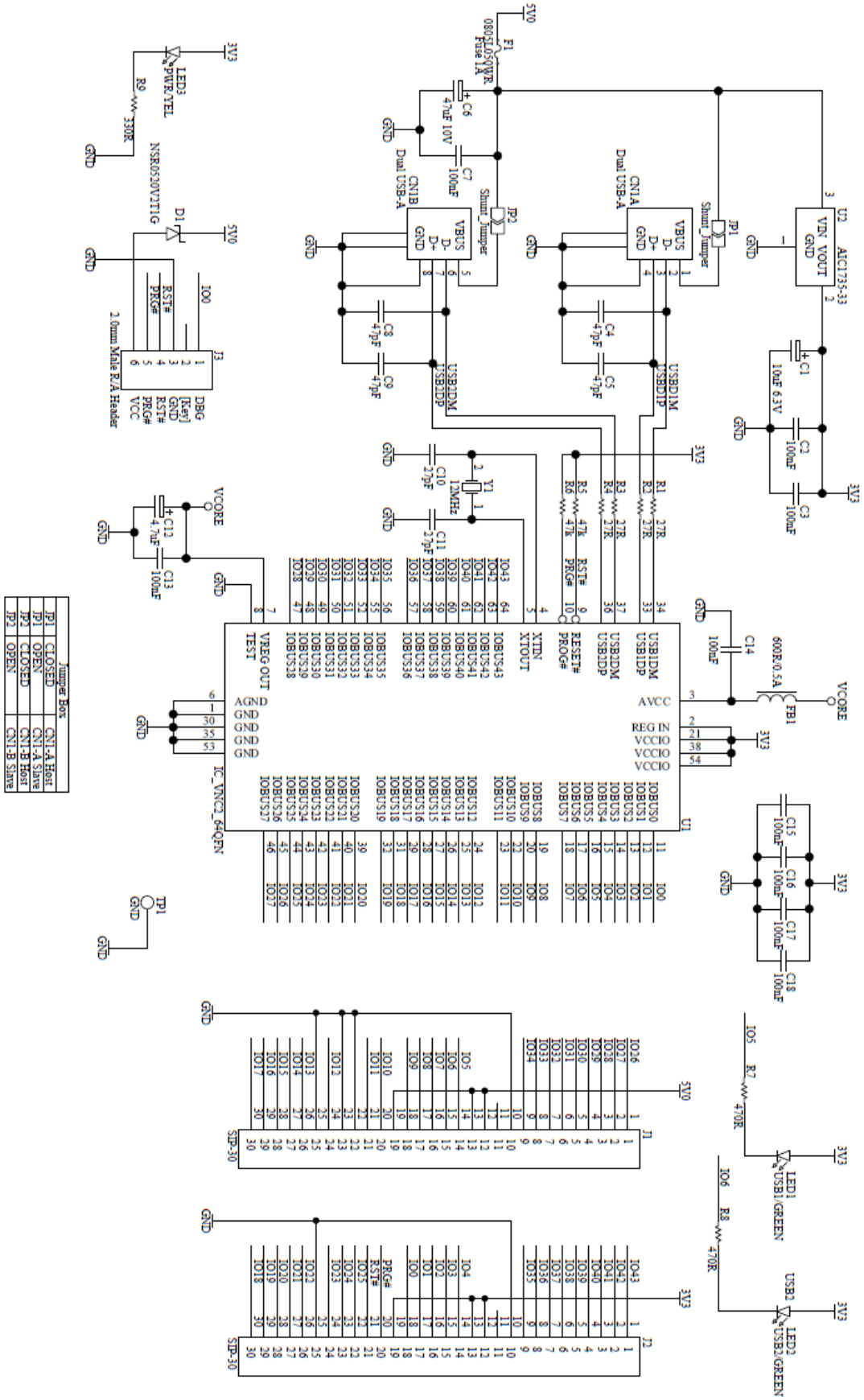


Figure 6.1 - V2DIP2 -64 Dimensions (Side View)

Copyright © 2010 Future Technology Devices International Limited

7 Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place,
Centurion Business Park
Glasgow, G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com
Web Site URL http://www.ftdichip.com
Web Shop URL http://www.ftdichip.com

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)
2F, No 516, Sec. 1 NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8791 3570
Fax: +886 (0) 2 8791 3576

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com
Web Site URL http://www.ftdichip.com

Branch Office – Hillsboro, Oregon, USA

Future Technology Devices International Limited (USA)
7235 NW Evergreen Parkway, Suite 600
Hillsboro, OR 97123-5803
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com
Web Site URL http://www.ftdichip.com

Branch Office – Shanghai, China

Future Technology Devices International Limited (China)
Room 408, 317 Xianxia Road,
ChangNing District,
ShangHai, China

Tel: +86 (21) 62351596
Fax: +86(21) 62351595

E-Mail (Sales): cn.sales@ftdichip.com
E-Mail (Support): cn.support@ftdichip.com
E-Mail (General Enquiries): cn.admin1@ftdichip.com
Web Site URL http://www.ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Copyright © 2010 Future Technology Devices International Limited

Appendix A – References

Application and Technical Notes

Vinculum-II IO Cell Description

Vinculum-II Debug Interface Description

Vinculum-II IO Mux Explained

Vinculum-II PWM Example

Migrating Vinculum Designs From VNC1L to VNC2-48L1A

Vinculum-II Errata Technical Note

Copyright © 2010 Future Technology Devices International Limited

Appendix B – List of Figures and Tables

List of Figures

Figure 1.1 - V2DIP2-64 1
Figure 3.1 - V2DIP2-64 Module Pin Out (Top View) 4
Figure 3.3 – Asynchronous FIFO Mode Read and Write Cycle. 13
Figure 3.4 - Synchronous FIFO Mode Read and Write Cycle 14
Figure 5.1 - V2DIP2 -64 Dimensions (Top View) 18
Figure 5.2 - V2DIP2 -64 Dimensions (Side View) 18
Figure 6.1 - V2DIP2 -64 Dimensions (Side View) 19

List of Tables

Table 3.1 - Pin Signal Descriptions 6
Table 3.2 - Default Interface I/O Pin Configuration 8
Table 3.3 - Data and Control Bus Signal Mode Options – UART 10
Table 3.4 - Data and Control Bus Signal Mode Options – SPI Slave 11
Table 3.5 - Data and Control Bus Signal Mode Options – SPI Master 11
Table 3.6 - Data and Control Bus Signal Mode Options – Parallel FIFO Interface 12
Table 3.7 Asynchronous FIFO Mode Read Cycle Timing 13
Table 3.8 - Data and Control Bus Signal Mode Options – Synchronous FIFO mode 14
Table 3.9 - Synchronous FIFO Mode Read and Write Cycle Timing 15
Table 3.10 - Signal Name and Description – Debugger Interface 16

Copyright © 2010 Future Technology Devices International Limited

Appendix C – Revision History

Version 1.0	First Release	19th April 2010
Version 1.01	Updated module's image and mechanical drawings	06th May 2010

Copyright © 2010 Future Technology Devices International Limited