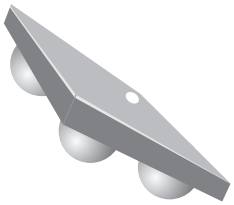
USBULC6-2F4

2-line, ultralow capacitance protection in 0.3 mm pitch

Datasheet - production data



Flip Chip USBULC6-2F4
(4 bumps)

Features

- Ultralow capacitance diode (1.5 pF max)
- 0.3 mm pitch
- Two data lines (D+ and D-) protected against ESD
- Breakdown voltage V_{BR} = 6.0 V min.
- Flip Chip, 300 µm pitch, lead-free
- Very low leakage current
- Very small PCB area
- RoHS compliant

Benefits

- Minimized impact on rise and fall times for maximum data integrity
- Low PCB space occupation
- Higher reliability offered by monolithic integration

Complies with the following standards

- IEC 61000-4-2 level 4:
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

Description

The USBULC6-2F4 is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces.

Its ultralow line capacitance secures a high level of signal integrity without compromising the protection of downstream sensitive chips against the most stringently characterized ESD strikes.

Figure 1. Pin layout (bump side)

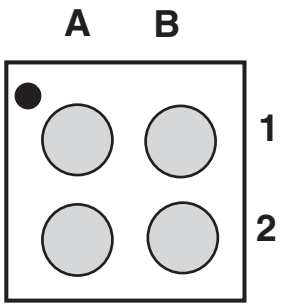
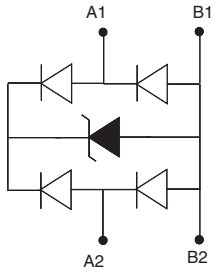


Figure 2. Device configuration



Note: B1 and B2 bumps must be grounded on the PCB together

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	IEC 61000-4-2, level 4, contact discharge	±8	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)	60	W
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-30 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Figure 3. Electrical characteristics - definitions

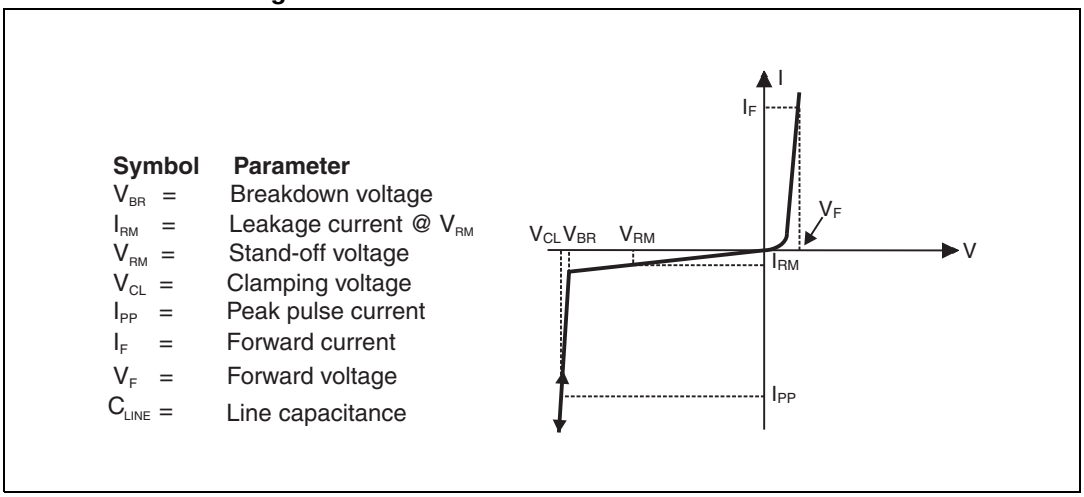


Table 2. Electrical characteristics - values (T_{amb} = 25 °C)

Symbol	Test conditions		Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA		6	-		V
I_{RM}	V_{RM} = 3 V per line		-	-	100	nA
C_{LINE}	V_{LINE} = 0 V, V_{OSC} = 30 mV, F = 1 MHz		-	-	1.5	pF
R_d	Dynamic resistance, pulse duration 100 ns	I/O to GND	-	0.73	-	Ω
		GND to I/O	-	0.72	-	

Figure 4. Eye diagram, board only (according to USB 2.0 high speed specification)

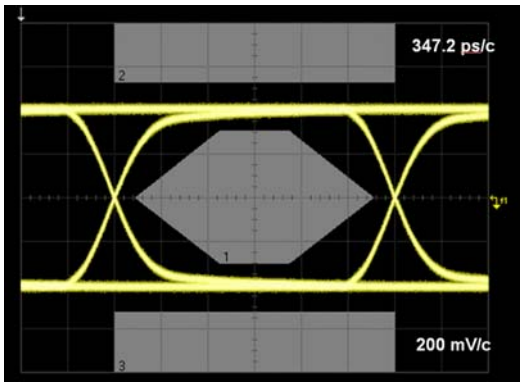


Figure 5. Eye diagram, board with USBULC6-2F4 (according to USB 2.0 high speed specification)

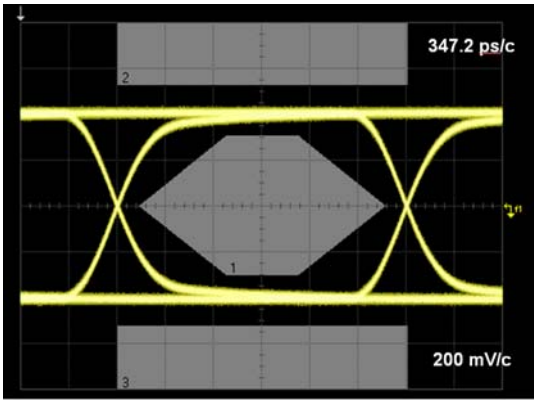


Figure 6. ESD response to IEC 61000-4-2 (+8 kV contact discharge)(1)

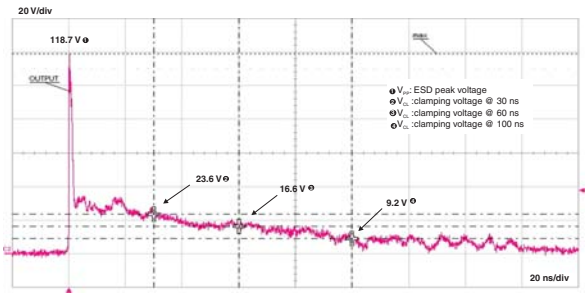
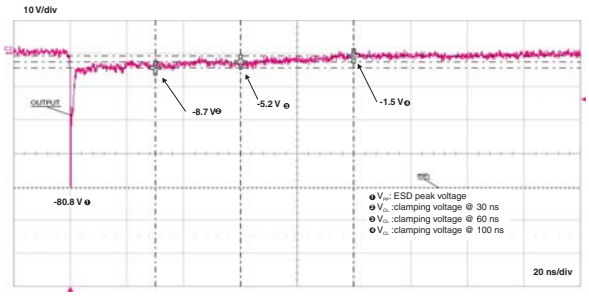


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge)(1)



1. Test board connected with a 50 Ohm cable and 20 dB + 20 dB attenuator to an oscilloscope on 50 Ohm input. ESD generator return path connected to PCB ground plane.

Figure 8. Junction capacitance versus frequency (typical values)

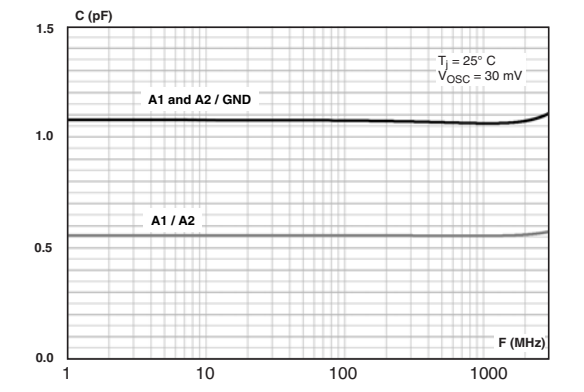


Figure 9. Analog crosstalk versus frequency (typical values)

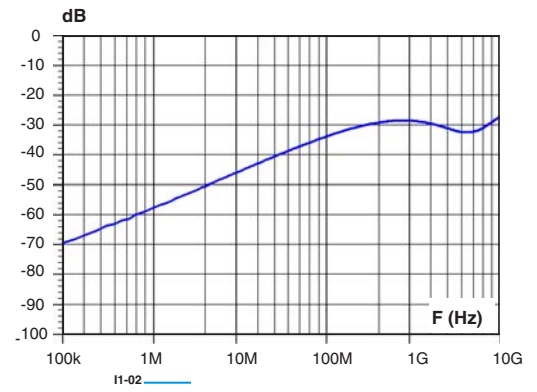


Figure 10. Insertion losses versus frequency

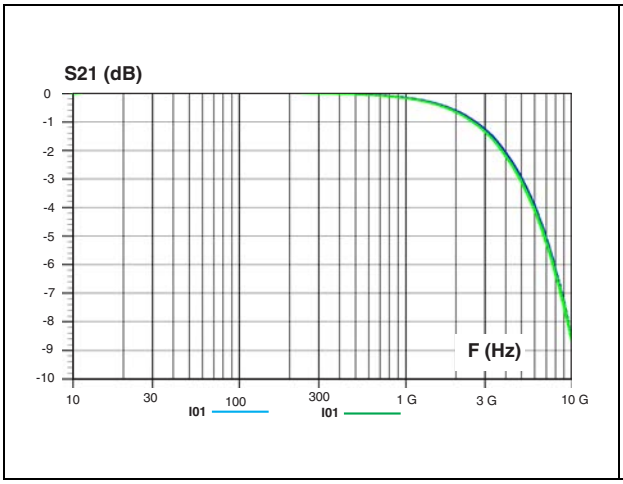


Figure 11. TLP measurement

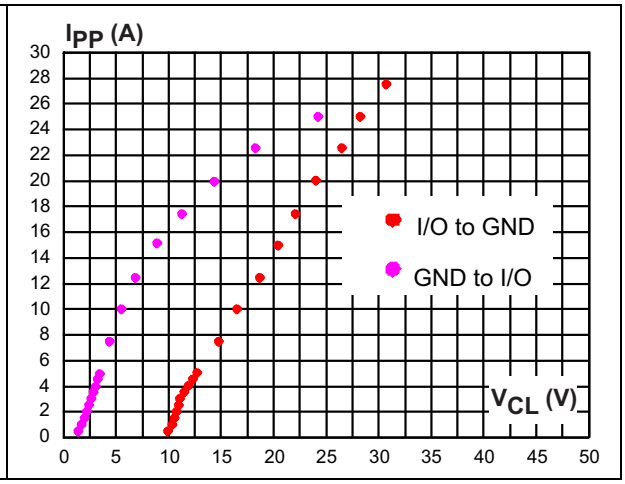


Figure 12. Peak pulse power versus initial junction temperature (maximum values, pulse 8/20 µs)

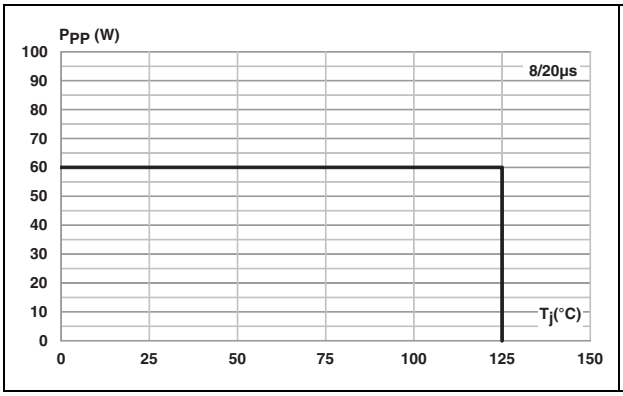


Figure 13. Peak pulse power versus exponential pulse duration (maximum values)

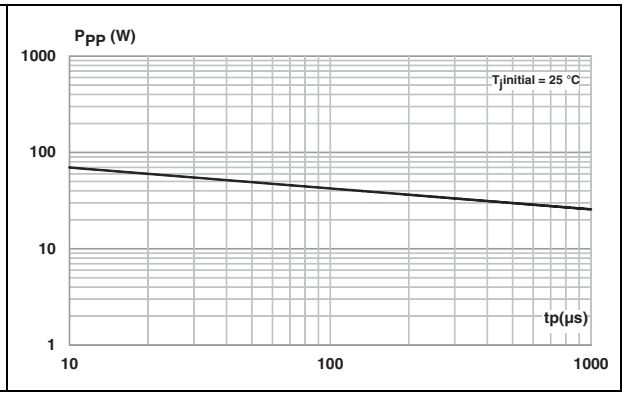


Figure 14. Clamping voltage versus peak pulse current (typical values)

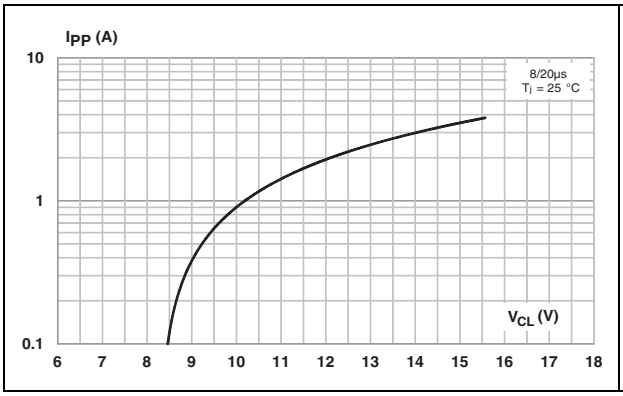
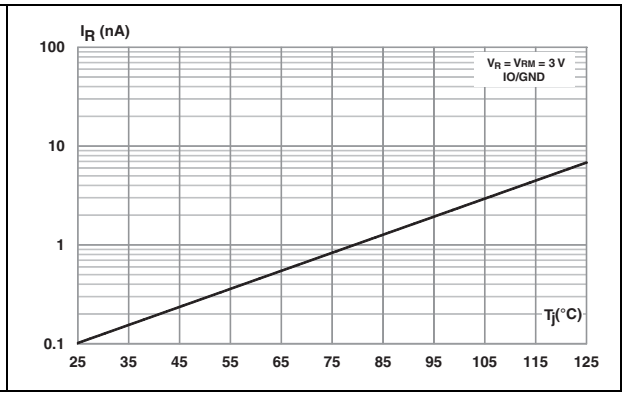


Figure 15. Leakage current versus junction temperature (typical values)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 16. Package dimensions

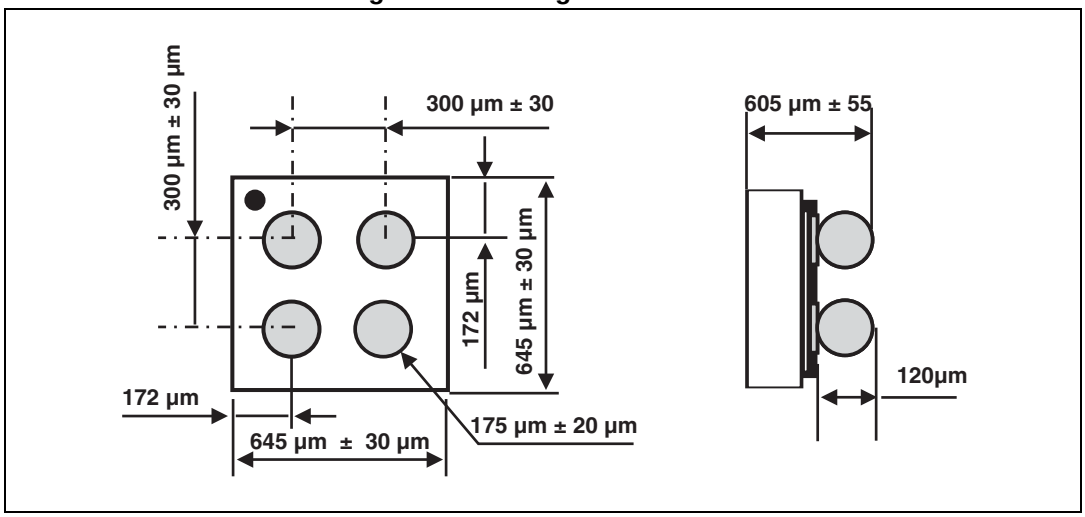


Figure 17. Footprint recommendations

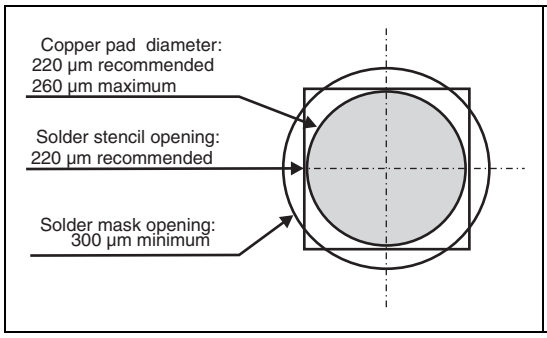


Figure 18. Marking

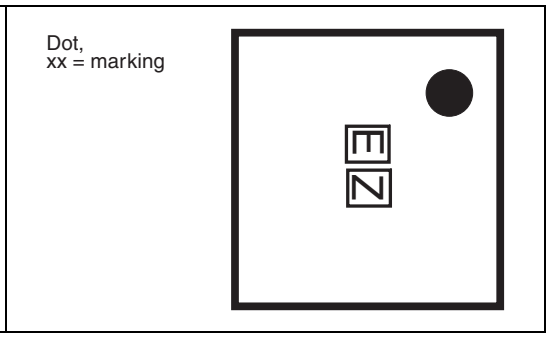
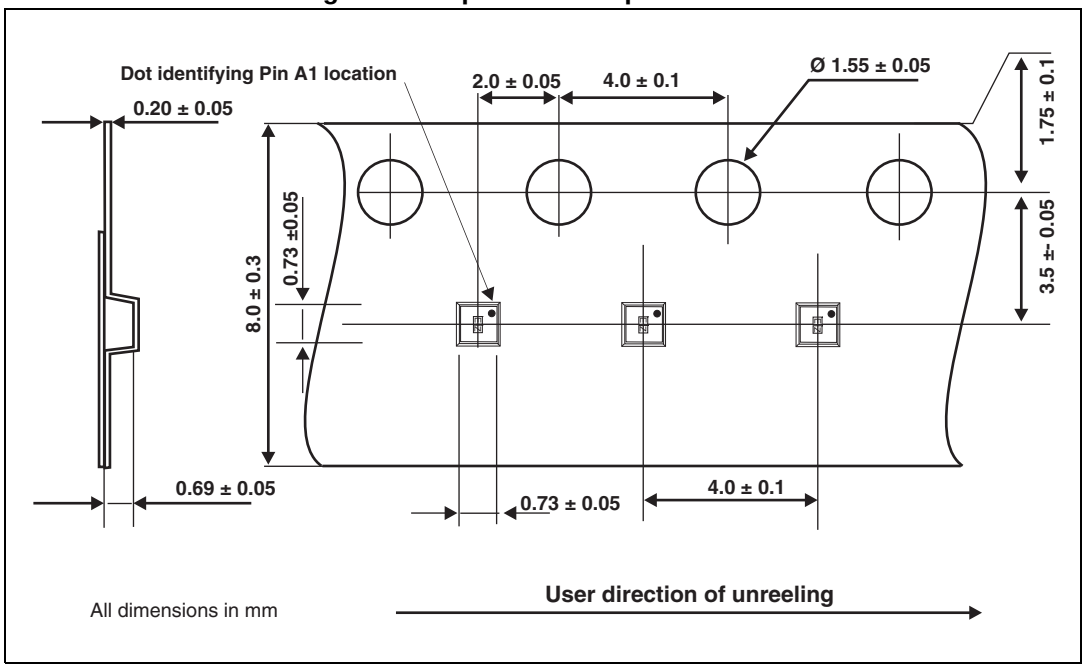


Figure 19. Tape and reel specifications



Note: More information is available in the STMicroelectronics Application notes:
AN4208: "Flip Chip: Package description and recommendations for use"
AN1751: "EMI Filters: Recommendations and measurements"

3 Ordering information

Figure 20. Ordering information scheme

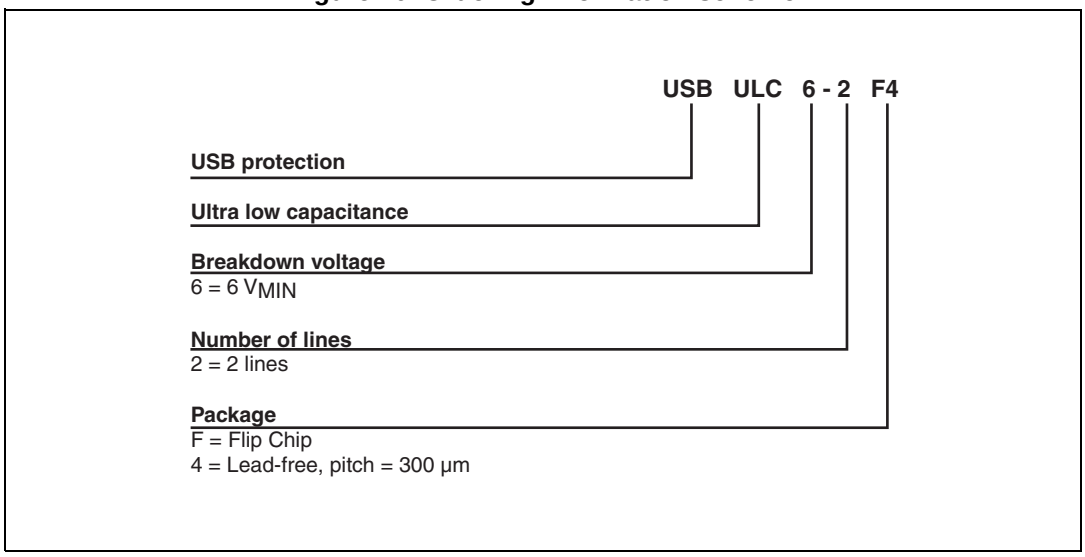


Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBULC6-2F4	EZ	Flip Chip	0.516 mg	5000	Tape and reel (7”)

4 Revision history

Table 4. Document revision history

Date	Revision	Changes
20-Dec-2013	1	Initial release.

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