USB5434B

4-Port SS/HS USB Hub Controller

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB5434B hub is a 4-port SuperSpeed/Hi-Speed, low-power, configurable hub controller family fully compliant with the *USB 3.0 Specification*. The USB5434B supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS) and 1.5 Mbps Low-Speed (LS) USB signalling for complete coverage of all defined USB operating speeds.

The USB5434B supports legacy USB speeds through its USB 2.0 hub controller. The new SuperSpeed hub controller operates in parallel with the USB 2.0 controller, so the 5 Gbps SuperSpeed data transfers are not affected by the slower USB 2.0 traffic.

The USB5434B is configured for operation through internal default settings.

Features

- USB 3.0 compliant 5 Gbps, 480 Mbps, 12 Mbps and 1.5 Mbps operation, USB pins are 5 V tolerant
  - Integrated termination and pull-up/pull-down resistors
- Four downstream USB 3.0 ports
- Optimized for low-power operation and low thermal dissipation
- Single 25 MHz XTAL or clock input for all on-chip PLL and clocking requirements
- Supports JTAG boundary scan
- IETF RFC 4122 compliant 128-bit UUID

Software Features

- Compatible with Microsoft Windows 7, Vista, XP, Mac OSX10.4+, and Linux Hub Drivers

Order Numbers:

ORDER NUMBERS*	DESCRIPTION	LEAD-FREE ROHS COMPLIANT PACKAGE	TEMPERATURE RANGE
USB5434B-JZX	USB 3.0 4-Port Hub	64QFN 9 x 9mm 6.0 mm exposed pad	0ºC to 70ºC

* Add “TR” to the end of any order number to order tape and reel. Reel size is 3000 pieces.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
`code`	Instruction code, or API function or parameter
Section Name	Section or Document name
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

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Chapter 1 Block Diagram

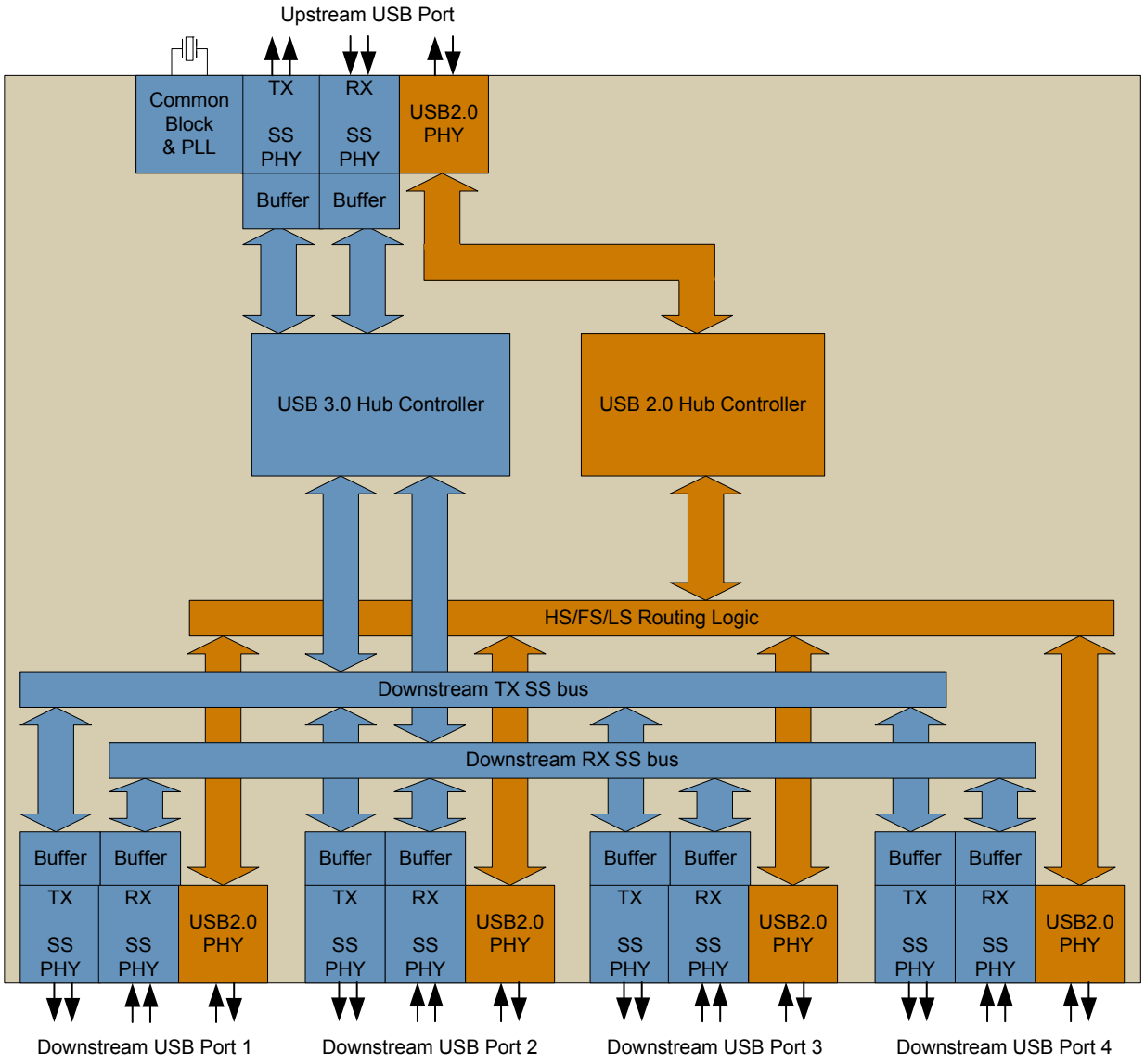


Figure 1.1 USB5434B Block Diagram

Chapter 2 Overview

The SMSC USB5434B hub is a 4-port, low-power Hub Controller fully compliant with the *USB 3.0 Specification* [2]. The USB5434B supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS) and 1.5 Mbps Low-Speed (LS) USB signalling for complete coverage of all defined USB operating speeds.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB5434B includes MultiTRAK™ technology, which implements a dedicated Transaction Translator (TT) for each port. Dedicated TTs help maintain consistent full-speed data throughput regardless of the number of active downstream connections.

The hub controller provides a default configuration, expediting implementation.

Chapter 3 Pin Information

This chapter outlines the pinning configurations for each chip. The detailed pin descriptions are listed by function in Section 3.2: *Pin Descriptions (Grouped by Function)* on page 10.

3.1 Pin Configurations

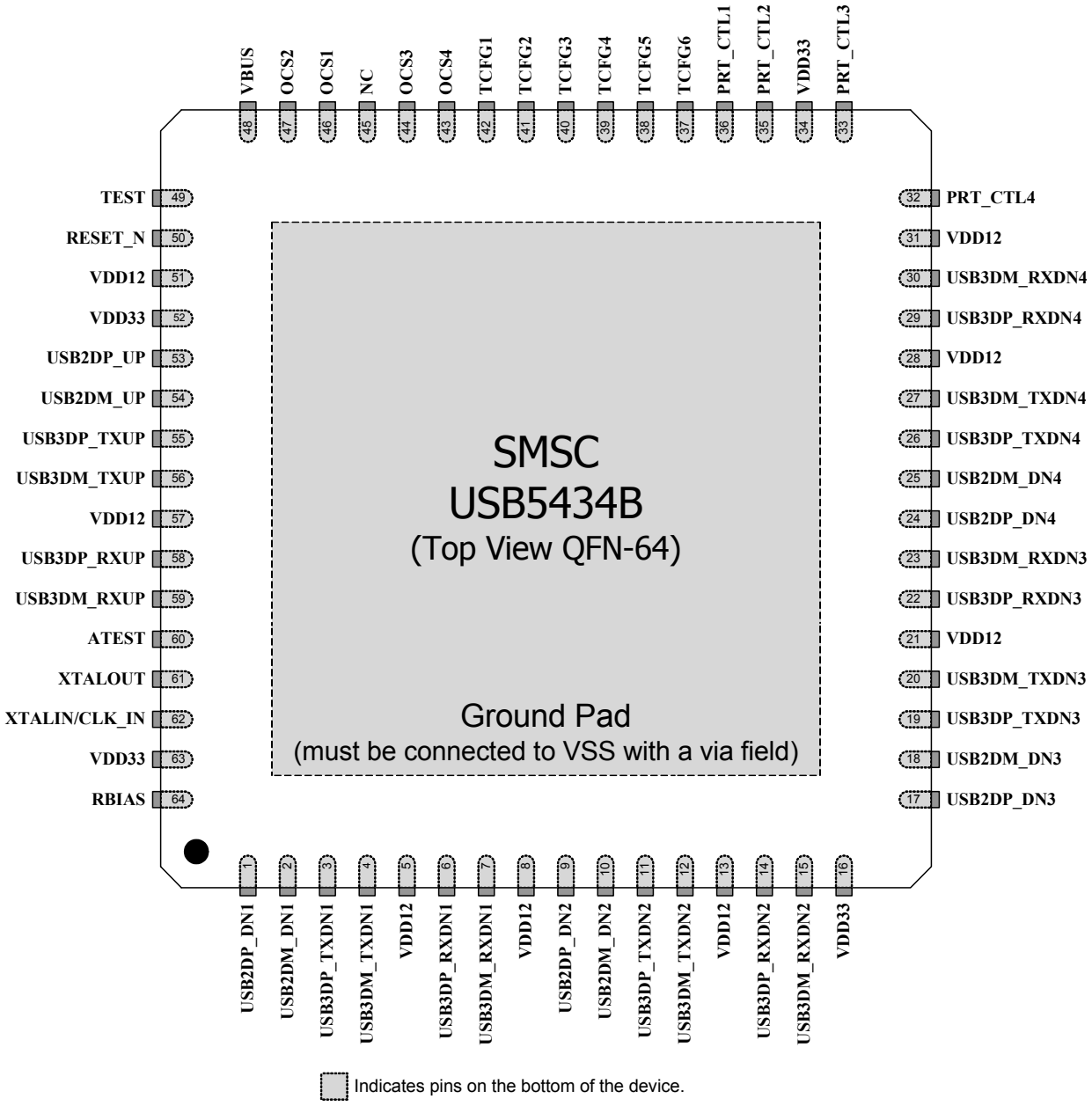


Figure 3.1 USB5434B 64-Pin QFN

3.2 Pin Descriptions (Grouped by Function)

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Table 3.1 USB5434B Pin Descriptions

SYMBOL	BUFFER TYPE	DESCRIPTION
USB 3.0 INTERFACE		
USB3DP_TXUP	IO-U	USB 3 Upstream Upstream SuperSpeed transmit data plus
USB3DM_TXUP	IO-U	USB 3 Upstream Upstream SuperSpeed transmit data minus
USB3DP_RXUP	IO-U	USB 3 Upstream Upstream SuperSpeed receive data plus
USB3DM_RXUP	IO-U	USB 3 Upstream Upstream SuperSpeed receive data minus
USB3DP_TXDN[4:1]	IO-U	USB 3 Downstream Downstream SuperSpeed transmit data plus for ports 1 through 4.
USB3DM_TXDN[4:1]	IO-U	USB 3 Downstream Downstream SuperSpeed transmit data minus for ports 1 through 4.
USB3DP_RXDN[4:1]	IO-U	USB 3 Downstream Downstream SuperSpeed receive data plus for ports 1 through 4.
USB3DM_RXDN[4:1]	IO-U	USB 3 Downstream Downstream SuperSpeed receive data minus for ports 1 through 4.
USB 2.0 INTERFACE		
USB2DP_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals.
USB2DM_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals.
USB2DP_DN[4:1]	IO-U	USB Downstream Downstream Hi-Speed data plus for ports 1 through 4.
USB2DM_DN[4:1]	IO-U	USB Downstream Downstream Hi-Speed data minus for ports 1 through 4.

Table 3.1 USB5434B Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
USB PORT CONTROL		
PRT_PWR[4:1]/ PRT_CTL[4:1]	O12	USB Power Enable Enables power to USB peripheral devices downstream.
VBUS	I/O12	Upstream VBUS Power Detect This pin can be used to detect the state of the upstream bus power.
OCS1	I/O12	Over-Current Sense 1 Input from external current monitor indicating an over-current condition.
OCS2	I/O12	Over-Current Sense 2 Input from external current monitor indicating an over-current condition.
OCS3	I/O12	Over-Current Sense 3 Input from external current monitor indicating an over-current condition.
OCS4	I/O12	Over-Current Sense 4 Input from external current monitor indicating an over-current condition.
MISC		
RESET_N	IS	Reset Input The system uses this active low signal to reset the chip. The active low pulse should be at least 1 μs wide.
XTALIN	ICLKx	Crystal Input: 25 MHz crystal. This pin connects to either one terminal of the crystal or to an external 25 MHz clock when a crystal is not used.
CLK_IN		External Clock Input This pin connects to either one terminal of the crystal or to an external 25 MHz clock when a crystal is not used.
XTALOUT	OCLKx	Crystal Output The clock output, providing a crystal 25 MHz. When an external clock source is used to drive **XTALIN/CLK_IN**, this pin becomes a no connect.
TEST	IPD	Test Pin Treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.
RBIAS	I-R	USB Transceiver Bias A12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
ATEST	A	Analog Test Pin This signal is used for testing the chip and must always be connected to ground.
TCFG1	-	Test Configuration 1 In the default configuration, this pin is tied to **VDD33**.

Table 3.1 USB5434B Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
TCFG2	-	Test Configuration 2 In the default configuration, this pin is pulled-up to **VDD33** through a 10 kΩ resistor.
TCFG3	-	Test Configuration 3 In the default configuration, this pin is tied to **VDD33**.
TCFG4	-	Test Configuration 4 In the default configuration, this pin is a no connect.
TCFG5	-	Test Configuration 5 In the default configuration, this pin is pulled-down to **VSS** through a 10 kΩ resistor.
TCFG6	-	Test Configuration 6 In the default configuration, this pin is pulled-up to **VDD33** through a 10 kΩ resistor.
(1) **NC**	-	No connect pins
DIGITAL AND POWER		
(4) **VDD33**		3.3 V Power
(8) **VDD12**		1.25 V Power
VSS		Ground Pad This exposed pad is the device's only connection to VSS and the primary thermal conduction path. Connect to an appropriate via field.

3.3 Buffer Type Descriptions

Table 3.2 Buffer Type Descriptions

BUFFER TYPE	DESCRIPTION
I	Input
I/O	Input/output
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
O12	Output 12 mA
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/OSD12	Open drain with Schmitt trigger and 12 mA sink.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
I/O-U	Analog input/output defined in USB specification

Chapter 4 DC Parameters

4.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_A	-55	150	°C	
Lead Temperature				°C	Refer to JEDEC Specification J-STD-020D.
1.25 V supply voltage	V_{DD12}	-0.5	1.6	V	
3.3 V supply voltage	V_{DD33}	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	(3.3 V supply voltage + 2) ≤ 6	V	
Voltage on any signal powered by VDD33 rail		-0.5	V_{DD33} + 0.3	V	
Voltage on any signal pin powered by the VDD12		-0.5	VDD12 + 0.3	V	
HBM ESD Performance			2	kV	

Notes:

- Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only. Therefore, functional operation of the device at any condition above those indicated in the operation sections of this specification are not implied.
- When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

4.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
USB5434Bi Operating Temperature	T_A	-40	85	°C	
USB5434B Operating Temperature	T_A	0	70	°C	
1.25 V supply voltage	V_{DD12}	1.22	1.31	V	
3.3 V supply voltage	V_{DD33}	3.0	3.6	V	
1.25 V supply rise time	t_{RT}	0	400	µs	(Figure 4.1)
3.3 V supply rise time	t_{RT}	0	400	µs	(Figure 4.1)
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal powered by VDD33 rail		-0.3	V_{DD33}	V	

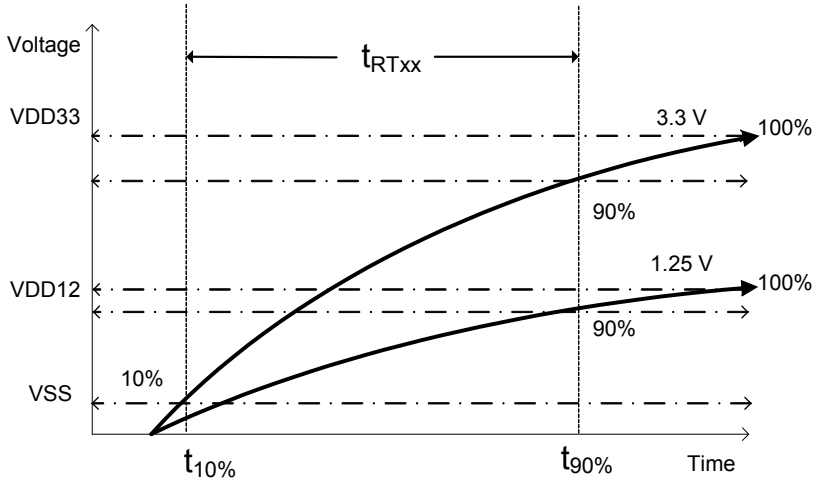


Figure 4.1 Supply Rise Time Model

4.3 DC Electrical Characteristics

Table 4.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis (IS only)	V_{HYSI}		420		mV	
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	V_{IN} = 0
Pull Up	PU		58		µA	V_{IN} = **VDD33**
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.3	V	
High Input Level	V_{IHCK}	0.8			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to **VDD33**
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = **VDD33**
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ **VDD33** = 3.3 V
High Output Level	V_{OH}	V_{DD33} -0.4			V	I_{OH} = -12 mA @ **VDD33** = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to **VDD33** (Note 4.1)

Table 4.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ **VDD33** = 3.3 V
High Output Level	V_{OH}	V_{DD33} -0.4			V	I_{OH} = -12 mA @ **VDD33** = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to **VDD33** (Note 4.1)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U (Note 4.2)						

Note 4.1 Output leakage is measured with the current pins in high impedance.

Note 4.2 See *USB 2.0 Specification* [1] for USB DC electrical characteristics.

4.4 Capacitance

Table 4.2 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins except USB pins and the pins under the test tied to AC ground
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

Note 4.3 Capacitance T_A = 25°C; fc = 1 MHz; VDD33 = 3.3 V

Chapter 5 AC Specifications

5.1 Oscillator/Crystal

Crystal: Parallel resonant, fundamental mode, 25 MHz ±30 ppm

External Clock: 50% duty cycle ± 10%, 25 MHz ± 30 ppm, jitter < 100 ps rms

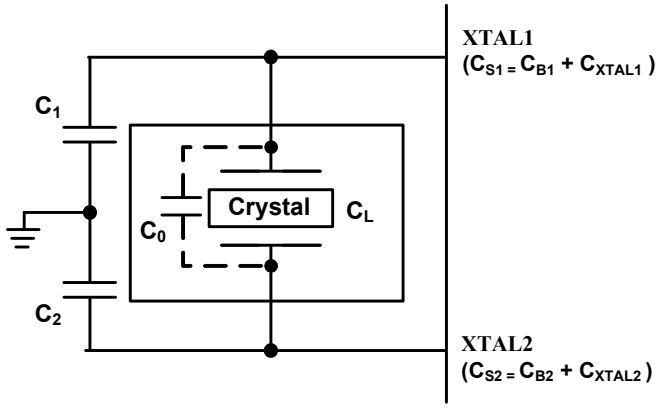


Figure 5.1 Typical Crystal Circuit

Table 5.1 Crystal Circuit Legend

SYMBOL	DESCRIPTION	IN ACCORDANCE WITH
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (Note 5.1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	SMSC IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	SMSC IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 5.2 (Note 5.2)
C_2		

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 5.2 Formula to Find the Value of C_1 and C_2

Note 5.1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to 0 for use in the calculation of the capacitance formulas in Figure 5.2. However, the PCB itself may present a parasitic capacitance between **XTALIN** and **XTALOUT**. For an accurate calculation of C_1 and C_2, take the parasitic capacitance between traces **XTALIN** and **XTALOUT** into account.

Note 5.2 Consult crystal manufacturer documentation for recommended capacitance values.

5.2 External Clock

50% duty cycle ± 10%, 25 MHz ± 30 ppm, jitter < 100 ps rms.

Note: The external clock is based upon 1.2 V CMOS Logic. **XTALOUT** should be treated as a no connect when an external clock is supplied.

5.2.1 USB 2.0

The SMSC hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification* [1].

Chapter 6 Package Drawing

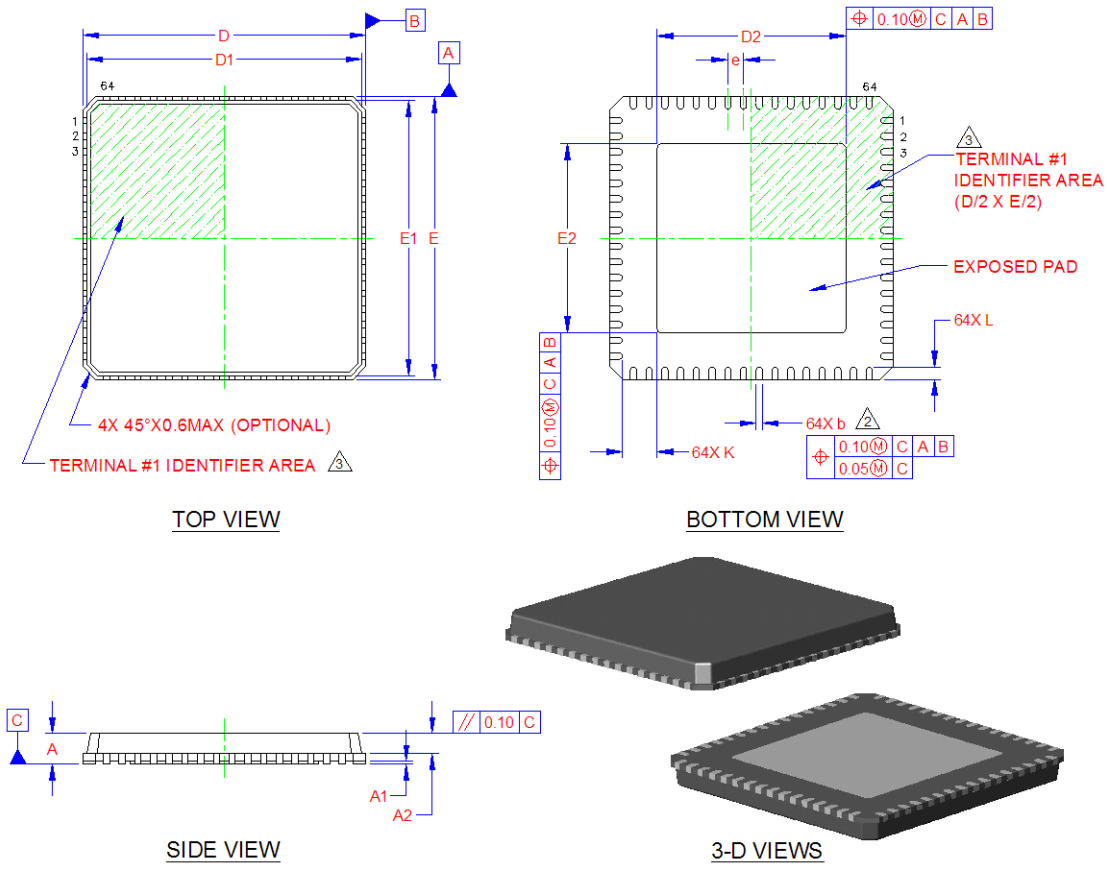


Figure 6.1 USB5434B 64 Pin QFN Package

Table 6.1 USB5434B 64-Pin QFN Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.80	0.85	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
A2	-	0.65	0.80	Mold Cap Thickness
D/E	8.90	9.00	9.10	X/Y Body Size
D1/E1	8.65	8.75	8.85	X/Y Mold Cap Size
D2/E2	5.90	6.00	6.10	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
K	0.90	-	-	Center Pad to Pin Clearance
e	0.50 BSC			Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.

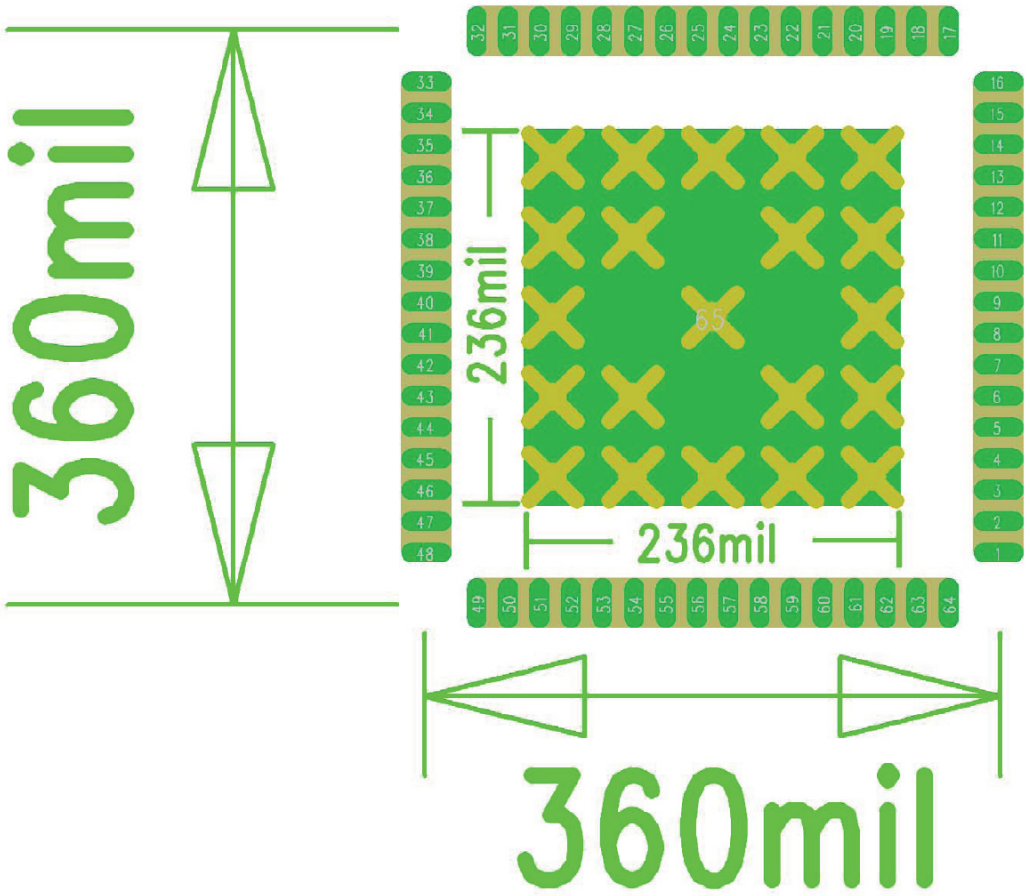


Figure 6.2 Recommended PCB Land Pattern

Chapter 7 Revision History

Table 7.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 (09-06-12)	All	Initial revision.

Appendix A (Acronyms)

I²C®: Inter-Integrated Circuit[1]

OCS: Over-Current Sense

PCB: Printed Circuit Board

PHY: Physical Layer

PLL: Phase-Locked Loop

QFN: Quad Flat No Leads

RoHS: Restriction of Hazardous Substances Directive

SCL: Serial Clock

SIE: Serial Interface Engine

SMBus: System Management Bus

TT: Transaction Translator

1.I²C is a registered trademark of Philips Corporation.

Appendix B (References)

[1] Universal Serial Bus Specification, Version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata)
USB Implementers Forum, Inc. http://www.usb.org

[2] Universal Serial Bus Specification, Version 3.0, November 13, 2008
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[3] System Management Bus Specification, version 1.0
SMBus. http://smbus.org/specs/

[4] MicroChip 24AA02/24LC02B (Revision C)
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