# USB2503/ USB2503A

# Integrated USB 2.0 Compatible 3-Port Hub

## PRODUCT FEATURES

**Datasheet**

- Integrated USB 2.0 Compatible 3-Port Hub
  - 3 Transaction Translators for highest performance
  - High-Speed (480Mbits/s), Full-Speed (12Mbits/s) and Low-Speed (1.5Mbits/s) compatible
  - Full power management with per port or ganged, selectable power control
  - Detects Bus-Power/Self-Power source and changes mode automatically
- Complete USB Specification 2.0 Compatibility
  - Includes USB 2.0 Transceivers
- VID/PID/DID, and Port Configuration for Hub via:
  - Single Serial $I^2C$ EEPROM
  - SMBus Slave Port
- Default VID/PID/DID, allows functionality when configuration EEPROM is absent
- Hardware Strapping options allow for configuration without an external EEPROM or SMBus Host
- On-Board 24MHz Crystal Driver Circuit or 24 MHz external clock driver
- Internal PLL for 480MHz USB 2.0 Sampling
- Internal 1.8V Linear Voltage Regulator
- Integrated USB termination and Pull-up/Pull-down resistors
- Internal Short Circuit protection of USB differential signal pins
- 1.8 Volt Low Power Core Operation
- 3.3 Volt I/O with 5V Input Tolerance
- 48 Pin QFN lead-free RoHS compliant package

## ORDER NUMBERS:

**USB2503/USB2503A-HZH FOR 48 PIN QFN LEAD-FREE ROHS COMPLIANT PACKAGE**

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# Chapter 1 General Description

The SMSC 3-Port Hub is fully compliant with the USB 2.0 Specification and will attach to a USB host as a Full-Speed Hub or as a Full-/High-Speed Hub. The 3-Port Hub supports Low-Speed, Full-Speed, and High-Speed (if operating as a High-Speed Hub) downstream devices on all of the enabled downstream ports.

A dedicated Transaction Translator (TT) is available for each downstream facing port. This architecture ensures maximum USB throughput for each connected device when operating with mixed-speed peripherals.

The Hub works with an external USB power distribution switch device to control $V_{BUS}$ switching to downstream ports, and to limit current and sense over-current conditions.

All required resistors on the USB ports are integrated into the Hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

Throughout this document the upstream facing port of the hub will be referred to as the upstream port, and the downstream facing ports will be called the downstream ports.

## 1.1 OEM Selectable Features

A default configuration is available in the USB2503/USB2503A following a reset. This configuration may be sufficient for some applications. Strapping option pins make it possible to modify a limited sub-set of the configuration options.

The USB2503/USB2503A may also be configured by an external EEPROM or a microcontroller. When using the microcontroller interface, the Hub appears as an SMBus slave device. If the Hub is pin-strapped for external EEPROM configuration but no external EEPROM is present, then a value of ‘0’ will be written to all configuration data bit fields (the hub will attach to the host with all ‘0’ values).

The 3-Port Hub supports several OEM selectable features:

- Operation as a Self-Powered USB Hub or as a Bus-Powered USB Hub.
- Operation as a Dynamic-Powered Hub (Hub operates as a Bus-Powered device if a local power source is not available and switches to Self-Powered operation when a local power source is available).
- Multiple Transaction Translator (Multi-TT) or Single-TT support.
- Optional OEM configuration via I2C EEPROM or via the industry standard SMBus interface from an external SMBus Host.
- Port power switching on an individual or ganged basis.
- Port over-current monitoring on an individual or ganged basis.
- Compound device support (port is permanently hardwired to a downstream USB peripheral device).
- Hardware strapping options enable configuration of the following features.
  Non-Removable Ports
  Port Power Polarity (active high or active low logic)
  Port Disable
  Ganged Vs Port power switching and over-current sensing

# Chapter 2 Pin Table 3-Port

**Table 2.1 3-Port Pin Table**

| | | | |
|---|---|---|---|
| **UPSTREAM USB 2.0 INTERFACE (3-PINS)** | | | |
| USBDP0 | USBDN0 | VBUS_DET | |
| **3-PORT USB INTERFACE (18-PINS)** | | | |
| USBDP1 | USBDN1 | USBDP2 | USBDN2 |
| USBDP3 | USBDN3 | GR1/<br>NON_REM0 | GR2/<br>NON_REM1 |
| GR3/<br>PRT_DIS0 | PRTPWR1 | PRTPWR2 | PRTPWR3 |
| PRTPWR_POL | OCS1_N | OCS2_N | OCS3_N |
| GANG_EN | RBIAS | | |
| **SERIAL PORT (3-PINS)** | | | |
| SDA/SMBDATA | SCL/SMB-<br>CLK/CFG_SEL0 | CFG_SEL1 | |
| **MISC (8-PINS)** | | | |
| XTAL1/CLKIN | XTAL2 | RESET_N | SELF_PWR |
| TEST1 | TEST0 | ATEST/<br>REG_EN | CLKIN_EN |
| **POWER & GROUNDS (16-PINS)** | | | |

# Chapter 3 Pin Configuration 3-Port Hub

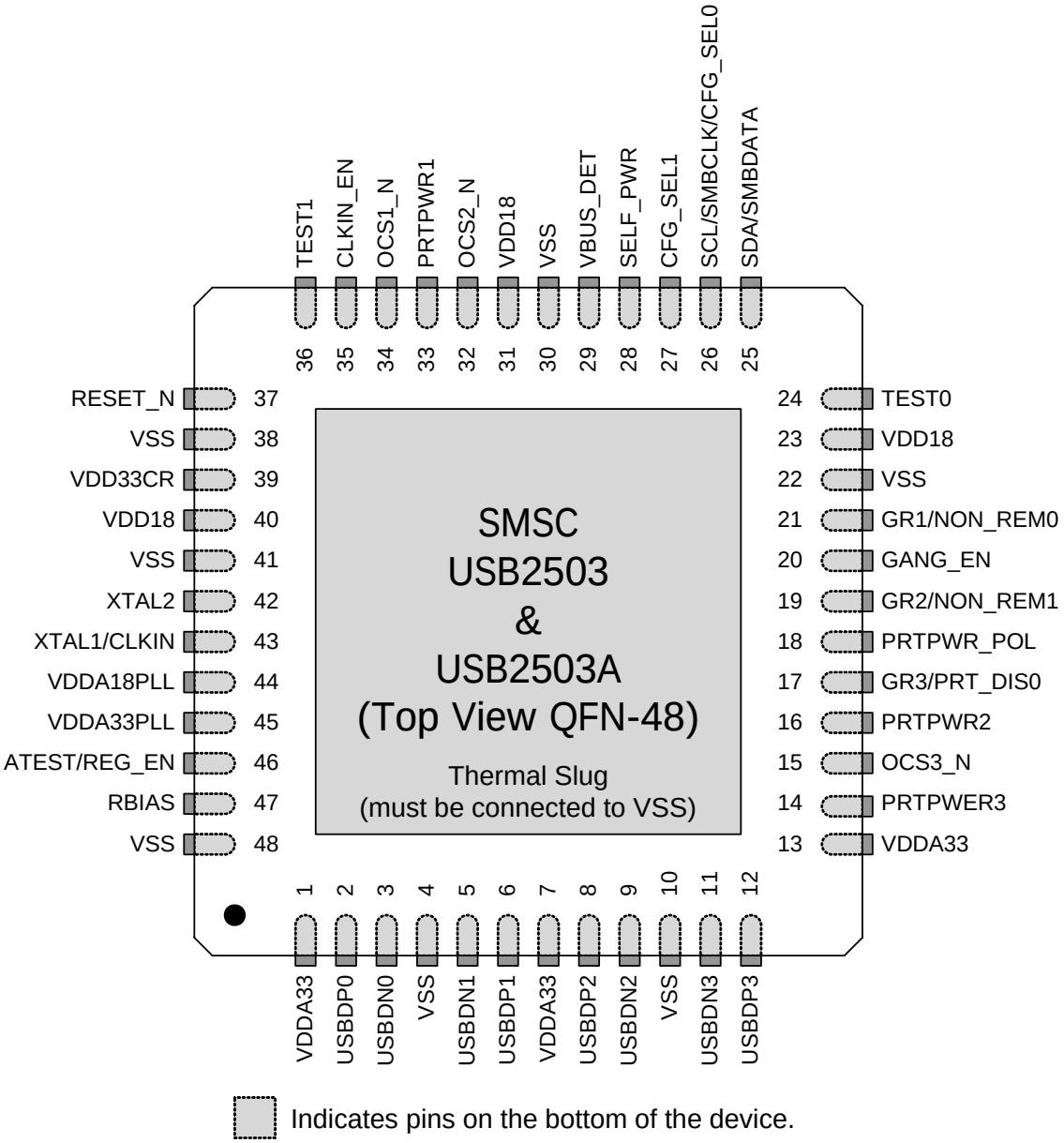



**Figure 3.1 3-Port 48-Pin QFN**

# Chapter 4 3-Port Hub Block Diagram

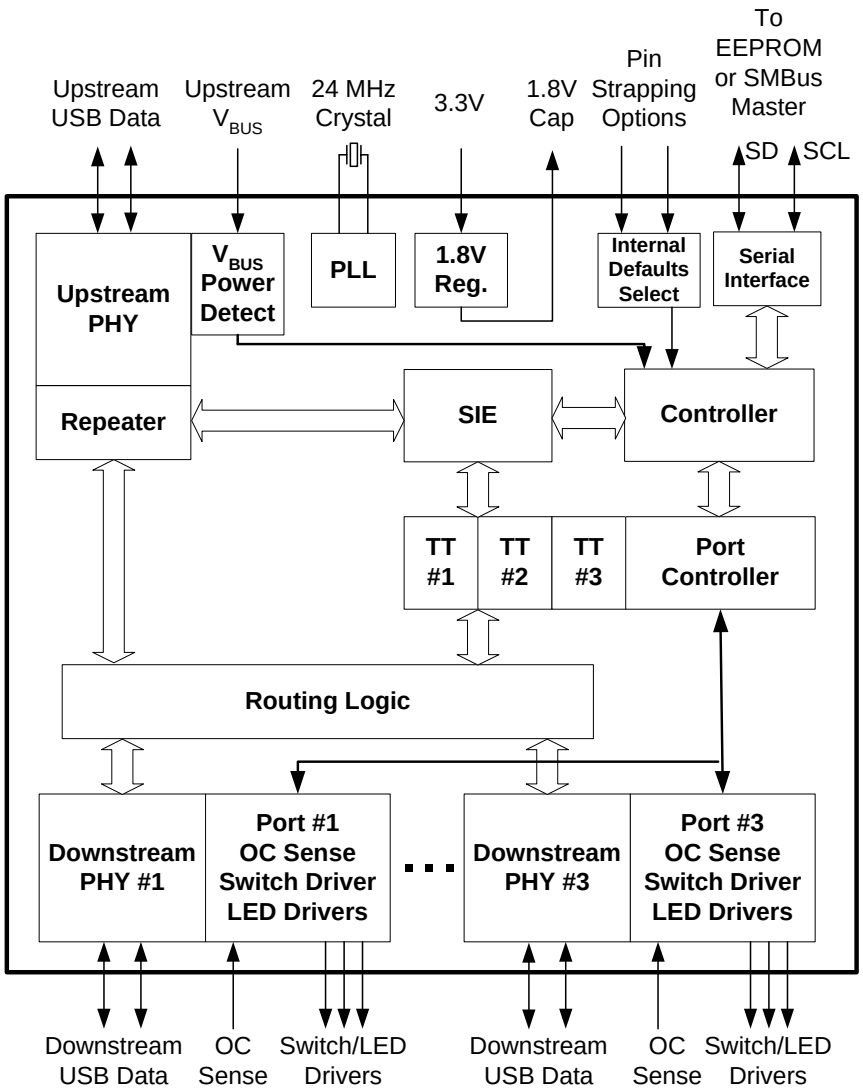



**Figure 4.1 3-Port Block Diagram**

**Table 4.1 3-Port Hub Pin Descriptions**

| NAME | SYMBOL | TYPE | FUNCTION |
|---|---|---|---|
| **UPSTREAM USB 2.0 INTERFACE** | | | |
| USB Bus Data | USBDN0<br>USBDP0 | IO-U | These pins connect to the USB bus data signals. |
| Detect Upstream VBUS Power | VBUS_DET | I/O12 | Detects state of Upstream VBUS power (indicates the power-managed state of the upstream device). |

**Table 4.1 3-Port Hub Pin Descriptions (continued)**

| NAME | SYMBOL | TYPE | FUNCTION |
|---|---|---|---|
| **3-PORT USB 2.0 HUB INTERFACE** | | | |
| High-Speed USB Data | USBDN[3:1]<br>USBDP[3:1] | IO-U | These pins connect to the downstream USB peripheral devices attached to the Hub's ports. |
| USB Power Enable | PRTPWR[3:1] | O12 | Enables power to USB peripheral devices (downstream).<br><br>The active signal level of the PRTPWR[3:1] pins are determined by the Power Polarity Strapping function of the PRTPWR_POL pin. |
| Port 3 Green LED<br>&<br>Port Disable strapping option. | GR3/<br>PRT_DIS0 | I/O12 | Green indicator LED for port 3. Will be active low when LED support is enabled via EEPROM or SMBus.<br><br>If the hub is configured by the internal default configuration, these pins will be sampled at RESET_N negation to determine if port 3 will be permanently disabled. Also, the active state of the LED will be determined as follows:<br><br>PRT_DIS0 = '0', All ports are enabled,<br>GR3 is active high.<br><br>PRT_DIS0 = '1', Port 3 is disabled,<br>GR3 is active low. |
| Port [2:1] Green LED<br>&<br>Port Non-Removable strapping option. | GR[2:1]/<br>NON_REM[1:0] | I/O12 | Green indicator LED for ports 2 and 1. Will be active low when LED support is enabled via EEPROM or SMBus.<br><br>If the hub is configured by the internal default configuration, these pins will be sampled at RESET_N negation to determine if ports [3:1] contain permanently attached (non-removable) devices. Also, the active state of the LED's will be determined as follows:<br><br>NON_REM[1:0] = '00', All ports are removable,<br>GR2 is active high,<br>GR1 is active high.<br><br>NON_REM1:0] = '01', Port 1 is non-removable,<br>GR2 is active high,<br>GR1 is active low.<br><br>NON_REM[1:0] = '10', Ports 1 & 2 are non-removable,<br>GR2 is active low,<br>GR1 is active high.<br><br>NON_REM[1:0] = '11', Ports 1, 2, & 3 are non-removable,<br>GR2 is active low,<br>GR1 is active low. |
| Gang Power Switching and Current Sensing strapping option. | GANG_EN | I/O12 | If the hub is configured by the internal default configuration, this pin will be sampled at RESET_N negation to determine if downstream port power switching and current sensing are ganged, or individual port-by-port.<br><br>'0' = Port-by-port sensing & switching.<br>'1' = Ganged sensing & switching. |

**Table 4.1 3-Port Hub Pin Descriptions (continued)**

| NAME | SYMBOL | TYPE | FUNCTION |
|---|---|---|---|
| Port Power Polarity strapping. | PRTPWR_POL | I/O12 | Port Power Polarity strapping determination for the active signal polarity of the PRTPWR[3:1] pins.<br><br>While RESET_N is asserted, the logic state of this pin will (though the use of internal combinatorial logic) determine the active state of the PRTPWR[3:1] pins in order to ensure that downstream port power is not inadvertently enabled to inactive ports during a hardware reset.<br><br>When RESET_N is negated, the logic value will be latched internally, and will retain the active signal polarity for PRTPWR[3:1] pins.<br><br>'1' = PRTPWR[3:1] pins have an active 'high' polartity<br>'0' = PRTPWR[3:1] pins have an active 'low' polarity |
| Over Current Sense | OCS[3:1]_N | IPU | Input from external current monitor indicating an over-current condition. {Note: Contains internal pull-up to 3.3V supply} |
| USB Transceiver Bias | RBIAS | I-R | A 12.0kΩ (+/– 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings. |
| **SERIAL PORT INTERFACE** | | | |
| Serial Data/SMB Data | SDA/SMBDATA | IOSD12 | (Serial Data)/(SMB Data) signal. |
| Serial Clock/SMB Clock<br>&<br>Chip Select / EEPROM Select | SCL/SMBCLK/ CFG_SEL0 | IOSD12 | (Serial Clock)/(SMB Clock) signal. This multifunction pin is read on the rising edge of RESET_N negation and will determine the hub configuration method as described in Table 4.2. |
| SMB Programming Select | CFG_SEL1 | I | This pin is read on the rising edge of RESET_N negation and will detemine the hub configuration method as described in Table 4.2. |

**Table 4.2 SMBus or EEPROM Interface Behavior**

| CFG_SEL1 | CFG_SEL0 | SMBus or EEPROM interface behavior. |
|---|---|---|
| 0 | X | Configured as an SMBus slave for external download of user-defined descriptors. SMBus slave address is :0101101 |
| 1 | 0 | Internal Default Configuration via strapping options. |
| 1 | 1 | 2-wire (I2C) EEPROMS are supported, and CFG_SEL0 has no other functionality. |

**Table 4.3 Miscellaneous Pins**

| NAME | SYMBOL | TYPE | FUNCTION |
|---|---|---|---|
| Crystal Input/External Clock Input | XTAL1/ CLKIN | ICLKx | 24MHz crystal or external clock input.<br>This pin connects to either one terminal of the crystal or to an external 24MHz clock when a crystal is not used. |

**Table 4.3 Miscellaneous Pins (continued)**

| NAME | SYMBOL | TYPE | FUNCTION |
|---|---|---|---|
| Crystal Output | XTAL2 | OCLKx | 24MHz Crystal<br>This is the other terminal of the crystal, or left unconnected when an external clock source is used to drive XTAL1/CLKIN. It must not be used to drive any external circuitry other than the crystal circuit. |
| Clock Input Enable | CLKIN_EN | I | Clock In Enable:<br>Low = XTAL1 and XTAL2 pins configured for use with external crystal<br>High = XTAL1 pin configured as CLKIN, and must be driven by an external CMOS clock. |
| RESET Input | RESET_N | IS | This active low signal is used by the system to reset the chip. The minimum active low pulse is 100ns. |
| Self-Power / Bus-Power Detect | SELF_PWR | I | Detects availability of local self-power source.<br>Low = Self/local power source is NOT available (i.e., 7-Port Hub gets all power from Upstream USB VBus).<br>High = Self/local power source is available. |
| TEST Pins | TEST[1:0] | IPD | Used for testing the chip. User must treat as a no-connect or connect to ground. For board testing, all signal pins are included in an XNOR chain, Please see Chapter 6, "XNOR Test," on page 37 for more details on the configuration and use of the XNOR mode. |
| Analog Test & Internal 1.8V voltage regulator enable | ATEST/ REG_EN | AIO | This signal is used for testing the analog section of the chip, and to enable or disable the internal 1.8v regulator.<br><br>This pin must be connected to VDDA3P3 to enable the internal 1.8V regulator, or to VSS to disable the internal regulator.<br><br>When the internal regulator is enabled, the 1.8V power pins must be left unconnected, except for the required bypass capacitors.When the PHY is in test mode, the internal regulator is disabled and the ATEST pin functions as a test pin. |

**Table 4.4 Power, Ground, and No Connect**

| NAME | SYMBOL | TYPE | FUNCTION |
|---|---|---|---|
| VDD1P8 | VDD18 | | +1.8V core power.<br><br>If the internal regulator is enabled, then VDD18 pin closest to VDD33CR must have a 4.7µF (or greater) ±20% (ESR <0.1Ω) capacitor to VSS |
| VDDPLL1P8 | VDDA18PLL | | +1.8V Filtered analog power for internal PLL.<br><br>If the internal regulator is enabled, then this pin must have a 4.7µF (or greater) ±20% (ESR <0.1Ω) capacitor to VSS |
| VDDAPLL3P3 | VDDA33PLL | | +3.3V Filtered analog power for the internal PLL<br><br>If the internal PLL 1.8V regulator is enabled, then this pin acts as the regulator input |
| VDDA3P3 | VDDA33 | | +3.3V Filtered analog power. |

**Table 4.4 Power, Ground, and No Connect (continued)**

| NAME | SYMBOL | TYPE | FUNCTION |
|---|---|---|---|
| VDD3P3 CORE PLL | VDD33CR | | +3.3V I/O and Core power. |
| VSS | VSS | | Ground. |

**Table 4.5 Buffer Type Descriptions**

| BUFFER | DESCRIPTION |
|---|---|
| I | Input. |
| IPD | Input, with a weak Internal pull-down. |
| IPU | Input, with a weak Internal pull-up. |
| IS | Input with Schmitt trigger. |
| O12 | Output 12mA. |
| I/O12 | Input/Output, 12mA |
| IOSD12 | Open drain….12mA sink with Schmitt trigger, and must meet I2C-Bus Specification Version 2.1 requirements. |
| ICLKx | XTAL Clock Input |
| OCLKx | XTAL Clock Output |
| I-R | *RBIAS. |
| IO-U | Defined in USB Specification.<br>Note: Meets USB 1.1 requirements when operating as a 1.1-compliant device and meets USB 2.0 requirements when operating as a 2.0-compliant device. |
| AIO | Analog Input/output. Per PHY test requirements. |

# Chapter 5 Functional Block Description

## 5.1 3-Port Hub

SMSC's USB 2.0 3-Port Hub is fully specification compliant to the Universal Serial Bus Specification Revision 2.0 April 27,2000 (12/7/2000 and 5/28/2002 Errata). Please reference Chapter 11 (Hub Specification) for general details regarding Hub operation and functionality.

For performance reasons, the 3-Port Hub provides 1 Transaction Translator (TT) per port (defined as Multi-TT configuration), divided into 4 non-periodic buffers per TT.

### 5.1.1 Hub Configuration Options

The SMSC Hub supports a large number of features and must be configured in order to correctly function when attached to a USB host controller. There are three principal ways to configure the hub: SMBus, EEPROM, or by internal default settings. In all cases, the configuration method will be determined by the CFG_SEL1 and CFG_SEL0 pins immediately after RESET_N negation.

#### 5.1.1.1 Vendor ID

Is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options. When using the internal default option, SMSC's VID (see Table 5.1) will be reported.

#### 5.1.1.2 Product ID

Is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options. When using the internal default option, SMSC's PID designation of (see Table 5.1) will be reported.

#### 5.1.1.3 Device ID

Is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options. When using the internal default option, SMSC's DID designation of (see Table 5.1) will be reported.

#### 5.1.1.4 Self-Powered/Bus-Powered

The Hub is  either Self-Powered (draws less than 2mA of upstream bus power) or Bus-Powered (limited to a 100mA maximum of upstream power prior to being configured by the host controller).

When configured as a Bus-Powered device, the SMSC Hub consumes less than 100mA of current prior to being configured. After configuration, the Bus-Powered SMSC Hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100mA per externally available downstream port) must consume no more than 500mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated.

When configured as a Self-Powered device, <1mA of upstream VBUS current is consumed and all 7 ports are available, with each port being capable of sourcing 500mA of current.

This field is set by the OEM using either the SMBus or EEPROM interface options. When using the internal default option, the SELF_PWR pin determines the Self-powered or Bus-powered status.

Please see the description under Dynamic Power for the self/bus power functionality when dynamic power switching is enabled.

#### 5.1.1.5 Port Indicators

Controls the use of LED indicator for Port status information. See Section 11.5.3 of the USB 2.0 Specification for additional details.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.6 High-Speed Disable

Allows an OEM to force the Hub to configure as a Full-Speed device only (i.e. High-Speed not available).

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.7 Multiple-TT Support

Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT) {Note: The host may force Single-TT mode only}.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.8 EOP Disable

During FS operation only, this permits the Hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.9 Current Sensing

Selects current sensing on a port-by-port basis, all ports ganged, or none(only for bus-powered hubs)The ability to support current sensing on a port or ganged basis is hardware implementation dependent.

This field can be set by the OEM using either the SMBus or EEPROM interface options.When using the internal default option, the SELF_PWR pin determines if current sensing will be ganged, or none (ganged if self-powered, none if bus-powered)

#### 5.1.1.10 Downstream Port Power Enabling

Enables all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis. The ability to support power enabling on a port or ganged basis is hardware implementation dependent.

This field is set by the OEM using either the SMBus or EEPROM interface options. When using the internal default option, the GANG_EN pin will configure the hub for ganged or individual port-by-port port power switching.

#### 5.1.1.11 Compound Device

Allows the OEM to indicate that the Hub is part of a compound (see the USB Specification for definition) device. The applicable port(s) must also be defined as having a “Non-Removable Device”.

This field is set by the OEM using either the SMBus or EEPROM interface options.

Note: When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device.

#### 5.1.1.12 Non-Removable Device

Informs the Host if one of the active ports has a permanent device that is undetachable from the Hub. (Note: The device must provide its own descriptor data.)

This field is set by the OEM using either the SMBus or EEPROM interface options. When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable.

#### 5.1.1.13 Self-Powered Port DISABLE

During Self-Powered operation, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The disabled ports must be contiguous, and must be in decreasing order starting with port 3.

This field is set by the OEM using either the SMBus or EEPROM interface options. When using the internal default option, the PRT_DIS0 pin will disable the appropriate ports.

#### 5.1.1.14 Bus-Powered Port DISABLE

During Bus-Powered operation, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The disabled ports must be contiguous, and must be in decreasing order starting with port 3.

This field is set by the OEM using either the SMBus or EEPROM interface options. When using the internal default option, the PRT_DIS0 pin will disable the appropriate ports.

#### 5.1.1.15 Dynamic Power

Controls the ability of the 3-Port Hub to automatically change from Self-Powered operation to Bus-Powered operation if the local power source is removed or is unavailable (and from Bus-Powered to Self-Powered if the local power source is restored). {Note: If the local power source is available, the 3-port Hub will always switch to Self-Powered operation.}

When Dynamic Power switching is enabled, the Hub detects the availability of a local power source by monitoring the external SELF_PWR pin. If the Hub detects a change in power source availability, the Hub immediately disconnects and removes power from all downstream devices and disconnects the upstream port. The Hub will then re-attach to the upstream port as either a Bus-Powered Hub (if local-power in unavailable) or a Self-Powered Hub (if local power is available).

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.16 Over-Current Timer

The time delay (in 2ms increments) for an over-current condition to persist before it is reported to the Host.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.17 Self-Powered Max Power

When in Self-Powered configuration, Sets value in 2mA increments.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.18 Bus-Powered Max Power

When in Bus-Powered configuration, Sets value in 2mA increments.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.19 Self-powered Hub Controller Current

When in Self-Powered configuration, Maximum current requirements of the Hub Controller in 2mA increments.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.20 Bus-Powered Hub Controller Current

When in Bus-Powered configuration, Maximum current requirements of the Hub Controller in 2mA increments.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.21 Power-On Timer

Time (in 2ms intervals) from the time power-on sequence begins on a port until power is good on that port. System software uses this value to determine how long to wait before accessing a powered-on port.

This field is set by the OEM using either the SMBus or EEPROM interface options.

#### 5.1.1.22 Power Switching Polarity

The selection of active state “polarity” for the PRTPWR[3:1] pins is made by a strapping option only.

### 5.1.2 VBus Detect

According to Section 7.2.1 of the USB 2.0 Specification, a downstream port can never provide power to its D+ or D- pull-up resistors unless the upstream port’s VBUS is in the asserted (powered) state. The VBUS_DET pin on the Hub monitors the state of the upstream VBUS signal and will not pull-up the D+ or D- resistor if VBUS is not active. If VBUS goes from an active to an inactive state (Not Powered), Hub will remove power from the D+ or D- pull-up resistor within 10 seconds.

## 5.2 EEPROM Interface

The SMSC Hub can be configured via a 2-wire (I2C) EEPROM. (Please see Figure 4.1, "3-Port Hub Pin Descriptions" for specific details on how to enable the I2C EEPROM option).

The Internal state-machine will, (when configured for EEPROM support) read the external EEPROM for configuration data. The hub will then “attach” to the upstream USB host.

Please see Table 5.1 User-Defined Descriptor Data for a list of data fields available.

### 5.2.1 I2C EEPROM

The I2C EEPROM interface implements a subset of the I2C Master Specification (Please refer to the Philips Semiconductor Standard I2C-Bus Specification for details on I2C bus protocols). The Hub’s I2C EEPROM interface is designed to attach to a single “dedicated” I2C EEPROM, and it conforms to the Standard-mode I2C Specification (100kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility.

**Note:** Extensions to the I2C Specification are not supported.

The Hub acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

#### 5.2.1.1 Implementation Characteristics

Please refer to the MicroChip 24AA00 DataSheet for Protocol and Programming specifics.

#### 5.2.1.2 Pull-Up Resistor

The Circuit board designer is required to place external pull-up resistors (10KΩ recommended) on the SDA/SMBDATA & SCL/SMBCLK/CFG_SELO lines (per SMBus 1.0 Specification, and EEPROM manufacturer guidelines) to Vcc in order to assure proper operation.

#### 5.2.1.3 I2C EEPROM Slave Address

Slave address is 1010000.

**Note:** 10-bit addressing is NOT supported.

### 5.2.2 In-Circuit EEPROM Programming

The EEPROM can be programmed via ATE by pulling RESET_N low (which tri-states the Hub's EEPROM interface and allows an external source to program the EEPROM).

### 5.2.3 EEPROM DATA

**Table 5.1 User-Defined Descriptor Data**

| FIELD | BYTE MSB: LSB | SIZE (BYTES) | DEFAULT CFG SELF (HEX) | DEFAULT CFG BUS (HEX) | DESCRIPTION |
|---|---|---|---|---|---|
| VID | 1:0 | 2 | 0424 | 0424 | Vendor ID (assigned by USB-IF). |
| PID | 3:2 | 2 | 2503 | 2503 | Product ID (assigned by Manufacturer). |
| DID | 5:4 | 2 | 0000 | 0000 | Device ID (assigned by Manufacturer). |
| Config Data Byte 1 | 6 | 1 | 98 | 1C | Configuration data byte #1 for Hub options. |
| Config Data Byte 2 | 7 | 1 | 90 | 90 | Configuration data byte #2 for Hub options. |
| Non Removable Device | 8 | 1 | 00 | 00 | Defines the ports that contain attached devices (this is used only when Hub is part of a compound device). |
| Port Disable Self-Powered | 9 | 1 | 00 | 00 | Selects the ports that will be permanently disabled |
| Port Disable Bus-Powered | A | 1 | 00 | 00 | Selects the ports that will be permanently disabled |
| Max Power Self-Powered | B | 1 | 01 | 01 | Max Current for this configuration (expressed in 2mA units). |
| Max Power Bus-Powered | C | 1 | 64 | 64 | Max Current for this configuration (expressed in 2mA units). |
| Hub Controller Max Current Self-Powered | D | 1 | 01 | 01 | Max Current (expressed in 2mA units). |
| Hub Controller Max Current Bus-Powered | E | 1 | 64 | 64 | Max Current (expressed in 2mA units). |
| Power-On Time | F | 1 | 32 | 32 | Time until power is stable. |

#### 5.2.3.1 EEPROM Offset 1:0(h) - Vendor ID

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 15:8 | VID_MSB | Most Significant Byte of the Vendor ID. |
| 7:0 | VID_LSB | Least Significant Byte of the Vendor ID. |

#### 5.2.3.2 EEPROM Offset 3:2(h) - Product ID

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 15:8 | PID_MSB | Most Significant Byte of the Product ID. |
| 7:0 | PID_LSB | Least Significant Byte of the Product ID. |

#### 5.2.3.3 EEPROM Offset 5:4(h) - Device ID

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 15:8 | DID_MSB | Most Significant Byte of the Device ID. |
| 7:0 | DID_LSB | Least Significant Byte of the Device ID. |

#### 5.2.3.4 EEPROM Offset 6(h) - CONFIG_BYTE_1

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7 | SELF_BUS_PWR | Self or Bus Power: Selects between Self- and Bus-Powered operation.<br><br>0 = Bus-Powered operation. (BUS Default)<br>1 = Self-Powered operation. (SELF Default)<br><br>Note: If Dynamic Power Switching is enabled, this bit is ignored and the SELF_PWR pin is used to determine if the hub is operating from self or bus power. |
| 6 | PORT_IND | Port Indicator Support: Indicates implementation of LED indicators<br><br>0 = No LED indicators.<br>1 = LED indicators. |
| 5 | HS_DISABLE | High Speed Disable: Disables the capability to attach as either a High/Full-speed device, and forces attachment as Full-speed only i.e. (no High-Speed support).<br><br>0 = High-/Full-Speed. (Default)<br>1 = Full-Speed-Only (High-Speed disabled!) |
| 4 | MTT_ENABLE | Multi-TT enable: Enables one transaction translator per port operation.<br><br>0 = single TT for all ports.<br>1 = one TT per port (multiple TT's supported) |

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 3 | EOP_DISABLE | EOP Disable: Disables EOP generation at EOF1 when no downstream directed traffic is in progress.<br><br>0 = EOP generation at EOF1 is enabled.<br>1 = EOP generation at EOF1 is disabled, (normal operation). (Default) |
| 2:1 | CURRENT_SNS | Over Current Sense: Indicates whether current sensing is on a port-by-port basis, or ganged.<br><br>00 = Ganged sensing (all ports together). (Default for self-power)<br>01 = Individual port-by-port.<br>1x = Over current sensing not supported. (may be used with Bus-Powered configurations only!, and is the default for bus-power) |
| 0 | PORT_PWR | Port Power Switching: Indicates whether port power switching is on a port-by-port basis or ganged.<br><br>0 = Ganged switching (all ports together)<br>1 = Individual port-by-port switching. |

#### 5.2.3.5 EEPROM Offset 7(h) - CONFIG_BYTE_2

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7 | DYNAMIC | Dynamic Power Enable: Controls the ability for the Hub to transition to Bus-Powered operation if the local power source is removed (can revert back to Self-Power if local power source is restored).<br><br>0 = No Dynamic auto-switching.<br>1 = Dynamic Auto-switching capable.(Default) |
| 6 | Reserved | Reserved |
| 5:4 | OC_TIMER | OverCurrent Timer: Over Current Timer delay.<br><br>00 = 0.1ms<br>01 = 2ms (Default)<br>10 = 4ms<br>11 = 6ms |
| 3 | COMPOUND | Compound Device: Designates if Hub is part of a compound device.<br><br>0 = No. (Default)<br>1 = Yes, Hub is part of a compound device. |
| 2:0 | Reserved | Reserved. |

### 5.2.3.6 EEPROM Offset 8(h) - Non-Removable Device

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | NR_DEVICE | Non-Removable Device: Indicates which port(s) include non-removable devices. '0' = port is removable, '1' = port is non-removable.<br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved<br>Bit 3= 1; Port 3 non-removable.<br>Bit 2= 1; Port 2 non-removable.<br>Bit 1= 1; Port 1 non removable.<br>Bit 0 is Reserved, always = '0'. |

### 5.2.3.7 EEPROM Offset 9(h) - Port Disable For Self Powered Operation

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PORT_DIS_SP | Port Disable Self-Powered: Disables 1 or more contiguous ports. '0' = port is available, '1' = port is disabled.<br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved.<br>Bit 3= 1; Port 3 is disabled.<br>Bit 2= 1; Port 2 is disabled.<br>Bit 1= 1; Port 1 is disabled.<br>Bit 0 is Reserved, always = '0' |

### 5.2.3.8 EEPROM Offset A(h) - Port Disable For Bus Powered Operation

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PORT_DIS_BP | Port Disable Bus-Powered: Disables 1 or more contiguous ports. '0' = port is available, '1' = port is disabled.<br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved.<br>Bit 3= 1; Port 3 is disabled.<br>Bit 2= 1; Port 2 is disabled.<br>Bit 1= 1; Port 1 is disabled.<br>Bit 0 is Reserved, always = '0' |

### 5.2.3.9 EEPROM Offset B(h) - Max Power For Self Powered Operation

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | MAX_PWR_SP | Max Power Self_Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors.<br><br>Note: The USB 2.0 Specification does not permit this value to exceed 100mA<br><br>A value of 50 (decimal) indicates 100mA. |

### 5.2.3.10 EEPROM Offset C(h) - Max Power For Bus Powered Operation

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | MAX_PWR_BP | Max Power Bus_Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors.<br><br>A value of 50 (decimal) indicates 100mA. |

### 5.2.3.11 EEPROM Offset D(h) - Hub Controller Max Current For Self Powered Operation

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | HC_MAX_C_SP | Hub Controller Max Current Self-Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.<br><br>Note: The USB 2.0 Specification does not permit this value to exceed 100mA<br><br>A value of 50 (decimal) indicates 100mA, which is the default value. |

#### 5.2.3.12 EEPROM Offset E(h) - Hub Controller Max Current For Bus Powered Operation

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | HC_MAX_C_BP | Hub Controller Max Current Bus-Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.<br><br>A value of 50 (decimal) indicates 100mA, which is the default value. |

#### 5.2.3.13 EEPROM Offset F(h) - Power-On Time

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | POWER_ON_TIME | Power On Time: The length of time that is takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is good on that port. |

## 5.3 SMBus Slave Interface

Instead of loading User-Defined Descriptor data from an external EEPROM, the SMSC Hub can be configured to receive a code load from an external processor via an SMBus interface. The SMBus interface shares the same pins as the EEPROM interface, if CFG_SEL1 & CFG_SEL0 activates the SMBus interface, external EEPROM support is no longer available (and the user-defined descriptor data must be downloaded via the SMBus). Due to system issues, the SMSC Hub waits indefinitely for the SMBus code load to complete and only “appears” as a newly connected device on USB after the code load is complete.

The Hub’s SMBus implementation is a subset of the SMBus interface to the host. The device is a *slave-only* SMBus device. The implementation in the device is a subset of SMBus since it only supports two protocols.

The Write Byte and Read Byte protocols are the only valid SMBus protocols for the Hub. The Hub responds to other protocols as described in Section 5.3.2, "Invalid Protocol Response Behavior," on page 24. Reference the System Management Bus Specification, Rev 1.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in Section 5.3.9, "Internal SMBus Memory Register Set," on page 25.

### 5.3.1 Bus Protocols

Typical Write Byte and Read Byte protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the Hub driving data on the SMBDATA line; otherwise, host data is on the SDA/SMBDATA line.

The slave address is the unique SMBus Interface Address for the Hub that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

**Note:** Data bytes are transferred MSB first (msb first).

#### 5.3.1.1 Byte Protocols

When using the Hub SMBus Interface for byte transfers, a write will always consist of the SMBus Interface Slave Address byte, followed by the Internal Address Register byte, then the data byte.

The normal read protocol consists of a write to the HUB with the SMBus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the SMBus Interface Address byte, followed by the data byte read from the Hub. This can be accomplished by using the Read Byte protocol.

**Note:** For the following SMBus tables:

Denotes Master-to-Slave  Denotes Slave-to-Master

Write Byte

The Write Byte protocol is used to write data to the registers. The data will only be written if the protocol shown in Table 5.2 is performed correctly. Only one byte is transferred at a time for a Write Byte protocol.

**Table 5.2 SMBus Write Byte Protocol**

| Field: | Start | Slave Addr | Wr | Ack | Reg. Addr | Ack | Reg. Data | Ack | Stop |
|---|---|---|---|---|---|---|---|---|---|
| Bits: | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |

Read Byte

The Read Byte protocol is used to read data from the registers. The data will only be read if the protocol shown in Table 5.3 is performed correctly. Only one byte is transferred at a time for a Read Byte protocol.

**Table 5.3 SMBus Read Byte Protocol**

| Field: | Start | Slave Addr | Wr | Ack | Reg. Addr | Ack | Start | Slave Addr | Rd | Ack | Reg. Data | Nack | Stop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bits: | 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 1 |

### 5.3.2 Invalid Protocol Response Behavior

Registers that are accessed with an invalid protocol are not updated. A register is only updated following a valid protocol. The only valid protocols are Write Byte and Read Byte, which are described above.

The Hub only responds to the hardware selected Slave Address.

Attempting to communicate with the Hub over SMBus with an invalid slave address or invalid protocol results in no response, and the SMBus Slave Interface returns to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. See Section 5.3.3 for the response to undefined registers.

### 5.3.3 General Call Address Response

The Hub does not respond to a general call address of 0000_000b.

### 5.3.4 Slave Device Time-Out

According to the SMBus Specification, V1.0 devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25ms ($T_{TIMEOUT, MIN}$). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35ms ($T_{TIMEOUT, MAX}$).

**Note:** Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition.

### 5.3.5 Stretching the SCLK Signal

The Hub supports stretching of the SCLK by other devices on the SMBus. The Hub does not stretch the SCLK.

### 5.3.6 SMBus Timing

The SMBus Slave Interface complies with the SMBus AC Timing Specification. See the SMBus timing in the “Timing Diagram” section.

### 5.3.7 Bus Reset Sequence

The SMBus Slave Interface resets and returns to the idle state upon a START field followed immediately by a STOP field.

### 5.3.8 SMBus Alert Response Address

The SMBALERT# signal is not supported by the Hub.

### 5.3.9 Internal SMBus Memory Register Set

The following table provides the SMBus slave interface register map values.

**Table 5.4 SMBus Slave Interface Register Map**

| REG ADDR | R/W | REGISTER NAME | ABBR | BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | R/W | Status/Command | STCD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 01h | R/W | VID LSB | VIDL | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 02h | R/W | VID MSB | VIDM | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 03h | R/W | PID LSB | PIDL | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 04h | R/W | PID MSB | PIDM | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 05h | R/W | DID LSB | DIDL | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 06h | R/W | DID MSB | DIDM | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 07h | R/W | Config Data Byte 1 | CFG1 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 08h | R/W | Config Data Byte 2 | CFG2 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 09h | R/W | Non-Removable Devices | NRD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0Ah | R/W | Port Disable (Self) | PDS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0Bh | R/W | Port Disable (Bus) | PDB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Table 5.4 SMBus Slave Interface Register Map (continued)**

| REG ADDR | R/W | REGISTER NAME | ABBR | BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Ch | R/W | Max Power (Self) | MAXPS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0Dh | R/W | Max Power (Bus) | MAXPB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0Eh | R/W | Hub Controller Max Current (Self) | HCMCS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0Fh | R/W | Hub Controller Max Current (bus) | HCMCB | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 10h | R/W | Power-on Time | PWRT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

#### 5.3.9.1 Register 00h: Status/Command (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:3 | Reserved | Reserved. {Note: Software must never write a '1' to these bits} |
| 2 | RESET | Reset the SMBus Interface and internal memory back to RESET_N assertion default settings. {Note: During this reset, this bit is automatically cleared to its default value of 0.}<br><br>0 = Normal Run/Idle State.<br>1 = Force a reset. |
| 1 | WRITE_PROT | Write Protect: The external SMBus host sets this bit after the Hub's internal memory is loaded with configuration data. {Note: The External SMBus Host is responsible for verification of downloaded data.}<br><br>0 = The internal memory (address range 01-10h) is not write protected.<br>1 = The internal memory (address range 01-10h) is "write-protected" to prevent unintentional data corruption.}<br><br>{Note: This bit is write once and is only cleared by assertion of the external RESET_N pin.} |
| 0 | USB_ATTACH | USB Attach & power-down the SMBus Interface.<br><br>0 = Default; SMBus slave interface is active.<br>1 = Hub will signal a USB attach event to an upstream device, Note: SMBus Slave interface will completely power down after the ACK has completed.<br><br>{Note: This bit is write once and is only cleared by assertion of the external RESET_N pin.} |

#### 5.3.9.2 Register 01h: Vendor ID (LSB) (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | VID_LSB | Least Significant Byte of the Vendor ID. |

#### 5.3.9.3 Register 02h: Vendor ID (MSB) (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | VID_MSB | Most Significant Byte of the Vendor ID. |

#### 5.3.9.4 Register 03h: Product ID (LSB) (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PID_LSB | Least Significant Byte of the Product ID. |

#### 5.3.9.5 Register 04h: Product ID (MSB) (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PID_MSB | Most Significant Byte of the Product ID. |

#### 5.3.9.6 Register 05h: Device ID (LSB) (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | DID_LSB | Least Significant Byte of the Device ID. |

#### 5.3.9.7 Register 06h: Device ID (MSB) (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | DID_MSB | Most Significant Byte of the Device ID. |

#### 5.3.9.8 Register 07h: CONFIG_BYTE_1 (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7 | SELF_BUS_PWR | Self or Bus Power: Selects between Self- and Bus-Powered operation.<br><br>0 = Bus-Powered operation.<br>1 = Self-Powered operation.<br><br>Note: If Dynamic Power Switching is enabled, this bit is ignored and the SELF_PWR pin is used to determine if the hub is operating from self or bus power. |
| 6 | PORT_IND | Port Indicator Support: Indicates implementation of LED indicators<br><br>0 = No LED indicators.<br>1 = LED indicators. |

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 5 | HS_DISABLE | High Speed Disable: Disables the capability to attach as either a High/Full-speed device, and forces attachment as Full-speed only i.e. (no High-Speed support).<br><br>0 = High-/Full-Speed.<br>1 = Full-Speed-Only (High-Speed disabled!) |
| 4 | MTT_ENABLE | Multi-TT enable: Enables one transaction translator per port operation.<br><br>0 = single TT for all ports.<br>1 = one TT per port (multiple TT's supported) |
| 3 | EOP_DISABLE | EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode.<br><br>0 = EOP generation is normal.<br>1 = EOP generation is disabled. |
| 2:1 | CURRENT_SNS | Over Current Sense: Indicates whether current sensing is on a port-by-port basis, or ganged.<br><br>00 = Ganged sensing (all ports together).<br>01 = Individual port-by-port.<br>1x = Over current sensing not supported. (must only be used with Bus-Powered configurations!) |
| 0 | PORT_PWR | Port Power Switching: Indicates whether port power switching is on a port-by-port basis or ganged.<br><br>0 = Ganged switching (all ports together)<br>1 = Individual port-by-port switching. |

#### 5.3.9.9 Register 08h: Configuration Data Byte 2 (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7 | DYNAMIC | Dynamic Power Enable: Controls the ability for the Hub to transition to Bus-Powered operation if the local power source is removed (can revert back to Self-Power if local power source is restored).<br><br>0 = No Dynamic auto-switching.<br>1 = Dynamic Auto-switching capable. |
| 6 | Reserved | Reserved |
| 5:4 | OC_TIMER | OverCurrent Timer: Over Current Timer delay.<br><br>00 = 0.1ms<br>01 = 2ms<br>10 = 4ms<br>11 = 6ms |
| 3 | COMPOUND | Compound Device: Designates if Hub is part of a compound device.<br><br>0 = No.<br>1 = Yes, Hub is part of a compound device. |
| 2:0 | Reserved | Reserved |

### 5.3.9.10 Register 09h: Non-Removable Device (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | NR_DEVICE | Non-Removable Device: Indicates which port(s) include non-removable devices. '0' = port is removable, '1' = port is non-removable.<br><br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= 1; Reserved .<br>Bit 3= 1; Port 3 non-removable.<br>Bit 2= 1; Port 2 non-removable.<br>Bit 1= 1; Port 1 non removable.<br>Bit 0 is Reserved, always = '0'. |

### 5.3.9.11 Register 0Ah: Port Disable For Self Powered Operation (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PORT_DIS_SP | Port Disable Self-Powered: Disables 1 or more contiguous ports. '0' = port is available, '1' = port is disabled.<br><br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved1<br>Bit 3= 1; Port 3 is disabled.<br>Bit 2= 1; Port 2 is disabled.<br>Bit 1= 1; Port 1 is disabled.<br>Bit 0 is Reserved, always = '0' |

### 5.3.9.12 Register 0Bh: Port Disable For Bus Powered Operation (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PORT_DIS_BP | Port Disable Bus-Powered: Disables 1 or more contiguous ports. '0' = port is available, '1' = port is disabled.<br><br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved1<br>Bit 3= 1; Port 3 is disabled.<br>Bit 2= 1; Port 2 is disabled.<br>Bit 1= 1; Port 1 is disabled.<br>Bit 0 is Reserved, always = '0' |

### 5.3.9.13 Register 0Ch: Max Power For Self Powered Operation (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|

| | | |
|---|---|---|
| 7:0 | MAX_PWR_SP | Max Power Self_Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors.<br><br>Note: The USB 2.0 Specification does not permit this value to exceed 100mA<br><br>A value of 50 (decimal) indicates 100mA. |

#### 5.3.9.14 Register 0Dh: Max Power For Bus Powered Operation (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | MAX_PWR_BP | Max Power Bus_Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors.<br><br>A value of 50 (decimal) indicates 100mA. |

#### 5.3.9.15 Register 0Eh: Hub Controller Max Current For Self Powered Operation (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | HC_MAX_C_SP | Hub Controller Max Current Self-Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.<br><br>Note: The USB 2.0 Specification does not permit this value to exceed 100mA<br><br>A value of 50 (decimal) indicates 100mA, which is the default value. |

#### 5.3.9.16 Register 0Fh: Hub Controller Max Current For Bus Powered Operation (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | HC_MAX_C_BP | Hub Controller Max Current Bus-Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.<br><br>A value of 50 (decimal) would indicate 100mA, which is the default value. |

#### 5.3.9.17 Register 10h: Power-On Time (Reset = 0x00)

| BIT NUMBER | BIT NAME | DESCRIPTION |
|---|---|---|
| 7:0 | POWER_ON_TIME | Power On Time: The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is good on that port. |

#### 5.3.9.18 Undefined Registers

The registers shown in Table 5.4 are the defined registers in the Hub. Reads to undefined registers return 00h. Writes to undefined registers have no effect and do not return an error.

#### 5.3.9.19 Reserved Registers

Unless otherwise instructed, only a ‘0’ may be written to all reserved registers or bits.

## 5.4 Default Configuration Option:

The SMSC Hub can be configured via its internal default configuration. (please see Chapter 3, Pin Configuration 3-Port Hub for specific details on how to enable default configuration.

Please refer to Table 5.1 on page 18 for the internal default values that are loaded when this option is selected.

## 5.5 Default Strapping Options:

The SMSC Hub can be configured via a combination of internal default values and pin strap options. Please see Table 4.1, "3-Port Hub Pin Descriptions" for specific details on how to enable the default/pin-strap configuration option.

The strapping option pins only cover a limited sub-set of the configuration options. The internal default values will be used for the bits & registers that are not controlled by a strapping option pin. Please refer to Table 5.1 on page 18 for the internal default values that are loaded when this option is selected.

The Green LED pins are sampled after RESET_N negation, and the logic values are used to configure the hub if the internal default configuration mode is selected. The implementation shown below (see Figure 5.1) shows a recommended passive scheme. When a pin is configured with a “Strap High” configuration, the LED functions with active low signalling, and the PAD will “sink” the current from the external supply. When a pin is configured with a “Strap Low” configuration, the LED functions with active high signalling, and the PAD will “source” the current to the external LED.

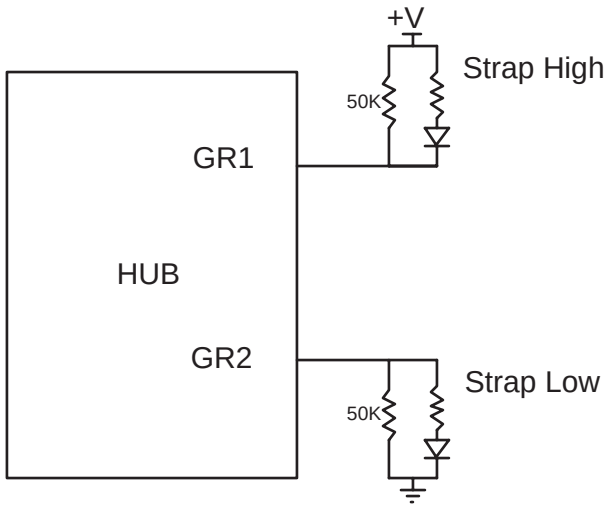



**Figure 5.1 LED Strapping Option**

## 5.6 Reset

There are two different resets that the Hub experiences. One is a hardware reset (via the RESET_N pin) and the second is a USB Bus Reset.

### 5.6.1 External Hardware RESET_N

A valid hardware reset is defined as, assertion of RESET_N for a minimum of 1us after all power supplies are within operating range. While reset is asserted, the Hub (and its associated external circuitry) consumes less than 500µA of current from the upstream USB power source (300µA for the Hub and 200µA for the external circuitry).

Assertion of RESET_N (external pin) causes the following:

1. All downstream ports are disabled, and PRTPWR power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00(h)).
5. The external crystal oscillator is halted.
6. The PLL is halted.
7. LED indicators are disabled.

The Hub is “operational” 500µs after RESET_N is negated.

Once operational, the Hub immediately reads OEM-specific data from the external EEPROM (if the SMBus option is not disabled).

### 5.6.1.1 RESET_N for Strapping Option Configuration

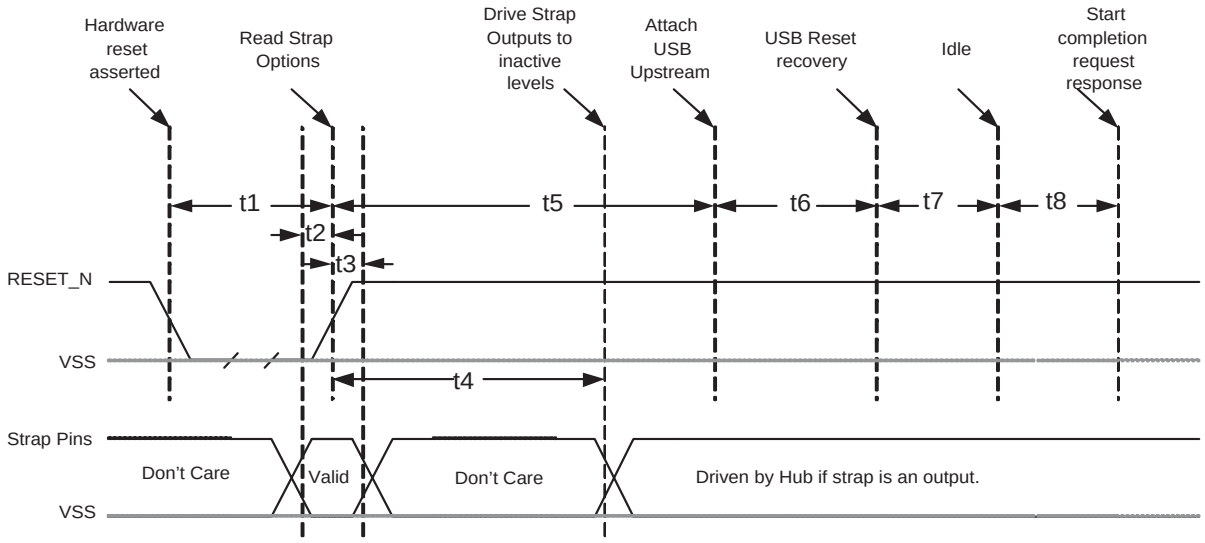



**Figure 5.2 Reset_N Timing for Default/Strap Option Mode**

**Table 5.5 Reset_N Timing for Default/Strap Option Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| t1 | RESET_N Asserted. | 1 | | | µsec |
| t2 | Strap Setup Time | 16.7 | | | nsec |
| t3 | Strap Hold Time. | 16.7 | | 1400 | nsec |
| t4 | hub outputs driven to inactive logic states | | 2.0 | 1.5 | µsec |
| t5 | USB Attach (See Note). | | | 100 | msec |
| t6 | Host acknowledges attach and signals USB Reset. | 100 | | | msec |
| t7 | USB Idle. | | undefined | | msec |
| t8 | Completion time for requests (with or without data stage). | | | 5 | msec |

**Notes:**

- When in Bus-Powered mode, the Hub and its associated circuitry must not consume more than 100mA from the upstream USB power source during t1+t5.
- All Power Supplies must have reached the operating levels mandated in Section Chapter 7, "DC Parameters", prior to (or coincident with) the assertion of RESET_N.

### 5.6.1.2 RESET_N for EEPROM Configuration

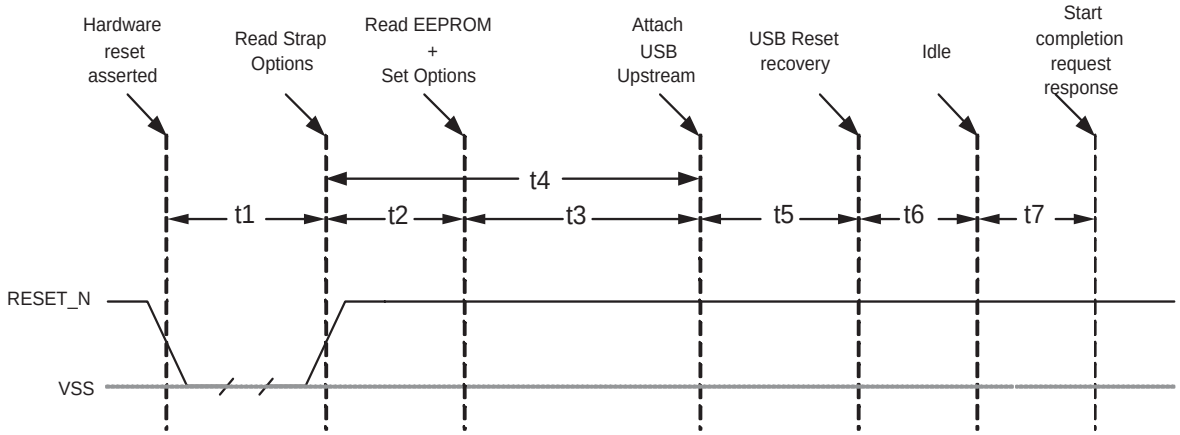



**Figure 5.3 Reset_N Timing for EEPROM Mode**

**Table 5.6 Reset_N Timing for EEPROM Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| t1 | RESET_N Asserted. | 1 | | | µsec |
| t2 | Hub Recovery/Stabilization. | | | 500 | µsec |
| t3 | EEPROM Read / Hub Config. | | 2.0 | 99.5 | msec |
| t4 | USB Attach (See Note). | | | 100 | msec |
| t5 | Host acknowledges attach and signals USB Reset. | 100 | | | msec |
| t6 | USB Idle. | | undefined | | msec |
| t7 | Completion time for requests (with or without data stage). | | | 5 | msec |

**Notes:**

- When in Bus-Powered mode, the Hub and its associated circuitry must not consume more than 100mA from the upstream USB power source during t4+t5+t6+t7.
- All Power Supplies must have reached the operating levels mandated in Section Chapter 7, "DC Parameters", prior to (or coincident with) the assertion of RESET_N.

### 5.6.1.3 RESET_N for SMBus Slave Configuration

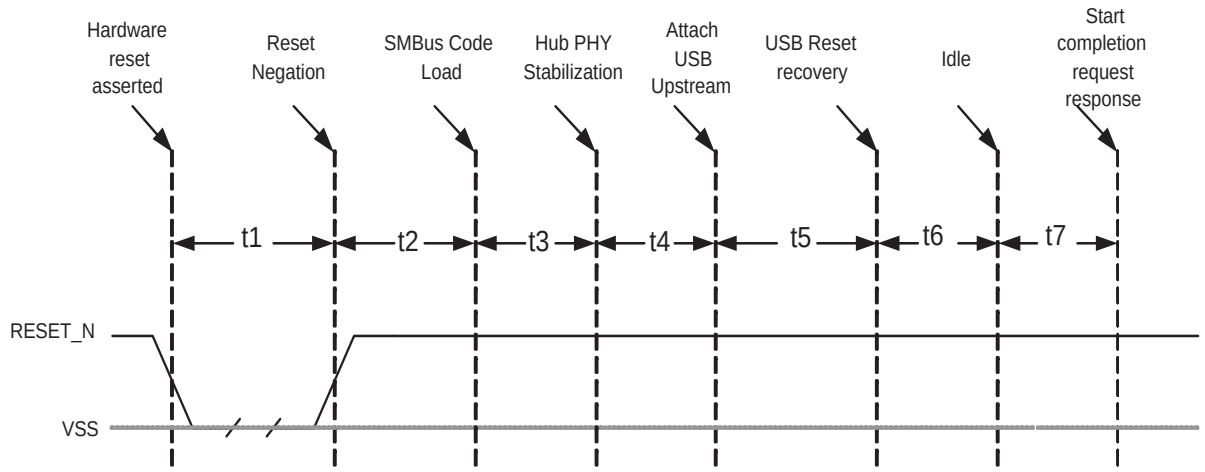



**Figure 5.4 Reset_N Timing for SMBus Mode**

**Table 5.7 Reset_N Timing for SMBus Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| t1 | RESET_N Asserted. | 1 | | | µsec |
| t2 | Hub Recovery/Stabilization. | | | 500 | µsec |
| t3 | SMBus Code Load (See Note). | | 10 | 99.5 | msec |
| t4 | Hub Configuration and USB Attach. | | | 100 | msec |
| t5 | Host acknowledges attach and signals USB Reset. | 100 | | | msec |
| t6 | USB Idle. | | Undefined | | msec |
| t7 | Completion time for requests (with or without data stage). | | | 5 | msec |

**Notes:**

- For Bus-Powered configurations, the 99.5ms (MAX) is required, and the Hub and its associated circuitry must not consume more than 100mA from the upstream USB power source during t2+t3+t4+t5+t6+t7. For Self-Powered configurations, t3 MAX is not applicable and the time to load the configuration is determined by the external SMBus host.
- All Power Supplies must have reached the operating levels mandated in Section Chapter 7, "DC Parameters", prior to (or coincident with) the assertion of RESET_N.

## 5.6.2 USB Bus Reset

In response to the upstream port signaling a reset to the Hub, the Hub does the following:

**Note:** The Hub does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0.
2. Sets configuration to: Unconfigured.
3. Negates PRTPWR[4:1] to all downstream ports.
4. Clears all TT buffers.

5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence.

The Host then configures the Hub and the Hub's downstream port devices in accordance with the USB Specification.

# Chapter 6 XNOR Test

XNOR continuity tests all signal pins on the Hub (every pin except for NC, XTAL1/CLKIN, XTAL2, ATEST/REG_EN, RBIAS, TEST1, Power, and Ground). This functionality is enabled by driving TEST1 and CFG_SEL[1] high, driving SCLK low and transition RESET_N from low to high. The output from the XNOR chain is driven to GR2 . For each pin tested for continuity GR2 should toggle.

# Chapter 7 DC Parameters

## 7.1 Maximum Guaranteed Ratings

| PARAMETER | SYMBOL | MIN | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| Storage Temperature | $T_A$ | -55 | 150 | °C | |
| Lead Temperature | | | 325 | °C | Soldering < 10 seconds |
| 1.8V supply voltage | $V_{DDA18PLL}$ $V_{DD18}$ | -0.5 | 2.5 | V | |
| 3.3V supply voltage | $V_{DDA33}$ $V_{DDA33PLL}$ $V_{DD33CR}$ | -0.5 | 4.0 | V | |
| Voltage on any I/O pin | | -0.5 | (3.3V supply voltage + 2) ≤ 6 | V | |
| Voltage on XTAL1 | | -0.5 | 4.0 | V | |
| Voltage on XTAL2 | | -0.5 | $V_{DD18}$ + 0.3V | V | |

**Note:** Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

## 7.2 Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| Operating Temperature | $T_A$ | 0 | 70 | °C | |
| 1.8V supply voltage | $V_{DDA18PLL}$ $V_{DD18}$ | 1.71 | 1.98 | V | |
| 3.3V supply voltage | $V_{DDA33}$ $V_{DDA33PLL}$ $V_{DD33CR}$ | 3.0 | 3.6 | V | |
| Voltage on any I/O pin | | -0.3 | 5.5 | V | If any 3.3V supply voltage drops below 3.0V, then the MAX becomes: (3.3V supply voltage + 0.5) |
| Voltage on XTAL1 | | -0.3 | $V_{DDA33}$ | V | |
| Voltage on XTAL2 | | -0.3 | $V_{DD18}$ | V | |

**Table 7.1 DC Electrical Characteristics**

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| I, IS Type Input Buffer | | | | | | |
| Low Input Level | $V_{ILI}$ | | | 0.8 | V | TTL Levels |
| High Input Level | $V_{IHI}$ | 2.0 | | | V | |
| Input Leakage | $I_{IL}$ | -10 | | +10 | uA | $V_{IN}$ = 0 to $V_{DD33}$CR |
| Hysteresis (‘IS’ Only) | $V_{HYSI}$ | 250 | 300 | 350 | mV | |
| Input Buffer with Pull-Up (IPU) | | | | | | |
| Low Input Level | $V_{ILI}$ | | | 0.8 | V | TTL Levels |
| High Input Level | $V_{IHI}$ | 2.0 | | | V | |
| Low Input Leakage | $I_{ILL}$ | +26 | | +72 | uA | $V_{IN}$ = 0 |
| High Input Leakage | $I_{IHL}$ | -10 | | +10 | uA | $V_{IN}$ = $V_{DD33}$CR |
| Input Buffer with Pull-Down IPD | | | | | | |
| Low Input Level | $V_{ILI}$ | | | 0.8 | V | TTL Levels |
| High Input Level | $V_{IHI}$ | 2.0 | | | V | |
| Low Input Leakage | $I_{ILL}$ | +10 | | -10 | uA | $V_{IN}$ = 0 |
| High Input Leakage | $I_{IHL}$ | -22 | | -82 | uA | $V_{IN}$ = $V_{DD33}$CR |

**Table 7.1 DC Electrical Characteristics (continued)**

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| ICLK Input Buffer | | | | | | |
| Low Input Level | $V_{ILCK}$ | | | 0.8 | V | TTL Levels |
| High Input Level | $V_{IHCK}$ | 2.0 | | | V | |
| Input Leakage | $I_{IL}$ | -10 | | +10 | uA | $V_{IN}$ = 0 to $V_{DD33}CR$ |
| Hysteresis | $V_{HYSC}$ | 50 | | 100 | mV | |
| O12 and I/O12 Type Buffer | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12mA @ $V_{DD33}CR$ = 3.3V |
| High Output Level | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -4mA @ $V_{DD33}CR$ = 3.3V |
| Output Leakage | $I_{OL}$ | | | +10 | uA | $V_{IN}$ = 0 to $V_{DD33}CR$ (Note 1) |
| I/OSD12 Type Buffer | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA @ $V_{DD33}CR$ = 3.3V |
| Output Leakage | $I_{OL}$ | -10 | | +10 | µA | $V_{IN}$ = 0 to $V_{DD33}CR$ (Note 1) |
| Hysteresis | $V_{HYSI}$ | 250 | 300 | 350 | mV | |
| IO-U (Note 2) | | | | | | |
| I-R (Note 3) | | | | | | |
| Supply Current Unconfigured | | | | | | |
| High-Speed Host | $I_{CCINIT}$ | | 100 | | mA | |
| Full-Speed Host | $I_{CCINIT}$ | | 95 | | mA | |
| Supply Current Configured (High-Speed Host) | | | | | | Total from all supplies |
| 2 Ports @ FS/LS | $I_{HCC2}$ | | 190 | | mA | |
| 2 Ports @ HS | $I_{HCH2}$ | | 235 | | mA | |
| 1 Port HS, 1 Port FS/LS | $I_{HCH1C1}$ | | 215 | | mA | |
| 3 Ports @ HS | $I_{HCH3}$ | | 265 | | mA | |

**Table 7.1 DC Electrical Characteristics (continued)**

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| Supply Current Configured (Full-Speed Host)<br><br>1 Port<br>2 Ports<br>3 Ports | <br><br>$I_{FCC1}$<br>$I_{FCC2}$<br>$I_{FCC3}$ | | <br><br>150<br>155<br>160 | | <br><br>mA<br>mA<br>mA | Total from all supplies |
| Supply Current Suspend | $I_{CSBY}$ | | 265 | | uA | Total from all supplies. |
| Supply Current Reset | $I_{RST}$ | | 150 | | uA | Total from all supplies. |

**Notes:**

1. Output leakage is measured with the current pins in high impedance.
2. See USB 2.0 Specification for USB DC electrical characteristics.
3. RBIAS is a 3.3V tolerant analog pin.

**CAPACITANCE $T_A$ = 25°C; fc = 1MHz; $V_{DD33CR}$ = 3.3*V***

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Clock Input Capacitance | $C_{IN}$ | | | 12 | pF | All pins except USB pins (and pins under test tied to AC ground) |
| Input Capacitance | $C_{IN}$ | | | 8 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 12 | pF | |

**Power Sequencing**

There are no power supply sequence restrictions for the Hub. The order in which power supplies power-up and power-down is implementation dependent.

# Chapter 8 AC Specifications

## 8.1 Oscillator/Clock

Crystal: Parallel Resonant, Fundamental Mode, 24 MHz ±100ppm.

External Clock: 50% Duty cycle ± 10%, 24 MHz ± 100ppm, Jitter < 100ps rms.

### 8.1.1 SMBus Interface:

The SMSC Hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the SMBus 1.0 Specification for Slave-Only devices (except as noted in Section 5.3).

### 8.1.2 I2C EEPROM:

Frequency is fixed at 59KHz ± 20%.

### 8.1.3 USB 2.0

The Hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 Specification. Please refer to the USB Specification for more information.

# Chapter 9 Package Outline

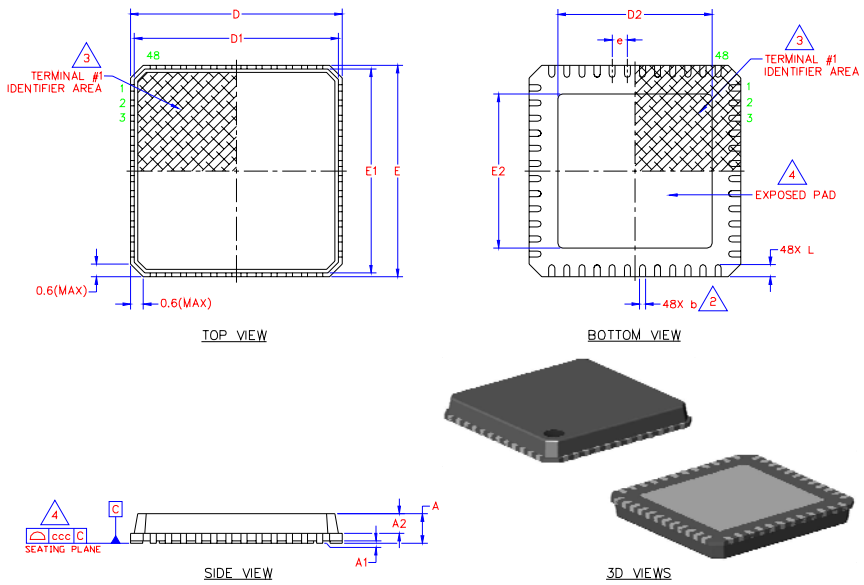



**Figure 9.1 48 Pin QFN Package Outline (7x7 mm body - 0.5 mm pitch)**

**Table 9.1 48 Pin QFN Package Parameters**

| | MIN | NOMINAL | MAX | REMARKS |
|---|---|---|---|---|
| A | 0.70 | ~ | 1.00 | Overall Package Height |
| A1 | 0 | 0.02 | 0.05 | Standoff |
| A2 | ~ | ~ | 0.80 | Mold Thickness |
| D | 6.85 | 7.00 | 7.15 | X Overall Size |
| D1 | 6.55 | ~ | 6.95 | X Mold Cap Size |
| D2 | 2.25 | ~ | 5.60 | X exposed Pad Size |
| E | 6.85 | 7.00 | 7.15 | Y Overall Size |
| E1 | 6.55 | ~ | 6.95 | Y Mold Cap Size |
| E2 | 2.25 | ~ | 5.60 | Y exposed Pad Size |
| L | 0.30 | ~ | 0.50 | Terminal Length |
| e | 0.50 Basic | | | Terminal Pitch |
| b | 0.18 | ~ | 0.30 | Terminal Width |
| ccc | ~ | ~ | 0.08 | Coplanarity |

**Notes:**

1. Controlling Unit: millimeter.
2. Dimension b applies to plated terminals and is measured between 0.15mm and 0.30mm from the terminal tip. Tolerance on the true position of the terminal is ± 0.05 mm at maximum material conditions (MMC).
3. Details of terminal #1 identifier are optional but must be located within the zone indicated.
4. Coplanarity zone applies to exposed pad and terminals.