User's Guide
SNVA343A–April 2008–Revised April 2013

AN-1840 USB I²C Interface Board Reference Manual

This application note discusses the features, requirements, and usages of the USB I²C Interface board.

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1 Introduction

The USB I²C Interface board interacts with your application hardware via an USB port in a PC. The microcontroller with flash memory enables to control your application hardware and develop specific application functions via software. (*Texas Instruments does not provide interaction software, which networks both application board and I²C board*).

2 USB I²C Interface Board Key Features

- TI's COP8CBE9 microcontroller in a TSSOP package
- TI's USBN9604 IC in a 28-pin PLGA package
- USB 2.0 compatible
- Bus powered
- 24 MHz clock from crystal
- 8–pin analog inputs for A/D converter

3 Block Diagram

Figure 1 shows basic connections between the PC, USB I²C Interface Module, and application board.

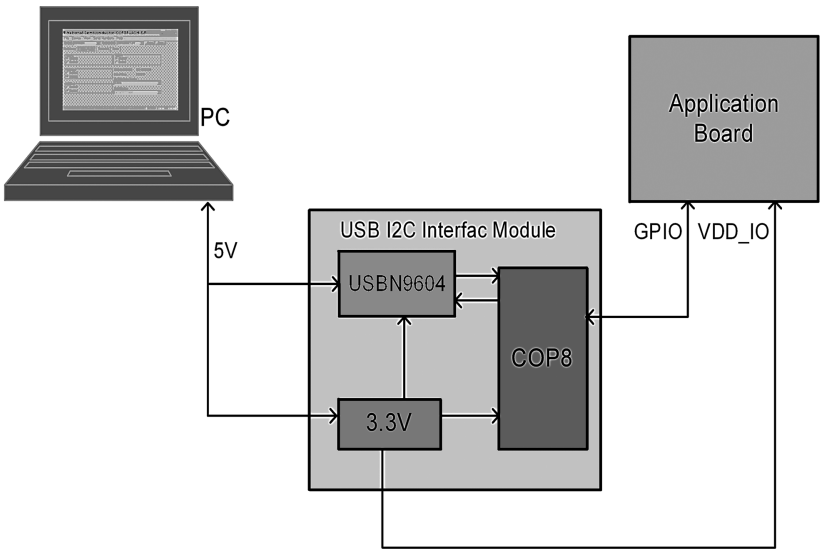

Figure 1. Block Diagram

4 System Requirements

The following requirements are vital in order to use the USB I²C Interface Module:

System Requirements

- Windows Operating System (Win98/ME/2000/XP)
- 32 MB RAM minimum)
- 2 MB available for disk space

4.1 Hardware Requirements

- 5-Pin Mini-B USB 2.0 cable (sold separately)

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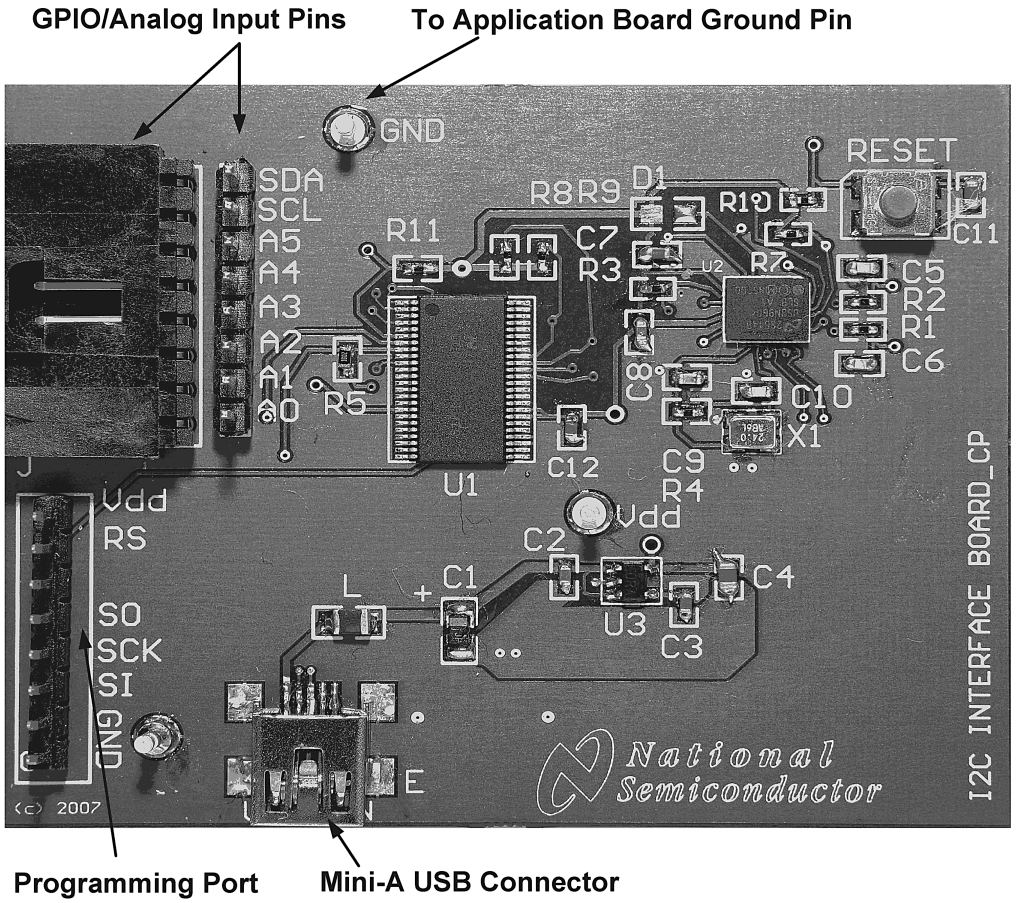

Figure 2. USB I²C Interface Module

5 Serial Interface and Programming Connectors

5.1 Serial Interface "J"

The table below shows the pin configuration for the COP8 controller for all interface modes.

Pin Name	I2C Board Pin/COP8 Pin	Comment
SDA (Data out)	SDA / 40	R = 2 kΩ (1)
SCL (Clock)	SCL / 39	R = 2 kΩ (1)
Analog Ch. 6/GPIO	A5 / 38	(2)
Analog Ch. 5/GPIO	A4 / 37	(2)
Analog Ch. 4/GPIO	A3 / 36	(2)
Analog Ch. 3/GPIO	A2 / 35	(2)
Analog Ch. 2/GPIO	A1 / 34	(2)
Analog Ch. 1/GPIO	A0 / 33	(2)

(1) Must have a pull-up resistor on application hardware for SCL and SDA lines.

(2) Do not use any of A5 - A0 pins as a ground connection. Connect both application and I²C grounds together to make a good ground connection between the two boards. (Refer to I²C picture for GND pin.)

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5.2 Electrical Characteristics of I²C

The USB I²C board requires 5V from a computer to function correctly. The maximum current that the I²C board will draw from the computer is 500 mA. This I²C board will function within the temperature range of $0°C \leq T_A \leq 70°C$.

For further information about the devices on the I²C board, refer to the following links:

COP8CBE9/CCE9 8-Bit CMOS Flash Microcontroller with 8k Memory, Virtual EEPROM, 10- Bit A/D and Brownout Reset (SNOS978)

150-mA Low-Noise, Low-Dropout Regulator With Shutdown (SLVS522)

6 I²C Compatible Interface

6.1 I²C Signals

In I²C-compatible mode, the SCL pin is used for the I²C clock and the SDA pin is used for the I²C data. Each of these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistors are determined by the capacitance of the bus (typ. ~2k). See I²C specification from Phillips for further details. Signal timing specifications are according to the I²C bus specification. Maximum frequency is 400 KHz.

6.2 I²C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

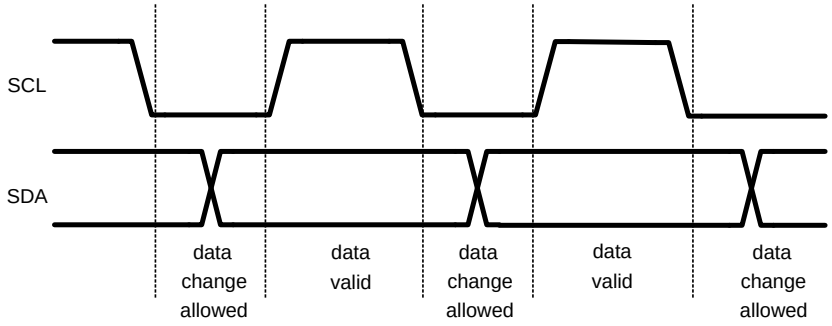

Figure 3. I²C Signals: Data Validity

6.3 I²C Start and Stop Conditions

START and STOP bits signify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

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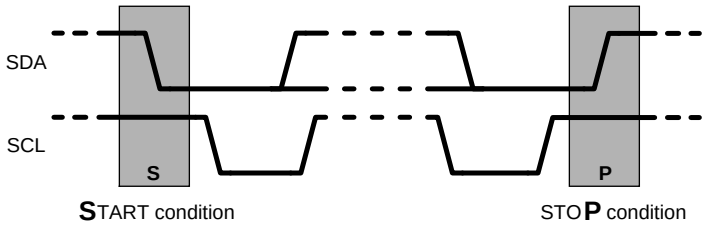


Figure 4. START and STOP Conditions

6.4 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. All clock pulses are generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

Figure 5. I²C Chip Address

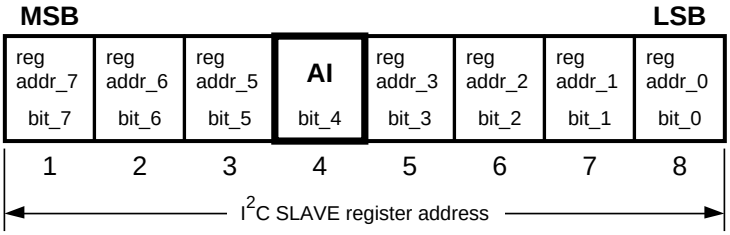
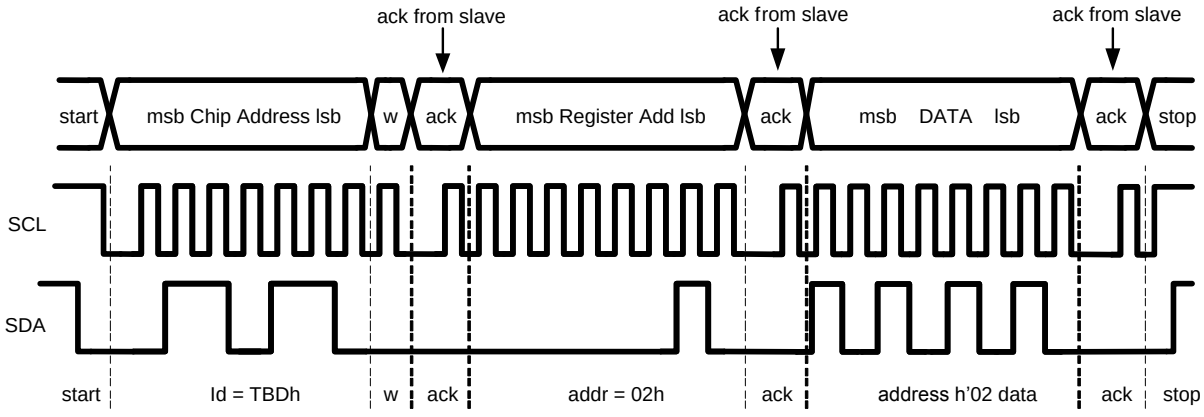


Figure 6. I²C Write Cycle



w = write (SDA = '0')
r = read (SDA = '1')
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = chip address

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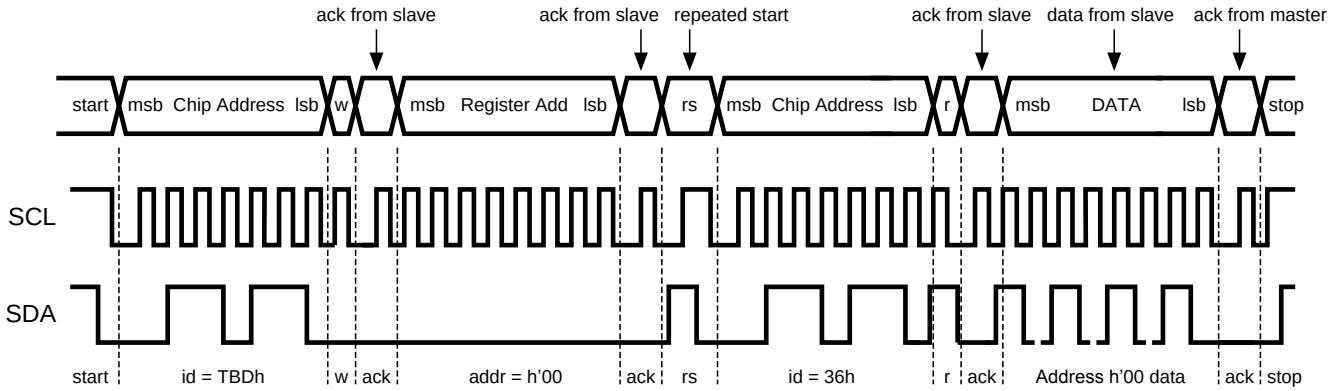
When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

Figure 7. I²C Read Cycle



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