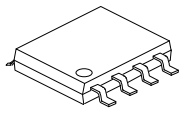
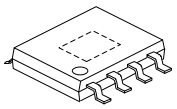
UR5595

CMOS IC

DDR TERMINATION REGULATOR



SOP-8



HSOP-8

Lead-free: UR5595L
Halogen-free: UR5595G

■ DESCRIPTION

The UTC **UR5595** is a linear bus termination regulator designed to meet JEDEC SSTL-2 and SSTL-3 (Stub Series Terminated Logic) specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to the load transients, and can deliver 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination.

With an independent V_{SENSE} pin, the **UR5595** can provide superior load regulation. The UR5595 provides a V_{REF} output as the reference for the application of the chipset and DIMMs.

The output, V_{TT}, is capable of sinking and sourcing current while regulating the output voltage equal to $V_{DDQ}/2$. The output stage has been designed to maintain excellent load regulation and with fast response time to minimum the transition preventing shoot-through. The UTC **UR5595** also incorporates two distinct power rails that separates the analog circuitry (AVIN) from the power output stage (PVIN). This power rail split can be utilized to reduce the internal power dissipation. And this also permits UTC **UR5595** to provide a termination solution for DDRII SDRAM.

■ FEATURES

* Power regulating with driving and sinking capability
* Low output voltage offset
* No external resistors required
* Low external component count
* Linear topology
* Low cost and easy to use
* Thermal shutdown protection

■ ORDERING INFORMATION

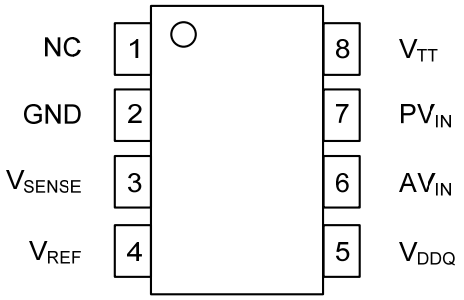
Ordering Number			Package	Packing
Normal	Lead Free	Halogen Free		
UR5595-S08-R	UR5595L-S08-R	UR5595G-S08-R	SOP-8	Tape Reel
UR5595-SH2-R	UR5595L-SH2-R	UR5595G-SH2-R	HSOP-8	Tape Reel

UR5595L-S08-R
(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) R: Tape Reel
(2) S08: SOP-8, SH2: HSOP-8
(3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn

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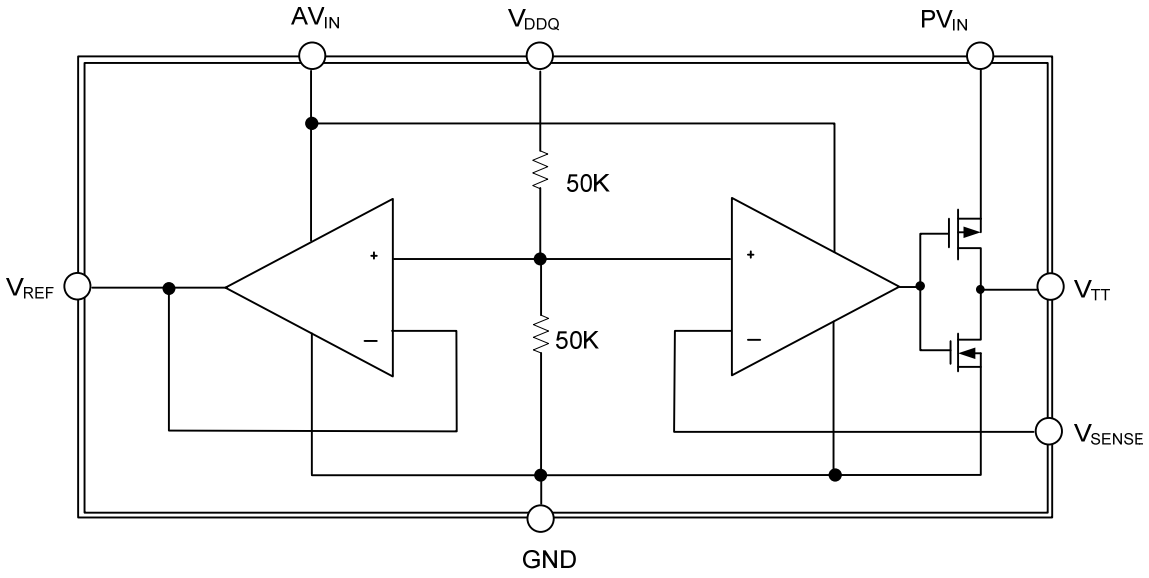
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	DESCRIPTION
1	NC	No internal connection. Can be used for vias.
2	GND	Ground.
3	V_{SENSE}	Feedback pin for regulating V_{OUT}.
4	V_{REF}	Buffered internal reference voltage of $V_{DDQ}/2$.
5	V_{DDQ}	Input for internal reference equal to $V_{DDQ}/2$.
6	AV_{IN}	Analog input pin.
7	P_{VIN}	Power input pin.
8	V_{TT}	Output voltage for connection to termination resistors.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage	PV_{IN}, AV_{IN}, V_{DDQ} to GND	V_{DD}	-0.3 ~ +6	V
	AV_{IN} to GND(Note 1)	V_{DD}	2.2 ~ 5.5	V
Junction Temperature		T_J	+150	℃
Operation Temperature		T_{OPR}	0 ~ +125	℃
Storage Temperature		T_{STG}	-65 ~ +150	℃

Note: 1.Signified recommend operating range that indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits.
2.Absolute maximum ratings indicate limits beyond which damage to the device may occur.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient	θ_{JA}	150	℃/W

■ ELECTRICAL CHARACTERISTICS

(T_J=25℃, V_{IN}=AV_{IN}=PV_{IN}=2.5V, V_{DDQ}=2.5V, unless otherwise specified).

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF} Voltage		V_{REF}	V_{IN} = V_{DDQ} = 2.3V V_{IN} = V_{DDQ} = 2.5V V_{IN} = V_{DDQ} = 2.7V	1.135 1.235 1.335	1.158 1.258 1.358	1.185 1.285 1.385	V
V_{TT} Output Voltage	I_{OUT} = 0A	V_{TT}	V_{IN} = V_{DDQ} = 2.3V V_{IN} = V_{DDQ} = 2.5V V_{IN} = V_{DDQ} = 2.7V	1.125 1.225 1.325	1.159 1.259 1.359	1.190 1.290 1.390	V
	I_{OUT} = ±1.5A		V_{IN} = V_{DDQ} = 2.3V V_{IN} = V_{DDQ} = 2.5V V_{IN} = V_{DDQ} = 2.7V	1.125 1.225 1.325	1.159 1.259 1.359	1.190 1.290 1.390	
V_{TT} Output Voltage Offset (V_{REF} - V_{TT})		$V_{O(OFF)}V_{TT}$	I_{OUT} = 0A I_{OUT} = -1.5A I_{OUT} = +1.5A	-20 -25 -25	0 0 0	20 25 25	mV
Quiescent Current		I_Q	I_{OUT} = 0A		320	500	μA
V_{SENSE} Input Current		I_{SENSE}			13		nA
V_{REF} Output Impedance		Z_{VREF}	I_{REF} = -30 ~ +30 μA		2.5		kΩ
V_{DDQ} Input Impedance		Z_{VDDQ}			100		kΩ
Thermal Shutdown		T_{SHDN}			165		℃
Thermal Shutdown Hysteresis		T_{HYS}			10		℃

■ PIN DESCRIPTIONS

AV_{IN} , PV_{IN}

Input supply pins. AV_{IN} and PV_{IN} are two independent input supply pins for UR5595. AV_{IN} is used to supply all the internal analog circuits and PV_{IN} is only used to supply the output stage to create the regulated V_{TT}. Using a higher PV_{IN} voltages will increase the driving capability of V_{TT}, but the internal power loss will also increase. If the junction temperature exceeds the thermal shutdown than the UR5595 will enter a shutdown state, where V_{TT} is tri-stated and V_{REF} remains active.
For SSTL-2 applications, the AV_{IN} and PV_{IN} can be short together at 2.5V to eliminate the need for bypassing capacitors for the two supply pins separately.

V_{DDQ}

The input pin used to create the internal reference voltage from a resistor divider of two internal 50kΩ resistors for regulating V_{TT} and to guarantee V_{TT} will track $V_{DDQ}/2$ precisely. As a remote sense by connecting V_{DDQ} directly to the 2.5V rail for SSTL-2 applications is an optimal implementation of V_{DDQ} at the DIMM. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines.

V_{SENSE}

The sense pin supply improved remote load regulation; if remote load regulation is not used then the V_{SENSE} pin must still be connected to V_{TT}. A long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. Connect V_{SENSE} pin to the middle of the bus to provide a better distribution across the entire termination bus can reduce the IR drop.

V_{REF}

V_{REF} supply the buffered output of the internal reference voltage ($V_{DDQ}/2$). It can provide the reference voltage of the Northbridge chipset and memory. For better performance, a bypass ceramic capacitor of 0.1μF~0.01μF, located close to the pin, can be used to to help with noise.

V_{TT}

V_{TT} is a regulated output that is used to terminate the bus resistors of DDR-SDRAM. It can precisely track the $V_{DDQ}/2$ voltage with the sinking and sourcing current capability. The UTC **UR5595** is designed to handle peak transient currents of up to ± 3A with a fast transient response. If a transient is expected to remain above the maximum continuous current rating for a significant amount of time then the output capacitor size should be large enough to prevent an excessive voltage drop.

■ CAPACITOR SELECTION

A capacitor is recommended for improve input stability performance during large load transients to prevent the input power rail from dropping, especially for PV_{IN}. The input capacitor should be located as close as possible to the PV_{IN} pin. A typical recommended value for AL electrolytic capacitors is 50μF and 10μF with X5R for Ceramic capacitors. If AV_{IN} and PV_{IN} are separated, the 47μF capacitor should be placed as close to possible to the PV_{IN} rail. An additional 0.1uF ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

UTC **UR5595** has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). The choice for output capacitor depends on the application and the requirements for load transient response of V_{TT}. As a general recommendation the output capacitor should be sized above 100μF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop.

■ THERMAL DISSIPATION

The UR5595 will generate heat result from internal power dissipation when current flow working. The device might be damaged any beyond maximum junction temperature rating. The maximum allowable internal temperature rise (T_{Rmax}) can be calculated given the maximum ambient temperature (T_{Amax}) of the application and the maximum allowable junction temperature (T_{Jmax}).

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

From this equation, the maximum power dissipation (P_{Dmax}) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA}$$

The θ_{JA} of UR5595 can be calculated (refer to JEDEC standard) and will depend on several package type, materials, ambient air temperature and so on.

■ TYPICAL APPLICATION CIRCUITS

Following demonstrate several different application circuits to illustrate some of the options that are possible in configuring the UTC **UR5595**. The individual circuit performance can be found in the Typical Performance Characteristics that curve graphs illustrate how the maximum output current is affected by changes in AV_{IN} and PV_{IN}.

STUB-SERIES TERMINATED LOGIC(SSTL) TERMINATION SCHEME

SSTL was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most popular form of termination is Class II single parallel termination. It involves one R_S series resistor from the chipset to the memory and one R_T termination resistor (refer to Figure 1). R_S and R_T are changeable to meet the current requirement from UR5595, the recommended values both R_S and R_T are 25Ω.

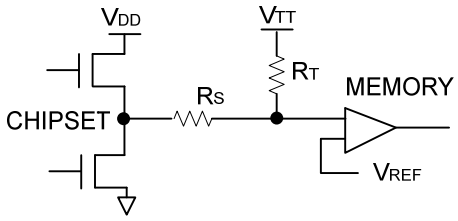


Figure 1. SSTL-Termination Scheme

FOR SSTL-2 APPLICATIONS

For the majority of applications that implement the SSTL- 2 termination scheme, it is recommended to connect all the input rails to the 2.5V rail as Figure 2. This provides an optimal trade-off between power dissipation and component count and selection.

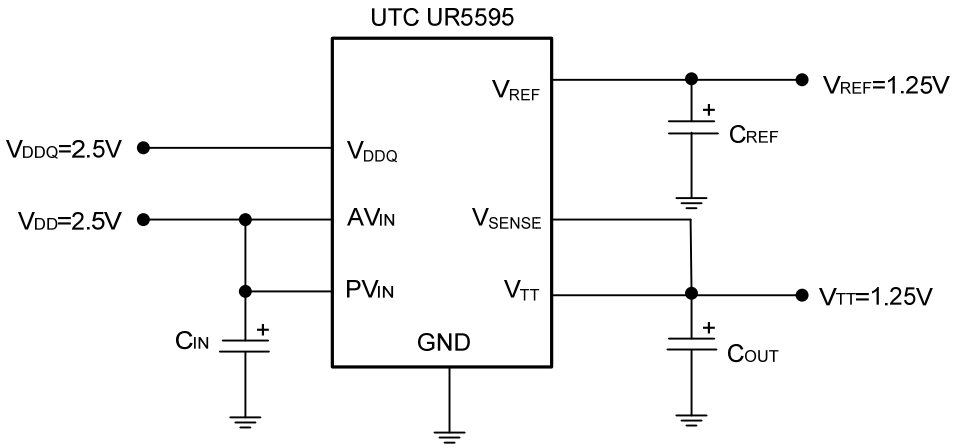


Figure 2. Recommended SSTL-2 Implementation

■ TYPICAL APPLICATION CIRCUITS(Cont.)

Figure 3 illustrate another application that the power rails are split when power dissipation or efficiency are concerned. The output stage (PV_{IN}) can be as lower as 1.8V, and the analog circuitry (AV_{IN}) can be connected to a higher rail such as 2.5V, 3.3V or 5V. This allows the internal power dissipation to be lowered when sourcing current from V_{TT}, but the disadvantage of this circuit is the maximum continuous current is reduced.

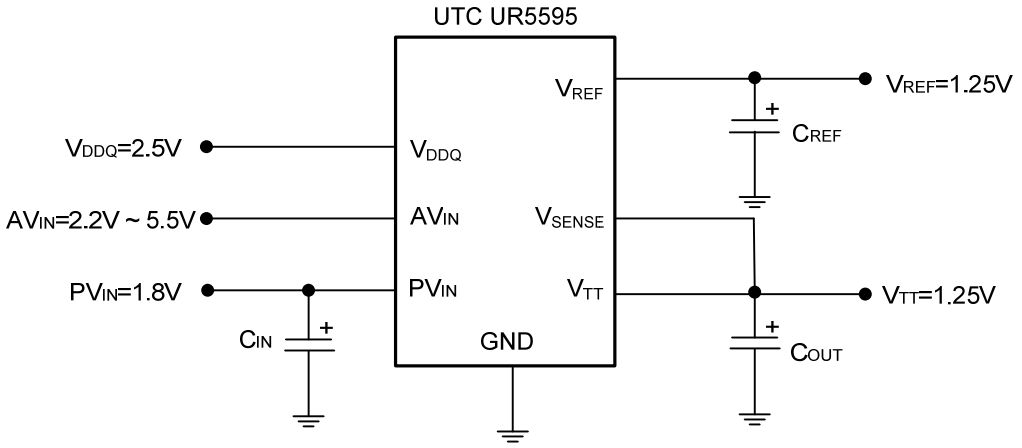


Figure 3. Lower Power Dissipation SSTL-2 Implementation

The third optional application is that PV_{IN} connect to 3.3V and AV_{IN} will be always limited to operation on the 3.3V or 5V to always equal or higher than PV_{IN}. This configuration has the ability to provide the maximum continuous output current at the downside of higher thermal dissipation. The power dissipation increasing problem must be careful to prevent the junction temperature to exceed the maximum ranting. Because of this risk it is not recommended to supply the output stage with a voltage higher than a nominal 3.3V rail.

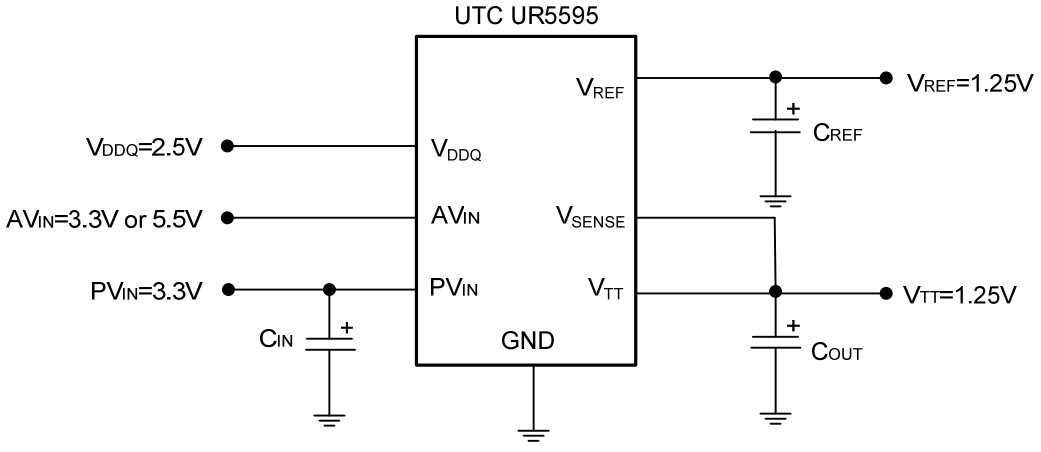


Figure 4. SSTL-2 Implementation with higher voltage rails

■ TYPICAL APPLICATION CIRCUITS(Cont.)

FOR DDR-II APPLICATIONS

As a result of the separate V_{DDQ} pin and an internal resistor divider, **UR5595** can be utilized in DDR-II system, figure 5 and 6 show two recommended circuits in DDR-II SDRAM application. The output stage is connected to the 1.8V rail and the AV_{IN} pin can be connected to either a 3.3V or 5V rail. If it is not desirable to use the 1.8V rail it is possible to connect the output stage to a 3.3V rail. The power dissipation increasing concern must be careful as well SSTL-II application. The advantage of configuration of figure 6 is that it has the ability to source and sink a higher maximum continuous current.

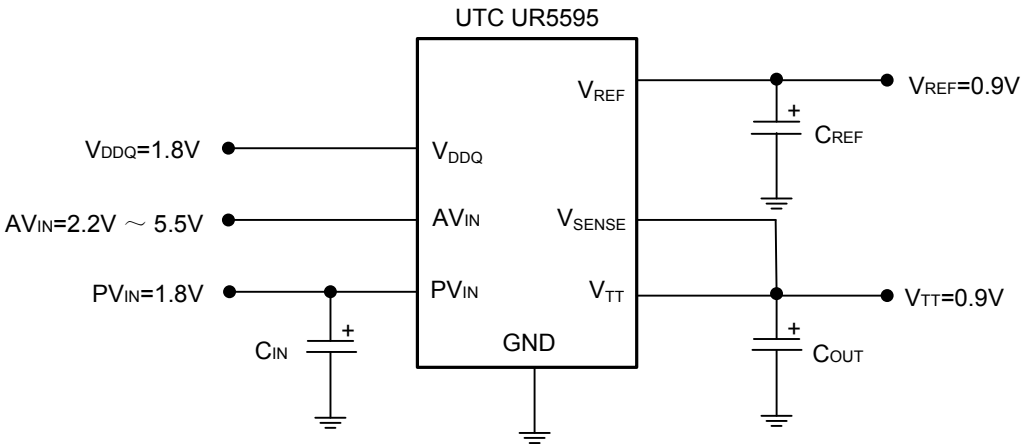


Figure 5. Recommended DDR-II Termination

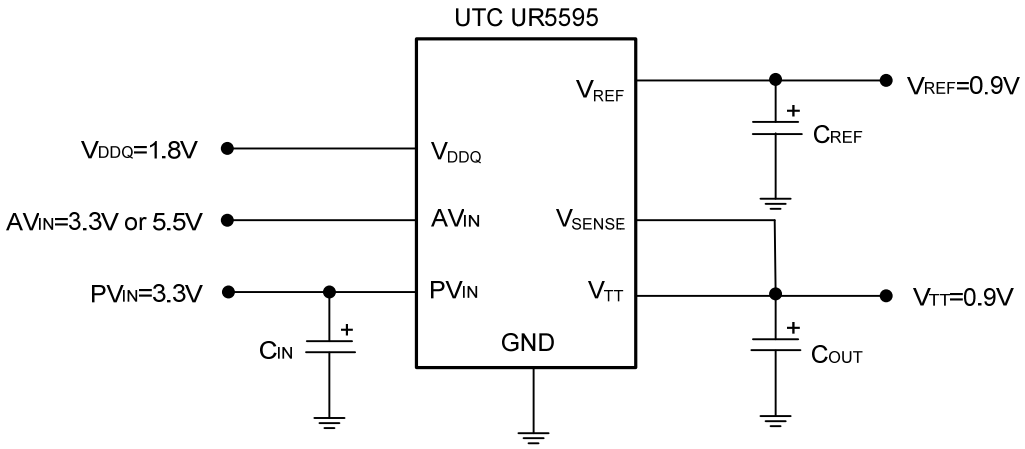
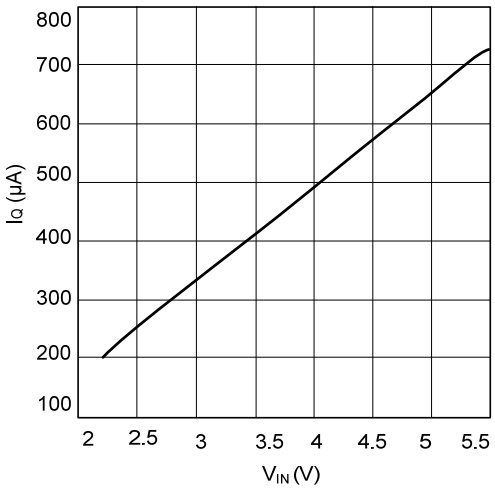


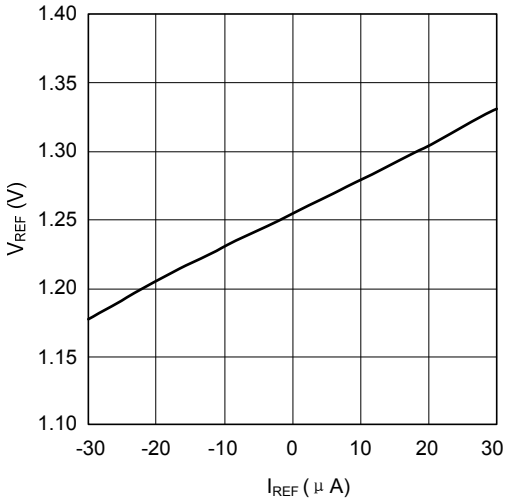
Figure 6. DDR-II Termination with higher voltage rails

■ TYPICAL CHARACTERISTICS

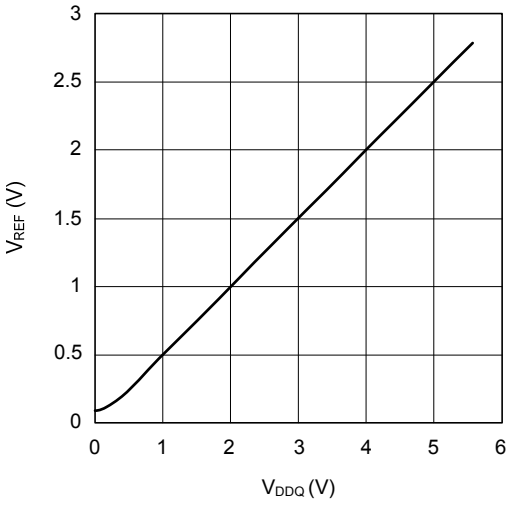
I_Q vs. V_{IN} (25℃)



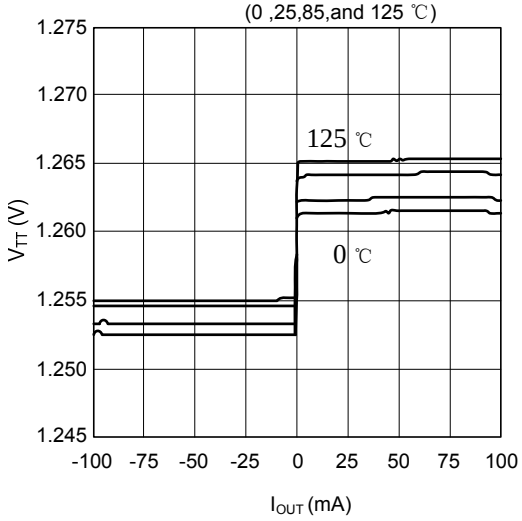
V_{REF} vs. I_{REF}



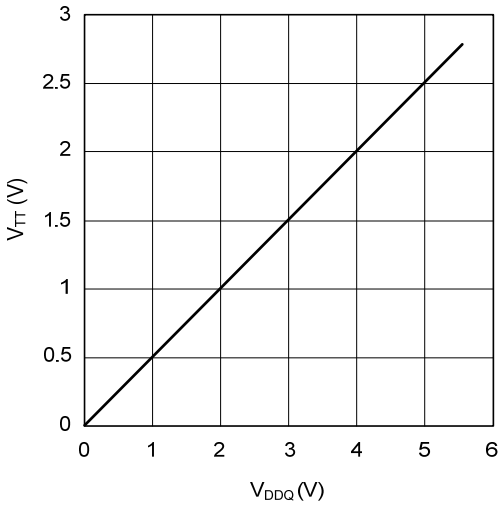
V_{REF} vs. V_{DDQ}



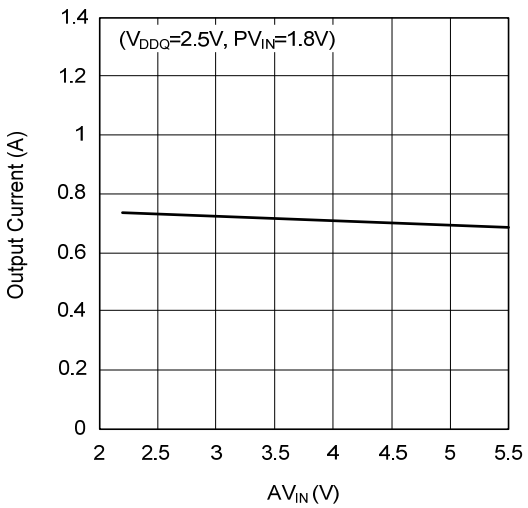
V_{TT} vs. I_{OUT}
(0 ,25,85,and 125 ℃)



V_{TT} vs. V_{DDQ}

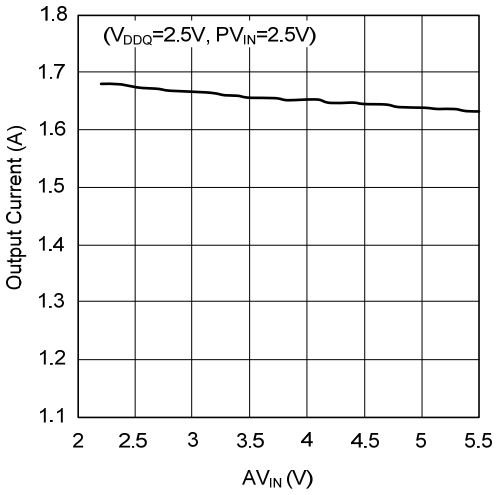


Maximum Sourcing Current vs. AV_{IN}

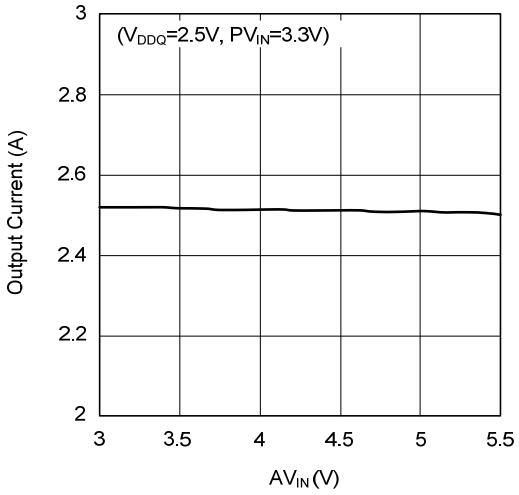


■ TYPICAL CHARACTERISTICS(Cont.)

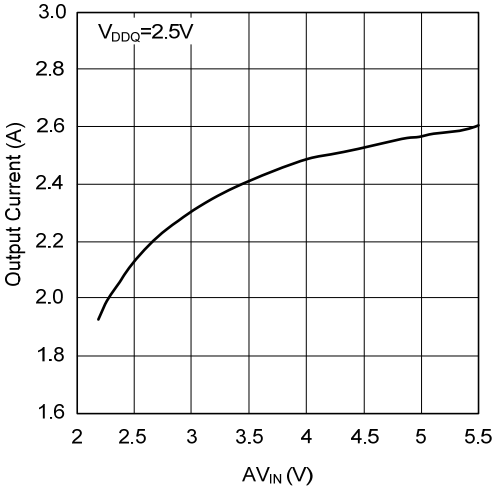
Maximum Sourcing Current vs. AV_{IN}



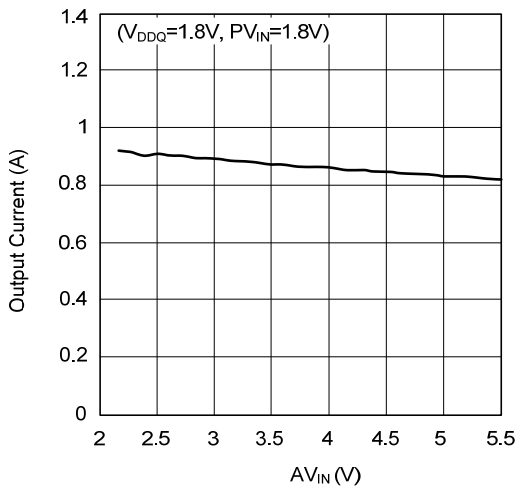
Maximum Sourcing Current vs. AV_{IN}



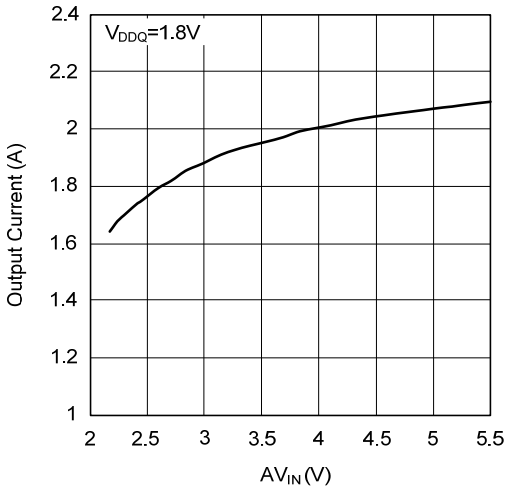
Maximum Sinking Current vs. AV_{IN}
(V_{DDQ}=2.5V)



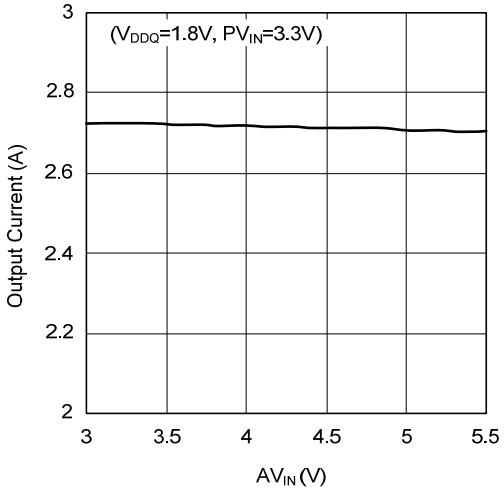
Maximum Sourcing Current vs. AV_{IN}



Maximum Sinking Current vs. AV_{IN}
(V_{DDQ}=1.8V)



Maximum Sourcing Current vs. AV_{IN}
(V_{DDQ}=1.8V, PV_{IN}=3.3V)



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