NEC

MOS INTEGRATED CIRCUIT

μPD75P4308

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD75P4308 replaces the μPD754304's internal mask ROM with a one-time PROM and features expanded ROM capacity.

Because the μPD75P4308 supports programming by users, it is suitable for use in prototype testing for system development using the μPD754302 and 754304 products, and for use in small-lot production.

Detailed descriptions of functions are provided in the following document. Be sure to read the document before designing.

μPD754304 User's Manual: U10123E

FEATURES

- Compatible with μPD754304
- Memory capacity:
  - PROM : 8192 × 8 bits
  - RAM : 256 × 4 bits
- Can operate in the same power supply voltage as the mask version μPD754304
  - V_{DD} = 1.8 to 5.5 V
- Adopts a compact shrink SOP package

ORDERING INFORMATION

Part Number	Package
μPD75P4308GS	36-pin plastic shrink SOP (300 mil, 0.8 mm pitch)

Caution On-chip pull-up resistors by mask option are not provided.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

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OVERVIEW OF FUNCTIONS

Item		Function	
Instruction execution time		• 0.95, 1.91, 3.81, or 15.3 μs (system clock: @ 4.19 MHz) • 0.67, 1.33, 2.67, or 10.7 μs (system clock: @ 6.0 MHz)	
Internal memory	PROM	8192 × 8 bits	
	RAM	256 × 4 bits	
General-purpose register		• 4-bit manipulation: 8 registers × 4 banks • 8-bit manipulation: 4 registers × 8 banks	
I/O ports	CMOS input	8	Connection of on-chip pull-up resistors can be specified by software: 7
	CMOS I/O	18	Connection of on-chip pull-up resistors can be specified by software: 18
	N-ch open-drain I/O	4	13-V withstand voltage
	Total	30	
Timers		3 channels • 8-bit timer/event counter: 2 channels (Can be used as a 16-bit timer/event counter) • 8-bit basic interval timer/watchdog timer: 1 channel	
Serial interface		• 3-wire serial I/O mode ... MSB/LSB-first switchable • 2-wire serial I/O mode	
Bit sequential buffer		16 bits	
Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (system clock: @ 4.19 MHz) • Φ, 750, 375, 93.8 kHz (system clock: @ 6.0 MHz)	
Vectored interrupts		External: 3, Internal: 4	
Test input		External: 1	
System clock oscillator		Ceramic/crystal oscillator	
Standby functions		STOP mode/HALT mode	
Operating ambient temperature		T_A = –40 to +85°C	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		36-pin plastic shrink SOP (300 mil, 0.8 mm pitch)	

CONTENTS

1. PIN CONFIGURATION (Top View) 4

2. BLOCK DIAGRAM 5

3. PIN FUNCTIONS 6
- 3.1 Port Pins 6
- 3.2 Non-port Pins 8
- 3.3 Pin I/O Circuits 9
- 3.4 Recommended Connection of Unused Pins 11

4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE 12
- 4.1 Differences between Mk I Mode and Mk II Mode 12
- 4.2 Setting of Stack Bank Selection (SBS) Register 13

5. DIFFERENCES BETWEEN μPD75P4308 AND μPD754302, 754304 14

6. MEMORY CONFIGURATION 15

7. INSTRUCTION SET 17

8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY 28
- 8.1 Operation Modes for Program Memory Write/Verify 28
- 8.2 Program Memory Write Procedure 29
- 8.3 Program Memory Read Procedure 30
- 8.4 One-Time PROM Screening 31

9. ELECTRICAL SPECIFICATIONS 32

10. CHARACTERISTIC CURVES (FOR REFERENCE ONLY) 45

11. PACKAGE DRAWINGS 47

12. RECOMMENDED SOLDERING CONDITIONS 48

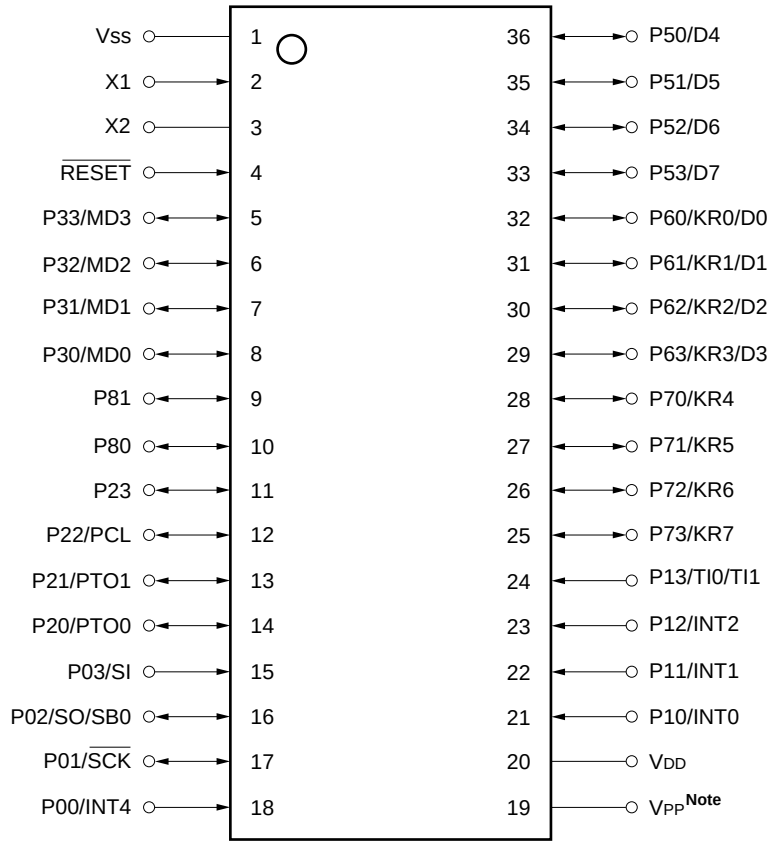
APPENDIX A. COMPARISON OF μPD750004, 754304, AND 75P4308 FUNCTIONS 49

APPENDIX B. DEVELOPMENT TOOLS 51

APPENDIX C. RELATED DOCUMENTS 55

1. PIN CONFIGURATION (Top View)

- 36-pin plastic shrink SOP (300 mil, 0.8 mm pitch)
  μPD75P4308GS

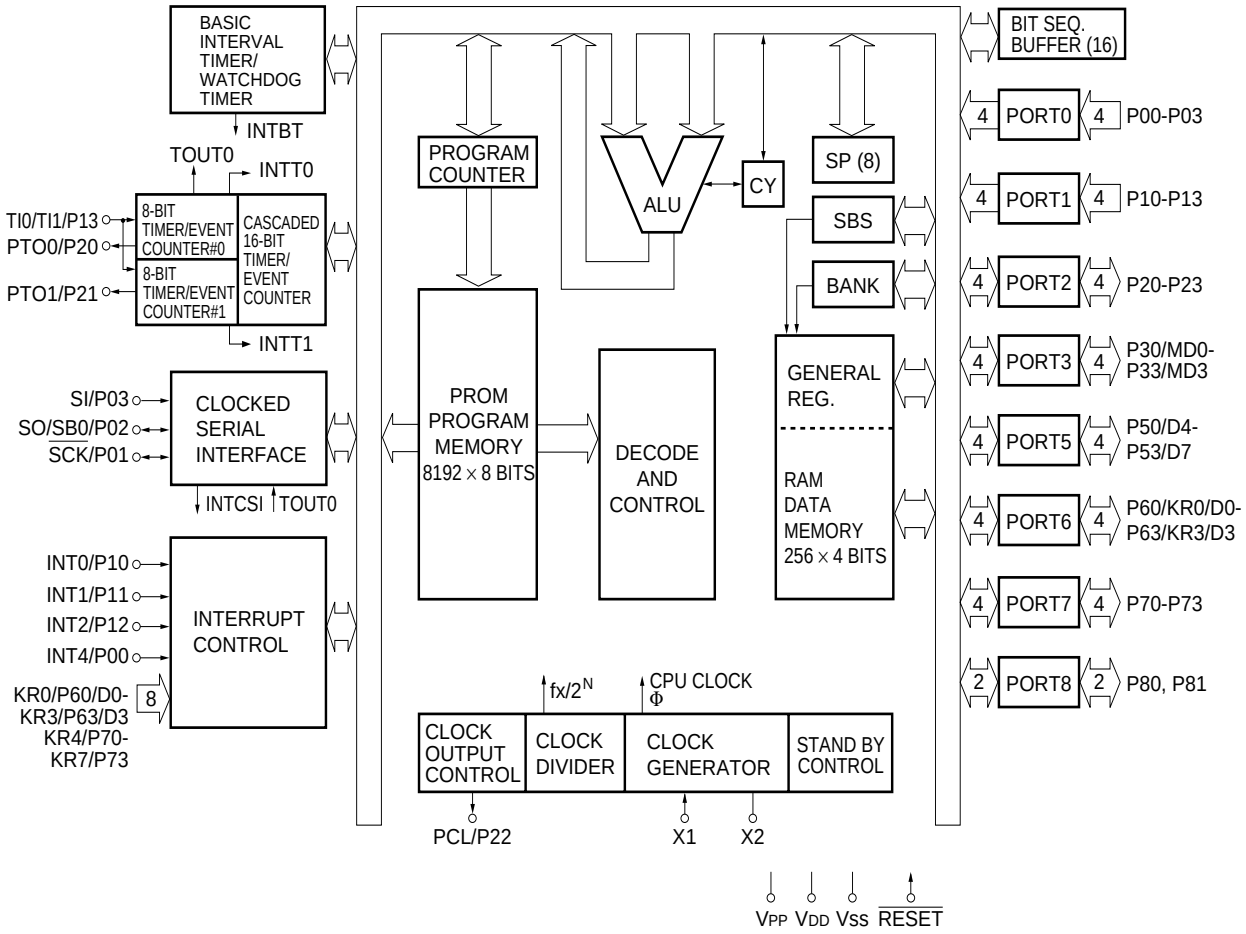


Note Connect V_{PP} directly to V_{DD} during normal operations.

PIN IDENTIFICATIONS

P00 to P03	: Port0	SI	: Serial Input
P10 to P13	: Port1	SO	: Serial Output
P20 to P23	: Port2	SB0	: Serial Bus 0
P30 to P33	: Port3	RESET	: Reset
P50 to P53	: Port5	TI0, 1	: Timer Input 0, 1
P60 to P63	: Port6	PTO0, 1	: Programmable Timer Output 0, 1
P70 to P73	: Port7	PCL	: Programmable Clock
P80, P81	: Port8	INT0, 1, 4	: External Vectored Interrupt 0, 1, 4
KR0 to KR7	: Key Return 0 to 7	INT2	: External Test Input 2
V_{DD}	: Positive Power Supply	X1, 2	: System Clock Oscillation 1, 2
V_{SS}	: GND	MD0 to 3	: Mode Selection 0 to 3
V_{PP}	: Programming Power Supply	D0 to D7	: Data Bus 0 to 7
SCK	: Serial Clock		

★ 2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin name	I/O	Alternate function	Function	8-bit I/O	After reset	I/O Circuit type[Note 1]
P00	Input	INT4	4-bit input port (PORT0). For P01 to P03, connections of on-chip pull-up resistors are software-specificable in 3-bit units.	No	Input	<B>
P01	I/O	$\overline{SCK}$				<F>-A
P02	I/O	SO/SB0				<F>-B
P03	Input	SI				<B>-C
P10	Input	INT0	4-bit input port (PORT1). Connections of on-chip pull-up resistors are software-specifiable in 4-bit units. Noise elimination circuit can be selected only for P10/INT0.	No	Input	<B>-C
P11		INT1				
P12		INT2				
P13		TI0/TI1				
P20	I/O	PTO0	4-bit I/O port (PORT2). Connections of on-chip pull-up resistors are software-specifiable in 4-bit units.	No	Input	E-B
P21		PTO1				
P22		PCL				
P23		—				
P30	I/O	MD0	Programmable 4-bit I/O port (PORT3). Input and output can be specified in single-bit units. Connections of on-chip pull-up resistors are software-specifiable in 4-bit units.	No	Input	E-B
P31		MD1				
P32		MD2				
P33		MD3				
★ P50[Note 2]	I/O	D4	N-ch open-drain 4-bit input/output port (PORT5). 13-V withstand during open-drain. Data input/output pin for program memory (PROM) write/verify (upper 4 bits).	No	High-impedance	M-E
P51[Note 2]		D5				
P52[Note 2]		D6				
P53[Note 2]		D7				

Notes 1. Circuit types in brackets indicate Schmitt trigger input.

2. Low-level input leakage current increases when input instructions or bit manipulation instructions are executed.

3.1 Port Pins (2/2)

Pin name	I/O	Alternate function	Function	8-bit I/O	After reset	I/O Circuit type[Note]
★ P60	I/O	KR0/D0	Programmable 4-bit I/O port (PORT6). Input and output can be specified in single-bit units. Connections of on-chip pull-up resistors are software-specifiable in 4-bit units. Data input/output pin for program memory (PROM) write/verify (lower 4 bits).	Yes	Input	<F>-A
P61		KR1/D1				
P62		KR2/D2				
P63		KR3/D3				
P70	I/O	KR4	4-bit I/O port (PORT7). Connections of on-chip pull-up resistors are software-specifiable in 4-bit units.		Input	<F>-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	I/O	—	2-bit I/O port (PORT8). Connections of on-chip pull-up resistors are software-specifiable in 2-bit units.	No	Input	E-B
P81		—				

Note Circuit types in brackets indicate the Schmitt trigger input.

3.2 Non-port Pins

Pin name	I/O	Alternate function	Function		After reset	I/O Circuit type[Note 1]
TI0/TI1	Input	P13	External event pulse input to timer/event counter		Input	<B>-C
PTO0	Output	P20	Timer/event counter output		Input	E-B
PTO1		P21				
PCL		P22	Clock output			
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	<F>-A
SO/SB0		P02	Serial data output Serial data bus I/O			<F>-B
SI	Input	P03	Serial data input			<B>-C
INT4		P00	Edge-triggered vectored interrupt input (triggered by both rising and falling edges).		—	<B>
INT0	Input	P10	Edge-triggered vectored interrupt input (detected edge is selectable). Noise elimination circuit selectable in INT0/P10.	Noise elimination circuit appended/ asynchronous selectable	—	<B>-C
INT1		P11		Asynchronous		
INT2		P12	Rising edge-triggered test input	Asynchronous		
KR0 to KR3	Input	P60/D0 to P63/D3	Falling edge-triggered testable input		Input	<F>-A
KR4 to KR7		P70 to P73				
X1	Input	—	Ceramic/crystal connection for system clock oscillation. If using an external clock, input it to X1 and input the inverted clock to X2.		—	—
X2	—					
$\overline{RESET}$	Input	—	System reset input		—	<B>
MD0 to MD3	Input	P30 to P33	Mode selection for program memory (PROM) write/ verify.		Input	E-B
★ D0 to D3	I/O	P60/KR0 to P63/KR3	Data bus pin for program memory (PROM) write/verify.		Input	<F>-A
★ D4 to D7		P50 to P53				M-E
V_{PP}[Note 2]	—	—	Program supply voltage in program memory (PROM) write/verify mode. In normal operation mode, connect directly to V_{DD}. Apply +12.5 V in PROM write/verify mode.		—	—
V_{DD}	—	—	Positive power supply		—	—
V_{SS}	—	—	Ground		—	—

Notes 1. Circuit types in brackets indicate Schmitt trigger input.

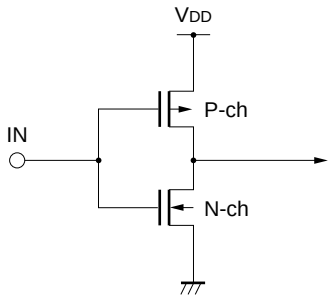
2. During normal operation, the V_{PP} pin will not operate normally unless connected to V_{DD} pin.

3.3 Pin I/O Circuits

The equivalent circuits for the μPD75P4308's pin are shown in simplified schematic diagrams below.

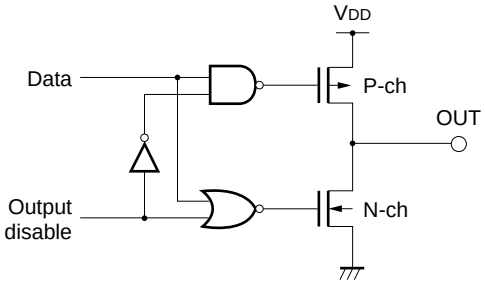
(1/2)

TYPE A



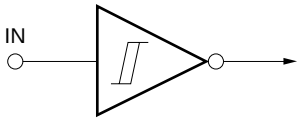
CMOS standard input buffer

TYPE D



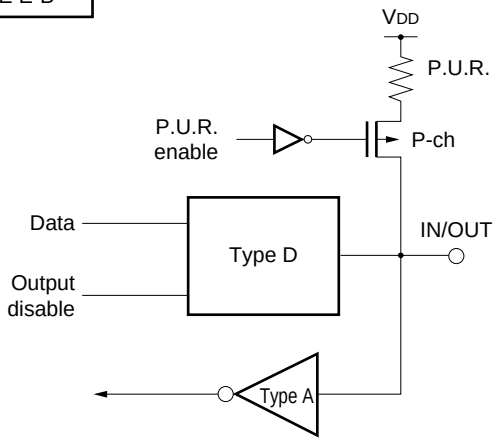
Push-pull output that can be set to high impedance output (with both P-ch and N-ch OFF).

TYPE B



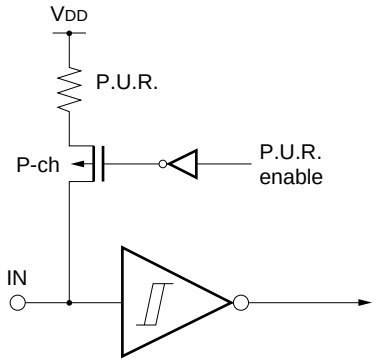
Schmitt trigger input with hysteresis characteristics.

TYPE E-B



P.U.R.: Pull-Up Resistor

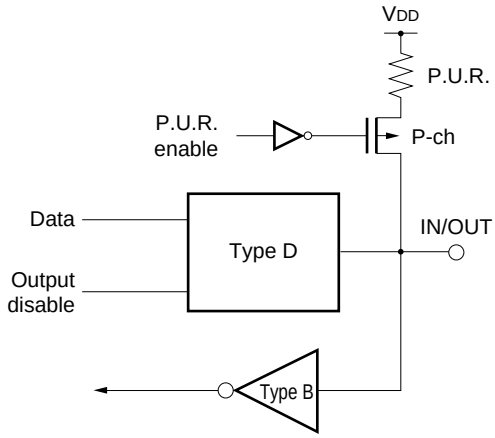
TYPE B-C



P.U.R. : Pull-Up Resistor

Schmitt trigger input with hysteresis characteristics.

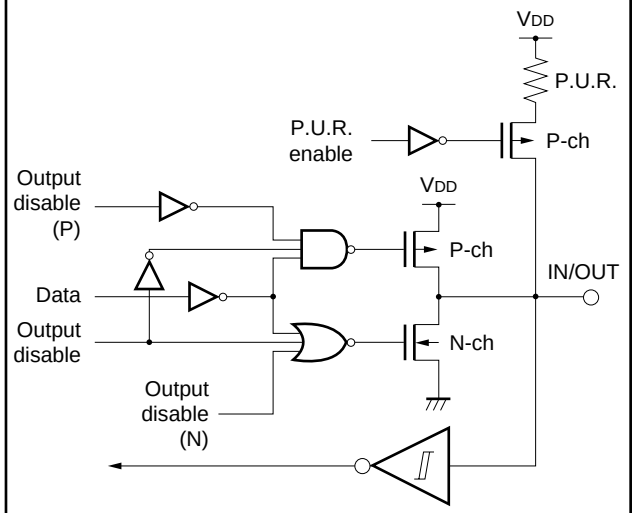
TYPE F-A



P.U.R.: Pull-Up Resistor

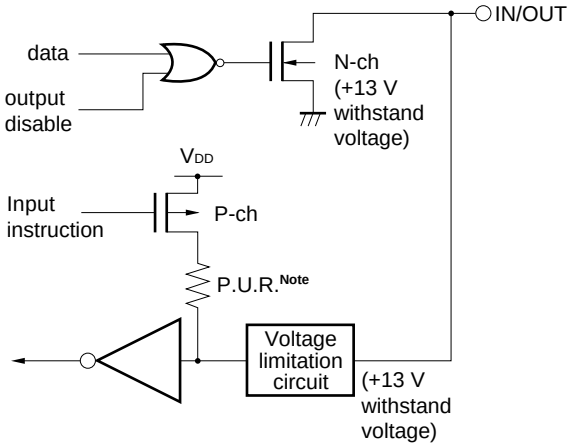
(2/2)

TYPE F-B



P.U.R.: Pull-Up Resistor

TYPE M-E★



Note Pull-up resistor that operates only when an input instruction has been executed (current flows from V_{DD} to the pin when the pin is low).

★ 3.4 Recommended Connection of Unused Pins

Pin	Recommended connection
P00/INT4	Connect to V_{SS} or V_{DD}.
P01/$\overline{SCK}$	Connect individually to V_{SS} or V_{DD} via a resistor.
P02/SO/SB0	
P03/SI	Connecto to V_{SS}.
P10/INT0 to P12/INT2	Connect to V_{SS} or V_{DD}.
P13/TI0/TI1	
P20/PTO0	Input mode : connect individually to V_{SS} or V_{DD} via a resistor. Output mode: open
P21/PTO1	
P22/PCL	
P23	
P30/MD0 to P33/MD3	
P50 to P53	Connect to V_{SS}.
P60/KR0 to P63/KR3	Input mode : connect individually to V_{SS} or V_{DD} via a resistor. Output mode: open
P70/KR4 to P73/KR7	
P80, P81	
V_{PP}	Be sure to connect directly to V_{DD}.

4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

Setting a stack bank selection (SBS) register for the μPD75P4308 enables the program memory to be switched between the Mk I mode and the Mk II mode. This capability enables the evaluation of the μPD754302 or 754304 using the μPD75P4308.

When the SBS bit 3 is set to 1: sets Mk I mode (corresponds to Mk I mode of μPD754302 and 754304)
When the SBS bit 3 is set to 0: sets Mk II mode (corresponds to Mk II mode of μPD754302 and 754304)

4.1 Differences between Mk I Mode and Mk II Mode

Table 4-1 lists the differences between the Mk I mode and the Mk II mode of the μPD75P4308.

Table 4-1. Differences between Mk I Mode and Mk II Mode

Item		Mk I Mode	Mk II Mode
Program counter		PC_{12-0}	
Program memory (bytes)		8192	
Data memory (bits)		256 × 4	
Stack	Stack bank	Memory bank 0	
	Stack bytes	2 bytes	3 bytes
Instruction	BRA !addr1 CALLA !addr1	Not provided	Provided
Instruction execution time	CALL !addr	3 machine cycles	4 machine cycles
	CALLF !faddr	2 machine cycles	3 machine cycles
Supported mask ROM versions		Mk I mode of μPD754302 and 754304	Mk II mode of μPD754302 and 754304

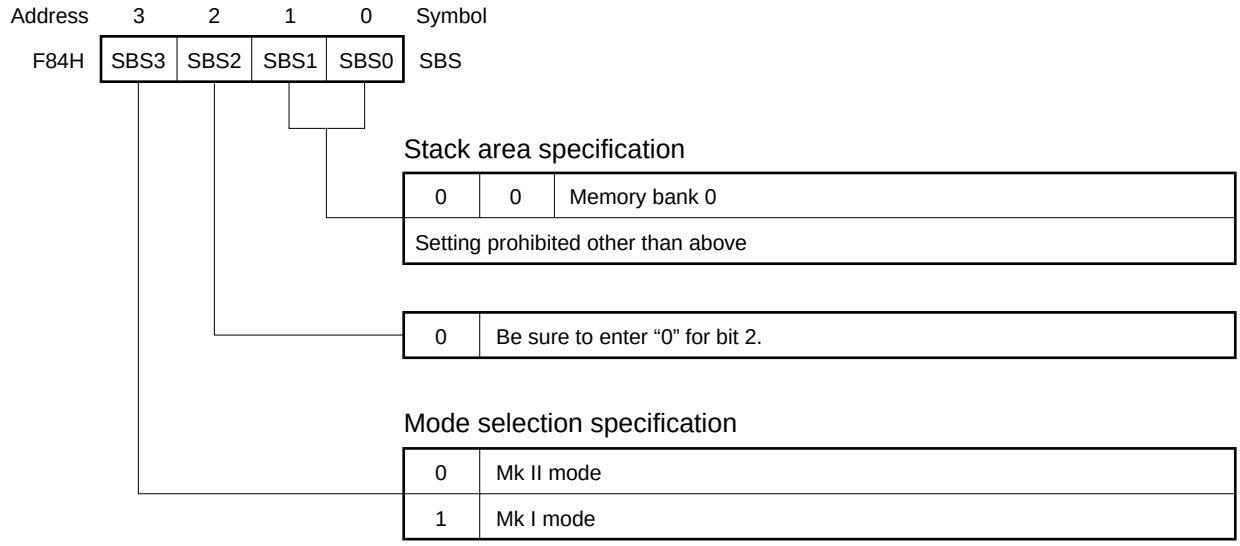
★ **Caution The Mk II mode supports 16 Kbytes or more of program area in the 75X and 75XL Series. This mode allows the software compatibility with 16-Kbyte or more versions to be improved. Compared with the Mk I mode, selecting the Mk II mode increases the stack bytes by one during execution of the subroutine call instruction. When a CALL !addr or CALLF !faddr instruction is used, the instruction execution time increases by one machine cycle. Therefore, if RAM efficiency or throughput is more important than software compatibility, use the Mk I mode.**

4.2 Setting of Stack Bank Selection (SBS) Register

Use the stack bank selection register to switch between the Mk I mode and the Mk II mode. Figure 4-1 shows the format for doing this.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 1000B at the beginning of the program. When using the Mk II mode, be sure to initialize it to 0000B.

Figure 4-1. Format of Stack Bank Selection Register



Cautions 1. SBS3 is set to “1” after $\overline{\text{RESET}}$ input, and consequently the CPU operates in the Mk I mode. When using instructions for the Mk II mode, set SBS3 to “0” to enter the Mk II mode before using the instructions.

2. When using the Mk II mode, execute a subroutine call instruction and an interrupt instruction after $\overline{\text{RESET}}$ input and after setting the stack bank selection register.

5. DIFFERENCES BETWEEN μPD75P4308 AND μPD754302, 754304

The μPD75P4308 replaces the internal mask ROM in the μPD754302 and 754304 with a one-time PROM and features expanded ROM capacity. The μPD75P4308's Mk I mode supports the Mk I mode in the μPD754302 and 754304 and the μPD75P4308's Mk II mode supports the Mk II mode in the μPD754302 and 754304.

Table 5-1 lists differences among the μPD75P4308 and the μPD754302 and 754304. Be sure to check the differences between corresponding versions beforehand, especially when a PROM version is used for debugging or prototype testing of application systems and later the corresponding mask ROM version is used for full-scale production.

For details of CPU functions and incorporated hardware, refer to **μPD754304 User's Manual** (**U10123E**).

Table 5-1. Differences between μPD75P4308 and μPD754302, 754304

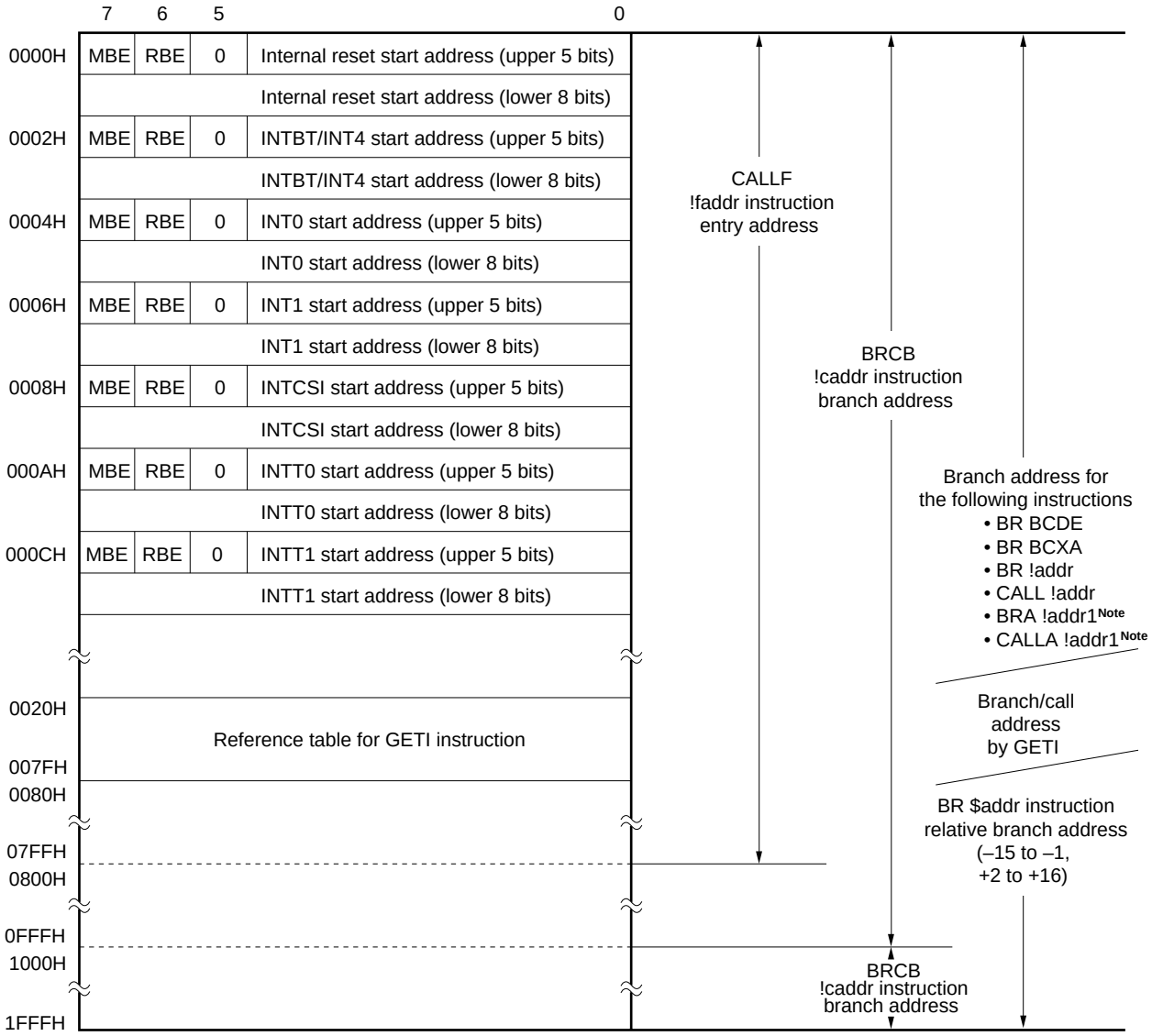
Item		μPD754302	μPD754304	μPD75P4308
Program counter		11-bit	12-bit	13-bit
Program memory (bytes)		Mask ROM 2048	Mask ROM 4096	One-time PROM 8192
Data memory (× 4 bits)		256		
Mask options	Pull-up resistor for PORT5	Yes (On-chip/not on-chip specifiable)		No (On-chip not possible)
	Wait time in $\overline{\text{RESET}}$ state	Yes (Selectable from $2^{17}/f_X$ and $2^{15}/f_X$)Note		No (fixed at $2^{15}/f_X$)Note
Pin configuration	Pins 5 to 8	P33-P30		P33/MD3-P30/MD0
	Pin 19	IC		V_{PP}
★	Pins 29 to 32	P63/KR3-P60/KR0		P63/KR3/D3-P60/KR0/D0
★	Pins 33 to 36	P53-P50		P53/D7-P50/D4
Other		Noise resistance and noise radiation may differ due to the different circuit complexities and mask layouts.		

Note $2^{17}/f_X$: 21.8 ms @6.0-MHz operation, 31.3 ms @4.19-MHz operation.
$2^{15}/f_X$: 5.46 ms @6.0-MHz operation, 7.81 ms @4.19-MHz operation.

Caution Noise resistance and noise radiation are different in PROM version and mask ROM versions. If using a mask ROM version instead of the PROM version for processes between prototype development and full production, be sure to fully evaluate the CS (not ES) of the mask ROM version.

6. MEMORY CONFIGURATION

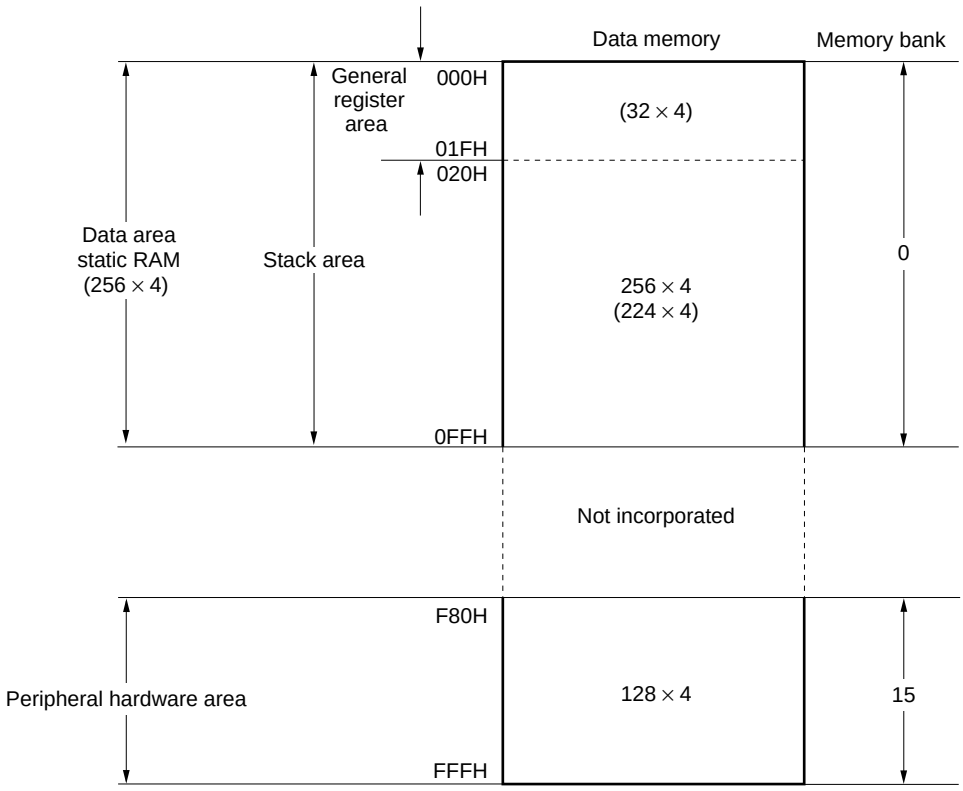
Figure 6-1. Program Memory Map



Note Can be used only in the Mk II mode.

Remark For instructions other than those noted above, the “BR PCDE” and “BR PCXA” instructions can be used to branch to addresses with changes in the PC’s lower 8 bits only.

Figure 6-2. Data Memory Map



7. INSTRUCTION SET

(1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, refer to **RA75X Assembler Package User's Manual Language (EEU-1363)**). When there are several codes, select and use just one. Uppercase letters, and + and – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Instead of mem, fmem, pmem, bit, etc., a register flag symbol can be described as a label descriptor (for details, refer to **μPD754304 User's Manual (U10123E)**). Labels that can be entered for fmem and pmem are restricted.

Representation	Coding format
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label[Note] 2-bit immediate data or label
fmem pmem	FB0H-FBFH, FF0H-FFFH immediate data or label FC0H-FFFH immediate data or label
addr addr1	0000H-1FFFH immediate data or label 0000H-1FFFH immediate data or label (in Mk II mode only)
caddr faddr taddr	12-bit immediate data or label 11-bit immediate data or label 20H-7FH immediate data (however, bit0 = 0) or label
PORTn IE××× RBn MBn	PORT0-PORT3, PORT5-PORT8 IEBT, IECSI, IET0, IET1, IE0-IE2, IE4 RB0-RB3 MB0, MB15

Note When processing 8-bit data, only even addresses can be specified.

(2) Operation legend

A	:	A register; 4-bit accumulator
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
X	:	X register
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
XA'	:	Expansion register pair (XA')
BC'	:	Expansion register pair (BC')
DE'	:	Expansion register pair (DE')
HL'	:	Expansion register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Port n (n = 0 to 3, 5 to 8)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority select register
IE×××	:	Interrupt enable flag
RBS	:	Register bank select register
MBS	:	Memory bank select register
PCC	:	Processor clock control register
.	:	Delimiter for address and bit
(××)	:	Contents of address ××
××H	:	Hexadecimal data

(3) Description of symbols used in addressing area

*1	MB = MBE·MBS (MBS = 0, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H-07FH) MB = 15 (F80H-FFFH) MBE = 1 : MB = MBS (MBS = 0, 15)	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr, addr1 = 0000H-1FFFH	Program memory addressing
*7	addr, addr1 = (Current PC) –15 to (Current PC) –1 (Current PC) +2 to (Current PC) +16	
*8	caddr = 0000H-0FFFH (PC_{12} = 0) or 1000H-1FFFH (PC_{12} = 1)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	
*11	addr1 = 0000H-1FFFH (Mk II mode only)	

Remarks 1. MB indicates access-enabled memory banks.

2. In area *2, MB = 0 for both MBE and MBS.

3. In areas *4 and *5, MB = 15 for both MBE and MBS.

4. Areas *6 to *11 indicate corresponding address-enabled areas.

(4) Description of machine cycles

S indicates the number of machine cycles required for skipping of skip-specified instructions. The value of S varies as shown below.

- No skip ····· S = 0
- Skipped instruction is 1-byte or 2-byte instruction ····· S = 1
- Skipped instruction is 3-byte instruction[Note] ····· S = 2

Note 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, CALLA !addr1

Caution The GETI instruction is skipped for one machine cycle.

One machine cycle equals one cycle (= t_{CY}) of the CPU clock Φ. Use the PCC setting to select among four cycle times.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A ← n4		String-effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String-effect A
		HL, #n8	2	2	HL ← n8		String-effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2 + S	A ← (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ← (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg1	2	2	A ← reg1		
		XA, rp’	2	2	XA ← rp’		
		reg1, A	2	2	reg1 ← A		
		rp’1, XA	2	2	rp’1 ← XA		
	XCH	A, @HL	1	1	A ⟷ (HL)	*1	
		A, @HL+	1	2 + S	A ⟷ (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ⟷ (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ⟷ (rpa1)	*2	
		XA, @HL	2	2	XA ⟷ (HL)	*1	
		A, mem	2	2	A ⟷ (mem)	*3	
		XA, mem	2	2	XA ⟷ (mem)	*3	
		A, reg1	1	1	A ⟷ reg1		
		XA, rp’	2	2	XA ⟷ rp’		
Table reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{12-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{12-8} + XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$ Note	*6	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$ Note	*6	

Note As for the B register, only the lower 1 bit is valid.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← (H + mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0})) ← CY	*5	
		@H + mem.bit, CY	2	2	(H + mem_{3-0}.bit) ← CY	*1	
Operation	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		XA, #n8	2	2 + S	XA ← XA + n8		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
		XA, rp'	2	2 + S	XA ← XA + rp'		carry
		rp'1, XA	2	2 + S	rp'1 ← rp'1 + XA		carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
		XA, rp'	2	2	XA, CY ← XA + rp' + CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 + XA + CY		
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
		XA, rp'	2	2 + S	XA ← XA – rp'		borrow
		rp'1, XA	2	2 + S	rp'1 ← rp'1 – XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
		XA, rp'	2	2	XA, CY ← XA – rp' – CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 – XA – CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ∀ n4		
		A, @HL	1	1	A ← A ∀ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∀ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∀ XA		

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Accumulator manipulate	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow An$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/ decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
		rp’	2	2 + S	rp’ ← rp’ – 1		rp’ = FFH
Compare	SKE	reg, #n4	2	2 + S	Skip if reg =n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp’	2	2 + S	Skip if XA = rp’		XA = rp’
Carry flag manipulate	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Memory bit manipulate	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← 1	*5	
		@H + mem.bit	2	2	(H+mem_{3-0}.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← 0	*5	
		@H + mem.bit	2	2	(H+mem_{3-0}.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit)=1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit)=1
		pmem.@L	2	2 + S	Skip if ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) = 1	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if (H + mem_{3-0}.bit) = 1	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) = 0	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if (H + mem_{3-0}.bit) = 0	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0})) = 1 and clear	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if (H + mem_{3-0}.bit) = 1 and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∧ (H + mem_{3-0}.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨ (H + mem_{3-0}.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∀ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∀ (H + mem_{3-0}.bit)	*1	

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Branch	BR[Note1]	addr	—	—	$PC_{12-0} \leftarrow$ addr (Assembler selects the most appropriate instruction among the following: • BR !addr • BRCB !caddr • BR $addr)	*6	
		addr1	—	—	$PC_{12-0} \leftarrow$ addr1 (Assembler selects the most appropriate instruction among the following: • BRA !addr1 • BR !addr • BRCB !caddr • BR $addr1)	*11	
		!addr	3	3	$PC_{12-0} \leftarrow$ addr	*6	
		$addr	1	2	$PC_{12-0} \leftarrow$ addr	*7	
		$addr1	1	2	$PC_{12-0} \leftarrow$ addr1		
		PCDE	2	3	$PC_{12-0} \leftarrow PC_{12-8} + DE$		
		PCXA	2	3	$PC_{12-0} \leftarrow PC_{12-8} + XA$		
		BCDE	2	3	$PC_{12-0} \leftarrow$ BCDE[Note 2]	*6	
		BCXA	2	3	$PC_{12-0} \leftarrow$ BCXA[Note 2]	*6	
	BRA[Note 1]	!addr1	3	3	$PC_{12-0} \leftarrow$ addr1	*11	
	BRCB	!caddr	2	2	$PC_{12-0} \leftarrow PC_{12} + caddr_{11-0}$	*8	

Notes 1. Shaded areas indicate support for the Mk II mode only.

2. Only the lower 2 bit in the B register is valid.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALLA[Note]	!addr1	3	3	(SP – 5) ← 0, 0, 0, PC_{12} (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 2) ← ×, ×, MBE, RBE PC_{12-0} ← addr1, SP ← SP – 6	*11	
	CALL[Note]	!addr	3	3	(SP –4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, 0, PC_{12} PC_{12-0} ← addr, SP ← SP – 4	*6	
				4	(SP – 5) ← 0, 0, 0, PC_{12} (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 2) ← ×, ×, MBE, RBE PC_{12-0} ← addr, SP ← SP – 6		
	CALLF[Note]	!faddr	2	2	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, 0, PC_{12} PC_{12-0} ← 00 + faddr, SP ← SP – 4	*9	
				3	(SP – 5) ← 0, 0, 0, PC_{12} (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 2) ← ×, ×, MBE, RBE PC_{12-0} ← 00 + faddr, SP ← SP – 6		
	RET[Note]		1	3	MBE, RBE, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4		
					×, ×, MBE, RBE ← (SP + 4) 0, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 6		
	RETS[Note]		1	3 + S	MBE, RBE, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4 then skip unconditionally		Unconditional
					×, ×, MBE, RBE ← (SP + 4) 0, 0, 0, PC_{12} ← (SP + 1) $PC_{11,0}$ ← (SP) (SP + 3) (SP + 2) SP ← SP + 6 then skip unconditionally		
	RETI		1	3	MBE, RBE, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
					0, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		

Note Shaded areas indicate support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	PUSH	rp	1	1	(SP – 1) (SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← RBS, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1) (SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), RBS ← (SP), SP ← SP + 2		
Interrupt control	EI		2	2	IME (IPS.3) ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IE×××	2	2	IE××× ← 0		
I/O	IN[Note 1]	A, PORTn	2	2	A ← PORTn (n = 0 - 3, 5 - 8)		
		XA, PORTn	2	2	XA ← PORTn + 1, PORTn (n = 6)		
	OUT[Note 1]	PORTn, A	2	2	PORTn ← A (n = 2 - 3, 5 - 8)		
		PORTn, XA	2	2	PORTn + 1, PORTn ← XA (n = 6)		
CPU control	HALT		2	2	Set HALT Mode(PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode(PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS ← n (n = 0 - 3)		
		MBn	2	2	MBS ← n (n = 0, 15)		
	GETI[Note 2, 3]	taddr	1	3	• When using TBR instruction $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$	*10	
					• When using TCALL instruction (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, 0, PC_{12} $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$ SP ← SP – 4		
					• When using instruction other than TBR or TCALL Execute (taddr) (taddr + 1) instructions		Determined by referenced instruction
			1		• When using TBR instruction $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$	*10	
				4	• When using TCALL instruction (SP – 5) ← 0, 0, 0, PC_{12} (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 2) ← ×, ×, MBE, RBE $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$ SP ← SP – 6		
				3	• When using instruction other than TBR or TCALL Execute (taddr) (taddr + 1) instructions		Determined by referenced instruction

Notes 1. Before executing the IN or OUT instruction, set MBE to 0 or 1 and set MBS to 15.

2. TBR and TCALL are assembler pseudo-instructions for the GETI instruction's table definitions.

3. Shaded areas indicate support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory in the μPD75P4308 is a 8192 × 8-bit electrically write-enabled one-time PROM. The pins listed in the table below are used for this one-time PROM's write/verify operations. Clock input from the X1 pin is used instead of address input as a method for updating addresses.

Pin name	Function
V_{PP}	Pin (usually V_{DD}) where programming voltage is applied during program memory write/verify
X1, X2	Clock input pin for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin.
MD0-MD3	Operation mode selection pin for program memory write/verify
D0/P60/KR0-D3/P63/KR3 (lower 4) D4/P50-D7/P53 (upper 4)	8-bit data I/O pin for program memory write/verify
V_{DD}	Pin where power supply voltage is applied. Power voltage range for normal operation is 1.8 to 5.5 V. Apply 6.0 V for program memory write/verify.

Caution Pins not used for program memory write/verify connect to Vss via a pull-down resistor.

8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the μPD75P4308's V_{DD} pin and +12.5 V is applied to its V_{PP} pin, program write/verify modes are in effect. Furthermore, the following detailed operation modes can be specified by setting pins MD0 to MD3 as shown below.

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Zero-clear program memory address
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

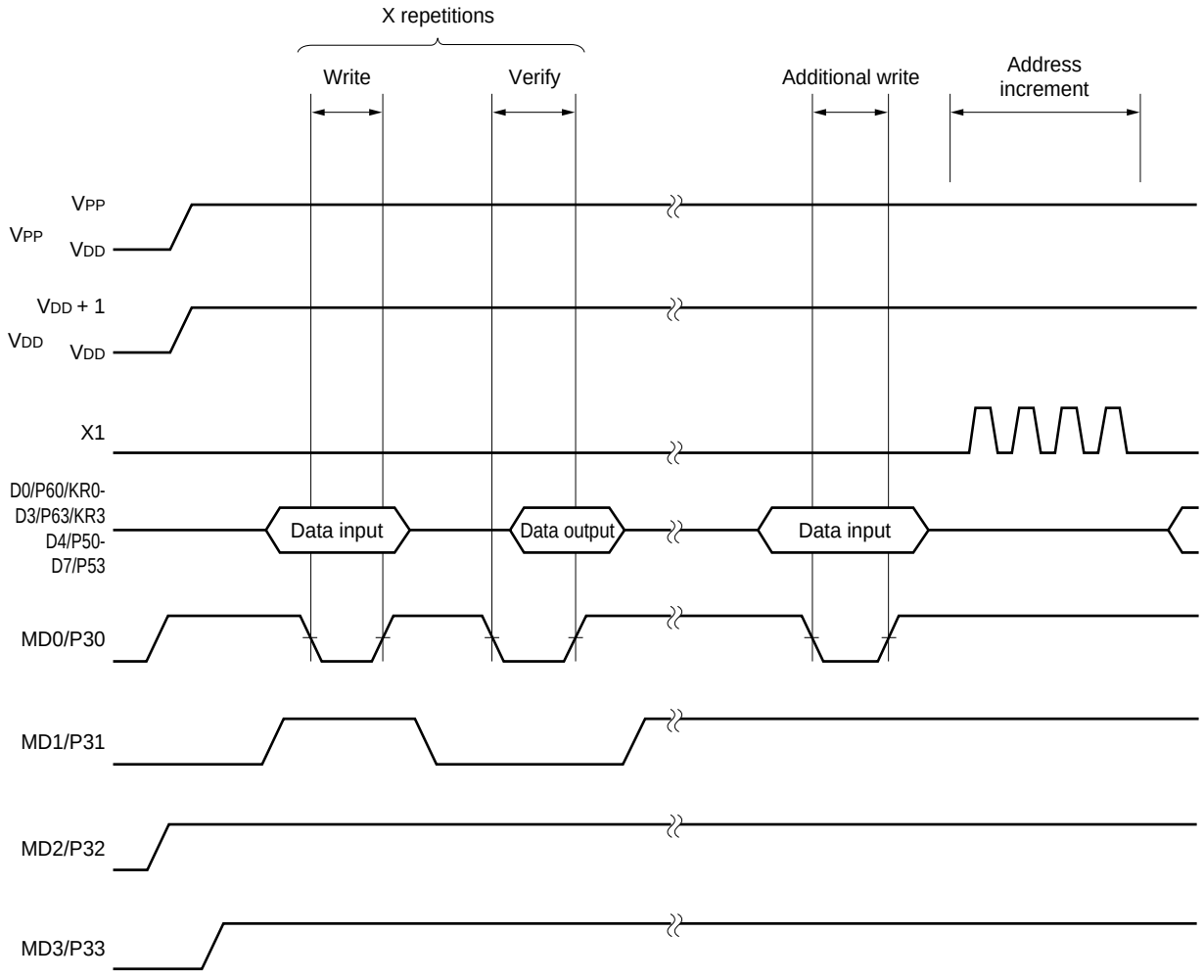
× : L or H

★ **8.2 Program Memory Write Procedure**

High-speed program memory write can be executed via the following steps.

(1) Pull down unused pins to V_{SS} via resistors. Set the X1 pin to low.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Zero-clear mode for program memory addresses.
(5) Apply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Write data using 1-ms write mode.
(7) Verify mode. If write is verified, go to step (8) and if write is not verified, go back to steps (6) and (7).
(8) X [= number of write operations from steps (6) and (7)] × 1 ms additional write
(9) 4 pulse inputs to the X1 pin updates (increments +1) the program memory address.
(10) Repeat steps (6) to (9) until the last address is completed.
(11) Zero-clear mode for program memory addresses.
(12) Apply +5 V to the V_{DD} and V_{PP} pins.
(13) Power supply OFF

The following diagram illustrates steps (2) to (9).

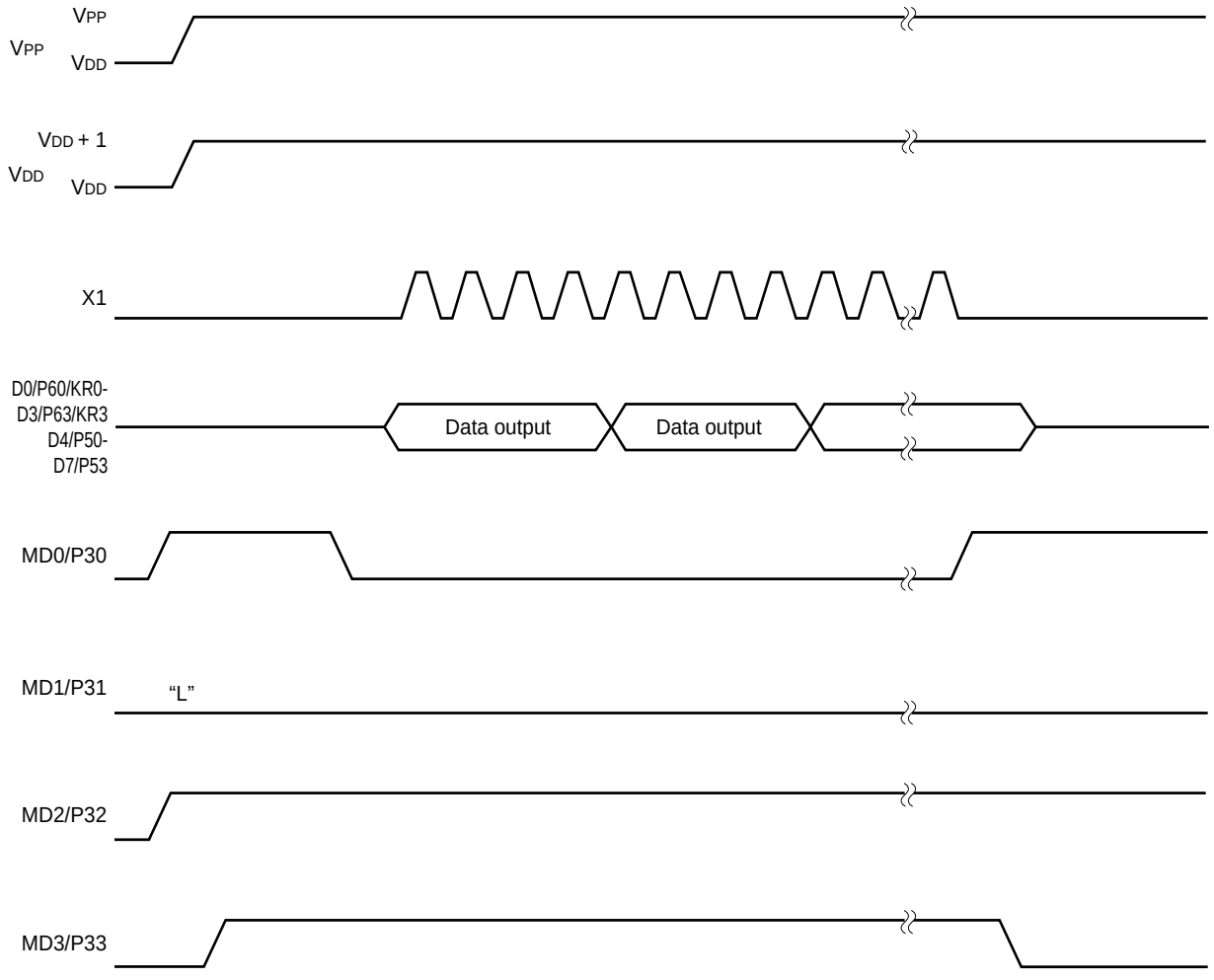


★ 8.3 Program Memory Read Procedure

The μPD75P4308 can read out the program memory contents via the following steps.

(1) Pull down unused pins to V_{SS} via resistors. Set the X1 pin to low.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Zero-clear mode for program memory addresses.
(5) Apply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Verify mode. When a clock pulse is input to the X1 pin, data is output sequentially to one address at a time based on a cycle of four pulse inputs.
(7) Zero-clear mode for program memory addresses.
(8) Apply +5 V to the V_{DD} and V_{PP} pins.
(9) Power supply OFF

The following diagram illustrates steps (2) to (7).



8.4 One-Time PROM Screening

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC. Therefore, NEC recommends the screening process, that is, after the required data is written to the PROM and the PROM is stored under the high-temperature conditions shown below, the PROM should be verified.

Storage temperature	Storage time
125°C	24 hours

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

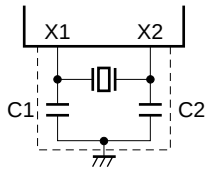
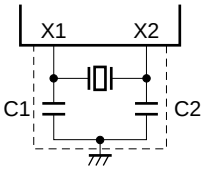
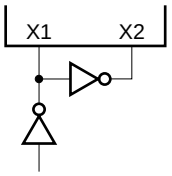
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
PROM supply voltage	V_{PP}		–0.3 to +13.5	V
Input voltage	V_{I1}	Other than port 5	–0.3 to V_{DD} +0.3	V
	V_{I2}	Port 5 (N-ch open-drain)	–0.3 to +14	V
Output voltage	V_O		–0.3 to V_{DD} +0.3	V
High-level output current	I_{OH}	Per pin	–10	mA
		Total for all pins	–30	mA
Low-level output current	I_{OL}	Per pin	30	mA
		Total for all pins	220	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If the absolute maximum ratings of even one of the parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are therefore values which, when exceeded, can cause the product to be damaged. Be sure that these values are never exceeded when using the product.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF

System Clock Oscillation Circuit Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5. V)

Resonator	Recommended constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1.0		6.0Note 3	MHz
		Oscillation stabilization timeNote 2	After V_{DD} has reached MIN. value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		6.0Note 3	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 5.0 V ± 10 %			10	ms
						30	ms
External clock		X1 input frequency (f_X)Note 1		1.0		6.0Note 3	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		83.3		500	ns

Notes 1. The oscillation frequency and X1 input frequency shown above indicate characteristics of the oscillation circuit only. For the instruction execution time, refer to AC Characteristics.

2. The oscillation stabilization time is necessary for oscillation to stabilize after applying V_{DD} or releasing the STOP mode.

3. When the oscillation frequency f_X satisfies 4.19 MHz < f_X ≤ 6.0 MHz at 1.8 V ≤ V_{DD} < 2.7 V, do not set PCC = 0011 as an instruction execution time. If PCC = 0011 is selected, one machine cycle takes less than 0.95 μs, and the MIN. value rating of 0.95 μs is not satisfied.

Caution When using the system clock oscillation circuit, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influence due to wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}. Do not ground to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

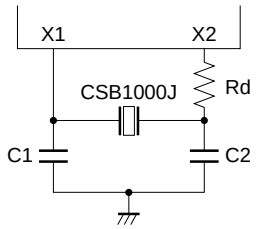
Recommended Oscillation Circuit Constant

Ceramic Resonator (T_A = –40 to +85°C)

Manufacturer	Product name	Frequency (MHz)	Recommended circuit constant (pF)		Oscillation voltage range (V_{DD})		Remark
			C1	C2	MIN.	MAX.	
Murata Manufacturing Co., Ltd.	CSB1000J[Note]	1.0	100	100	2.6	5.5	Rd = 5.6 kΩ
	CSA2.00MG	2.0	30	30	1.8	5.5	
	CST2.00MG		—	—			On-chip capacitor
	CSA3.58MG	3.58	30	30	1.8	5.5	
	CST3.58MGW		—	—			On-chip capacitor
	CSA3.58MGU		30	30	1.8		
	CST3.58MGWU		—	—			On-chip capacitor
	CSA4.00MG	4.0	30	30	2.0	5.5	
	CST4.00MGW		—	—			On-chip capacitor
	CSA4.00MGU		30	30	1.8		
	CST4.00MGWU		—	—			On-chip capacitor
	CSA4.19MG	4.19	30	30	1.9	5.5	
	CST4.19MGW		—	—			On-chip capacitor
	CSA4.19MGU		30	30	1.8		
	CST4.19MGWU		—	—			On-chip capacitor
	CSA6.00MG	6.0	30	30	2.9	5.5	
	CST6.00MGW		—	—			On-chip capacitor
	CSA6.00MGU		30	30	2.0		
	CST6.00MGWU		—	—			On-chip capacitor
Kyocera Corp.	KBR-1000F/Y	1.0	100	100	1.8	5.5	T_A = –20 to +80°C
	KBR-2.0MS	2.0	47	47	2.4	5.5	
	KBR-4.0MSA	4.0	33	33	1.8	5.5	
	KBR-4.0MKS		—	—			On-chip capacitor, T_A = –20 to +80°C
	PBRC4.00A		33	33			T_A = –20 to +80°C
	PBRC4.00B		—	—			On-chip capacitor, T_A = –20 to +80°C
	KBR-4.19MSA	4.19	33	33	1.8	5.5	T_A = –20 to +80°C
	KBR-4.19MSB						
	KBR-4.19MKS		—	—			On-chip capacitor, T_A = –20 to +80°C
	PBRC4.19A		33	33			T_A = –20 to +80°C
	PBRC4.19B		—	—			On-chip capacitor, T_A = –20 to +80°C
	KBR-6.0MSA	6.0	33	33	1.8	5.5	T_A = –20 to +80°C
	KBR-6.0MSB						
	KBR-6.0MKS		—	—			On-chip capacitor, T_A = –20 to +80°C
	PBRC6.00A		33	33			T_A = –20 to +80°C
	PBRC6.00B		—	—			On-chip capacitor, T_A = –20 to +80°C

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

Note When using a CSB1000J (1.0 MHz) of Murata Manufacturing Co., Ltd. as a ceramic resonator, a limiting resistor (Rd = 5.6 kΩ) is necessary (See diagram below). When using any other recommended resistor, it is not necessary.



DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level output current	I_{OL}	Per pin				15	mA
		Total for all pins				150	mA
High-level input voltage	V_{IH1}	Ports 2, 3, 8	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7 V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9 V_{DD}		V_{DD}	V
	V_{IH3}	Port 5 (N-ch open-drain)	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7 V_{DD}		13	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9 V_{DD}		13	V
	V_{IH4}	X1		V_{DD}–0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2, 3, 5, 8	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1 V_{DD}	V
	V_{IL3}	X1		0		0.1	V
High-level output voltage	V_{OH}	$\overline{\text{SCK}}$, SO, Ports 2, 3, 6 to 8 I_{OH} = –1 mA		V_{DD}–0.5			V
Low-level output voltage	V_{OL1}	$\overline{\text{SCK}}$, SO, Ports 2, 3, 5 to 8	I_{OL} = 15 mA, V_{DD} = 5.0 V ± 10 %		0.2	2.0	V
			I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0	N-ch open-drain Pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
High-level input leakage current	I_{LIH1}	V_I = V_{DD}	Pins other than port 5 and X1			3	μA
	I_{LIH2}		X1			20	μA
	I_{LIH3}	V_I = 13 V	Port 5 (N-ch open-drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_I = 0 V	Pins other than port 5 and X1			–3	μA
	I_{LIL2}		X1			–20	μA
★	I_{LIL3}		Port 5 (N-ch open-drain) Other than the input instruction execution time			–3	μA
			Port 5 (N-ch open-drain) At the input instruction execution time			–30	μA
			V_{DD} = 5.0 V		–10	–27	μA
			V_{DD} = 3.0 V		–3	–8	μA

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
High-level output leakage current	I_{LOH1}	$V_O = V_{DD}$	$\overline{SCK}$, SO/SB0, Ports 2, 3, 6 to 8				3	μA
	I_{LOH2}	V_O = 13 V	Port 5 (N-ch open-drain)				20	μA
Low-level output leakage current	I_{LOL}	V_O = 0 V					–3	μA
On-chip pull-up resistor	R_L	V_I = 0 V	Ports 0 to 3, 6 to 8 (except P00 pin)		50	100	200	kΩ
Supply current[Note 1]	I_{DD1}	6.0 MHz crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ± 10 %[Note 2]			2.20	7.00	mA
			V_{DD} = 3.0 V ± 10 %[Note 3]			0.43	1.30	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10 %		0.53	1.60	mA
				V_{DD} = 3.0 V ± 10 %		0.21	0.70	mA
	I_{DD1}	4.19 MHz crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ± 10 %[Note 2]			1.70	5.10	mA
			V_{DD} = 3.0 V ± 10 %[Note 3]			0.35	1.10	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10 %		0.51	1.60	mA
				V_{DD} = 3.0 V ± 10 %		0.19	0.60	mA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ± 10 %			0.05	10.0	μA
			V_{DD} = 3.0 V ± 10 %			0.02	5.00	μA
				T_A = 25°C		0.02	3.00	μA

Notes 1. The current flowing through the on-chip pull-up resistor is not included.

2. When the device operates in high-speed mode with the processor clock control register (PCC) set to 0011.

3. When the device operates in low-speed mode with PCC set to 0000.

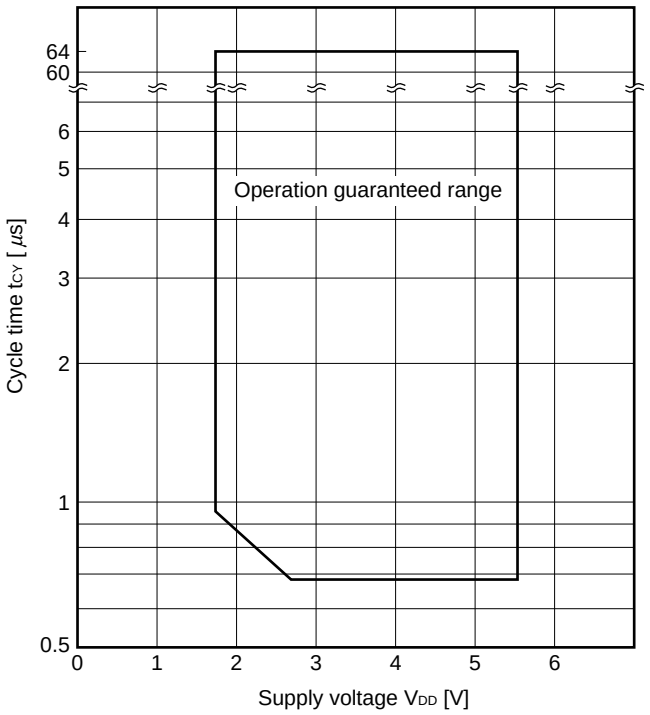
AC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time[Note 1] (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operates with system clock	V_{DD} = 2.7 to 5.5 V	0.67		64	μs
				0.95		64	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1	MHz
				0		275	kHz
TI0, TI1 input high-, low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
★ Interrupt input high-, low-level widths	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 2**			μs
			IM02 = 1	10			
		INT1, 2, 4		10			μs
		KR0-7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator and processor clock control register (PCC).
The figure on the right shows the supply voltage V_{DD} vs. cycle time t_{CY} characteristics when the device operates with the system clock.

2. $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(with system clock)



Serial transfer operation

2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ··· internal clock output): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-, low-level widths	t_{KL1}, t_{KH1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI[Note 1] setup time (to $\overline{SCK}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI[Note 1] hold time (from $\overline{SCK}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$ ↓ → SO[Note 1] output delay time	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF[Note 2]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

★ **Notes 1.** In the 2-wire serial I/O mode, read SB0 instead.

2. R_L and C_L are the load resistance and load capacitance of the SO output line.

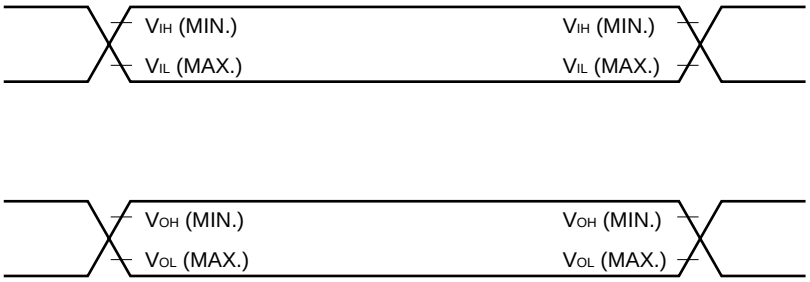
2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ··· external clock input): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-, low-level widths	t_{KL2}, t_{KH2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI[Note 1] setup time (to $\overline{SCK}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI[Note 1] hold time (from $\overline{SCK}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$ ↓ → SO[Note 1] output delay time	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF[Note 2]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns

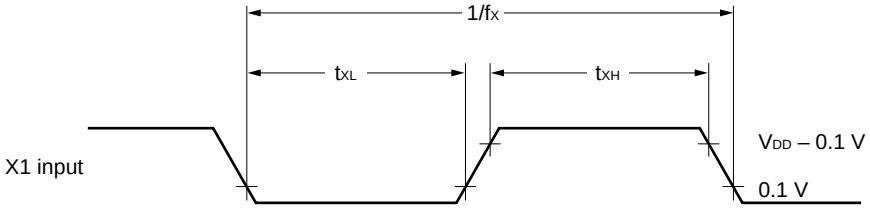
★ **Notes 1.** In the 2-wire serial I/O mode, read SB0 instead.

2. R_L and C_L are the load resistance and load capacitance of the SO output line.

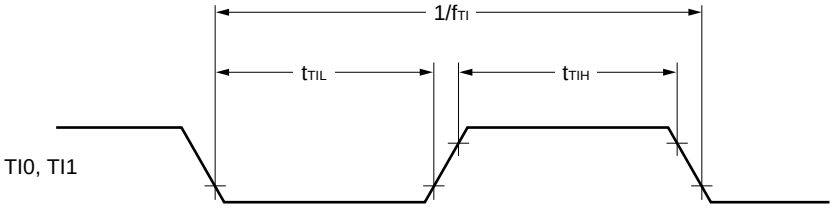
★ **AC timing test points (except X1 input)**



★ **Clock timing**

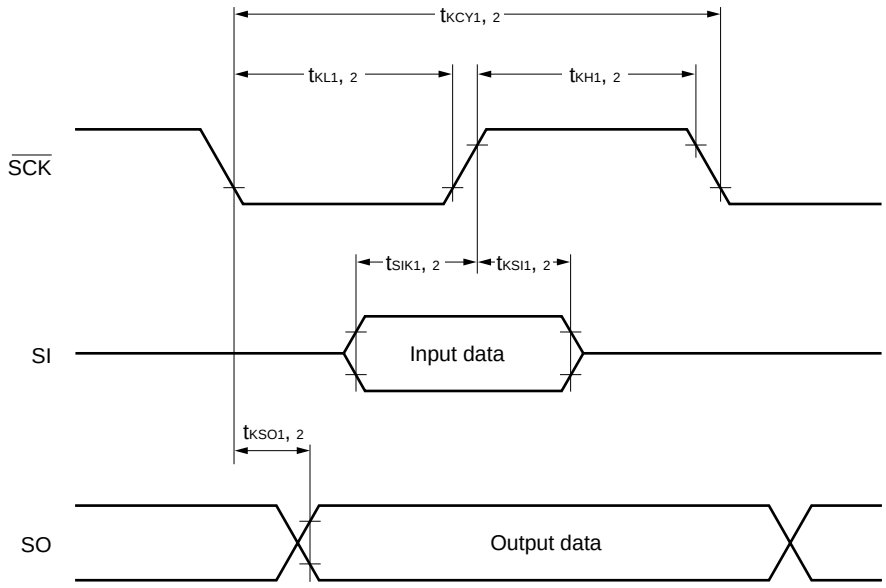


TI0, TI1 timing

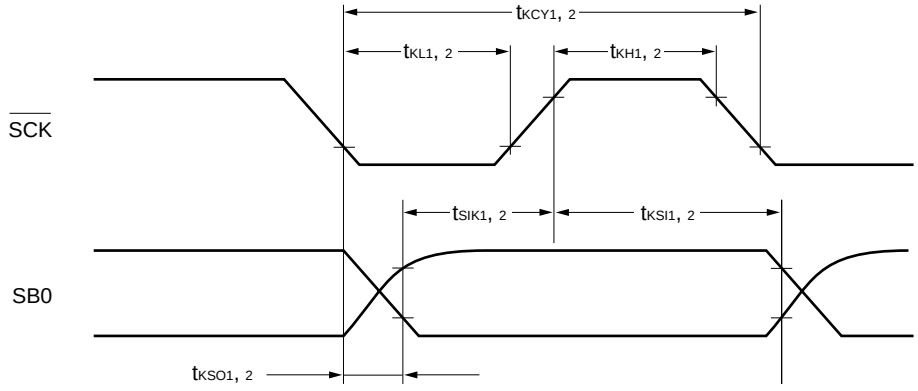


Serial transfer timing

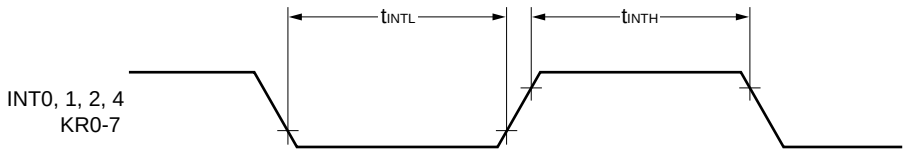
3-wire serial I/O mode



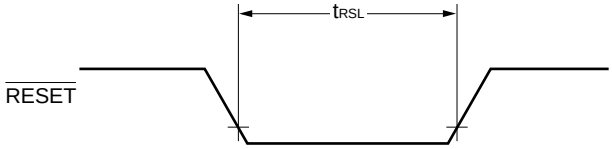
2-wire serial I/O mode



Interrupt input timing



$\overline{\text{RESET}}$ input timing



Data retention characteristics of data memory in STOP mode and at low supply voltage (T_A = –40 to +85°C)

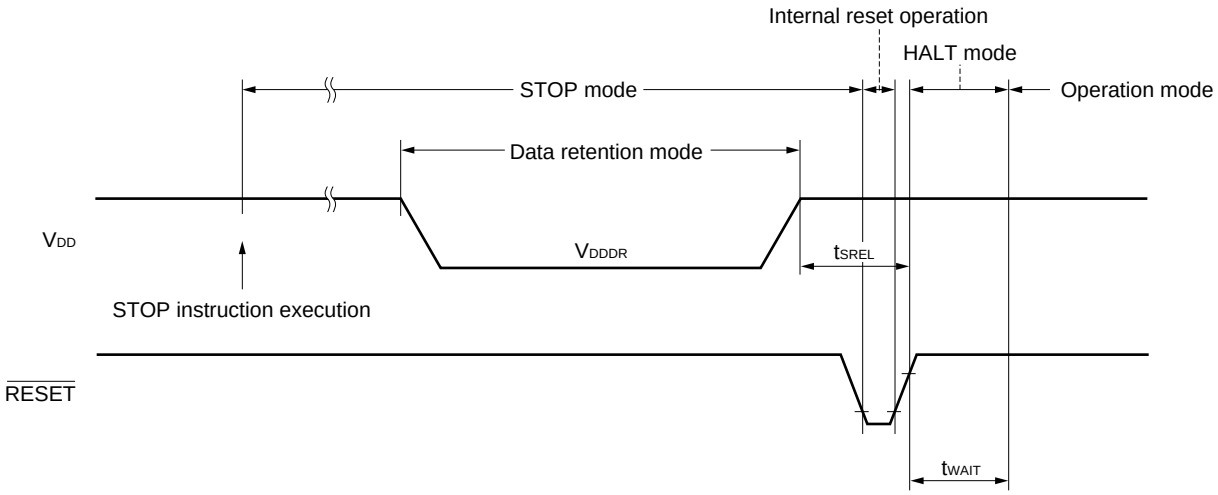
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Released by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Released by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time during which the CPU stops operating to prevent unstable operation when oscillation is started.

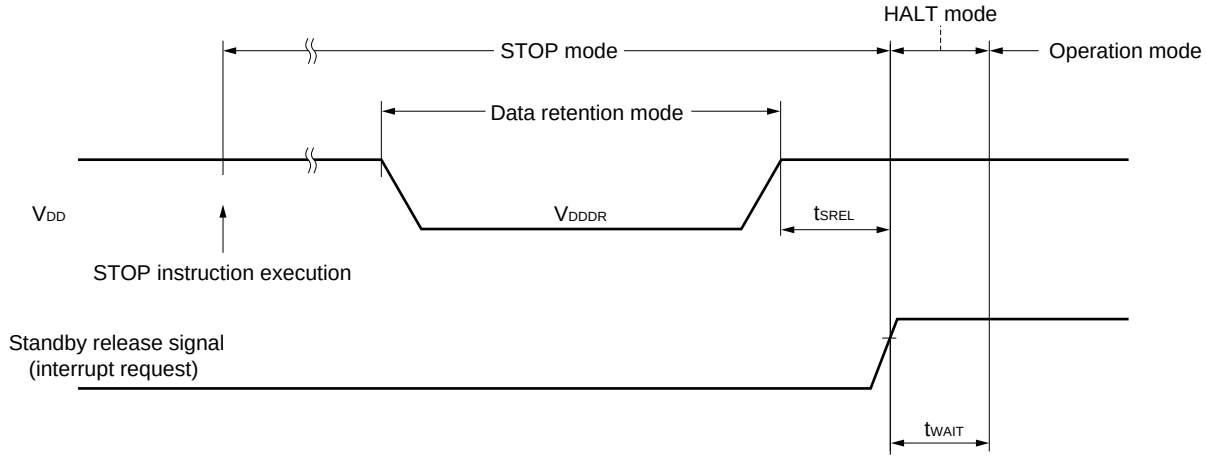
2. Set by the basic interval timer mode register (BTM). (Refer to the table below.)

BTM3	BTM2	BTM1	BTM0	Wait time	
				f_X = 4.19 MHz	f_X = 6.0 MHz
–	0	0	0	$2^{20}/f_X$ (approx. 250 ms)	$2^{20}/f_X$ (approx. 175 ms)
–	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)	$2^{17}/f_X$ (approx. 21.8 ms)
–	1	0	1	$2^{15}/f_X$ (approx. 7.81 ms)	$2^{15}/f_X$ (approx. 5.46 ms)
–	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)	$2^{13}/f_X$ (approx. 1.37 ms)

★ **Data retention timing (when STOP mode released by $\overline{\text{RESET}}$)**



Data retention timing (standby release signal: when STOP mode released by interrupt signal)



★ **DC Programming Characteristics (T_A = 25 ± 5°C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Other than X1, X2	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD}–0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Other than X1, X2	0		0.3 V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-level output voltage	V_{OH}	I_{OH} = – 1 mA	V_{DD}–1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Keep V_{PP} to within +13.5 V, including overshoot.

2. Apply V_{DD} before V_{PP} and turn it off after V_{PP}.

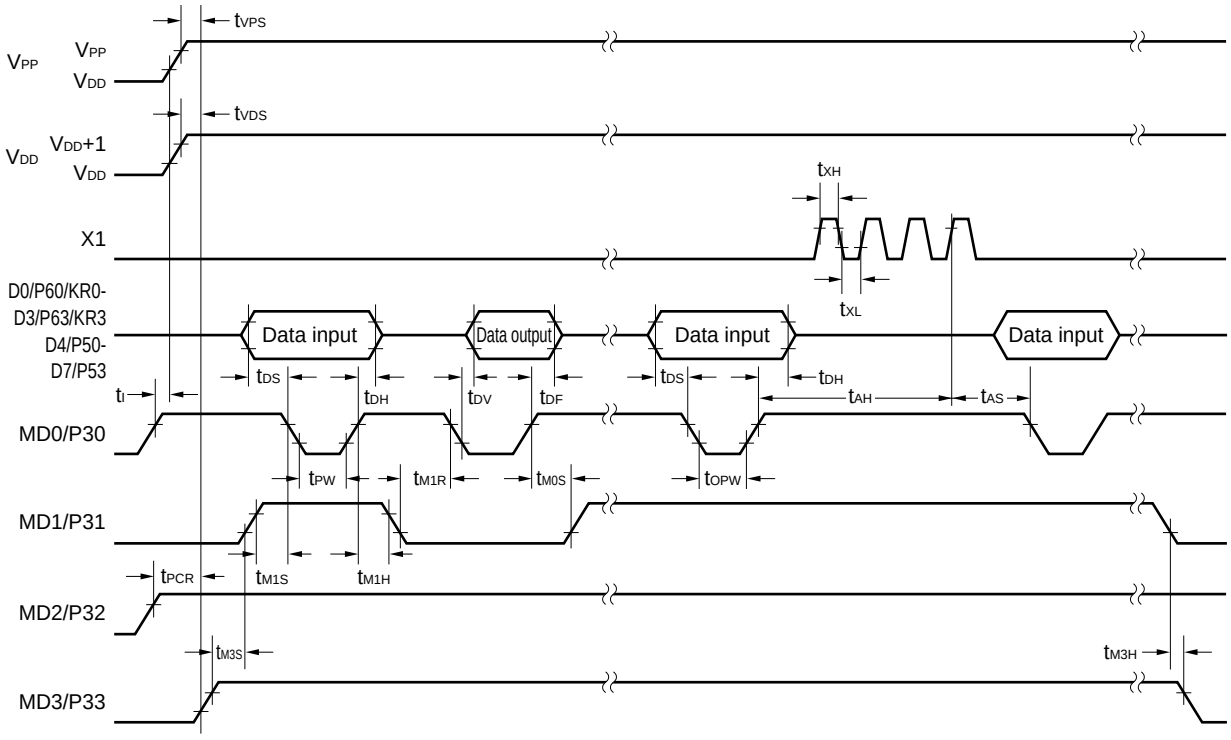
★ **AC Programming Characteristics (T_A = 25 ± 5°C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)**

Parameter	Symbol	**Note 1**	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time[Note 2] (to MD0 ↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0 ↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0 ↓)	t_{DS}	t_{DS}		2			μs
Address hold time[Note 2] (from MD0 ↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0 ↑)	t_{DH}	t_{DH}		2			μs
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3 ↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3 ↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1 ↑)	t_{M0S}	t_{CES}		2			μs
MD0 ↓ → data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0 ↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (from MD0 ↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
X1 input high-, low-level widths	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	f_X	—				4.19	MHz
Initial mode set time	t_I	—		2			μs
MD3 setup time (to MD1 ↑)	t_{M3S}	—		2			μs
MD3 hold time (from MD1 ↓)	t_{M3H}	—		2			μs
MD3 setup time (to MD0 ↓)	t_{M3SR}	—	When program memory is read	2			μs
Address[Note 2] → data output delay time	t_{DAD}	t_{ACC}	When program memory is read			2	μs
Address[Note 2] → data output hold time	t_{HAD}	t_{OH}	When program memory is read	0		130	ns
MD3 hold time (from MD0 ↑)	t_{M3HR}	—	When program memory is read	2			μs
MD3 ↓ → data output float delay time	t_{DFR}	—	When program memory is read			2	μs

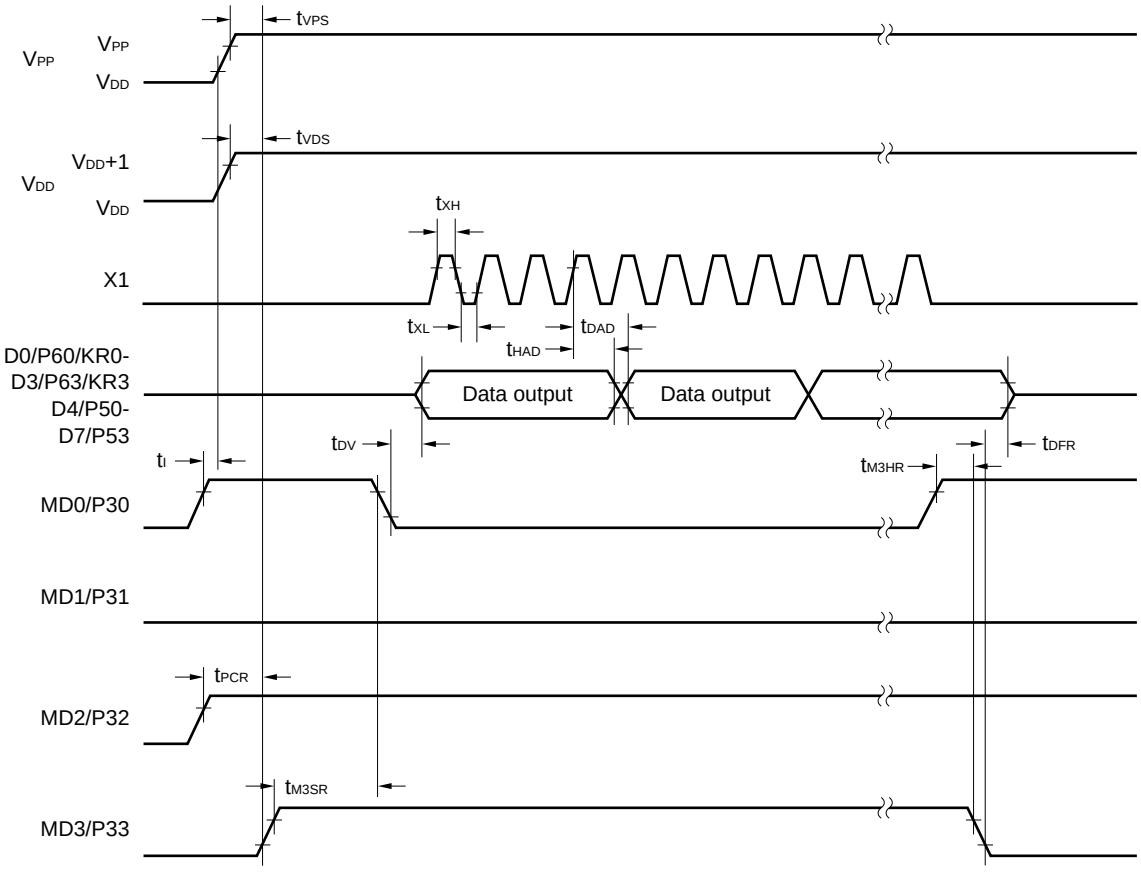
Notes 1. Symbol of corresponding μPD27C256A

2. The internal address signal is incremented by one at the rising edge of the fourth X1 input and is not connected to a pin.

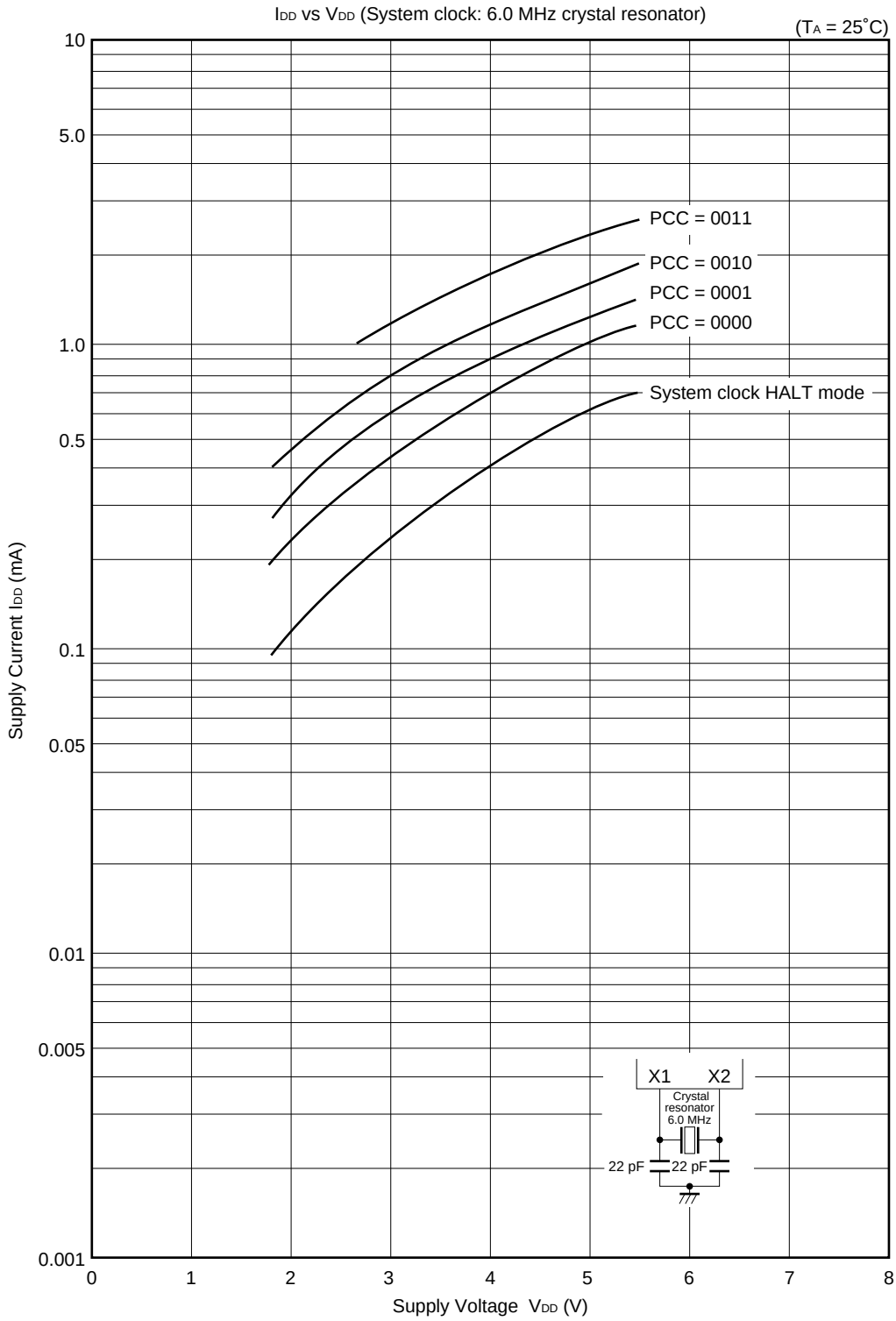
★ **Program Memory Write Timing**

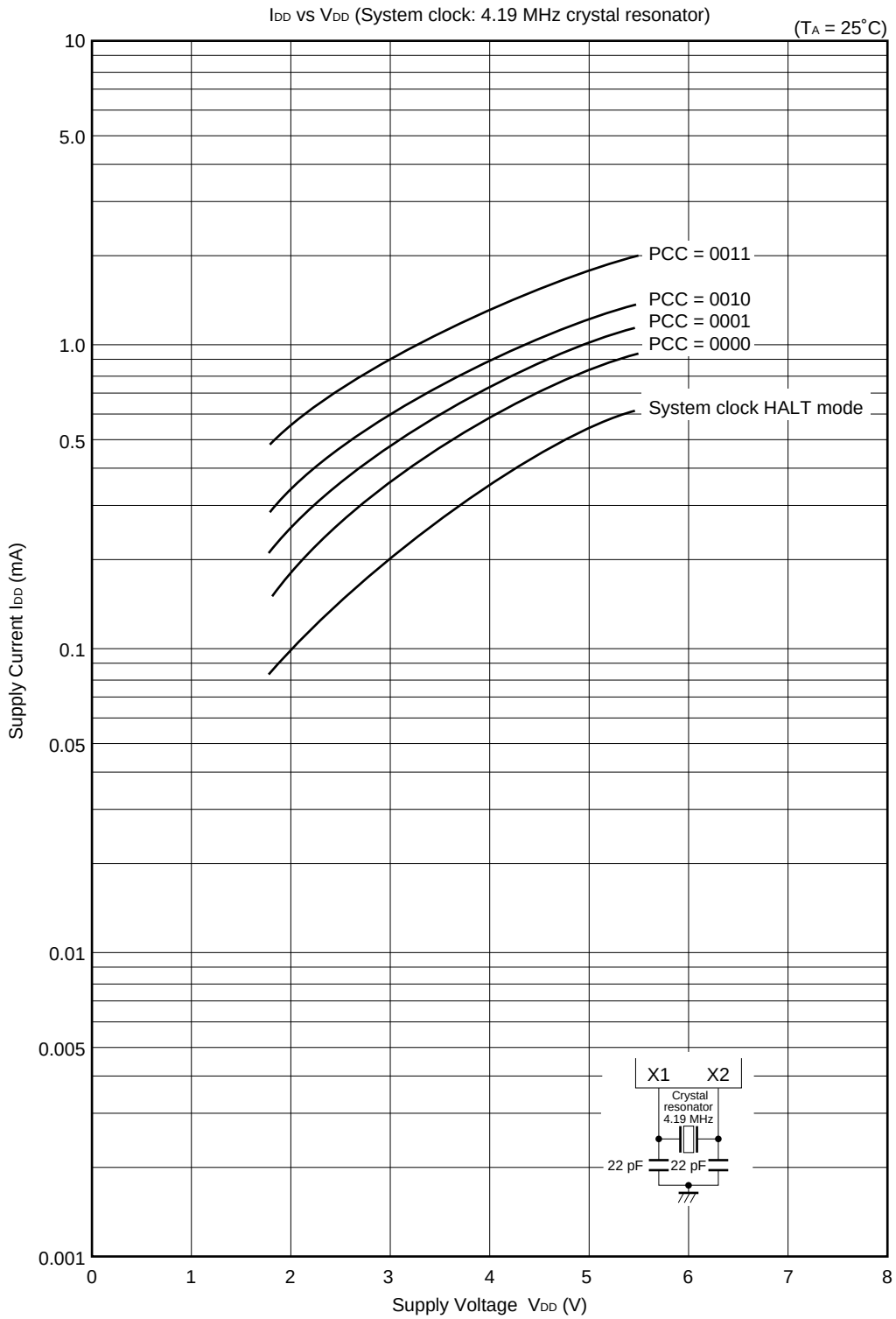


★ **Program Memory Read Timing**



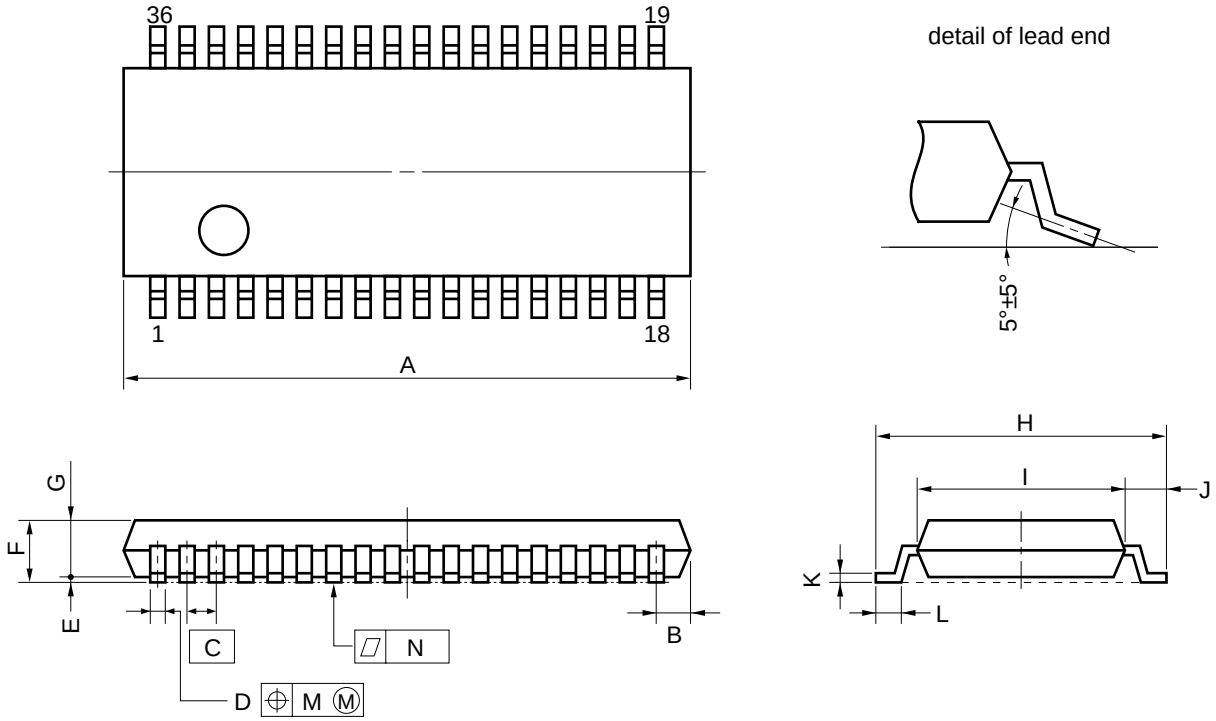
★ 10. CHARACTERISTIC CURVES (FOR REFERENCE ONLY)




IDD vs VDD (System clock: 4.19 MHz crystal resonator)
(TA = 25°C)
10
5.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
Supply Current IDD (mA)
0
1
2
3
4
5
6
7
8
Supply Voltage VDD (V)
PCC = 0011
PCC = 0010
PCC = 0001
PCC = 0000
System clock HALT mode
X1
X2
Crystal resonator 4.19 MHz
22 pF
22 pF

11. PACKAGE DRAWINGS

36 PIN PLASTIC SHRINK SOP (300 mil)



P36GM-80-300B-3

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.97 MAX.	0.039 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.35^{+0.10}_{-0.05}$	$0.014^{+0.004}_{-0.003}$
E	0.125±0.075	0.005±0.003
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.10	0.004
N	0.10	0.004

12. RECOMMENDED SOLDERING CONDITIONS

Solder the μPD75P4308 under the following recommended conditions.

For the details on the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For the soldering methods and conditions other than those recommended, consult NEC.

Table 12-1. Soldering Conditions of Surface Mount Type

μPD75P4308GS: 36-pin plastic shrink SOP (300 mil, 0.8-mm pitch)

Soldering method	Soldering conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or below, Number of flow processes: 1 Preheating temperature: 120°C or below (package surface temperature) Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	WS60-107-1
Pin partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	–

Note The number of days for storage after the dry pack has been opened. Storage conditions are 25°C and 65% RH max.

Caution Do not use two or more soldering methods in combination (except the pin partial heating method).

APPENDIX A. COMPARISON OF μPD750004, 754304, AND 75P4308 FUNCTIONS

(1/2)

Item		μPD750004	μPD754304	μPD75P4308
Program memory		Mask ROM 0000H-0FFFH (4096 × 8 bits)	Mask ROM 0000H-0FFFH (4096 × 8 bits)	One-time PROM 0000H-1FFFH (8192 × 8 bits)
Data memory		000H-1FFH (512 × 4 bits)	000H-0FFH (256 × 4 bits)	
CPU		75XL CPU		
Instruction execution time	When main system clock is selected	• 0.95, 1.91, 3.81, 15.3 μs (@ 4.19 MHz) • 0.67, 1.33, 2.67, 10.7 μs (@ 6.0 MHz)		
	When subsystem clock is selected	122 μs (@ 32.768 kHz)	No subsystem clock	
I/O ports	CMOS input	8 (connections of on-chip pull-up resistors are software-specifiable: 7)		
	CMOS I/O	18 (connections of on-chip pull-up resistors are software-specifiable)		
	N-ch open-drain I/O (13-V withstand)	8 (on-chip pull-up resistors are specified by mask option)	4 (on-chip pull-up resistors are specified by mask option)	4 (No mask option)
	Total	34	30 (No port 4 pin)	
Timers		4 channels • Basic interval timer/ watchdog timer • 8-bit timer/event counter • 8-bit timer • Watch timer	3 channels • Basic interval timer/watchdog timer • 8-bit timer/event counter 0 (fx/2^2 added) • 8-bit timer/event counter 1 (TI1, fx/2^2 added) (Can be used as a 16-bit timer/event counter)	
Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (main system clock: @ 4.19 MHz) • Φ, 750, 375, 93.8 kHz (main system clock: @ 6.0 MHz)		
BUZ output		Yes	No	
Serial interface		Can support three modes • 3-wire serial I/O mode ...MSB/LSB-first switchable • 2-wire serial I/O mode • SBI mode	Can support two modes • 3-wire serial I/O mode...MSB/LSB-first switchable • 2-wire serial I/O mode	
Watch mode register (WM)		Yes	No	
System clock control register (SCC)				
Sub-oscillator control register (SOS)				

(2/2)

Item	μPD750004	μPD754304	μPD75P4308
Memory bank select register (MBS)	Selectable from memory banks 0 and 1	Fixed at memory bank 0	
Stack bank select register (SBS)			
Timer/event counter mode register (TM0, TM1)	Bits 0, 1, and 7 are fixed at 0	–	
Vectored interrupts	External: 3, Internal: 4		
Test inputs	External: 1, Internal: 1	External: 1	
Test enable flag (IEW)	Yes	No	
Test request flag (IRQW)			
Power supply voltage	V_{DD} = 2.2 to 5.5 V	V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature	T_A = –40 to +85°C		
Package	• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm)	• 36-pin plastic shrink SOP (300 mil, 0.8-mm pitch)	

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD75P4308. In the 75XL series, the common relocatable assembler is used together with the device file of each model.

RA75X relocatable assembler	Host machine		Part No. (name)
	OS	Supply medium	
	PC-9800 Series	MS-DOS™ (Ver.3.30 to Ver.6.2[Note])	3.5" 2HD	μS5A13RA75X
			5" 2HD	μS5A10RA75X
	IBM PC/AT™ or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13RA75X
			5" 2HC	μS7B10RA75X

Device file	Host machine		Part No. (name)
	OS	Supply medium	
	PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note])	3.5" 2HD	μS5A13DF754304
			5" 2HD	μS5A10DF754304
	IBM PC/AT or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13DF754304
			5" 2HC	μS7B10DF754304

Note Ver. 5.00 and above include a task swapping function, but this software is not able to use that function.

Remark Operations of the assembler and the device file are guaranteed only when using the host machine and OS described above.

PROM Write Tools

<table>
<tr><td rowspan="2">Hardware</td><td>PG-1500</td><td colspan="4">A stand-alone system can be configured of a single-chip microcontroller with on-chip PROM when connected to an auxiliary board (attached) and a programmer adapter (separately sold). Alternatively, a PROM programmer can be operated on a host machine for programming. In addition, typical PROMs in capacities ranging from 256 K to 4 Mbits can be programmed.</td></tr>
<tr><td>PA-75P4308GS</td><td colspan="4">This is a PROM programmer adapter for the μPD75P4308GS. It can be used when connected to a PG-1500.</td></tr>
<tr><td rowspan="4">Software</td><td rowspan="4">PG-1500 controller</td><td colspan="4">Establishes serial and parallel connections between the PG-1500 and a host machine for host-machine control of the PG-1500.</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Supply medium</td><td rowspan="2">Part No. (name)</td></tr>
<tr></tr>
<tr><td>PC-9800 Series</td><td>MS-DOS (Ver.3.30 to Ver.6.2[Note])</td><td>3.5" 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td>5" 2HD</td><td>μS5A10PG1500</td></tr>
<tr><td rowspan="2">IBM PC/AT or compatible</td><td rowspan="2">Refer to OS for IBM PCs</td><td>3.5" 2HD</td><td>μS7B13PG1500</td></tr>
<tr><td>5" 2HC</td><td>μS7B10PG1500</td></tr>
</table>

Note Ver. 5.00 and above include a task swapping function, but this software is not able to use that function.

Remark Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

Debugging Tools

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the μPD75P4308. Various system configurations using these in-circuit emulators are listed below.

Hardware	IE-75000-R[Note 1]	The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems that use 75X or 75XL Series products. For development of the μPD754304 subseries, the IE-75000-R is used with a separately sold emulation board (IE-75300-R-EM) and emulation probe (EP-754304GS-R). These products can be applied for highly efficient debugging when connected to a host machine and PROM programmer. The IE-75000-R can include a connected emulation board (IE-75000-R-EM).			
	IE-75001-R	The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems that use 75X or 75XL Series products. The IE-75001-R is used with a separately sold emulation board (IE-75300-R-EM) and emulation probe (EP-754304GS-R). These products can be applied for highly efficient debugging when connected to a host machine and PROM programmer.			
	IE-75300-R-EM	This is an emulation board for evaluating application systems that use the μPD754304 subseries. It is used in combination with the IE-75000-R or IE-75001-R in-circuit emulator.			
	EP-754304GS-R	This is an emulation probe for the μPD75P4308.			
	EV-9500GS-36	When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM. It includes a flexible board (EV-9500GS-36) to facilitate connections with various target systems.			
Software	IE control program	This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232-C or Centronics interface.			
		Host machine			Part No. (name)
			OS	Supply medium	
		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note 2])	3.5" 2HD	μS5A13IE75X
				5" 2HD	μS5A10IE75X
		IBM PC/AT or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13IE75X
				5" 2HC	μS7B10IE75X

Notes 1. This is a service part provided for maintenance purpose only.

2. Ver. 5.00 and above include a task swapping function, but this software is not able to use that function.

Remarks 1. Operation of the IE control program is guaranteed only when using the host machine and OS described above.

2. The μPD754302, 754304, and 75P4308 are commonly referred to as the μPD754304 subseries.

OS for IBM PCs

The following operating systems for the IBM PC are supported.

OS	Version
PC DOS™	Ver.5.02 to Ver.6.3 J6.1/V to J6.3/V
MS-DOS	Ver.5.0 to Ver.6.22 5.0/V to 6.2/V
IBM DOS™	J5.02/V

Caution Ver 5.0 and above include a task swapping function, but this software is not able to use that function.

★ APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions.
However, preliminary versions are not marked as such.

Documents Related to Device

Document Name	Document Number	
	Japanese	English
μPD754302, 754304 Data Sheet	U10797J	U10797E
μPD75P4308 Data Sheet	U10909J	U10909E (this document)
μPD754304 User's Manual	U10123J	U10123E
μPD754304 Instruction Table	IEM-5605	—
75XL Series Selection Guide	U10453J	U10453E

Documents Related to Development Tools

Document Name			Document Number	
			Japanese	English
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846	EEU-1416
	IE-75300-R-EM User's Manual		U11354J	U11354E
	EP-754304GS-R User's Manual		U10677J	U10677E
	PG-1500 User's Manual		EEU-651	EEU-1335
Software	RA75X Assembler Package	Operation	EEU-731	EEU-1346
	User's Manual	Language	EEU-730	EEU-1363
	PG-1500 Controller User's Manual	PC9800 Series (MS-DOS) base	EEU-704	EEU-1291
		IBM PC/AT Series (PC DOS) base	EEU-5008	U10540E

Other Related Documents

Document Name	Document Number	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcomputer-Related Product Guide –Third Party Products–	U11416J	—

Caution The related documents listed above are subject to change without notice. Be sure to use the latest documents for designing, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 800-729-9288

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Fax: 0211-65 03 490

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Fax: 01908-670-290

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NEC Electronics Taiwan Ltd.
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