NEC
NEC Electronics Inc.

μPD75316 Family (μPD75304/306/308/312/316/P308/P316A) 4-Bit, Single-Chip Microcontrollers With LCD Controller/Driver

June 1994

Description

The μPD75316 family of high-performance 4-bit single chip CMOS microcontrollers includes the following devices:

μPD75304	μPD75306	μPD75308
μPD75312	μPD75316	μPD75P308
μPD75P316A		

The 75316 family features an on-chip LCD controller and driver with up to 16K bytes of ROM and 1024 nibbles of RAM. The instruction set operates on 1-, 4-, and 8-bit data.

Timing is generated by two oscillators. The main oscillator normally drives the CPU and most peripherals. The 32.768-kHz subsystem oscillator provides time keeping when the main oscillator is turned off. Since CMOS power dissipation is proportional to clock rate, the 75316 family provides a software selectable instruction cycle time from 0.95 μsec to 122 μsec. The STOP and HALT modes turn off parts of the microcontroller for additional power savings. The data retention mode retains RAM contents down to 2.0 V.

Features

- LCD controller/driver for up to 128 segments
  - 32 segment lines
  - Four common lines
  - Static, 1/2 or 1/3 bias
  - LCD resistor ladder available on ROM versions
- Subsystem oscillator allows watch timer and LCD to operate in power-down modes
- 8-bit synchronized serial interface
  - Full-duplex, three-wire mode
  - Half-duplex, two-wire mode
  - NEC serial bus interface (SBI) mode
- Timers: three channels
  - 8-bit timer/event counter
  - 8-bit interval timer
  - Watch (clock) timer: 0.5-sec interrupt request
- 32 I/O lines
  - Eight input-only lines
  - 16 bidirectional I/O lines
  - Eight 10-volt n-channel, open-drain I/O lines
  - Direct LED drive from 12 lines
  - 31 software selectable pullup resistors
  - Eight mask selectable resistors (ROM versions only)
- Bit sequential buffer
  - 16-bit, bit addressable memory
- Standard 75X instruction set
  - 4-bit arithmetic and logic
  - 4- and 8-bit transfer instructions
- Minimum instruction execution times
  - 0.95, 1.91, and 15.3 μs using 4.19-MHz main system clock
  - 122 μs selectable using 32.768-kHz subsystem clock
- Eight 4-bit registers
  - Usable as four 8-bit registers
- Memory-mapped on-chip peripherals
- Vectored interrupt controller
  - 12 edge detect inputs
  - Five vectored interrupts
- CMOS power saving and battery operation
  - Normal operating mode; 2.5 mA typical at 5 V
  - HALT mode; 0.5 mA typical
  - STOP mode; 0.1 μA typical
  - Data retention down to 2 volts
- Operating voltage ranges
  - ROM and 75P316A OTP/EPROM version; V_{DD} from 2.7 to 6.0 V
  - 75P308 (standard OTP/EPROM); V_{DD} = 5 V ±5%

Internal High-Capacity ROM and RAM

	75304	75306	75308	75312	75316	75P308	75P316A
ROM	4K bytes	6K bytes	8K bytes	12K bytes	16K bytes	—	—
PROM	—	—	—	—	—	8K bytes	16K bytes
RAM	512 nibbles	512 nibbles	512 nibbles	512 nibbles	512 nibbles	512 nibbles	1024 nibbles

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Ordering Information

Part Number	Quality Grade	ROM	Package Type	Package Drawing
μPD75304GF-xxx-3B9	Standard	Mask	80-pin plastic QFP	P80GF-80-3B9-1
μPD75304GF(A)-xxx-3B9	Special			
μPD75306GF-xxx-3B9	Standard			
μPD75306GF(A)-xxx-3B9	Special			
μPD75308GF-xxx-3B9	Standard			
μPD75308GF(A)-xxx-3B9	Special			
μPD75312GF-xxx-3B9	Standard			
μPD75312GF(A)-xxx-3B9	Special			
μPD75316GF-xxx-3B9	Standard			
μPD75316GF(A)-xxx-3B9	Special			
μPD75P308GF	Standard	OTP	80-pin plastic QFP	P80GF-80-3B9-1
μPD75P308K	Standard	EPROM	80-pin ceramic LCC with window	X80KW-80A
μPD75P316GF (Note 3)	Standard	OTP	80-pin plastic QFP	P80GF-80-3B9-1
μPD75P316AGF	Standard	Low-voltage OTP	80-pin plastic QFP QFP	P80GF-80-3B9-1
μPD75P316AK	Standard	Low-voltage EPROM	80-pin ceramic LCC with window	X80KW-80A

Notes:

(1) Engineering samples are supplied in an 80-pin ceramic QFP.

(2) xxx indicates ROM code.

(3) This part has been superseded by the μPD75P316AGF

Device Grades

The devices in the μPD75316 family are available in standard or special quality grades. Special grade devices have the symbol (A) embedded in the part number; a μPD75308GF is a standard grade device and a μPD75308GF(A) is a special grade device. The selection of the correct grade depends upon the application.

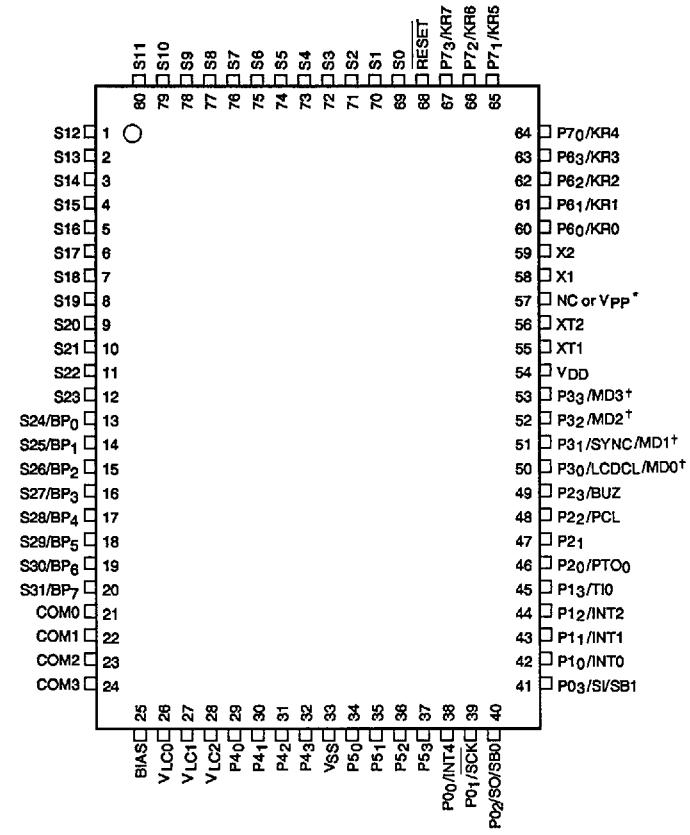
Differences Between Special and Standard Quality Grades

	Special	Standard
Applications	Automotive and transportation equipment, traffic control systems, anti-disaster systems, anti-crime systems	Computers, office equipment, communications, test and measurement, machine tools, industrial robots, audio and visual equipment, other consumer products.
LED direct drive	No	Yes
Absolute maximum ratings	Differences in low-level and high-level output current; refer to Electrical Specifications.	
DC characteristics	Differences in low-voltage outputs; refer to Electrical Specifications.	

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Pin Configurations

80-Pin Plastic QFP or Ceramic LCC



* Pin 57 is VPP in the programmable package. Connect this pin to V DD in the μPD75P308/P316/P316A.

† MD0-MD3 are used as the programming mode selection pins on the μPD75P308/P316/P316A during EPROM and OTP programming and verification.

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Pin Identification

Symbol	Function
BIAS	LCD power bias output
BP_0/S24 BP_1/S25 BP_2/S26 BP_3/S27 BP_4/S28 BP_5/S29 BP_6/S30 BP_7/S31	1-bit output ports BP_0 - BP_7; LCD segments S24-S31
COM0-COM3	LCD common output 0-3
NC/V_{PP}	No connection (programming pin for μPD75P308A)
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/$\overline{SCK}$	Port 0 input; serial clock
$P0_2$/SO/SB0	Port 0 input; serial out; serial bus interface 0
$P0_3$/SI/SB1	Port 0 input; serial in; serial bus interface 1
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/TI0	Port 1 input; timer 0 input
$P2_0$/PTO_0	Port 2 I/O; timer/event counter output
$P2_1$	Port 2 I/O
$P2_2$/PCL	Port 2 I/O; programmable clock output
$P2_3$/BUZ	Port 2 I/O; buzzer output
$P3_0$/LCDCL/MD0	Port 3 I/O; LCD clock output ; programming mode select 0 (μPD75P308A)
$P3_1$/SYNC/MD1	Port 3 I/O; LCD SYNC output; programming mode select 1 (μPD75P308A)
$P3_2$/MD2	Port 3 I/O; programming mode select 2 (μPD75P308A)
$P3_3$/MD3	Port 3 I/O; programming mode select 3 (μPD75P308A)
$P4_0$ - $P4_3$	Port 4 I/O
$P5_0$ - $P5_3$	Port 5 I/O
$P6_0$/KR0	Port 6 I/O; key scan input 0
$P6_1$/KR1	Port 6 I/O; key scan input 1
$P6_2$/KR2	Port 6 I/O; key scan input 2
$P6_3$/KR3	Port 6 I/O; key scan input 3
$P7_0$/KR4	Port 7 I/O; key scan input 4
$P7_1$/KR5	Port 7 I/O; key scan input 5
$P7_2$/KR6	Port 7 I/O; key scan input 6
$P7_3$/KR7	Port 7 I/O; key scan input 7
$\overline{RESET}$	Reset input
S0 - S23	LCD segment output
V_{LC0}	LCD drive level 0
V_{LC1}	LCD drive level 1
V_{LC2}	LCD drive level 2
X1, X2	Main clock inputs
XT1, XT2	Subsystem clock inputs
V_{DD}	Positive power supply
V_{SS}	Ground

PIN FUNCTIONS

$P0_0$/INT4, $P0_1$/$\overline{SCK}$, $P0_2$/SO/SB0, $P0_3$/SI/SB1. These pins can be used as 4-bit input port 0. $P0_0$ can also be used for vectored interrupt 4, which interrupts on either the leading edge or the trailing edge of the signal. $P0_1$ - $P0_3$ may also be used for the serial interface in the SBI or the 2- or 3-wire modes.

SI is the serial input, SO is the serial output, and $\overline{SCK}$ is the serial clock. SB0 and SB1 are the NEC serial bus interface pins 0 and 1. Reset causes these pins to default to the port 0 input mode.

$P1_0$/INT0, $P1_1$/INT1, $P1_2$/INT2, $P1_3$/TI0. These pins can be used as 4-bit input port 1. $P1_0$ and $P1_1$ can also be used for edge-triggered interrupts INT0 and INT1. $P1_2$ can be used for INT2, which is also an edge-triggered input, but one that generates an Interrupt request but does not cause a vectored interrupt.

$P1_3$ can be used as an input clock to the timer/event counter to count external events. Reset causes all PI pins to default to the port 1 input mode.

$P2_0$/PTO_0, $P2_1$, $P2_2$/PCL, $P2_3$/BUZ. These pins can be used as 4-bit I/O port 2. When used as an output, the data is latched. When used as an input port, the port outputs are three-state. $P2_0$ can also be used as PTO_0, the output of the timer/event counter flip-flop (TOUT); $P2_2$ can be used as the output (PCL) for the clock generator; and $P2_3$ can be used to output square waves for a buzzer. Reset causes these pins to default to the port 2 input mode.

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$P3_0$/LCDCL/MD0, $P3_1$/SYNC/MD1, $P3_2$/MD2, $P3_3$/MD3. These pins are used for I/O port 3. Each bit in this port can be independently programmed to be either an input or an output. This port has latched outputs, and can directly drive LEDs. $P3_0$ and $P3_1$ can also be used respectively as LCD clock and LCD sync outputs.

$P3_0$ - $P3_3$ are used as the programming mode select pins for the μPD75P308/P316A during EPROM/OTP programming and verification. A reset signal causes this port to default to the input mode.

$P4_0$ - $P4_3$, $P5_0$ - $P5_3$. Port 4 and Port 5 are identical 4-bit I/O ports, which can be combined to function as a single 8-bit port. Latched outputs will directly drive LEDs. Outputs are n-channel open drain, and can withstand up to 10 volts; pullup resistor mask options are available for these ports. A reset signal causes these ports to default to the input mode at a high impedance or to a high level if a pullup resistor is present.

$P6_0$/KR0, $P6_1$/KR1, $P6_2$/KR2, $P6_3$/KR3 $P7_0$/KR4, $P7_1$/KR5, $P7_2$/KR6, $P7_3$/KR7. Ports 6 and 7 are 4-bit I/O ports, which can be combined to function as a single 8-bit port. Outputs are latched. Each pin of port 6 can be independently programmed to be either an input or an output; port 7 can be programmed to be either all inputs or all outputs. Alternately, these pins may be used to detect the falling edge of inputs KR0 - KR3 (port 6) and KR4 - KR7 (port 7). A reset signal causes these ports to default to the input mode.

S0 - S23. These are the LCD segment drivers.

COM0 - COM3. These are the LCD common input drivers.

BP_0/S24 - BP_7/S31. These can be used either as eight 1-bit ports or as additional LCD segment drivers. When used as segment outputs they are selectable in 4-bit increments.

V_{LC0} - V_{LC2}. These pins are used to set the drive levels for the LCD. If the internal resistor ladder mask option is selected (on the μPD7530x/31x only), these pins are outputs; if the internal resistor ladder is not selected, these pins are inputs to which an external resistor network must be connected.

BIAS. This output is used in conjunction with the V_{LC0} - V_{LC2} pins to set the LCD contrast level.

NC/V_{PP}. This pin may be left unconnected when using the μPD7530x/31x. For the μPD75P308/P316A, the pin is used as the programming voltage input during the EPROM write/verify cycles. When the devices are not being programmed, this pin should be connected to V_{DD}. It must be connected to V_{DD} if the same circuit board is to be used for both programmable and non-programmable devices.

X1, X2. These pins are the main system clock inputs. The input can be from a ceramic resonator or a crystal; an external logic signal may also be used by applying it to X1 and its inverse to X2.

XT1, XT2. These pins are the subsystem clock inputs. The input can be from a ceramic resonator or a crystal; an external logic signal may also be used by applying it to XT1 with XT2 left open.

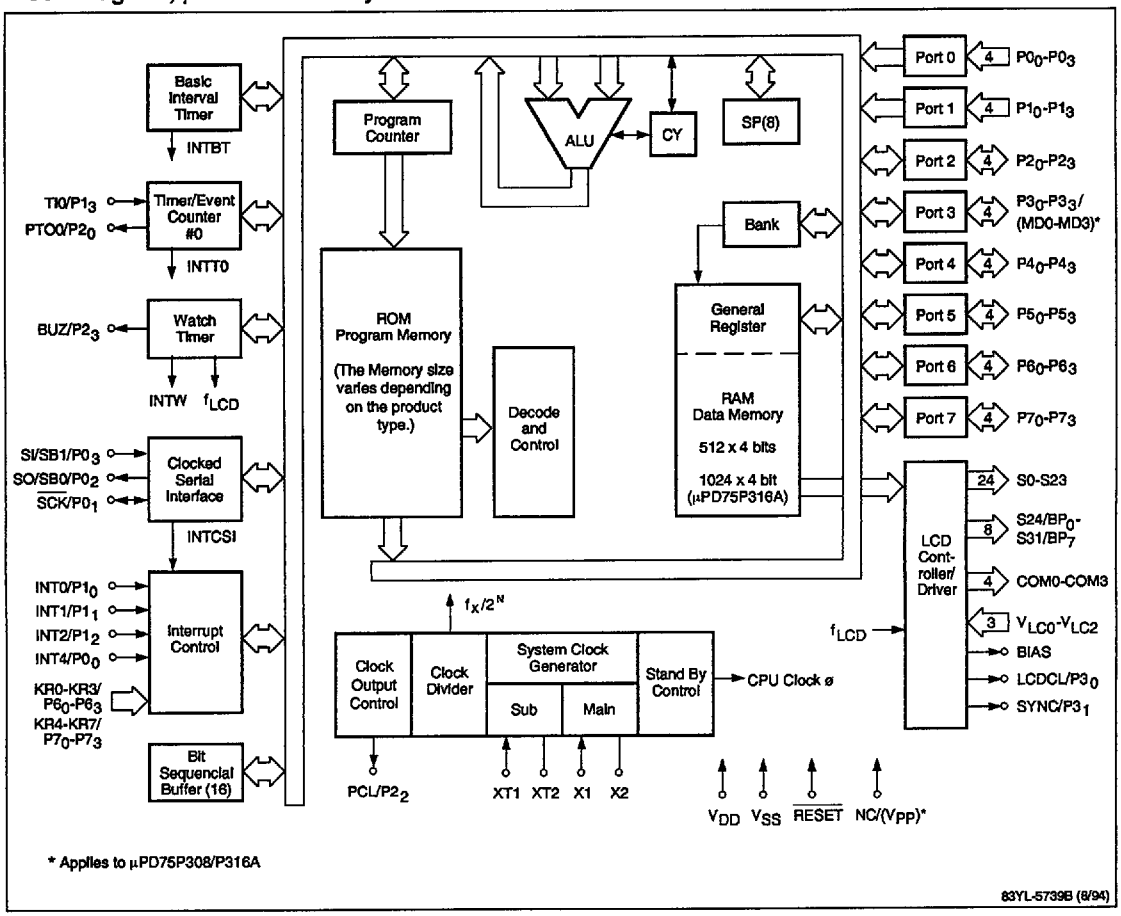
$\overline{\text{RESET}}$. This is the reset input, and it is active low.

V_{DD}. The system positive power supply pin.

V_{SS}. System ground.

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Block Diagram; μPD75316 Family



* Applies to μPD75P308/P316A

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Product Comparison

Item	75304	75306	75308	75P308	75312	75316	75P316 (Note)	75P316A
Program memory	Mask ROM 000H–FFFH 4096 x 8 bits	Mask ROM 0000H–177FH 6016 x 8 bits	Mask ROM 0000H–1F7FH 8064 x 8 bits	OTP; EPROM 0000H–1F7FH 8064 x 8 bits	Mask ROM 0000H–2F7FH 12,160 x 8 bits	Mask ROM 0000H–3F7FH 16,256 x 8 bits	OTP 0000H–3F7FH 16,256 x 8 bits	OTP; EPROM 0000H–3F7FH 16,256 x 8 bits
Data memory	512 x 4 bits							1024 x 4 bits
3-byte branch instructions	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Other instruction set	Common to the products							
Program counter	12-bit	13-bit	13-bit	13-bit	14-bit	14-bit	14-bit	14-bit
Ports 4 and 5 pullup resistor	Mask option	Mask option	Mask option	No	Mask option	Mask option	No	No
LCD resistor ladder	Mask option	Mask option	Mask option	No	Mask option	Mask option	No	No
V_{PP}, PROM programming pins	No	No	No	Yes	No	No	Yes	Yes
Operating voltage range	2.7 to 6.0 V	2.7 to 6.0 V	2.7 to 6.0 V	5 V ± 5%	2.7 to 6.0 V	2.7 to 6.0 V	5 V ± 5%	2.7 to 6.0 V
Package	80-pin plastic QFP			80-pin plastic QFP; 80-pin ceramic LCC with window	80-pin plastic QFP			80-pin plastic QFP; 80-pin ceramic LCC with window

Note: The μPD75P316 has been superseded by the μPD75P316A.

CPU AND MEMORY ARCHITECTURE

The 75X architecture has two separate address spaces, one for program memory (ROM) and another for data memory (RAM).

Program Memory (ROM)

The ROM is addressed by the 12-, 13-, or 14-bit program counter. The size of the program counter and the amount of ROM present depend on which part is being used. The ROM contains program object code, interrupt vector table, a GETI instruction reference table, and table data. Table data can be obtained using table reference instruction MOVT.

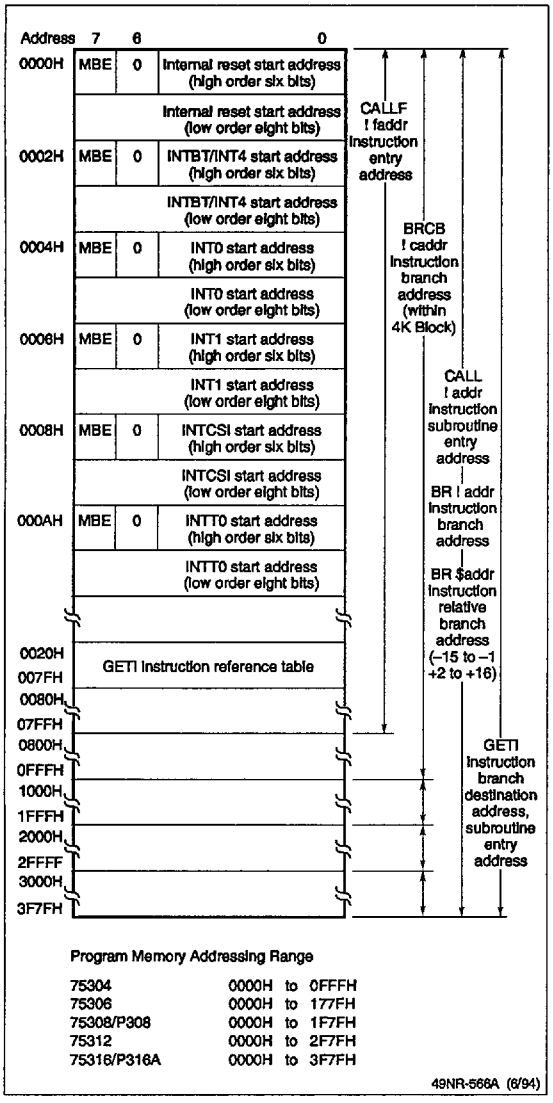
Figure 1 is the program memory map for the 75316 family. It also shows the addressing range that can be made using a branch instruction or subroutine call instruction. In addition, the BR PCDE and BR PCXA instructions can be used for a branch where only the low 8 bits of the PC are changed.

All locations in ROM except 0000H and 0001H can be used as program memory. However, if interrupts or GETI instructions are used, the locations corresponding to those functions cannot be used. Addresses are normally reserved as follows:

0000H and 0001H	Vector address for $\overline{\text{RESET}}$, and also contains the MBE bit.
0002H to 000BH	Interrupt vector addresses. Each vector address contains an MBE bit value. The interrupt service routines can start from any location except where noted above.
0020H to 007FH	Table area for GETI instructions. The GETI instruction is used to access one 2-byte/3-byte or two 1-byte instructions using one byte of program memory. This is useful in compacting code.

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Figure 1. Program Memory Map



Program Counter (PC)

This is a 12/13/14-bit binary counter that contains the address of the current program memory location. The μPD75304 contains a 12-bit PC; the 75306/308/P308 have a 13-bit PC; and the 75312/316/P316A have a 14-bit PC.

When an instruction is executed, the PC is automatically incremented by the number of bytes of the current instruction. When a branch instruction (BR, BRCB) is executed, the contents of the immediate data or register pair indicating the new address are loaded into some or all bits of the PC.

When a subroutine call instruction (CALL, CALLF) is executed or an interrupt is generated, the PC is incremented to point to the next instruction, and this information is saved on the stack. During an interrupt, the program status word (PSW) is also automatically saved on the stack. The address to be jumped to by the CALL or interrupt is then loaded into the PC.

When a return instruction (RET or RETS) is executed, the contents of the stack are restored to the PC. When a return instruction from interrupt (RETI) is executed, the PC and the PSW are restored.

Data Memory (RAM)

The data memory contains three memory banks (0, 1, and 15) in all devices except the μPD75P316A, which contains five memory banks (0, 1, 2, 3, and 15). The RAM memory maps are shown in figures 2 and 3. The memory consists of general-purpose static RAM and peripheral control registers.

The memory banks are accessed using MBE (memory bank enable) and by programming the BS (bank select register). If MBE = 0, the lower 128 nibbles of memory bank 0 and the upper 128 nibbles of memory bank 15 are accessed. If MBE = 1, the upper four bits in the BS register will specify the memory bank. The values are 0H for memory bank 0, 1H for memory bank 1, 2H for memory bank 2, 3H for memory bank 3, and 0FH for memory bank 15.

Memory banks 0, 1, 2, and 3 each contain 256 nibbles. Although the memory is organized in nibbles, the 75X architecture allows the data to be manipulated in bytes, nibbles, and individual bits.

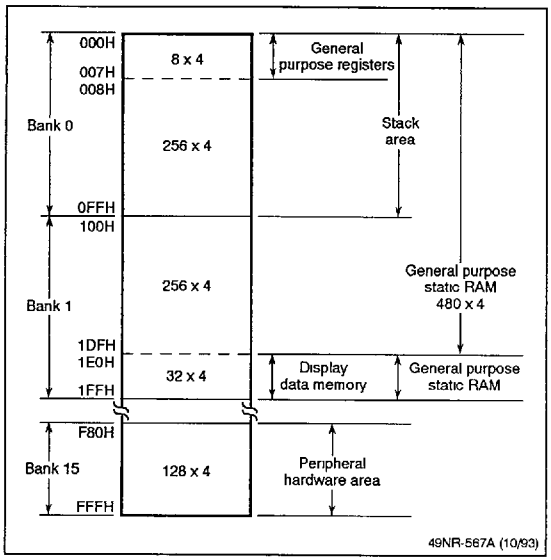
The data memory is used for storing processed data, general-purpose registers, and as a stack for subroutine or interrupt service. The last 32 nibbles of bank 1 are used to store the LCD display data. If this area is not completely used by the LCD, it may be used as general-purpose RAM. Because of its static nature, the RAM will

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retain its data when CPU operation is stopped and the chip is in the standby mode, provided V_{DD} is at least 2 volts.

There are eight 4-bit, general-purpose registers in bank 0 starting at location 00H (see figure 4). These registers may also be used as four 8-bit registers. The on-chip peripheral control registers and ports reside in the upper 128 nibbles of bank 15. Bank 15 addresses not assigned to a register are not available as random memory except for the 16-bit sequential buffer. Also, the lower 128 nibbles of bank 15 do not contain RAM.

Figure 2. Data Memory Map (except μPD75P316A)



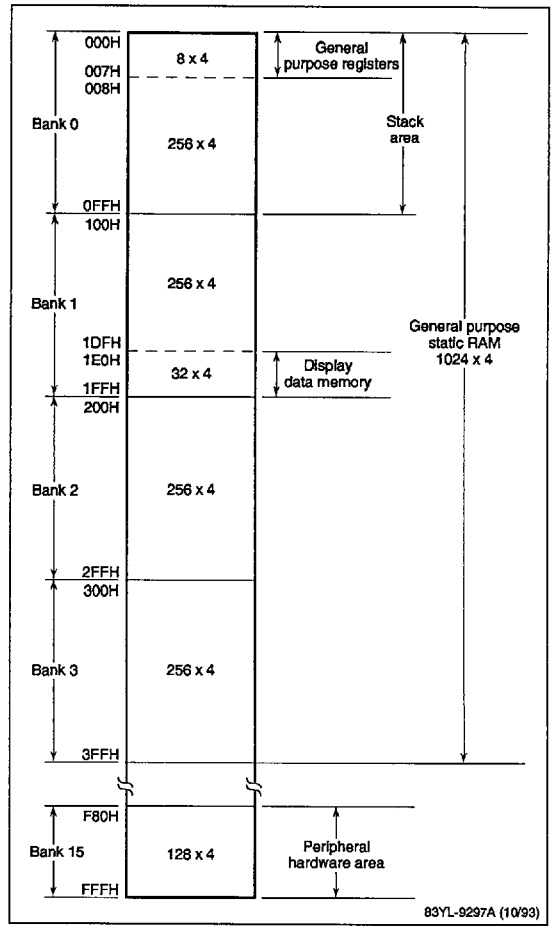
Addressing Modes

The μPD75316 family can address data memory and ports as individual bits, nibbles, or bytes. These addressing modes are as follows:

- 1-bit direct data memory
- 4-bit immediate
- 4-bit direct data memory
- 4-bit register indirect (@rpa)
- 8-bit immediate
- 8-bit direct data memory
- 8-bit register indirect (@HL)
- Bit manipulation
- Stack addressing

Table 1 shows the data memory addressing modes and table 2 shows the peripheral control register addressing. Figure 5 shows the data memory addressing modes for the μPD75316 family.

Figure 3. μPD75P316A Data Memory Map



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Figure 4. General-Purpose Register Configurations

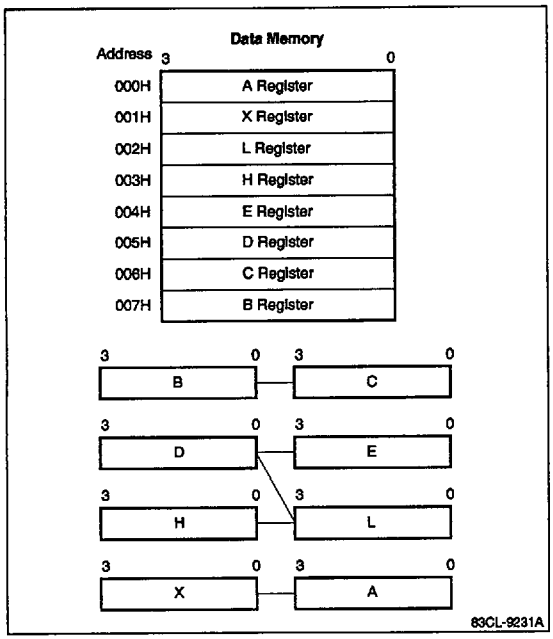


Table 1. Data Memory Addressing Modes

Addressing Mode	Format	How The Address is Formed
1-bit direct addressing	mem.bit	If MBE = 0, the memory bank is bank 0 for addresses 00H-7FH and bank 15 for addresses 80H-FFH. If MBE = 1, the memory bank is selected by the 4 bits of the MBS. The bit to be manipulated is specified in mem.bit
4-bit direct addressing	mem	If MBE = 0, the memory bank is bank 0 for addresses 00H-7FH,and bank 15 for addresses 80H-FFH. If MBE = 1, the memory bank is selected by the 4 bits of the MBS. The nibble to be manipulated is specified in mem.
8-bit direct addressing	mem (must be an even address)	If MBE = 0, the memory bank is bank 0 for addresses 00H-7FH and bank 15 for addresses 80H-FFH. If MBE = 1, the memory bank is selected by the 4 bits of the MBS. The byte to be manipulated is specified in mem.
4-bit register indirect addressing	@HL	The memory bank is selected by MBE and the 4 bits of the MBS. The location within the memory bank is contained in register HL.
	@DE	The memory bank is always bank 0. The location within the memory bank is contained in register DE.
	@DL	The memory bank is always bank 0. The location within the memory bank is contained in register DL
8-bit register indirect addressing	@HL (must be an even address)	The memory bank is selected by MBE and the 4 bits of the MBS. The location within the memory bank is contained in register HL.

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Table 1. Data Memory Addressing Modes (cont)

Addressing Mode	Format	How The Address is Formed
Bit manipulation addressing	fmem.bit	The memory bank is bank 15, and the location is fmem, where fmem = FB0H-FBFH for interrupts fmem = FF0H-FFFH I/O ports The actual bit is specified in fmem.bit
	pmem.@L	The memory location is always FC0H to FFFH and is independent of MBE and MBS. The upper 10 address bits of the location are contained in the 10 high order bits of pmem and the 2 lower address bits are contained in the 2 upper bits of register L. The bit to be manipulated is specified by the 2 lower bits of register L.
	@H + mem.bit	The memory bank is selected by MBE and the 4 bits of the MBS, and the location within the memory bank is determined by the following: The 4 upper bits are the contents of register H The 4 lower bits are mem. The actual bit is specified in mem.bit.
Stack addressing		The memory bank is always bank 0. The location is indicated by the stack pointer (SP)

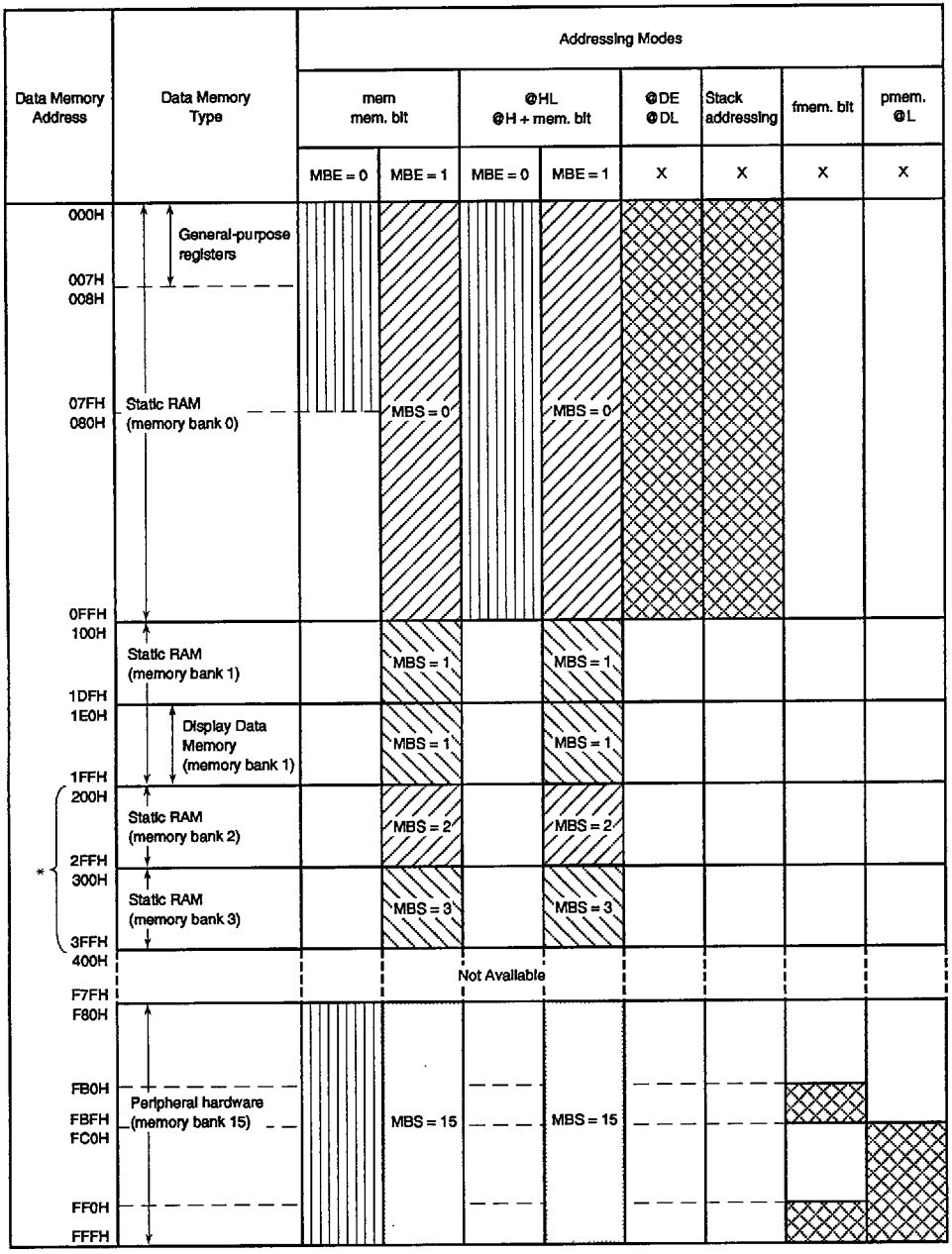
MBE	Memory bank enable bit
MBS	Memory bank select register
mem	Location within a memory bank
mem.bit	Bit at a specified memory location
fmem and pmem	Specialized cases of mem

Table 2. On-Chip Peripheral Addressing Modes

Manipulation	Addressing Mode	Applicable Hardware
1-bit	With MBE = 0 (or MBE = 1 and MBS = 15), direct addressing with peripheral address specified in mem.bit	All hardware where bit manipulation can be performed
	Direct addressing regardless of the setting of MBE and MBS with peripheral address specified in fmem.bit	ISTO, MBE IExxx, IRQxxx, PORTn.x
	Indirect addressing regardless of the setting of MBE and MBS with peripheral address specified in pmem. @L	BSBn.x PORTn.x
4-bit	With MBE = 0 (or MBE = 1 and MBS = 15), direct addressing with peripheral address specified in mem.bit	All hardware where 4-bit manipulation can be performed
	With MBE = 1 and MBS = 15, register indirect addressing with peripheral address specified in HL	
8-bit	With MBE = 0 (or MBE = 1 and MBS = 15), direct addressing with peripheral address specified in mem; mem must be an even address	All hardware where 8-bit manipulation can be performed
	With MBE = 1 and MBS = 15, register indirect addressing with peripheral address specified in HL; L register must contain an even number	

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Figure 5. Data Memory Organization and Addressing Modes



X: MBE has no effect
*: For μPD75P316A only
MBE: Memory bank enable bit
MBS: Memory bank select register

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FUNCTIONAL DESCRIPTION

Input/Output Ports

The μPD75316 family has eight 4-bit ports; six are input/output, two are input only. They also have eight 1-bit output ports. Figure 6 shows the structure of the ports and table 3 lists the features. Figure 6 also shows the structure of inputs and outputs of the other pins.

Software selectable internal pullup resistors are available on ports 0, 1, 2, 3, 6, and 7. They are selectable in 4-bit units. Port 0, bit 0 does not have a pullup resistor. Mask option, bit-selectable internal pullup resistors are available for ports 4 and 5 of all mask ROM devices.

Table 3. Types and Features of Digital Ports

Port	Function	Operation and Features	Remarks
Port 0	4-bit input	Can always be read or tested regardless of the operation mode.	Pins also used for INT4, $\overline{SCK}$, SO/SB0, SI/SB1.
Port 1			Pins also used for INT0, INT1, INT2, TI0.
Port 3 (Note 1)	4-bit input/output	Can be placed in input or output mode in 1-bit units.	Pins also used for LCDCL, SYNC, and MD0-MD3 (Note 2)
Port 6			Pins also used for KR0 - KR3.
Port 2	4-bit input/output	Can be placed in input or output mode in 4-bit units. Ports 6 and 7 can be paired for data input/output in 8-bit units.	Port 2 pins are also used for PTO_0, PCL, BUZ.
Port 7			Pins also used for KR4 - KR7.
Ports 4, 5 (Note 1)	4-bit input/output (n-channel, open drain, 10 volts)	Can be placed in input or output mode in 4-bit units. Ports 4 and 5 can be paired for data input/output in 8-bit units.	Internal pullup resistor can be specified in 1-bit units by mask option. (μPD7530x/31x only)
Ports BP0-BP7	1-bit output	Data is output in 1-bit units. The BP0 - BP7 pins are also used as LCD segment pins S24 - S31. BP0 - BP7 and S24 - S31 can be changed by software.	The drive capacity is very small. Used for CMOS load drive.

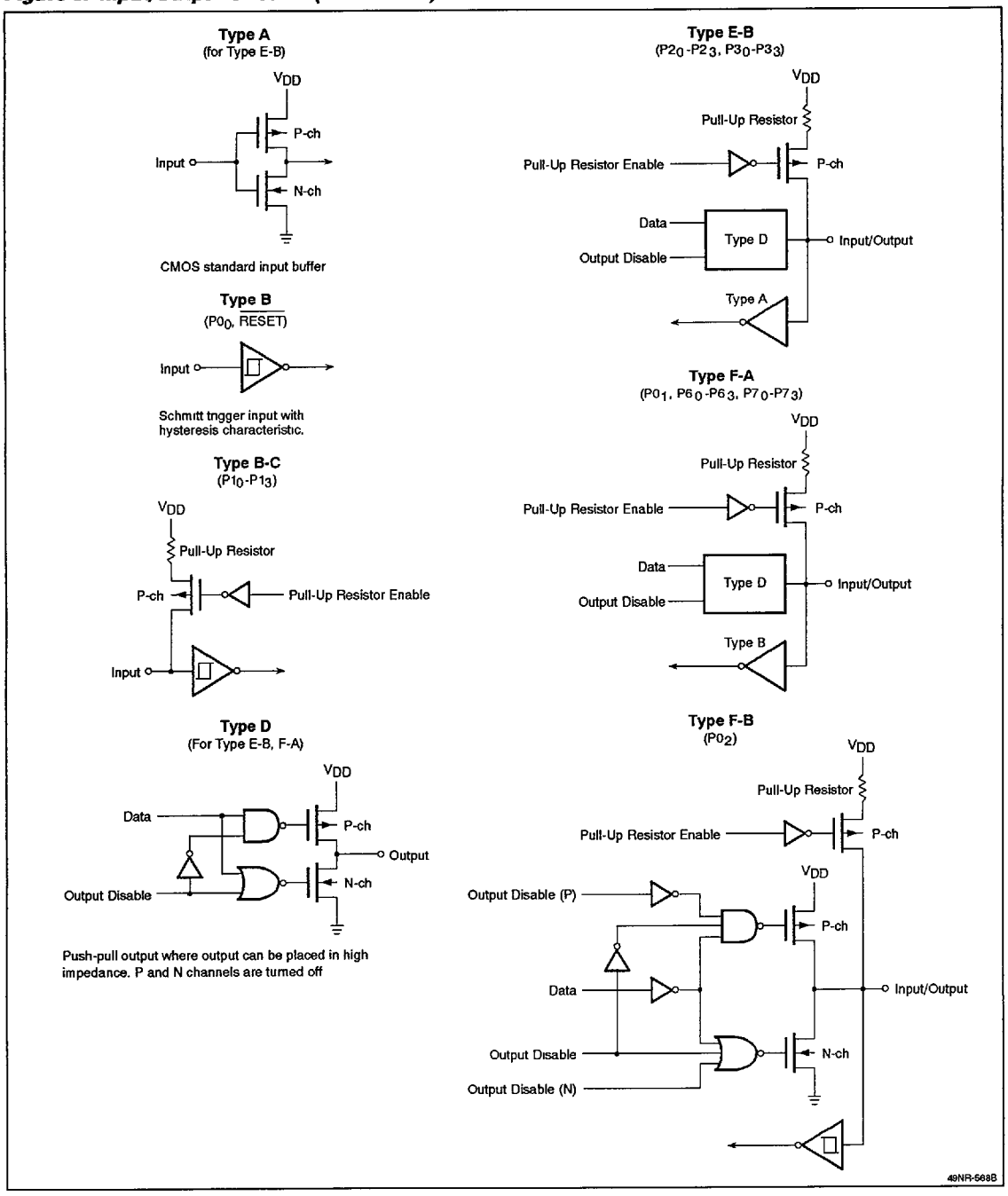
Notes:

(1) These ports directly drive LEDs.

(2) Port 3 lines are also used for MD0 - MD3 in μPD75P308/P316A.

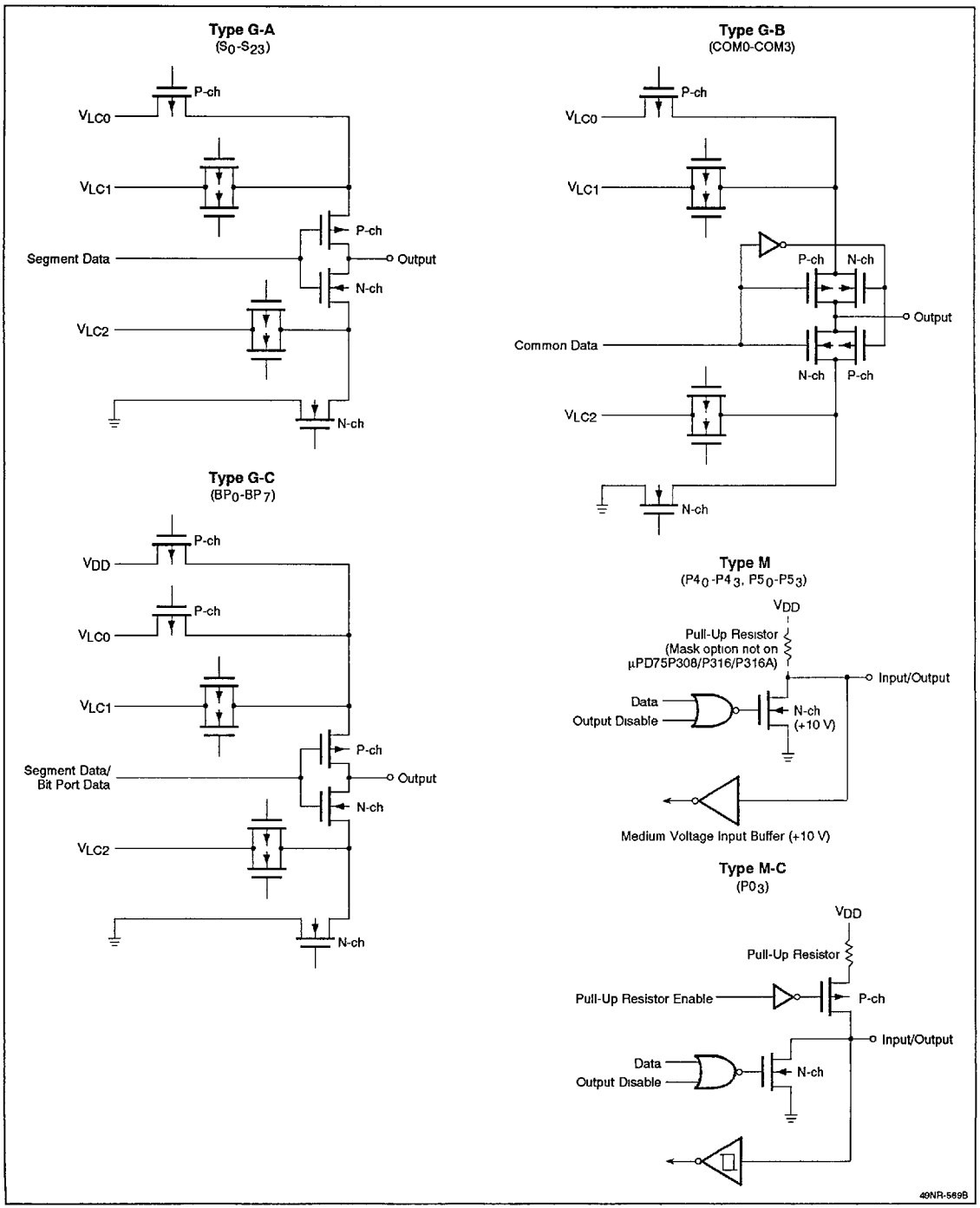
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Figure 6. Input/Output Circuits (Sheet 1 of 2)



6427525 0052686 89T

Figure 6. Input/Output Circuits (Sheet 2 of 2)



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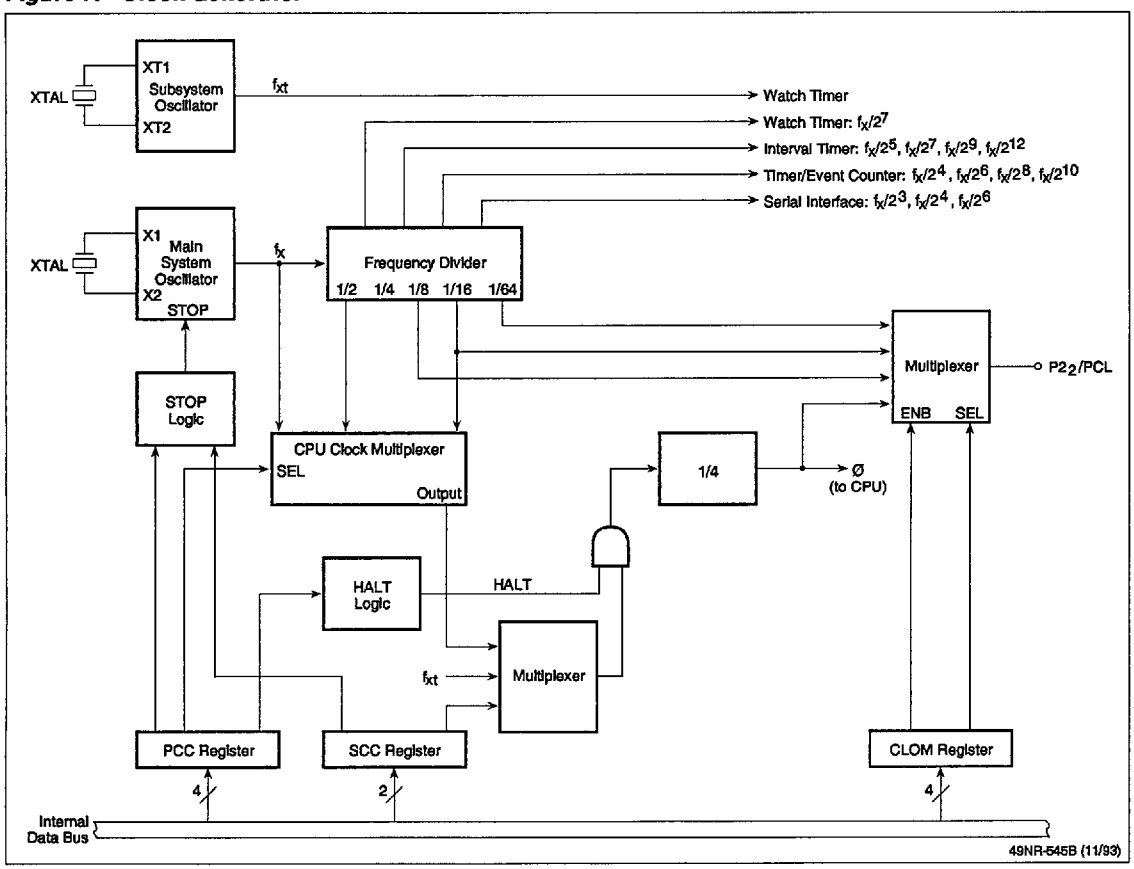
Clock Generator

The clock generator (figure 7) uses the crystal inputs X1 and X2 as a time base to provide clocks for the μPD75316 family. The generator consists of an oscillator, frequency dividers, multiplexers, and three control registers (PCC, SCC, and CLOM). By programming PCC and CLOM, frequencies derived from the crystal are supplied to the CPU, interval timer, timer/event counter, watch timer, serial interface, and output pin PCL.

The PCC and SCC registers control the HALT and STOP logic and can also be used to set the CPU to operate at one of four speeds. The CLOM register controls the PCL output clock.

The clock generator also contains a subsystem clock consisting of an oscillator driven by an external crystal. It operates at 32-35 kHz and can be used as a clock source to the watch timer, LCD controller, and CPU.

Figure 7. Clock Generator

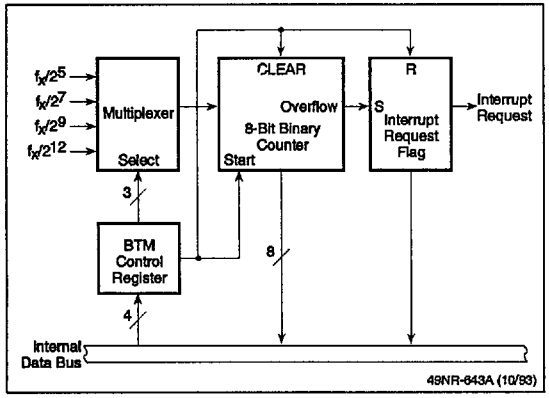


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Basic Interval Timer

The basic interval timer (figure 8) provides continuous real-time interrupts. It consists of a multiplexer, 8-bit free-running counter, and 4-bit BTM control register. Each time the counter reaches FFH it causes an interrupt, overflows to 00H, and continues to count. The BTM register selects one of four clock inputs to the counter, clears the counter, and clears its interrupt request. The counter can generate 250-ms interrupts with a 4.19-MHz crystal; it also provides oscillator stabilization time when the chip leaves the STOP mode.

Figure 8. Basic Interval Timer

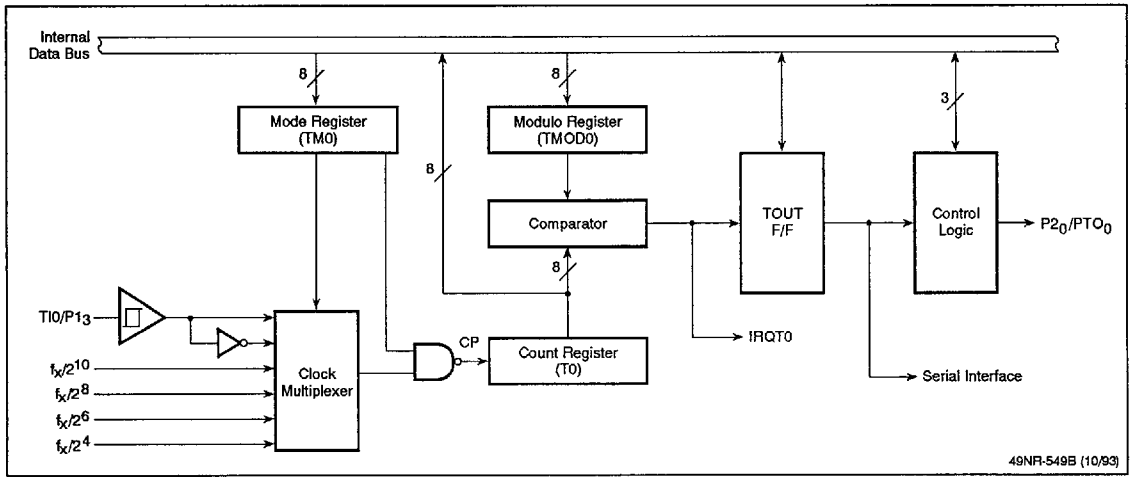


Timer/Event Counter (TM0)

The timer/event counter (figure 9) consists of an 8-bit modulo register, 8-bit comparator, 8-bit count register, clock multiplexer, mode control register TM0, and a TOUT flip-flop. Control logic allows the flip-flop signal PTO_0 to be output to port 2, bit 0.

An 8-bit value is loaded into the modulo register and a count register clock is selected by the clock multiplexer via control register TM0. The count register is incremented each time it receives a counter pulse (CP). When the value in the count register is equal to the count in the modulo register, the comparator generates a signal. This signal toggles the TOUT flip-flop and resets the count register to 00H. The count register will continue to count up unless stopped. Each time the comparator has a match, TOUT changes state and interrupt IRQT0 is generated. This signal can also be used as a clock for the serial interface.

Figure 9. Timer/Event Counter



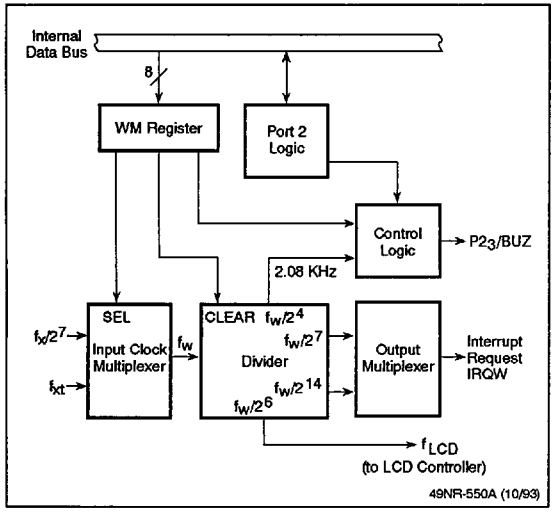
6427525 0052689 5T9

Watch Timer

The watch timer (figure 10) is normally the time source for keeping track of time of day. With a 4.19-MHz crystal, it will generate interrupt requests (not vectored interrupts) at 0.5-second or 3.91-ms intervals.

The watch timer consists of an input clock multiplexer, frequency divider, output multiplexer, control logic, and control register WM. When a subsystem clock is present, the timer can operate when the chip is in the STOP mode. It is also a clock source for the LCD controller and is capable of generating a 2-kHz buzzer output signal.

Figure 10. Watch Timer



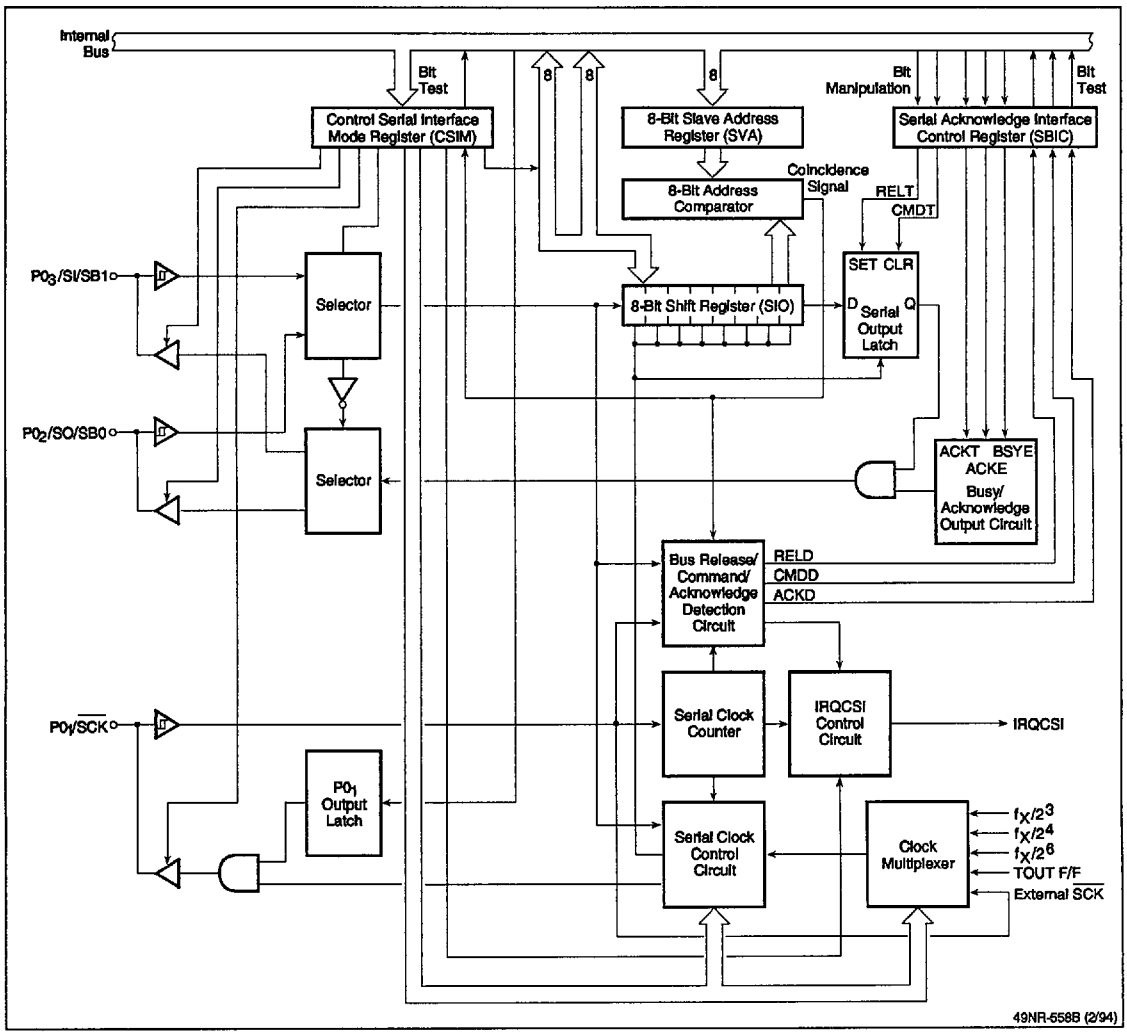
Serial Interface

The 8-bit serial interface (figure 11) allows the μPD75316 family to communicate with other NEC or NEC-like serial interfaces. It consists of an 8-bit shift register (SIO), serial-out latch (SO), 8-bit address comparator, slave address register (SVA), control registers CSIM and SBIC, busy/acknowledge circuitry, bus release/detect circuitry, serial clock counter, clock multiplexer, and clock control circuitry. The three-wire interface consists of the serial data in (SI/SB1), serial data out (SO/SB0), and serial shift clock ($\overline{SCK}$).

There are three modes of operation: 2-wire serial, 3-wire serial, and 2-wire SBI. The simplest modes are the 2/3-wire serial. In these modes, the 8-bit shift register is loaded with a byte of data and 8 clock pulses are generated. These pulses shift data out the SO line and data in from the SI line, thus, communicating in full duplex. Each time a byte of data is sent, a burst of eight clock pulses is generated and eight bits of data will be sent. Data may be sent either LSB or MSB first. The interface may also be set to receive data only; in this case SO is in the high-impedance state. One of four internal clocks or an external clock may be used to clock the data.

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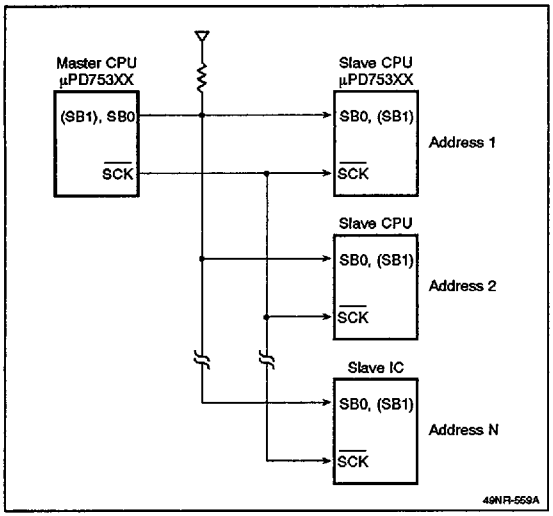
Figure 11. Serial Interface Block Diagram



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The SBI mode uses a 2-wire interface (figure 12) with devices in a master/slave configuration. At any one time, there is a single master, with all other devices being slaves. The master can send addresses, commands, and data over the bus. The slaves are able to detect in hardware if their particular address has been sent, and can also detect whether a command or piece of data has been sent. There can be as many as 256 slave addresses, 256 commands, and 256 data types. All commands are user-defined, and it is possible to send commands that change slaves into masters; when this happens, the previous master becomes a slave. This type of work is done in firmware, and the bus can be as simple or complex as the user wishes.

Figure 12. SBI Mode Master/Slave Configuration



LCD Controller/Driver

The LCD controller/driver (figure 13) can be programmed to operate in any of four modes. It can operate in the static mode (drive 32 segments), the duplex mode (drive 64 segments), the triplex mode (drive 96 segments), or quadruplex mode (drive 128 segments). The duplex mode uses 1/2 bias, the triplex mode can use either 1/2 or 1/3 bias, and the quadruplex mode uses 1/3 bias.

The LCD controller automatically refreshes the LCD by taking data from the upper 32 nibbles of RAM in memory bank 1, and uses display data multiplexers, segment drivers S0 - S31, and common drivers COM0 - COM3 to drive the LCD. It is controlled by registers LCDM, LCDC, and PGMA. The LCD main controller clock (f_{LCD}) is provided by the watch timer. The LCD controller/driver can operate in the STOP mode as long as the watch timer is clocked by the subsystem clock.

Drive levels can be set internally by ordering the resistor ladder mask option on the μPD7530x/31x mask ROM devices. Otherwise, external resistors can be connected to pins V_{LC0} - V_{LC2} and the BIAS pin. The BIAS pin can be used to control the contrast of the LCD.

Bit Sequential Buffer

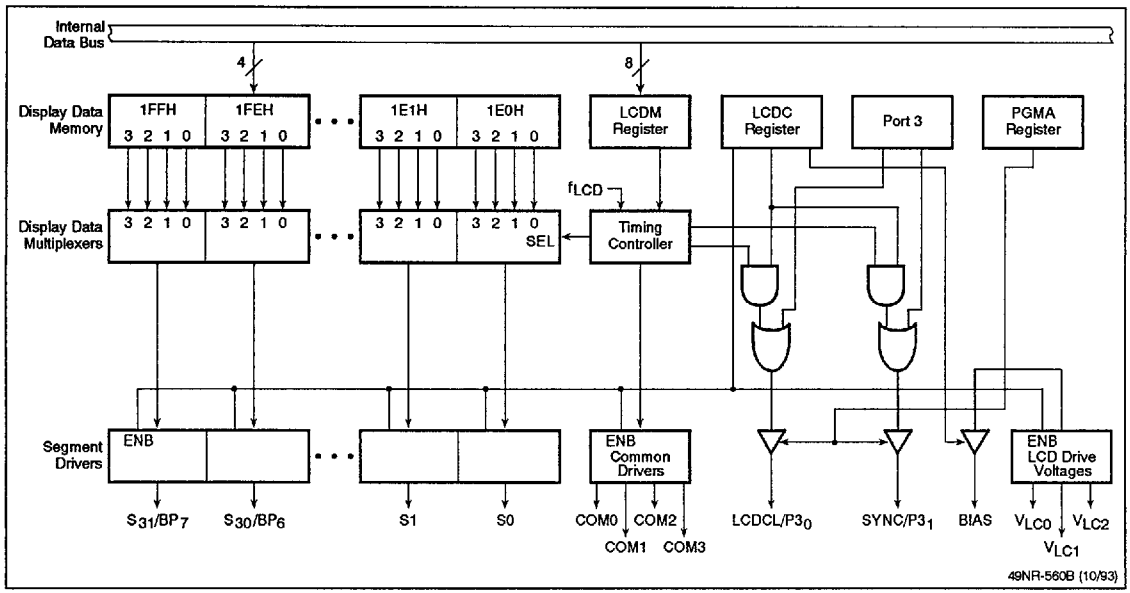
The 16-bit sequential buffer is the only general-purpose RAM in the upper half of data memory bank 15. All other locations in this bank either contain the on-chip peripheral control registers or are unused addresses.

The bit sequential buffer can be bit, nibble, or byte manipulated. Its bits are addressed by register L and they can be sequentially scanned by incrementing or decrementing L.

A typical application for this buffer might be to store data for the next serial output or to store data from a serial input. It could also be used to store data that is to be sent from a port.

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Figure 13. LCD Controller Block Diagram



6427525 0052693 T2T

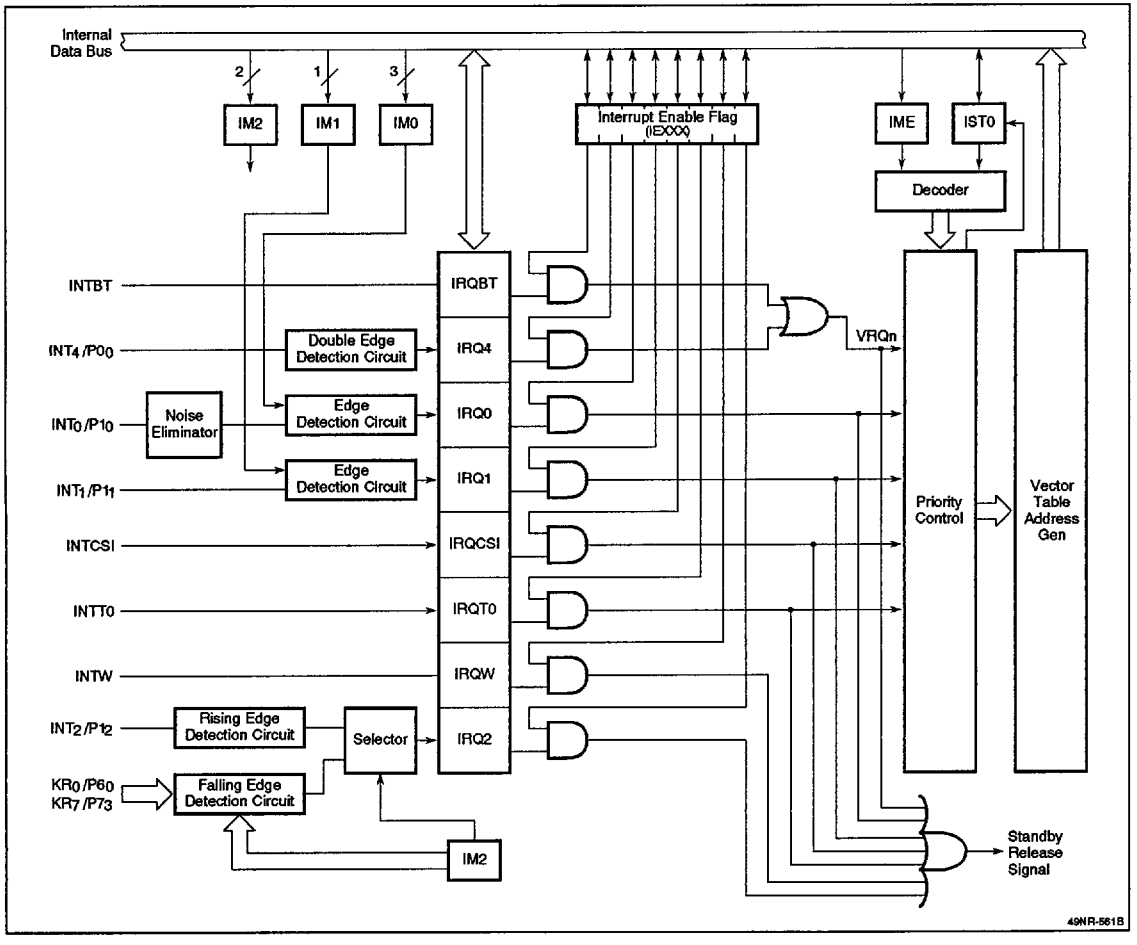
Interrupts

The μPD75316 family has a total of six interrupts (three external and three internal) that share five interrupt vectors. Refer to table 4 and figure 14.

Interrupts INTBT and INT4 share one interrupt vector and the interrupt to be serviced is determined by software in the interrupt service routine. In addition, INT2 detects the rising edge inputs and generates an interrupt request flag, which is testable. Inputs KR0–KR7 will detect falling edges and generate the same interrupt request flag as INT2.

Neither INT2 nor KR0–KR7 will cause a vectored interrupt, but they can be used to release the standby mode. Interrupt INTW also does not generate a vectored interrupt but can be tested and used to release the standby mode. All interrupts and interrupt requests except INT0 will release the standby mode.

Figure 14. Interrupt Controller Block Diagram



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Standby Modes

The three standby modes are described below and in table 5.

HALT Mode. The HALT mode is entered by executing the HALT instruction. In this mode, the clock to the CPU is shut off (thus stopping the CPU), while all other functions with the exception of INT0, remain fully operational.

STOP Mode. The STOP mode is entered by executing the STOP instruction. In this mode, the chip's main system oscillator is shut off, thereby stopping all functions except those which operate off the subsystem clock. If the subsystem clock is used, it always remains on.

The HALT and STOP modes are released by a $\overline{\text{RESET}}$ or by any interrupt request except INT0.

Data Retention Mode. This mode may be entered after entering the STOP mode. Here, supply voltage V_{DD} may be lowered to 2 volts to further reduce power consumption. The contents of the RAM and registers are retained. This mode is released by first raising V_{DD} to the proper operating range and then releasing the STOP mode.

Reset

Refer to table 6 for the state of the device after reset.

Table 4. Interrupt Sources

Interrupt Source	Operation	Internal/ External	Interrupt Priority (Note)	Vectored Interrupt Request Signal(Vector Table Address)
INTBT	Reference time interval signal from basic interval timer	Internal	1	VRQ1 (0002H)
INT4	Both rising and falling edge detection	External		
INT0	Selection of rising or falling edge detection	External	2	VRQ2 (0004H)
INT1	Selection of rising or falling edge detection	External	3	VRQ3 (0006H)
INTCSI	Serial data transfer end signal	Internal	4	VRQ4 (0008H)
INTT0	Coincidence signal between programmable timer/event counter count register and modulo register	Internal	5	VRQ5 (000AH)
INT2	Rising edge detection of input to INT2 pin, or falling edge detection of any input to KR0–KR7	External	Testable input signals (can test if IRQ2 or IRQW is set)	
INTW	Signal from watch timer	Internal		

Note: The interrupt priority determines the priority order when two or more interrupts are generated simultaneously.

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Table 5. Standby Mode Operation

Item	STOP Mode	HALT Mode
Method of setting standby mode	STOP instruction by main clock or SCC register by subsystem clock	HALT instruction by main or subsystem clock
Clock oscillator	Only the main system clock oscillator is stopped	Only CPU clock ϕ is stopped (oscillation of main and subsystem clock continues)
Basic interval timer	Operation stopped	Operational
Serial interface	Operates only when external $\overline{SCK}$ input is selected for serial clock	Operational
Timer/event counter	Operates only when TIO pin input is selected for count clock	Operational
Watch timer	Operates only when f_{XT} is selected for count clock	Operational
LCD controller	Operates only when f_{XT} is selected by the watch timer	Operational
External interrupts	INT1, INT2, INT4 can operate; INT0 cannot	INT1, INT2, INT4 can operate; INT0 cannot
CPU	Operation stops	Operation stops
Release signal	Enabled interrupt request signal (except INT0) or $\overline{RESET}$	Enabled interrupt request signal (except INT0) or $\overline{RESET}$

Table 6. State of the Device After Reset

Hardware		$\overline{RESET}$ Input During Standby Mode	$\overline{RESET}$ Input During Operation
Program counter (PC)	μPD75304	The low-order 4 bits of program memory address 0000H are loaded into PC11 - PC8. The contents of address 0001H are loaded into PC7 - PC0.	
	μPD75306 μPD75308 μPD75P308	The low-order 5 bits of program memory address 0000H are loaded into PC12 - PC8. The contents of address 0001H are loaded into PC7 - PC0.	
	μPD75312 μPD75316 μPD75P316A	The low-order 6 bits of program memory address 0000H are loaded into PC13 - PC8. The contents of address 0001H are loaded into PC7 - PC0.	
PSW	Carry flag (CY)	Held	Undefined
	Skip flags (SK0 - SK2)	0	0
	Interrupt status flag (IST0)	0	0
	Memory bank enable flag (MBE)	Bit 7 of program memory address 0000H is loaded into MBE	
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held (Note 1)	Undefined
General-purpose registers (X, A, H, L, D, E, B, C)		Held	Undefined
Memory bank selection register (MBS)		0	0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0

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Table 6. State of the Device After Reset (cont)

Hardware		$\overline{\text{RESET}}$ Input During Standby Mode	$\overline{\text{RESET}}$ Input During Operation
Watch timer	Mode register (WM)	0	0
Serial interface	Shift register (SIO)	Held	Undefined
	Operation mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Held	Undefined
Clock generator and clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
LCD controller	Display mode register (LCDM)	0	0
	Display control register (LCDC)	0	0
Interrupt function	Interrupt request flags (IRQxxx)	Reset to 0	Reset to 0
	Interrupt enable flags (IExxx)	0	0
	Interrupt master enable flag (IME)	0	0
	INT0, INT1, and INT2 and mode registers (IM0, IM1, and IM2)	0, 0, 0	0, 0, 0
Digital ports	Output buffers	Off	Off
	Output latches	Cleared to 0	Cleared to 0
	Input/output mode registers (PMGA, B)	0	0
	Pullup resistor specification register (POGA)	0	0
Bit sequential buffer		Held	Undefined
Pin conditions	$P0_0$–$P0_3$, $P1_0$–$P1_3$, $P2_0$–$P2_3$, $P3_0$–$P3_3$, $P6_0$–$P6_3$, $P7_0$–$P7_3$	Input	Input
	$P4_0$–$P4_3$, $P5_0$–$P5_3$,	With incorporated pullup resistor, high level; with open drain, high impedance	
	S0–S31 COM0–COM3	Note 2	Note 2
	BIAS	With incorporated resistor ladder, low level; with no incorporated resistor ladder, high impedance	

Notes:

(1) The data of data memory address 0F8H-0FDH is undefined by RESET.

(2) S0 to S31 use V_{LC1}, COM0 to COM2 use V_{LC2}, and COM3 uses V_{LC0} as an input source. However, each display output level is based on each display output and V_{LCx}'s external circuit.

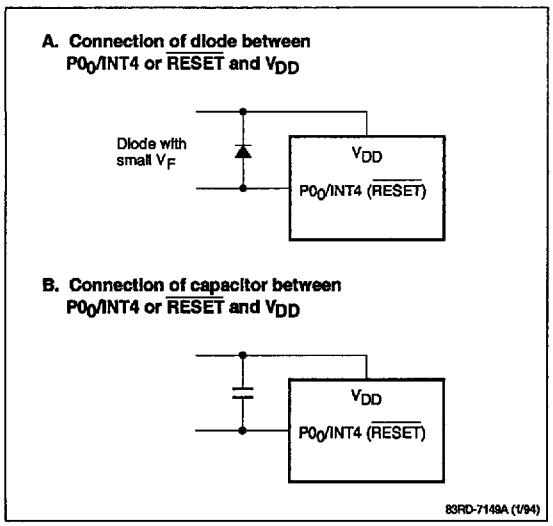
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Caution

Apart from their normal functions, the $P0_0$/INT4 and $\overline{RESET}$ pins are used to test the internal operation of the devices. The test mode is entered by applying a voltage greater than V_{DD} to either of these pins.

For this reason, care must be taken to limit the voltage applied to these two pins. For example, it is conceivable that even during normal operation enough spurious noise may be present to set the chip into the test mode. If this happens, further normal operation is impossible. Consequently, it is important that interwiring noise be suppressed as much as possible. If this is inconvenient, anti-noise measures, like those shown in figure 15, should be implemented.

Figure 15. Noise Reduction Techniques



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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Supply voltage, V_{PP} (75P308/P316A)	−0.3 to +13.5 V
Input voltage, V_{I1} (other than ports 4, 5)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I2} (ports 4, 5; internal pullup resistor; 7530x/31x only)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I3} (ports 4, 5; open drain)	−0.3 to +11 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
High-level output current, I_{OH} (Single pin; standard grade)	−15 mA peak
High-level output current, I_{OH} (Single pin; special grade)	−10 mA peak
High-level output current, I_{OH} (Total of all pins)	−30 mA peak
Low-level output current, I_{OL} (Single pin; standard grade)	30 mA peak 15 mA rms †
Low-level output current, I_{OL} (Single pin; special grade)	10 mA peak 5 mA rms †
Low-level output current, I_{OL} (Total of ports 0, 2, 3, 5)	100 mA peak 60 mA rms †
Low-level output current, I_{OL} (Total of ports 4, 6, 7; standard grade)	100 mA peak 60 mA rms †
Low-level output current, I_{OL} (Total of ports 4, 6, 7; special grade)	100 mA peak 50 mA rms †
Storage temperature, t_{STG}	−65 to + 150°C
Operating temperature, t_{OPT} (7530x/31x/P316A)	−40 to +85°C
Operating temperature, t_{OPT} (75P308)	−10 to +70°C

† Rms value = peak value x (duty cycle)$^{1/2}$.

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

Capacitance (All devices)

V_{DD} = 0 V; T_A = 25°C

Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_{IN}	15	pF	f = 1 MHz; all unmeasured pins returned to ground
Output capacitance	C_{OUT}	15	pF	
I/O capacitance	C_{IO}	15	pF	

Main System Clock Oscillator

Refer to figures 16 and 18.

μPD7530x/31x/P316A: T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V;

μPD75P308: T_A = −10 to +70°C; V_{DD} = 5 V ± 5%

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Ceramic resonator (Figure 16A)	Oscillation frequency (Note 1)	f_X	1.0		5.0	MHz	
	Oscillation stabilization time (Note 2)				4 (Note 3)	ms	After V_{DD} reaches oscillator operating voltage
Crystal resonator (Figure 16A)	Oscillation frequency (Note 1)	f_X	1.0	4.19	5.0	MHz	
	Oscillation stabilization time (Note 2)				10 (Note 3)	ms	V_{DD} = 4.5 to V_{DD} max
					30 (Note 3)	ms	V_{DD} = 2.7 to 6.0 V (7530x/31x/P316A)
External clock (Figure 16B)	X1 input frequency (Note 1)	f_X	1.0		5.0	MHz	
	X1 input low- and high-level width	t_{XH}, t_{XL}	100		500	ns	

Notes:

(1) The oscillation frequency and X1 input frequency are shown only to present the characteristics of the oscillators. Refer to the AC Characteristics table for actual instruction execution times.

(2) The oscillation stabilization time is the time required for the oscillator to stabilize after voltage is applied or the STOP mode is released.

(3) Values shown are for the recommended resonators. Values for resonators not shown in this data sheet should be obtained from the manufacturer's spec sheets.

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Figure 16. Main System Clock Configurations

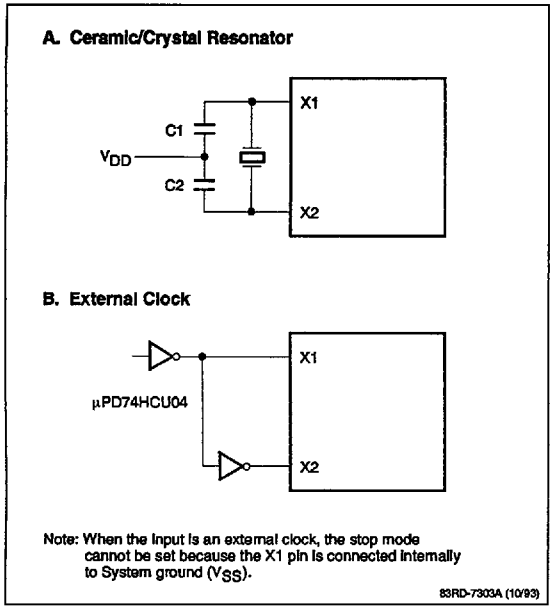
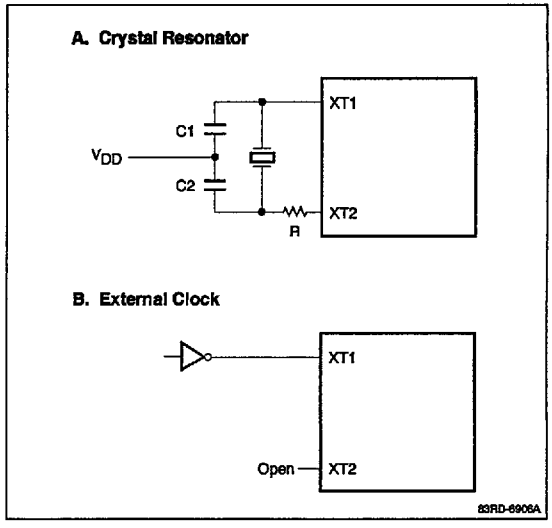


Figure 17. Subsystem Clock Configurations



Subsystem Clock Oscillator

Refer to figures 17 and 18.

μPD7530x/31x/P316A: T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V;

μPD75P308: T_A = −10 to +70°C; V_{DD} = 5 V ± 5%

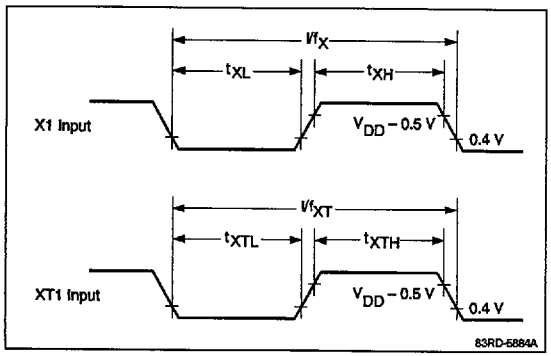
Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal resonator (Figure 17A)	Oscillation frequency	f_{XT}	32	32.768	35	kHz	
	Oscillation stabilization time (Note 1)			1.0	2	s	V_{DD} = 4.5 to V_{DD} max
					10	s	V_{DD} = 2.7 to 6.0 V (7530x/31x/P316A)
External clock (Figure 17B)	XT1 input frequency	f_{XT}	32		100	kHz	
	XT1 input low- and high-level width	t_{XTH}, t_{XTL}	5		15	μs	

Note:

(1) Values shown are for recommended resonators. Values for resonators not in this data sheet should be obtained from the manufacturer's spec sheets.

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Figure 18. Clock AC Timing Points X1 and XT1



Recommended Main System Ceramic Resonators (μPD7530x/31x Standard Grade Only)

Manufacturer	Part Number	C1 (pF)	C2 (pF)	Remarks
Murata	CSA 2.00MG093	15	15	V_{DD} = 2.5 to 3.5 V
	CSB 1000D20	220	220	V_{DD} = 2.7 to 6.0 V
	CSA 2.00MG093	30	30	
	CSA 4.19MGU	30	30	
	CSA 4.91MGU	30	30	
	CST 2.00MG093	None	None	V_{DD} = 2.7 to 6.0 V (Note 1)
	CST 4.19MGU	None	None	
	CST 4.91MGU	None	None	
Kyocera	KBR-1000H	100	100	V_{DD} = 3.0 to 6.0 V
	KBR-2.0MS	68	68	
	KBR-4.0MS	33	33	
	KBR-4.19MS	33	33	
	KBR-4.91MS	33	33	

Note:

(1) C1 and C2 are contained in the oscillator.

Recommended Main System Crystal Resonators (μPD7530x/31x Standard Grade Only)

Manufacturer	Frequency (MHz)	Retainer	C1 (pF)	C2 (pF)	Remarks
Kinseki	2.00	HC-18/U	22	22	V_{DD} = 2.7 to 6.0 V
	4.19	HC-49/U	22	22	
	4.91	HC-43/U	22	22	

Recommended Subsystem Crystal Resonators (μPD7530x/31x Standard Grade)

Manufacturer	Type	C1 (pF)	C2 (pF)	R (kΩ)	Remarks
Kinseki	P-3	22	22	330	V_{DD} = 2.7 to 6.0 V

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DC Characteristics (μPD7530x/31x/P316A)

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V; refer to figures 19 through 22

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Ports 2, 3
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	Ports 0, 1, 6, 7; and $\overline{\text{RESET}}$
	V_{IH3}	0.7 V_{DD}		V_{DD}	V	Ports 4 and 5; internal pullup resistor, 7530x/31x
		0.7 V_{DD}		10	V	Ports 4 and 5; open drain
	V_{IH4}	V_{DD} − 0.5		V_{DD}	V	X1, X2, XT1
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	Ports 2, 3, 4, 5
	V_{IL2}	0		0.2 V_{DD}	V	Ports 0, 1, 6, 7; $\overline{\text{RESET}}$
	V_{IL3}	0		0.4	V	X1, X2, XT1
High-level output voltage	V_{OH1}	V_{DD} − 1.0			V	Ports 0, 2, 3, 6, 7, BIAS; V_{DD} = 4.5 to 6.0 V; I_{OH} = −1 mA
		V_{DD} − 0.5			V	Ports 0, 2, 3, 6, 7, BIAS; V_{DD} = 2.7 to 6.0 V; I_{OH} = −100 μA
	V_{OH2}	V_{DD} − 2.0			V	BP_{0-7} (with two I_{OH} outputs) V_{DD} = 4.5 to 6.0 V; I_{OH} = −100 μA
		V_{DD} − 1.0			V	BP_{0-7} (with two I_{OH} outputs) V_{DD} = 2.7 to 6.0 V; I_{OH} = −30 μA
Low-level output voltage	V_{OL1}		0.4	2.0	V	Ports 3, 4, 5; V_{DD} = 4.5 to 6.0 V; I_{OL} = 15 mA (standard grade)
			0.2	1.0	V	Ports 3, 4, 5; V_{DD} = 4.5 to 6.0 V; I_{OL} = 5 mA (special grade)
				0.4	V	Ports 0, 2-7; V_{DD} = 4.5 to 6.0 V; I_{OL} = 1.6 mA
				0.5	V	Ports 0, 2-7; V_{DD} = 2.7 to 6.0 V; I_{OL} = 400 μA
				0.2 V_{DD}	V	SB0, 1; V_{DD} = 2.7 to 6.0 V; open drain pullup resistance ≥ 1kΩ
	V_{OL2}			1.0	V	BP_{0-7} (with two I_{OL} outputs) V_{DD} = 4.5 to 6.0 V; I_{OL} = 100 μA
				1.0	V	BP_{0-7} (with two I_{OL} outputs) V_{DD} = 2.7 to 6.0 V; I_{OL} = 50 μA
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, XT1 and ports 4, 5 (open drain); V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH3}			20	μA	Ports 4 and 5 (with open drain); V_{IN} = 10 V
Low-level input leakage current	I_{LIL1}			−3	μA	All except X1, X2, and XT1; V_{IN} = 0 V
	I_{LIL2}			−20	μA	X1, X2, and XT1; V_{IN} = 0 V
High-level output leakage current	I_{LOH1}			3	μA	Other than ports 4 and 5 (open drain); V_{OUT} = V_{DD}
	I_{LOH2}			20	μA	Ports 4 and 5 (open drain); V_{OUT} = 10 V
Low-level output leakage current	I_{LOL}			−3	μA	V_{OUT} = 0 V

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DC Characteristics (μPD7530x/31x/P316A) (cont)

Parameter	Symbol		Min	Typ	Max	Unit	Conditions
Internal pullup resistor	R_{L1}		15	40	80	kΩ	Ports 0-3, 6, 7 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 5.0 V ±10%
			30		200	kΩ	Ports 0-3, 6, 7 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 3.0 V ±10%; 7530x/31x
			30		300	kΩ	Ports 0-3, 6, 7 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 3.0 V ±10%; 75P316A
	R_{L2}		15	40	70	kΩ	Ports 4, 5; V_{OUT} = V_{DD} − 2 V; V_{DD} = 5.0 V ± 10%; 7530x/31x
			10		60	kΩ	Ports 4, 5; V_{OUT} = V_{DD} − 2 V; V_{DD} = 3.0 V ± 10%; 7530x/31x
LCD drive voltage	V_{LCD}		2.5		V_{DD}	V	
LCD split resistor	R_{LCD} (Note 1)		60	100	150	kΩ	7530x/31x
LCD output voltage deviation; common (Note 2)	V_{ODC}		0		±0.2	V	I_O = ±5 μA; V_{LCD} = V_{LCD0} = 2.7 V to V_{DD}; V_{LCD1} = 2/3 V_{LCD} V_{LCD2} = 1/3 V_{LCD}
LCD output voltage deviation; segment (Note 2)	V_{ODS}		0		±0.2	V	I_O = ±1 μA; V_{LCD} = V_{LCD0} = 2.7 V to V_{DD}; V_{LCD1} = 2/3 V_{LCD} V_{LCD2} = 1/3 V_{LCD}
Supply current (Note 3)	I_{DD1} (Note 4)	† ‡	2.5 4.5	8 14	mA mA		V_{DD} = 5 V ±10% (Note 5)
		† ‡	0.35 0.9	1.2 3	mA mA		V_{DD} = 3 V ±10% (Note 6)
	I_{DD2} (Note 4)	† ‡	500 700	1500 2100	μA μA		HALT mode; V_{DD} = 5 V ±10%
		† ‡	150 300	450 900	μA μA		HALT mode; V_{DD} = 3 V ±10%
	I_{DD3} (Note 7)	† ‡	30 100	90 300	μA μA		V_{DD} = 3 V ±10% (Note 8)
	I_{DD4} (Note 7)	† ‡	5 20	15 60	μA μA		HALT mode; V_{DD} = 3 V ±10% (Note 8)
	I_{DD5}		0.5	20	μA		STOP mode; XT1 = 0 V; V_{DD} = 5 V ±10%
			0.1	10	μA		STOP mode; XT1 = 0 V; V_{DD} = 3 V ±10%
			0.1	5	μA		STOP mode; XT1 = 0 V; V_{DD} = 3 V ±10%; T_A = 25°C
	I_{DD6} (Note 7)	‡	5	15	μA		STOP mode; 3 V ±10%; (Note 9: 75P316A)

† 7530x/31x ‡ 75P316A

Notes:

(1) LCD split resistor is a mask option. See LCD Drive Power Supply section in the user's manual. R = R_{LCD}.

(2) Voltage deviation is the difference between the ideal value of segment or common output (V_{LCDn}; n = 0, 1, 2) and the output voltage.

(3) Does not include internal pullup resistor current and current through LCD resistor ladder.

(4) 4.19-MHz crystal oscillator; (C1 = C2 = 22 pF); subsystem clock running.

(5) When operated in the high-speed mode with the processor clock control register (PCC) set to 0011.

(6) When operated in the low-speed mode with the PCC set to 0000.

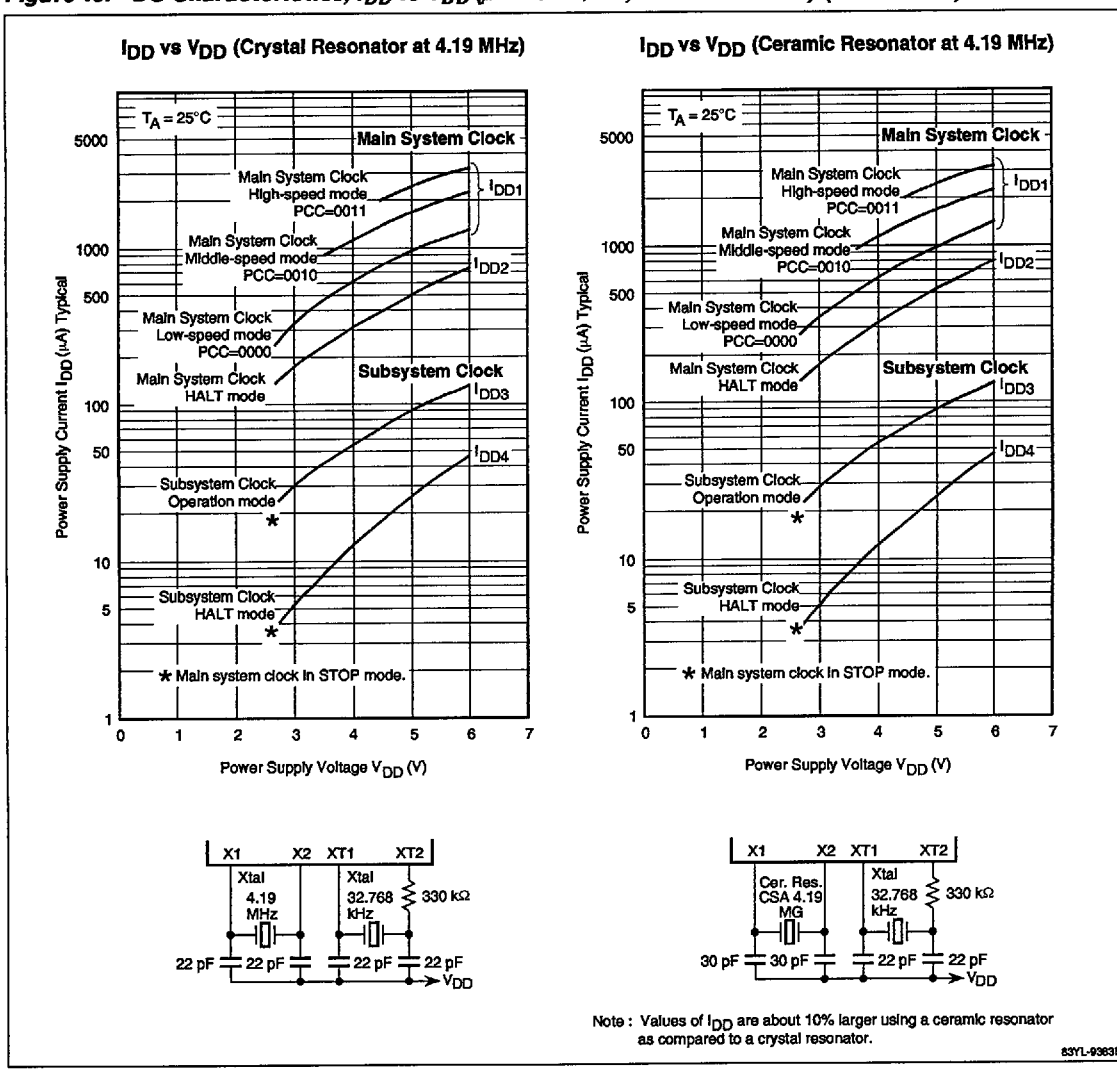
(7) 32-kHz crystal oscillator

(8) Main system clock stopped and subsystem clock running (SCC = 1001).

(9) When STOP instruction is executed during main system clock operation and the subsystem clock is oscillating.

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Figure 19. DC Characteristics, I_{DD} vs V_{DD} (μPD7530x/31x, Standard Grade) (Sheet 1 of 2)

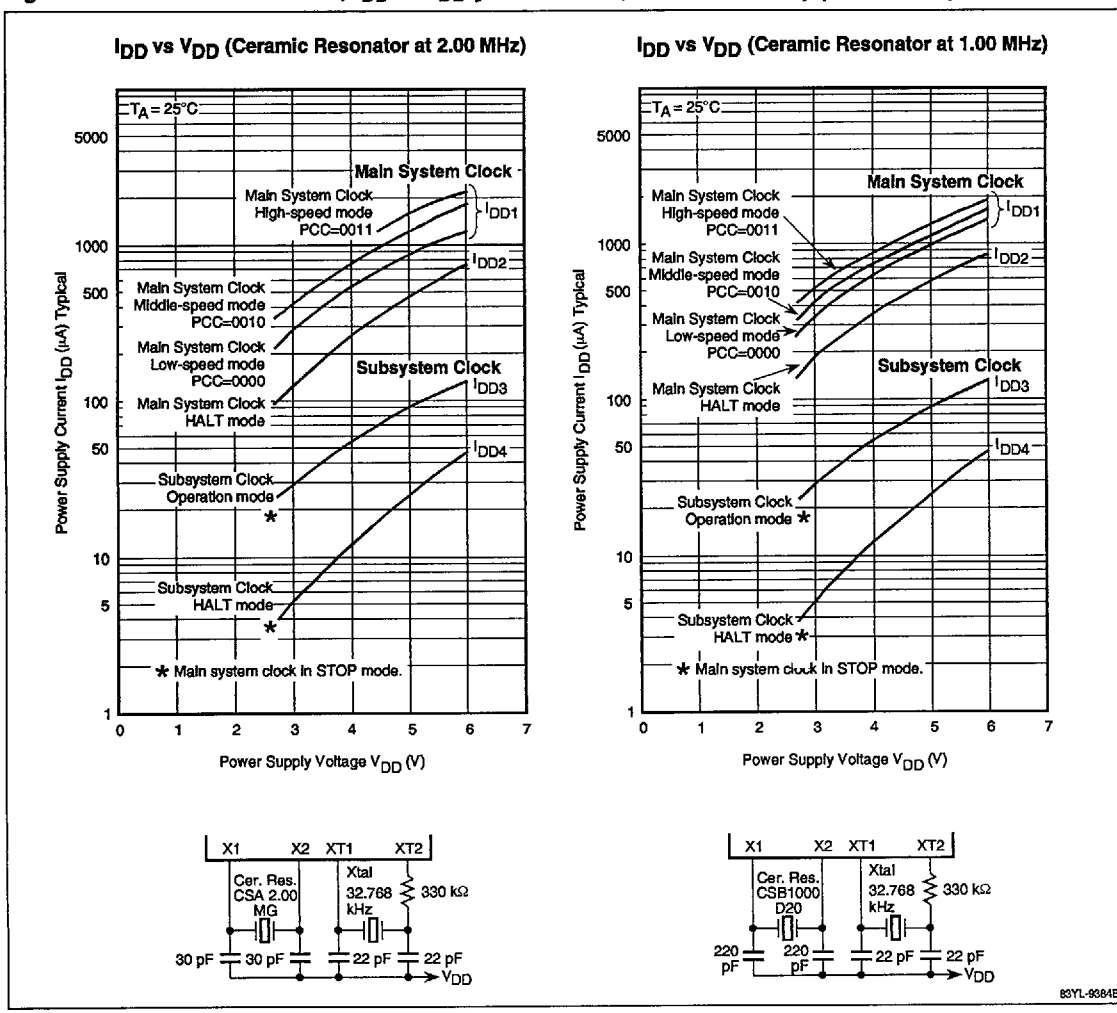


Note : Values of I_{DD} are about 10% larger using a ceramic resonator as compared to a crystal resonator.

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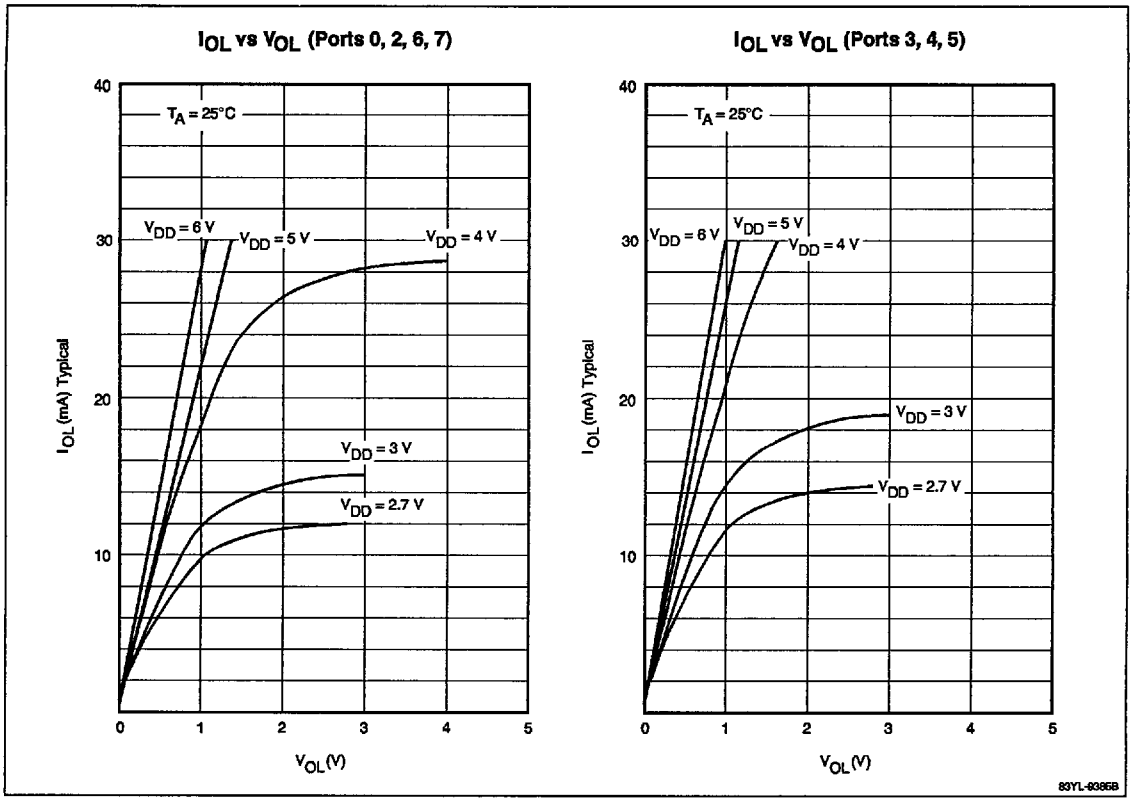
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Figure 19. DC Characteristics, I_{DD} vs V_{DD} (μPD7530x/31x, Standard Grade) (Sheet 2 of 2)



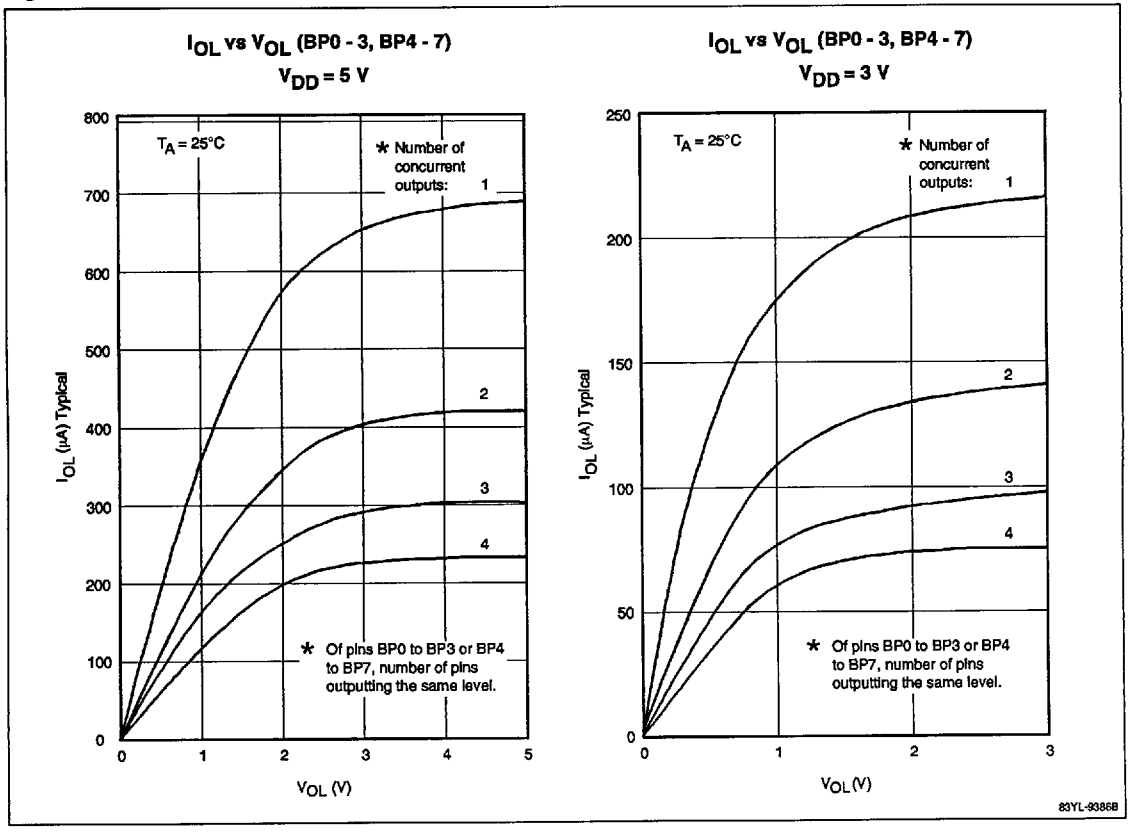
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Figure 20. DC Characteristics, I_{OL} vs V_{OL} (μPD7530x/31x, Standard Grade) (Sheet 1 of 2)



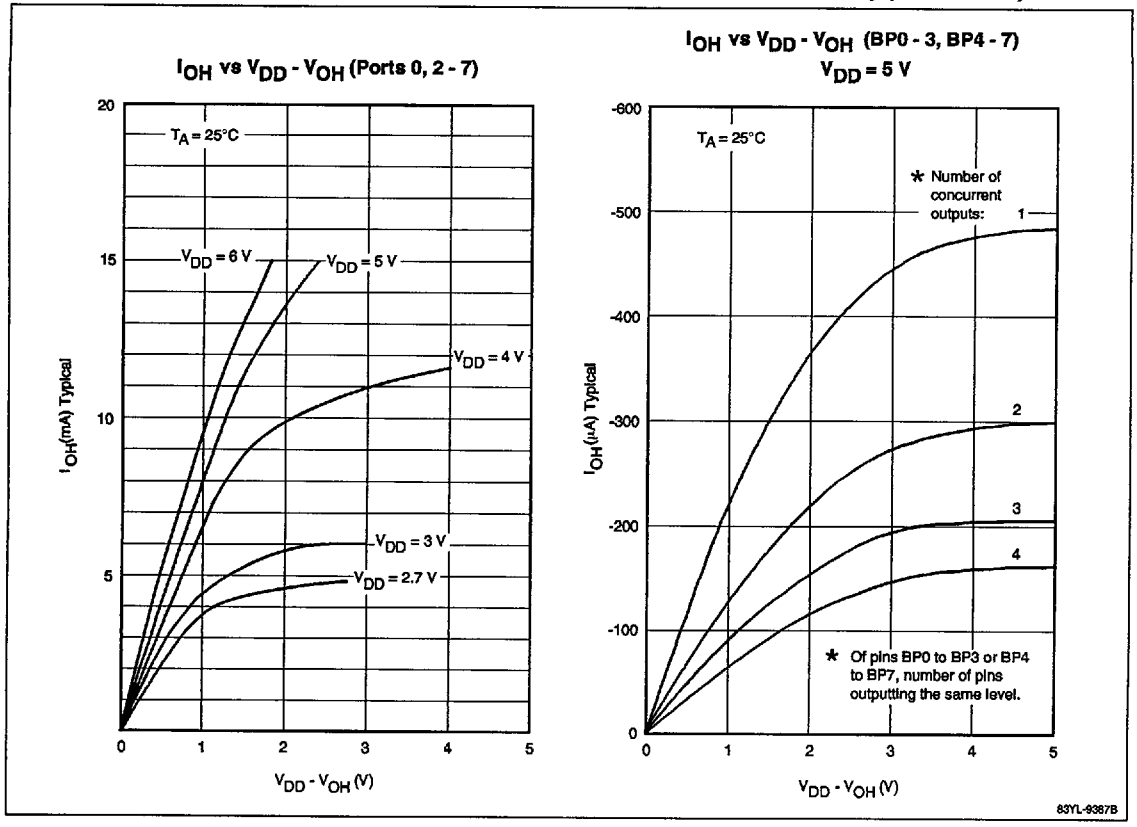
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Figure 20. DC Characteristics, I_{OL} vs V_{OL} (μPD7530x/31x, Standard Grade) (Sheet 2 of 2)



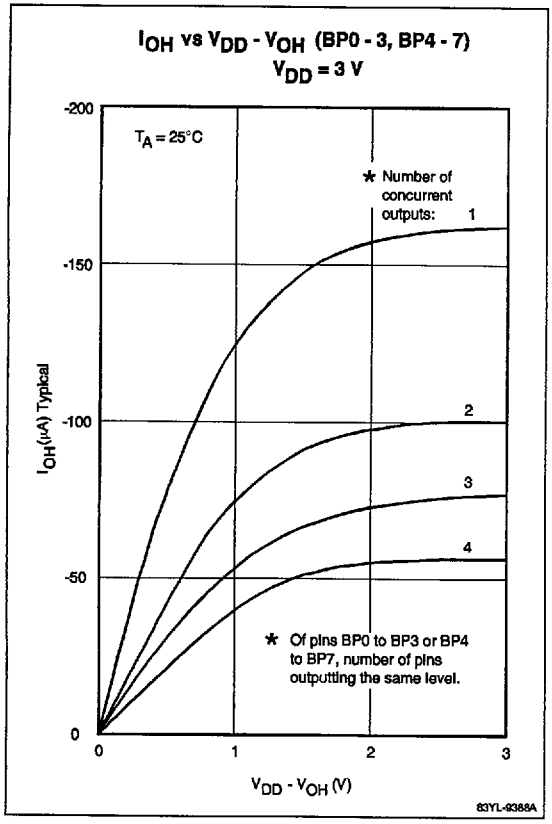
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Figure 21. DC Characteristics, I_{OH} vs V_{DD}–V_{OH} (μPD7530x/31x, Standard Grade) (Sheet 1 of 2)



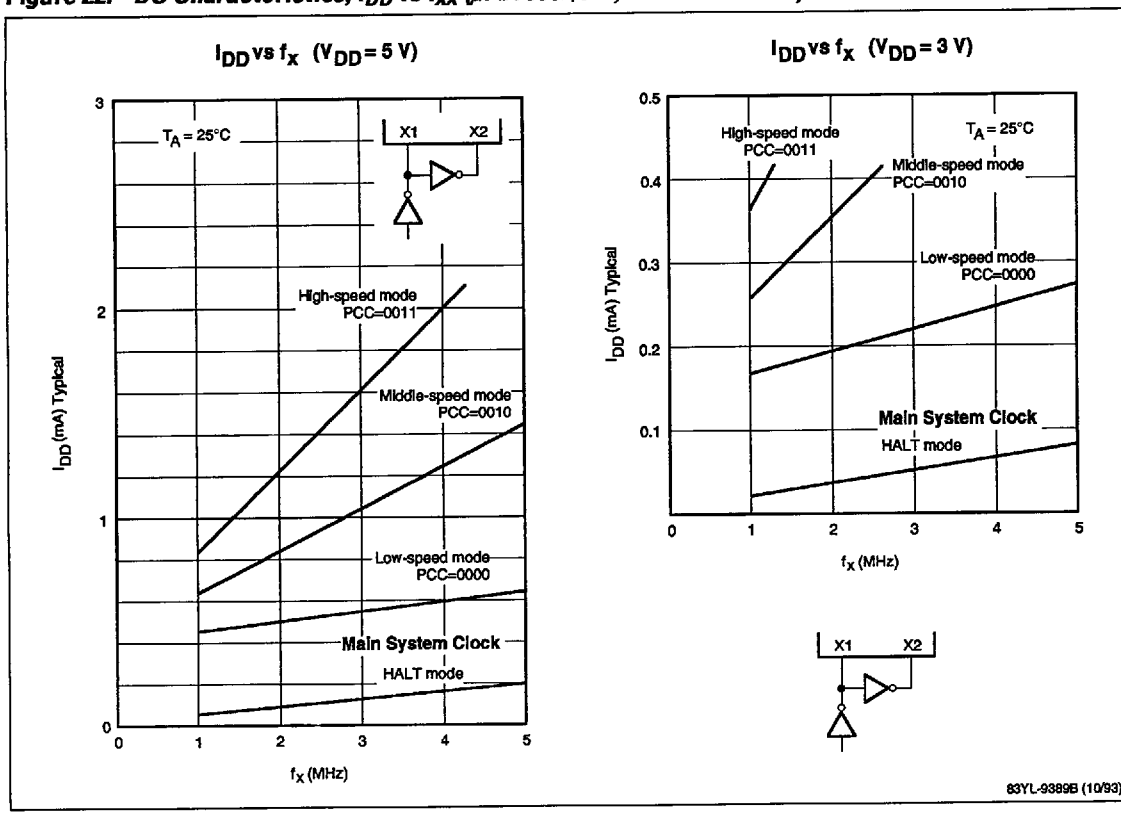
6427525 0052708 280

Figure 21. DC Characteristics, I_{OH} vs V_{DD}–V_{OH} (μPD7530x/31x, Standard Grade) (Sheet 2 of 2)



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Figure 22. DC Characteristics, I_{DD} vs f_{XX} (μPD7530x/31x, Standard Grade)



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AC Characteristics (μPD7530x/31xP316A)

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V; refer to figures 23 through 27

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time (Note 1)	t_{CY} (figure 24)	0.95		64	μs	Main system clock; V_{DD} = 4.5 to 6.0 V
		3.8		64	μs	Main system clock; V_{DD} = 2.7 to 6.0 V
		114	122	125	μs	Subsystem clock
TI0 input frequency	f_{TI} (figure 25)	0		1	MHz	V_{DD} = 4 5 to 6.0 V
		0		275	kHz	V_{DD} = 2.7 to 6.0 V
TI0 input high-and low-level width	t_{TIH}, t_{TIL} (figure 25)	0.48			μs	V_{DD} = 4.5 to 6.0 V
		1.8			μs	V_{DD} = 2.7 to 6.0 V
Interrupt inputs high-and low-level width	t_{INTH}, t_{INTL} (figure 26)	(Note 2)			μs	INT0
		10			μs	INT1, 2, 4
		10			μs	KR0-KR7
$\overline{\text{RESET}}$ low-level width	t_{RSL} (figure 27)	10			μs	After $V_{DD} \geq$ 2.7 V

Notes:

(1) Cycle time (minimum instruction execution time) is determined by the frequency of the oscillator connected to the microcomputer, system clock control register (SCC), and the processor clock control (PCC). See figure 24.

(2) $2t_{CY}$ or $128/f_X$, depending on the setting of the interrupt mode register (IM0).

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Figure 23. AC Timing Measurement Points (except X1 and XT1)

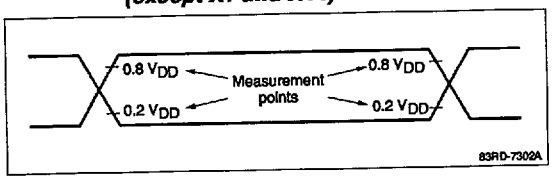


Figure 24. Main System Clock Operation; t_{CY} vs V_{DD} (μPD7530x/31x/P316A)

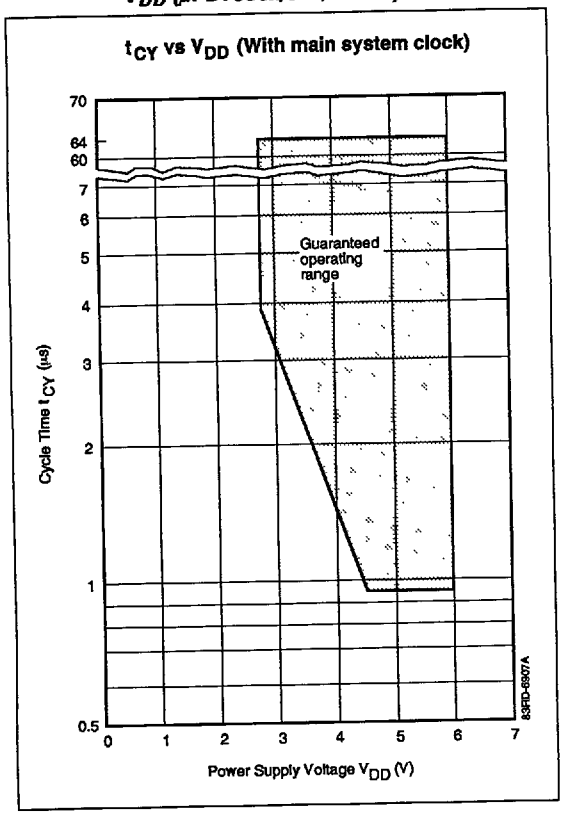


Figure 25. TI0 Timing

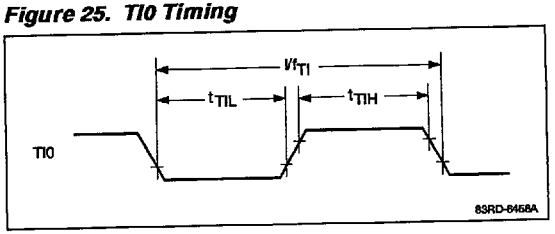


Figure 26. Interrupt Input Timing

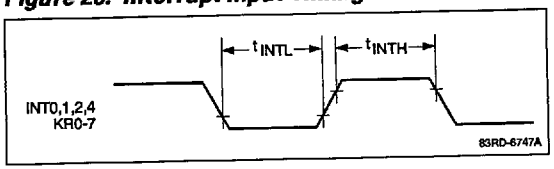
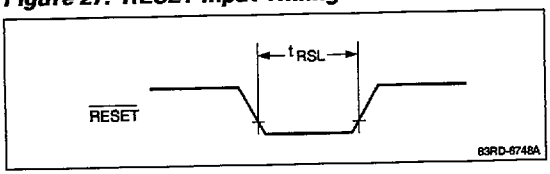


Figure 27. $\overline{RESET}$ Input Timing



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Serial Interface, 2/3-Line Serial I/O Mode; Internal $\overline{SCK}$ Output (μPD7530x/31x/P316A)

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY1}	1600			ns	V_{DD} = 4.5 to 6.0 V
		3800			ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ high- and low-level width	t_{KH1}, t_{KL1}	0.5 t_{KCY1} − 50			ns	V_{DD} = 4.5 to 6.0 V
		0.5 t_{KCY1} − 150			ns	V_{DD} = 2.7 to 6.0 V
SI setup time to $\overline{SCK}$ ↑	t_{SIK1}	150			ns	
SI hold time from $\overline{SCK}$ ↑	t_{KSI1}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time	t_{KSO1}			250	ns	V_{DD} = 4.5 to 6.0 V (Note)
				1000	ns	V_{DD} = 2.7 to 6.0 V (Note)

Note: R_L = 1 kΩ and C_L = 100 pf are load resistance and load capacitance for the SO line.

Serial Interface, 2/3-Line Serial I/O Mode; External $\overline{SCK}$ Input (μPD7530x/31x/P316A)

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY2}	800			ns	V_{DD} = 4.5 to 6.0 V
		3200			ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ high- and low-level width	t_{KH2}, t_{KL2}	400			ns	V_{DD} = 4.5 to 6.0 V
		1600			ns	V_{DD} = 2.7 to 6.0 V
SI setup time to $\overline{SCK}$ ↑	t_{SIK2}	100			ns	
SI hold time from $\overline{SCK}$ ↑	t_{KSI2}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time	t_{KSO2}			300	ns	V_{DD} = 4.5 to 6.0 V (Note)
				1000	ns	V_{DD} = 2.7 to 6.0 V (Note)

Note: R_L = 1 kΩ and C_L = 100 pf are load resistance and load capacitance for the SO line.

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Serial Interface, SBI Mode; Internal $\overline{SCK}$ Output (Master) (μPD7530x/31x/P316A)

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY3}	1600			ns	V_{DD} = 4.5 to 6.0 V
		3800			ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ high- and low-level width	t_{KH3}, t_{KL3}	0.5 t_{KCY3} − 50			ns	V_{DD} = 4.5 to 6.0 V
		0.5 t_{KCY3} − 150			ns	V_{DD} = 2.7 to 6.0 V
SB0, SB1 setup time to $\overline{SCK}$ ↑	t_{SIK3}	150			ns	
SB0, SB1 hold time from $\overline{SCK}$ ↑	t_{KSI3}	0.5 t_{KCY3}			ns	
$\overline{SCK}$ ↓ to SB0, SB1 output delay time	t_{KSO3}	0		250	ns	V_{DD} = 4.5 to 6.0 V (Note)
		0		1000	ns	V_{DD} = 2.7 to 6.0 V (Note)
$\overline{SCK}$ ↑ to SB0, SB1 ↓	t_{KSB}	t_{KCY3}			ns	
SB0, SB1 ↓ to $\overline{SCK}$ ↓	t_{SBK}	t_{KCY3}			ns	
SB0, SB1 low-level width	t_{SBL}	t_{KCY3}			ns	
SB0, SB1 high-level width	t_{SBH}	t_{KCY3}			ns	

Note: R_L = 1 kΩ and C_L = 100 pf are load resistance and load capacitance for the SB0, SB1 output lines.

Serial Interface, SBI Mode; External $\overline{SCK}$ Input (Slave) (μPD7530x/31x/P316A)

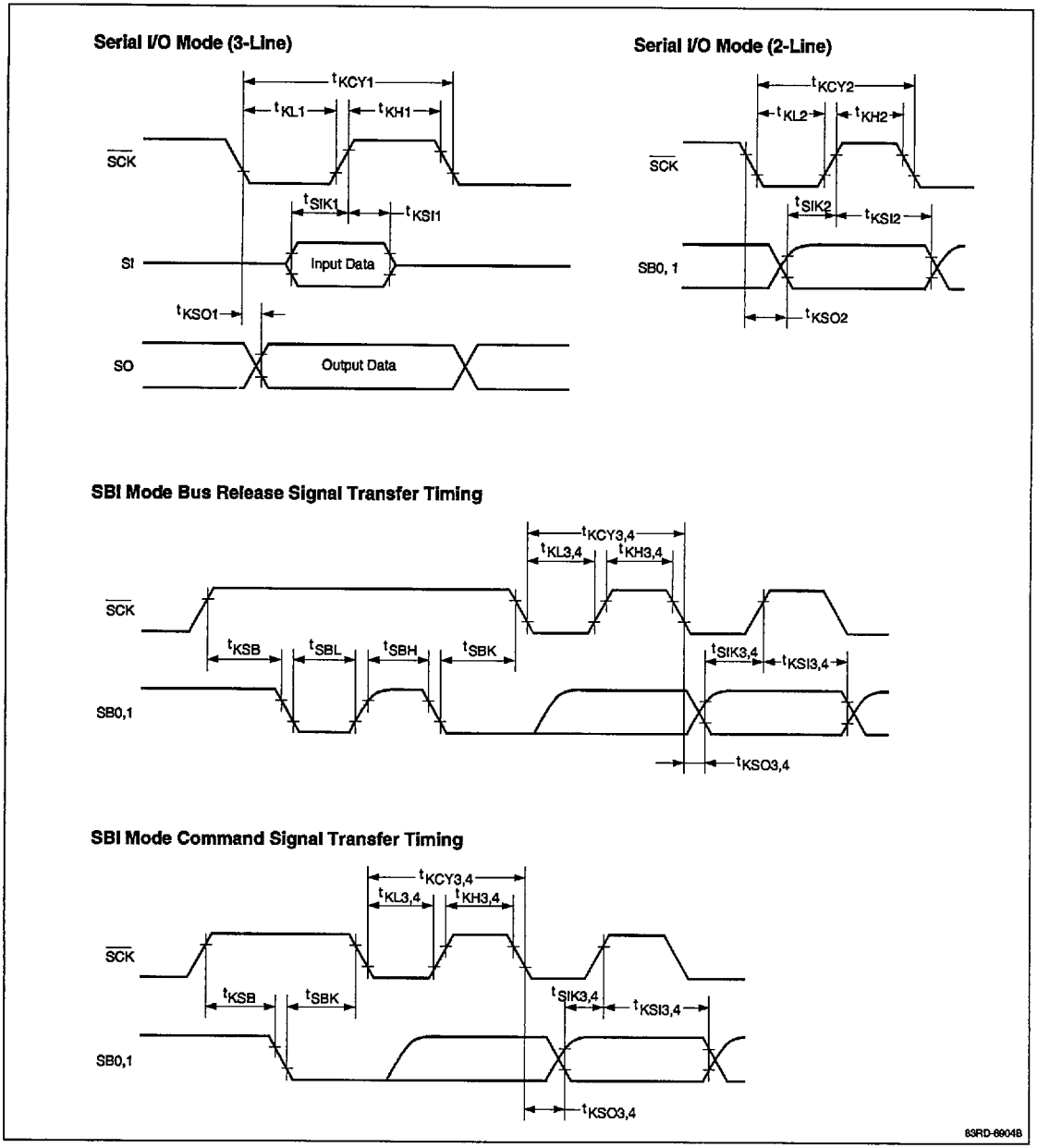
T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY4}	800			ns	V_{DD} = 4.5 to 6.0 V
		3200			ns	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ high- and low-level width	t_{KH4}, t_{KL4}	400			ns	V_{DD} = 4.5 to 6.0 V
		1600			ns	V_{DD} = 2.7 to 6.0 V
SB0, SB1 setup time to $\overline{SCK}$ ↑	t_{SIK4}	100			ns	
SB0, SB1 hold time from $\overline{SCK}$ ↑	t_{KSI4}	0.5 t_{KCY4}			ns	
$\overline{SCK}$ ↓ to SB0, SB1 output delay time	t_{KSO4}	0		300	ns	V_{DD} = 4.5 to 6.0 V (Note)
		0		1000	ns	V_{DD} = 2.7 to 6.0 V (Note)
$\overline{SCK}$ ↑ to SB0, SB1 ↓	t_{KSB}	t_{KCY4}			ns	
SB0, SB1 ↓ to $\overline{SCK}$ ↓	t_{SBK}	t_{KCY4}			ns	
SB0, SB1 low-level width	t_{SBL}	t_{KCY4}			ns	
SB0, SB1 high-level width	t_{SBH}	t_{KCY4}			ns	

Note: R_L = 1 kΩ and C_L = 100 pf are load resistance and load capacitance for the SB0, SB1 output lines.

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Figure 28. Serial Interface Timing



6427525 0052715 410

Data Memory STOP Mode; Low-Voltage Data Retention Characteristics

T_A = −40 to +85°C; refer to figure 29

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		6.0	V	
Data retention current (Note 1)	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V; XT1 = 0
Release signal set time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 2)	t_{WAIT}		(Notes 3, 4)		ms	Release by $\overline{\text{RESET}}$ input
			(Note 3)		ms	Release by interrupt request

Notes:

(1) Excludes current in the internal pullup resistors and LCD resistor ladder.

(2) Oscillation stabilization WAIT time is the time during which the CPU is stopped and the crystal is stabilizing. This time is required to prevent unstable operation while the oscillation is started. The interval timer can be used to delay the CPU from executing instructions using the basic interval timer mode register (BTM) according to the following table:

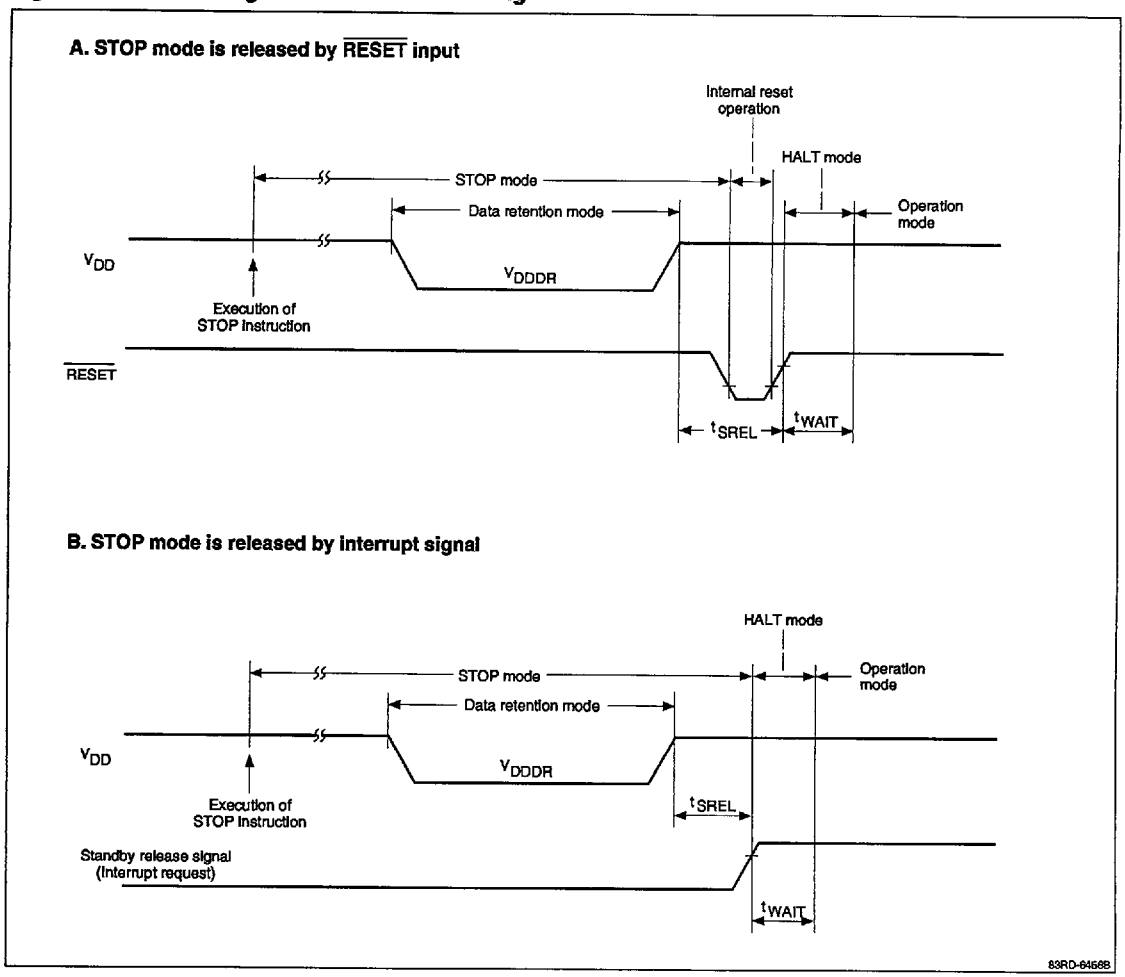
BTM3	BTM2	BTM1	BTM0	WAIT Time (f_X = 4.19 MHz)
–	0	0	0	$2^{20}/f_X$ (250 ms approx)
–	0	1	1	$2^{17}/f_X$ (31.3 ms approx)
–	1	0	1	$2^{15}/f_X$ (7.82 ms approx)
–	1	1	1	$2^{13}/f_X$ (1.95 ms approx)

(3) Consult the manufacturer's resonator or crystal specification sheet for this value.

(4) The interval timer will cause a delay of $2^{17}/f_X$ after a reset.

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Figure 29. Low-Voltage Data Retention Timing



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Recommended Ceramic Resonators (μPD75P308)

V_{DD} = 4.75 to 5.25 V; T_A = −10 to +70°C

Manufacturer	Part Number	C1 (pF)	C2 (pF)	Remarks
Murata	CSA 2.00MG	30	30	
	CSA 4.19MG	30	30	
	CSA 4.91MGU	30	30	
	CST 4.19MG	(Note)	(Note)	

Note: 30 pF capacitors are internally provided.

DC Characteristics (μPD75P308)

T_A = −10 to +70°C; V_{DD} = 5 V ± 5%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Ports 2, 3
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	Ports 0, 1, 6, 7; $\overline{\text{RESET}}$
	V_{IH3}	0.7 V_{DD}		10	V	Ports 4, 5; open drain
	V_{IH4}	V_{DD} − 0.5		V_{DD}	V	X1, X2, XT1
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	Ports 2, 3, 4, 5
	V_{IL2}	0		0.2 V_{DD}	V	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$
	V_{IL3}	0		0.4	V	X1, X2, XT1
High-level output voltage	V_{OH1}	V_{DD} − 1.0			V	Ports 0, 2, 3, 6, 7, BIAS; I_{OH} = −1 mA
	V_{OH2}	V_{DD} − 2.0			V	BP_{0-7}; I_{OH} = −100 μA (Note 1)
Low-level output voltage	V_{OL1}		0.4	2.0	V	Ports 3, 4, 5; I_{OL} = 15 mA
				0.4	V	All output pins; I_{OL} = 1.6 mA
	V_{OL2}			0.2 V_{DD}	V	SB0, SB1; open drain pullup resistor ≥ 1kΩ
	V_{OL3}			1.0	V	BP_{0-7}; I_{OL} = 100 μA (Note 1)
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH3}			20	μA	Ports 4 and 5; V_{IN} = 10 V
Low-level input leakage current	I_{LIL1}			−3	μA	All except X1, X2, and XT1; V_{IN} = 0 V
	I_{LIL2}			−20	μA	X1, X2, and XT1; V_{IN} = 0 V
High-level output leakage current	I_{LOH1}			3	μA	All output pins except ports 4, 5; V_{OUT} = V_{DD}
	I_{LOH2}			20	μA	Ports 4, 5; V_{OUT} = 10 V
Low-level output leakage current	I_{LOL}			−3	μA	V_{OUT} = 0 V
Internal pullup resistor	R_{LI}	15	40	80	kΩ	Ports 0-3, 6, 7 (except PO_0); V_{IN} = 0 V
LCD drive voltage	V_{LCD}	2.5		V_{DD}	V	
LCD output voltage deviation; common (Note 7)	V_{ODC}	0		±0.2	V	I_O = ±5 μA; V_{LCD} = V_{LCD0} = 2.7 V to V_{DD}; V_{LCD1} = 2/3V_{LCD} V_{LCD2} = 1/3V_{LCD}
LCD output voltage deviation; segment (Note 7)	V_{ODS}	0		±0.2	V	I_O = ±1 μA; V_{LCD} = V_{LCD0} = 2.7 V to V_{DD}; V_{LCD1} = 2/3V_{LCD} V_{LCD2} = 1/3V_{LCD}

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DC Characteristics (μPD75P308) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply current (Note 2)	I_{DD1}		5.0	15.0	mA	(Notes 3, 4)
	I_{DD2}		500	1500	μA	HALT mode (Note 3)
	I_{DD3}		350	1000	μA	(Notes 5, 6)
			35	100	μA	HALT mode (Notes 5, 6)
	I_{DD4}		0.5	20	μA	STOP mode; XT1 = 0 V

Notes:

(1) When any two pins of BP0-BP3 or any two pins of BP4-BP7 are used simultaneously for output.

(2) Does not include pullup resistor current.

(3) 4.19-MHz crystal oscillator; C1 = C2 = 22 pF; subsystem clock running.

(4) Value during high-speed operation and the processor control clock (PCC) is set to 0011.

(5) Value when the system clock control register (SCC) is set to 1001; generation of the main system clock pulse is stopped, and the SCC is operated by the subsystem clock.

(6) 32-kHz crystal oscillator.

(7) Voltage deviation is the difference between the ideal value of segment or common output (V_{LCDn}; n = 0, 1, 2) and the output voltage.

AC Characteristics (μPD75P308)

T_A = −10 to +70°C; V_{DD} = 5 V ± 5%; refer to figure 30

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time (minimum instruction execution time, Note 1)	t_{CY} (figure 29)	0.95		64	μs	Main system clock
		114	122	125	μs	Subsystem clock
TI0 input frequency	f_{TI} (figure 24)	0		1	MHz	
TI0 input high- and low-level width	t_{TIH}, t_{TIL} (figure 24)	0.48			μs	
Interrupt inputs high- and low-level width	t_{INTH}, t_{INTL} (figure 25)	(Note 2)			μs	INT0
		10			μs	INT1, INT2, INT4 KR0–KR7
$\overline{RESET}$ low-level width	t_{RSL} (figure 26)	10			μs	After $V_{DD} \geq 4.75$ V

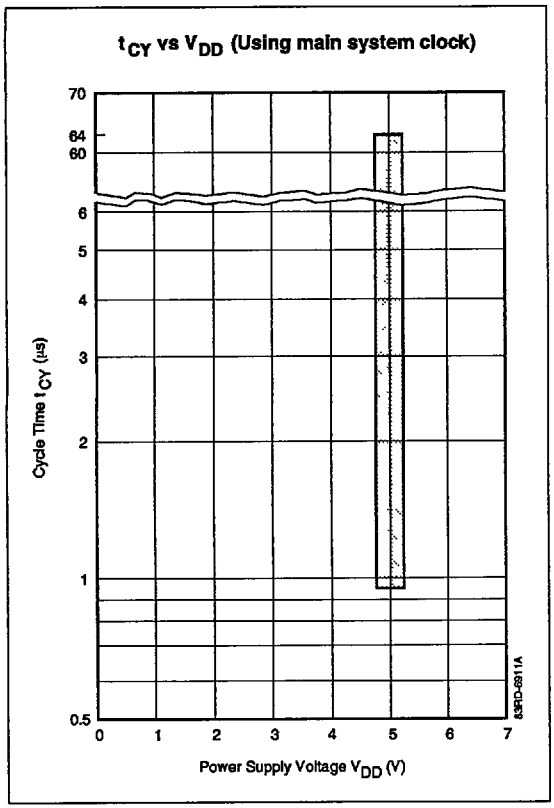
Notes:

(1) Cycle time is determined by the frequency of the oscillator connected to the microcomputer, system clock control register (SCC), and the processor clock control (PCC).

(2) $2t_{CY}$ or $128/f_X$, depending on the setting of the interrupt mode register (IM0).

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Figure 30. Guaranteed Operating Range (μPD75P308)



Serial Interface, 2/3-Line Serial I/O Mode; Internal $\overline{SCK}$ Output (μPD75P308)

T_A = −10 to +70°C; V_{DD} = 5 V ± 5%; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY1}	1600			ns	Output
$\overline{SCK}$ high- and low-level width	t_{KH1}, t_{KL1}	0.5 t_{KCY1} − 50			ns	Output
SI setup time (against $\overline{SCK}$ ↑)	t_{SIK1}	150			ns	
SI hold time (against $\overline{SCK}$ ↑)	t_{KSI1}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time	t_{KSO1}			250	ns	

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Serial Interface, 2/3-Line Serial I/O Mode; External $\overline{SCK}$ Input (μPD75P308)

T_A = −10 to +70°C; V_{DD} = 5 V ± 5%; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY2}	800			ns	Input
$\overline{SCK}$ high- and low-level width	t_{KH2}, t_{KL2}	400			ns	Input
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK2}	100			ns	
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI2}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time	t_{KSO2}			300	ns	

Serial Interface, SBI Mode; Internal $\overline{SCK}$ Output (Master) (μPD75P308)

T_A = −10 to +70°C; V_{DD} = 5 V ± 5%; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY3}	1600			ns	
$\overline{SCK}$ high- and low-level width	t_{KH3}, t_{KL3}	0.5 t_{KCY3} − 50			ns	
SB0, SB1 setup time to $\overline{SCK}$ ↑	t_{SIK3}	150			ns	
SB0, SB1 hold time from $\overline{SCK}$ ↑	t_{KSI3}	0.5 t_{KCY3}			ns	
$\overline{SCK}$ ↓ to SB0, SB1 output delay time	t_{KSO3}	0		250	ns	
$\overline{SCK}$ ↑ to SB0, SB1 ↓	t_{KSB}	t_{KCY3}			ns	
SB0, SB1 ↓ to $\overline{SCK}$ ↓	t_{SBK}	t_{KCY3}			ns	
SB0, SB1 low-level width	t_{SBL}	t_{KCY3}			ns	
SB0, SB1 high-level width	t_{SBH}	t_{KCY3}			ns	

Serial Interface, SBI Mode; External $\overline{SCK}$ Input (Slave) (μPD75P308)

T_A = −10 to +70°C; V_{DD} = 5 V ± 5%; refer to figure 28

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY4}	800			ns	
$\overline{SCK}$ high- and low-level width	t_{KH4}, t_{KL4}	400			ns	
SB0, SB1 setup time to $\overline{SCK}$ ↑	t_{SIK4}	100			ns	
SB0, SB1 hold time from $\overline{SCK}$ ↑	t_{KSI4}	0.5 t_{KCY4}			ns	
$\overline{SCK}$ ↓ to SB0, SB1 output delay time	t_{KSO4}	0		300	ns	
$\overline{SCK}$ ↑ to SB0, SB1 ↓	t_{KSB}	t_{KCY4}			ns	
SB0, SB1 ↓ to $\overline{SCK}$ ↓	t_{SBK}	t_{KCY4}			ns	
SB0, SB1 low-level width	t_{SBL}	t_{KCY4}			ns	
SB0, SB1 high-level width	t_{SBH}	t_{KCY4}			ns	

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PROM PROGRAMMING

The PROM in the μPD75316 family is one-time programmable (OTP) or ultraviolet erasable (UVE). In the μPD part numbers below, GF and K denote QFP and LCC packages, respectively.

μPD	PROM	Bytes	Package
75P308GF	OTP	8064	QFP
75P308K	UVE	8064	LCC w/window
75P316AGF	OTP	16,256	QFP
75P316AK	UVE	16,256	LCC w/window

The PROM is programmed using the pins listed in table 7. Note that it is not necessary to enter an address since the address is updated by pulsing the clock pins. During programming, addresses are incremented by applying clock pulses to the X1 and X2 input pins. When +6 V is applied to V_{DD} and +12.5 V to V_{PP}, the PROM is placed in the write/verify mode. Pins MD0 - MD3 select the applicable operation as shown in table 8.

Table 7. PROM Write and Verify Pin Functions

Pin	Function
X1, X2	Pulsed to increment address during PROM write/verify operation. The inverse of X1 is applied to X2. Note that these pins are also pulsed during a read.
MD0 - MD3	Operation mode selection pins.
$P4_0$ - $P4_3$ (four low-order bits) $P5_0$ - $P5_3$ (four high-order bits)	8-bit data input/output pins for write/verify
V_{DD}	Supply voltage. Normally 5 volts; 6 volts is applied during write/verify
V_{PP}	Normally 5 volts; 12.5 volts is applied during write/verify

Note: To prevent erasure, the window on the ceramic LCC package of the 75P308K/316AK should be covered with an opaque film. Since the μPD75P308GF/P316GFAGF do not have windows, the contents of their EPROM cannot be erased.

Table 8. Mode Selection

V_{PP} = +12.5 V; V_{DD} = +6.0 V

MD0	MD1	MD2	MD3	Operation Mode
1	0	1	0	Program memory address clear
0	1	1	1	Write mode
0	0	1	1	Verify mode
1	x	1	1	Program inhibit

x = Don't care.

PROM Write/Verify Procedure

PROMs can be written at high speed using the following procedure. Figure 31 is the timing diagram.

(1) Connect unused pins to V_{SS} through resistors. Set the X1 pin low.

(2) Supply +5 volts to V_{DD} and V_{PP} pins.

(3) Wait 10 μs.

(4) Select program memory address clear mode.

(5) Supply +6 volts to V_{DD} pin and +12.5 volts to V_{PP} pin.

(6) Select program inhibit mode.

(7) Write data in the 1-ms write mode.

(8) Select program inhibit mode.

(9) Select verify mode. If data is correct, proceed to step 10. If not, repeat steps 7, 8, and 9 up to a maximum of 20 times. If data is still incorrect, terminate programming and declare the device defective.

(10) Perform one additional write with an MD0 pulse width (in ms) equal to the number of writes performed in step 7. For example, MD0 = 10 ms if the location was written to 10 times in step 7.

(11) Select program inhibit mode.

(12) Apply four pulses to the X1 pin to increment the program memory address by one.

(13) Repeat steps 7-12 until the end address is reached.

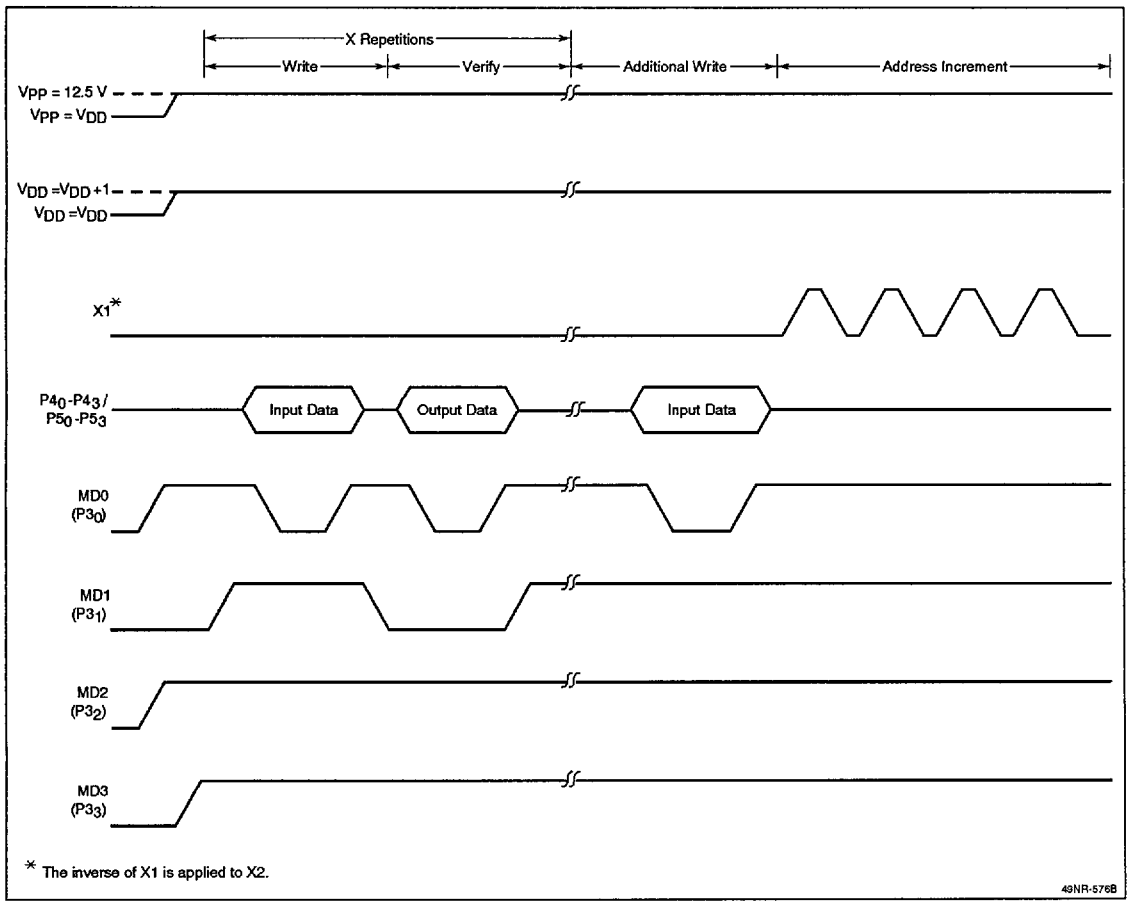
(14) Select program memory address clear mode.

(15) Return V_{DD} and V_{PP} pins to +5 volts.

(16) Turn off power.

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Figure 31. PROM Write/Verify Cycle Timing



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PROM Read Procedure

The PROM contents can be read by using the following procedure. Figure 32 is the timing diagram for steps 2-9.

(1) Connect unused pins to V_{SS} through resistors. Set the X1 pin low.

(2) Supply +5 volts to V_{DD} and V_{PP} pins.

(3) Wait 10 μs.

(4) Select program memory address clear mode.

(5) Supply +6 volts to V_{DD} pin and +12.5 volts to V_{PP} pin.

(6) Select program inhibit mode.

(7) Select verify mode. Apply four pulses to the X1 pin. The data in address 0 will be output. Every additional four clock pulses will output the data stored in the next address.

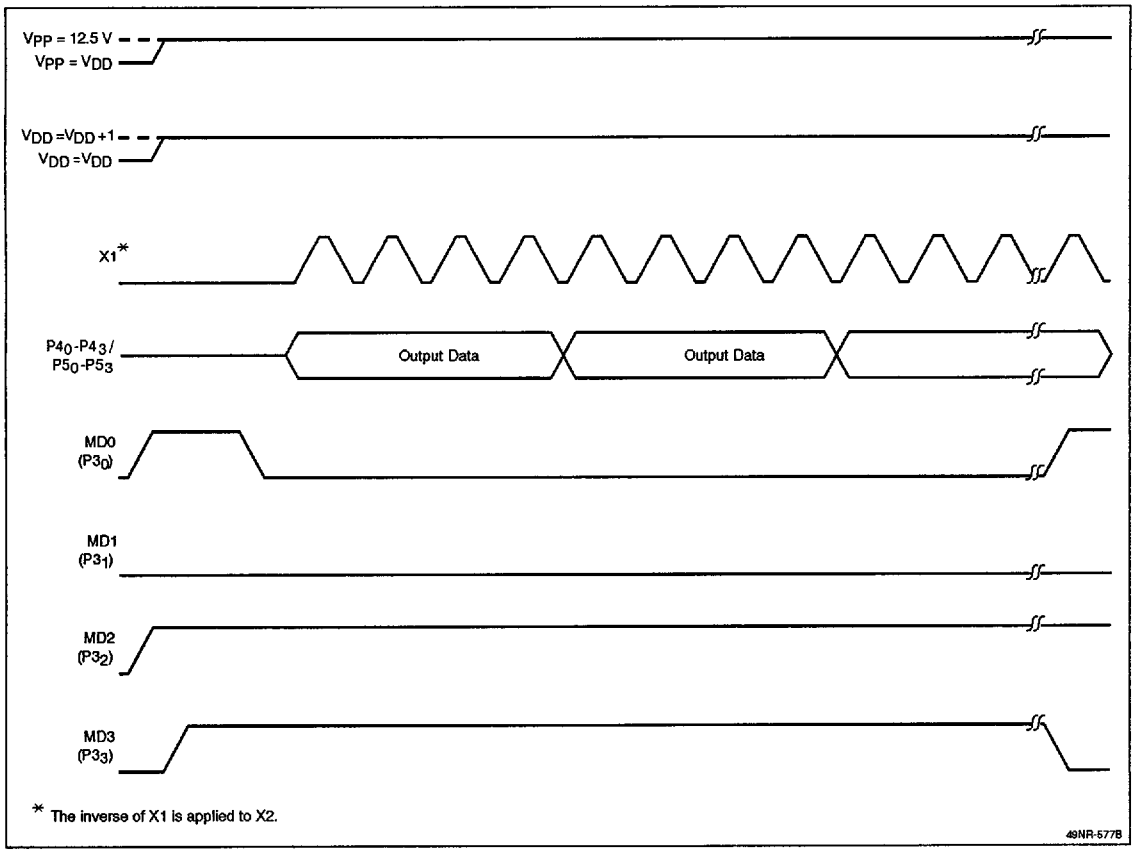
(8) Select program inhibit mode.

(9) Select program memory address clear mode.

(10) Return V_{DD} and V_{PP} pins to +5 volts.

(11) Turn off power.

Figure 32. PROM Read Cycle Timing



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Program Erasure (μPD75P308K/P316AK)

The UVE PROM (EPROM) can be erased by light rays whose wavelength is shorter than about 250 nm. The programmed data contents may also be erased if the uncovered window is exposed to direct sunlight or a fluorescent light for several hours. Thus, to protect the data contents, cover the window with an opaque film. NEC attaches quality-tested shading film to the UVE PROM products for shipping.

For normal EPROM erasure, place the device under an ultraviolet light source (254 nm). The minimum radiation exposure required to erase the written data completely is 15 Ws/cm^2 (ultraviolet ray strength times erase time). This corresponds to about 15 to 20 minutes with a a UV lamp of 12,000 μW/cm^2. However, the time may be prolonged if the UV lamp is old or if the device window is dirty. The distance between the light source and the window should be 2.5 cm or less.

DC Programming Characteristics (μPD75P308/P316A)

T_A = 25 ±5°C; V_{DD} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V; V_{SS} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	All except X1, X2
	V_{IH2}	V_{DD} – 0.5		V_{DD}	V	X1, X2
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	All except X1, X2
	V_{IL2}	0		0.4	V	X1, X2
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-level output voltage	V_{OH}	V_{DD} – 1.0			V	I_{OH} = –1 mA
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} supply current	I_{DD}			30	mA	
V_{PP} supply current	I_{PP}			30	mA	MD0 = V_{IL}; MD1 = V_{IH}

Notes:

(1) V_{PP} must not exceed +13.5 V, including overshoot.

(2) V_{DD} must be applied before V_{PP}. V_{DD} should be removed after V_{PP} is removed.

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AC Programming Characteristics (μPD75P308/P316A)

T_A = 25 ± 5°C; V_{DD} = 6.0 ± 0.25 V; V_{PP} = 12.5 ± 0.3 V; V_{SS} = 0 V; refer to figures 33 and 34

Parameter	Symbol	(Note 1)	Min	Typ	Max	Unit	Conditions
Address setup time to MD0 ↓ (Note 2)	t_{AS}	t_{AS}	2			μs	
MD1 setup to MD0 ↓	t_{M1S}	t_{OES}	2			μs	
Data setup to MD0 ↓	t_{DS}	t_{DS}	2			μs	
Address hold from MD0 ↑ (Note 2)	t_{AH}	t_{AH}	2			μs	
Data hold from MD0 ↑	t_{DH}	t_{DH}	2			μs	
Data output float delay from MD0 ↑	t_{DF}	t_{DF}	0		130	ns	
V_{PP} setup to MD3 ↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} setup to MD3 ↑	t_{VDS}	t_{VCS}	2			μs	
Initialized program pulse width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95		21	ms	
MD0 setup to MD1 ↑	t_{M0S}	t_{CES}	2			μs	
Data output delay from MD0 ↓	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 hold from MD0 ↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50\ \mu s$
MD1 recovery from MD0 ↓	t_{M1R}	t_{OR}	2			μs	$t_{M1H} + t_{M1R} \geq 50\ \mu s$
Program counter reset	t_{PCR}	—	10			μs	
X1 input high and low-level width	t_{XH}, t_{XL}	—	0.125			μs	
X1 input frequency	f_X	—			4.19	MHz	
Initial mode set	t_I	—	2			μs	
MD3 setup to MD1 ↑	t_{M3S}	—	2			μs	
MD3 hold from MD1 ↓	t_{M3H}	—	2			μs	
MD3 setup to MD0 ↓	t_{M3SR}	—	2			μs	During Program Read cycle
Address to data output delay time (Note 2)	t_{DAD}	t_{ACC}			2	μs	
Address to data output hold time (Note 2)	t_{HAD}	t_{OH}	0		130	ns	
MD3 output hold from MD0 ↑	t_{M3HR}	—	2			μs	
Data output float delay from MD3 ↓	t_{DFR}	—			2	μs	

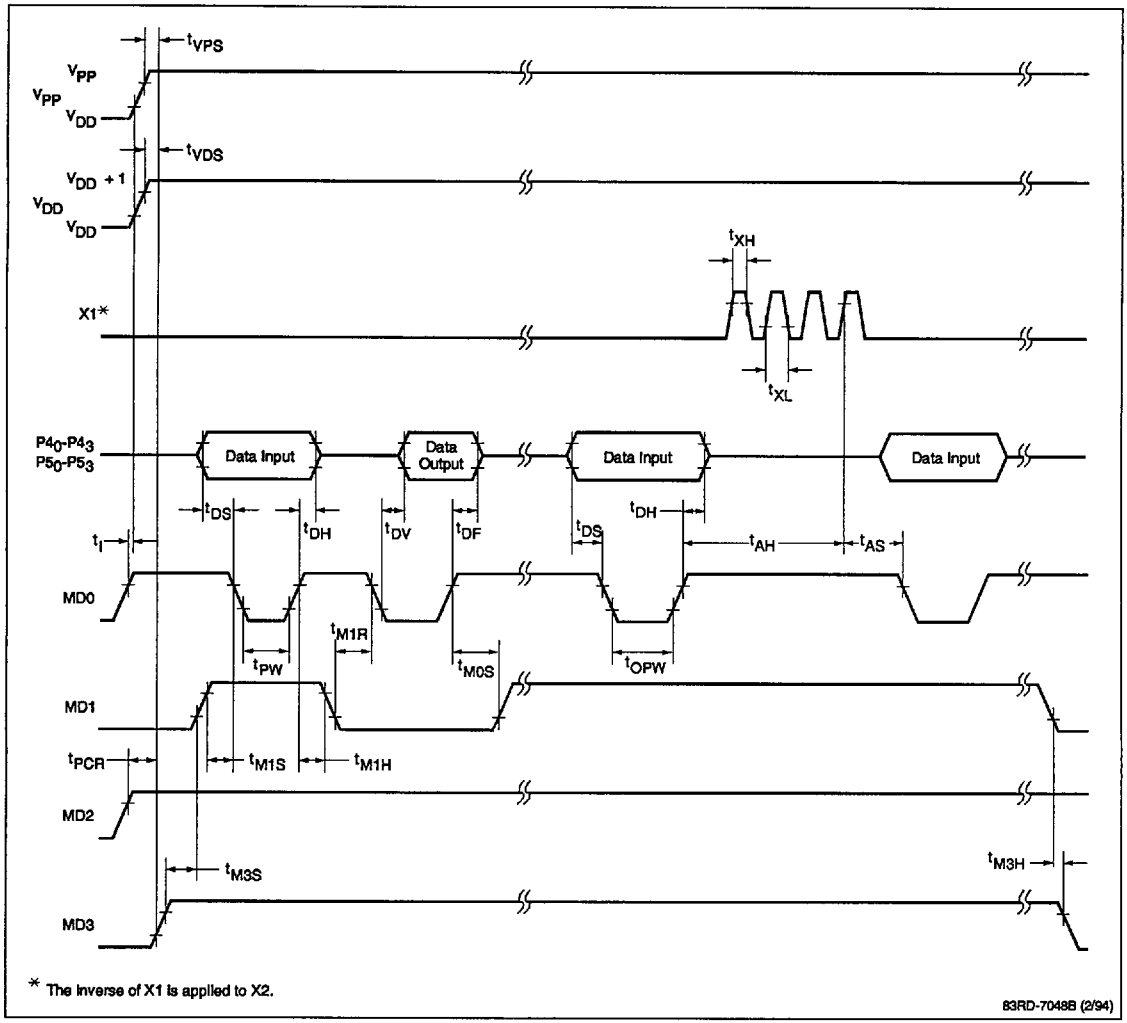
Notes:

(1) These symbols correspond to those on the μPD27C256/C256A EPROM.

(2) The internal address signal is incremented by one at the rising edge of the fourth X1 pulse; it is not connected to an external pin.

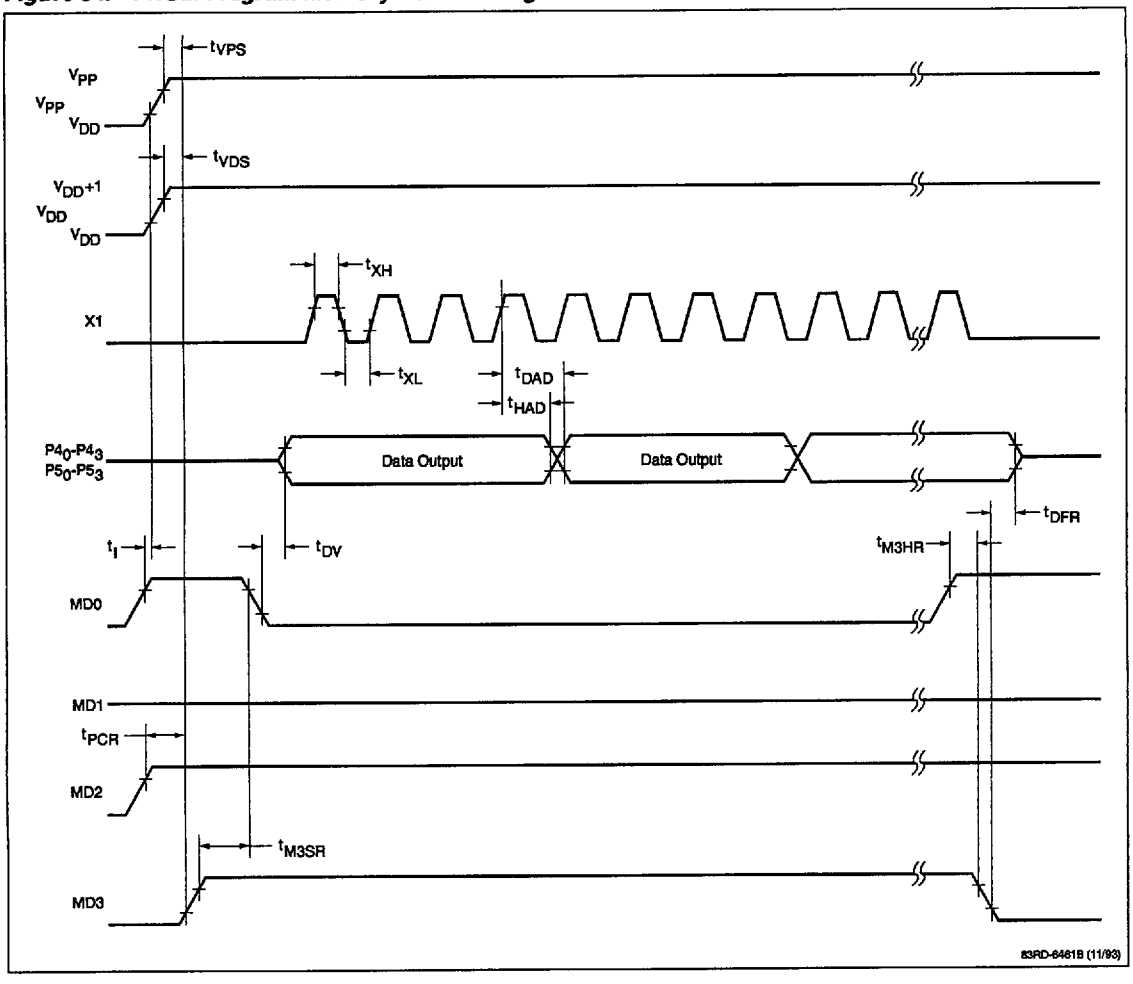
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Figure 33. PROM Program Memory Write Timing



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Figure 34. PROM Program Memory Read Timing



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INSTRUCTION SET

There are four CPUs in the μPD75x product line and one instruction set. The CPUs are (1) expanded high-end CPU, (2) high-end CPU, (3) standard CPU, and the (4) low-end CPU. The expanded high-end CPU uses the complete instruction set. The high-end CPU, standard CPU, and the low-end CPU use a subset of the instruction set. Table 1 shows the type of CPU in each μPD75x device.

Table 1. Type of CPU in Each μPD75x Device

Expanded High-end	μPD75117H, 75P117H; μPD75217, 75218,75P218; μPD75237, 75238, 75P238; μPD75517, 75518, 75P518
High-end	μPD75104, 75104A, 75106, 75108, 75108F, 75108A, 75P108, 75P108B, 75112, 75112F; μPD75116, 75116F, 75P116, 75116H; μPD75206, 75208, 75CG208, 75212A, 75216A, 75P216A, 75CG216A, 75236; μPD75336, 75P336; μPD75512, 75516, 75P516
Standard	μPD75004, 75006, 75008, 75P008, 75028, 75036, 75P036, 75048, 75P048, 75064, 75066, 75068, 75P068; μPD75268; μPD75304, 75304B, 75306, 75306B, 75308, 75308B, 75P308, 75312, 75312B, 75316, 75316B, 75P316, 75P316A, 75P316B; μPD75328, 75P328
Low-end	μPD75P402, 75402A

When the user assembles their program, they should designate the mask ROM device type rather than the OTP device at assembly time. This will prevent the user from using more ROM or RAM than is available on the mask ROM device. For example, the μPD75P108 or μPD75P116 can be used as an OTP for the μPD75104 device, but both OTP versions have more ROM and RAM than the μPD75104.

The user designates the device being used to the assembler using the -C command (-CXXX). This is not an optional command, and it must be input to the assembler. For example if the μPD75104 is being used, the user invokes the assembler by typing:

```
RA75X  FILENAME  -C104
```

The -C104 on the command line tells the assembler that the μPD75104 is being used. Once the assembler knows the chip, it will check to be sure the user does not exceed the amount of ROM or RAM, or use features not available on the chip

The μPD75x product line instruction set is unusually powerful for a 4-bit microcontroller. It contains instructions that operate on 1-bit, 4-bit, and 8-bit data. It contains 8-bit instructions which are generically equivalent to virtually every 4-bit instruction type. Specifically, the instruction set contains the following 8-bit instruction types:

- Arithmetic: ADD W/CARRY, ADD W/SKIP, SUB W/BORROW, SUB W/SKIP
- Logical: AND, OR, XOR
- Comparison: SKE (skip if equal)
- Transfer: MOV, MOVT, XCH, IN, OUT, PUSH, POP, BR, CALL
- Manipulation: INC W/SKIP, DEC W/SKIP

In addition, some of the 4-bit ports may be paired together to function as one 8-bit port. The combination of 8-bit ports and 8-bit instructions allows IN and OUT instructions to move a byte of data with one instruction.

The μPD75x product line provides unusual instructions including the following types.

- GETI instructions to reduce program size
- Skip instructions
- String instructions
- Table reference instructions
- 1-byte relative branch instructions

GETI Instructions

GETI instructions are used to compact code, thereby reducing the ROM size and hence product cost. In general, GETI instructions reduce code by 10%. If the program is 9K bytes long, using GETI instructions will result in an 8K-byte ROM-based product.

The GETI converts 2-byte instructions and pairs of 1-byte instructions into a single 1-byte instruction. After the code is written, the code is analyzed fo find the most frequently used 2-byte instructions and/or the most frequently used pairs of 1-byte instructions. A GETI table (2 bytes per entry with up to 48 entries) based upon the most frequently used instructions is made. The frequently used instructions in the code are replaced by their respective GETI instructions. When a GETI instruction is encountered, the CPU gets and executes the instruction from the GETI table.

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Because of the way it works, GETI is an acronym for "Get Instruction." An example is shown below:

```
        CSEG    IENT        ;This is the GETI table.
MOVA:   MOV     A,@HL       ;1-byte instruction.
        INCS    L           ;1-byte instruction.
INCR:   INCS    @HL         ;2-byte instruction.

        CSEG                ;This is a code segment.
Start   DI                  ;This is a GETI instruction;
        MOV     HL,#0F4H    ;it is 1-byte long.
        GETI    MOVA        ;Execution of this 1-byte
        MOV     A,#0FH      ;instruction will cause the two
                            ;1-byte instructions at MOVA in
                            ;the GETI table to be executed.
        EI                  ;Program continues after GETI
                            ;at the MOV A,#0FH instruction
```

The GETI instruction can also convert 3-byte branch and CALL instructions into a single 1-byte instruction. In this case, the GETI table contains the branch or subroutine address.

Skip Instructions

Skip instructions replace the need for a conditional branch. Usable with 1, 4, or 8 bits of data, they are available in arithmetic, comparison, transfer, and manipulation type instructions. All skip instructions are implemented such that if the skip condition is met, the next instruction is skipped. For example:

```
LOOP:   SKT     PORT3.1
        BR      !LOOP
        MOV     A,X
```

In this example, the instruction SKT PORT3.1 tests port 3 bit 1 for a one; this is the skip condition. If port 3 bit 1 is zero, the skip condition is not met and the CPU executes the next instruction, which branches to LOOP and retests port 3 bit 1. When port 3 bit 1 is a one, the skip condition is met; the next instruction (BR !LOOP) is skipped and the MOV A, X instruction is executed.

String Instructions

The μPD75x product line has two types of string effect Instructions:

(1) MOV A,#n4 or MOV XA,#n8

(2) MOV HL,#n8

String effect means to place the same type of instruction in consecutive addresses. Only the first instruction of a string is executed normally; the remainder of the same type instructions in the string are treated as NOPs. The string instructions increase efficiency when setting constants into an accumulator (register A or XA) or into a data pointer (register pair HL). For example:

```
A0:     MOV     A,#0H
A1:     MOV     A,#1H
XA7:    MOV     XA,#0F8H
        SET1    MBE
```

If the first instruction address in the string to be executed is A0, the two subsequent instructions (at A1 and at XA7) are treated as NOP instructions during program execution. The SET1 MBE instruction is the first instruction after A0 to be executed normally. If the first instruction address in the string to be executed is A1, the instruction at XA7 is treated as an NOP and the SET1 MBE instruction is the first after A1 to be executed normally.

Instruction Execution Times

The minimum instruction execution time is 0.95 μs with a 4.19-MHz clock. The PCC register can be used to program the CPU's instruction cycle time to 0.95, 1.91, or 15.3 μs; all three speeds presuppose a 4.19-MHz crystal. Reducing the CPU clock speed will reduce the microcontroller's power consumption.

The machine cycle column in the Instruction Set table lists the number of cycles required to execute the instruction. One machine cycle equals one CPU clock period ϕ. In the machine cycle column, S equals the number of extra machine cycles required for skip operation when executing a skip instruction:

S	Skip Operation
0	No skip
1	1- or 2-byte instruction or GETI instruction is skipped.
2	3-byte instruction is skipped (BR !addr, CALL !addr)

Symbols, Operand Formats, and Addressing Areas

Table 2 defines the instruction set registers, flags, and symbols. Table 3 defines the instruction set operands and table 4 describes the addressing areas.

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Table 2. Instruction Set Register, Flags, and Symbols

Symbol	Definition
A	A register; 4-bit accumulator
B	B register; 4-bit register
C	C register; 4-bit register
D	D register; 4-bit register
E	E register; 4-bit register
H	H register; 4-bit register
L	L register; 4-bit register
X	X register; 4-bit register
XA	XA register pair; 8-bit accumulator
BC	BC register pair; 8-bit register
DE	DE register pair; 8-bit register
DL	DL register pair; 8-bit register
HL	HL register pair; 8-bit register
XA'	XA' register pair; 8-bit register
BC'	BC' register pair; 8-bit register
DE'	DE' register pair; 8-bit register
HL'	HL' register pair; 8-bit register
PC	Program counter
SP	Stack pointer
CY	Carry flag; bit accumulator
PSW	Program status word
MBE	Memory bank enable flag
RBE	Register bank enable flag
PORTn	Port n (n = 0-15)
IME	Interrupt master enable flag
IPS	Interrupt priority selection register
IExxx	Interrupt enable flag
RBS	Register bank selection register
MBS	Memory bank selection register
PCC	Processor Clock Control Register
.	Separation between address and bit
(xx)	The contents addressed by xx
xxH	Hexadecimal data
∧	Logical AND
∨	Logical OR
∀	Logical Exclusive OR

Operation Representation Format and Description Method

An operand is entered in the operand field of each instruction according to the format of the instruction (see assembler specifications). When two or more entries are indicated in the description method, one should be selected. Capital letters and symbols must be entered exactly as shown. For immediate data, a proper numeric value or label should be entered as shown in table 3. See table 4 for a description of the addressing areas.

Table 3. Operand Formats

Symbol	Description
reg	X, A, B, C, D, E, H, L (reg = X, A, H, L for low-end CPU)
reg1	X, B, C, D, E, H, L (reg = X, H, L for low-end CPU)
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC' DE', HL'
rp'1	BC, DE, HL, XA', BC' DE', HL'
rpa	HL, HL+, HL–, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem (Note 1)	8-bit immediate data or label
bit	2-bit immediate data or label
fmem	FB0H-FBFH, FF0H-FFFH immediate data or label
pmem	FC0H-FFFH immediate data or label
addr	Immediate data or label of the entire ROM area
faddr	11-bit immediate data or label
taddr	20H-7EH immediate data (where bit 0 = 0) or label
PORTn	
IExxx	
RBn	Register bank n
MBn	Memory bank n

Note:

(1) Memory address must be an even number in 8-bit processing.

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Table 4. Addressing Areas

Address Area (Note 1)	Addressing Area Description (Note 2)	Memory Area
1	MB = (MBE)•(MBS) (Note 3)	Data memory
2	MB = 0 (Note 4)	
3	MB = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (Note 3)	
4	MB = 15, fmem = FB0H-FBFH (Note 5) FF0H-FFFH	
5	MB = 15, pmem = FC0H-FFFH (Note 5)	
6	addr immediate data or label of the entire ROM area up to 3F7FH	Program memory
7	addr = (current PC) – 15 to (current PC) – 1 or (current PC) + 2 to (current PC) + 16	
8	caddr x000H to xFFFH; x = 0H to FH and specifies a 4K area of ROM	
9	faddr = 0000H-07FFH	
10	taddr = 0020H-007FH	
11	addr1 = immediate data or label of the entire ROM area 0000H - 7F7FH	

Notes:

(1) Symbols 1 thru 11 refer to the Addressing Area column of the Instruction Set table.

(2) MB = data memory bank that can be addressed.

(3) MBS = 0 - 7, or 15.

(4) MB = 0 regardless of the status of MBE and MBS.

(5) MB = 15 regardless of the status of MBE and MBS.

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Instruction Set

Mnemonic	Operand	Operation	Bytes	MC†	AA†	Skip Condition	EHE† CPU	HE† CPU	Std† CPU	LE† CPU
Transfer										
MOV	A, #n4	A ← n4	1	1		String A	x	x	x	x
	reg1, #n4	reg1 ← n4	2	2			x	x	x	—
	XA, #n8	XA ← n8	2	2		String A	x	x	x	x
	HL, #n8	HL ← n8	2	2		String B	x	x	x	x
	rp2, #n8	rp2 ← n8	2	2			x	x	x	—
	A, @HL	A ← (HL)	1	1	1		x	x	x	x
	A, @HL+	A ← (HL), then L←L+1	1	2+S	1	L = 0	x	x	—	—
	A, @HL–	A ← (HL), then L←L–1	1	2+S	1	L = FH	x	x	—	—
	A, @rpa1	A ← (rpa1)	1	1	2		x	x	x	—
	XA, @HL	XA ← (HL)	2	2	1		x	x	x	—
	@HL, A	(HL) ← A	1	1	1		x	x	x	x
	@HL, XA	(HL) ← XA	2	2	1		x	x	x	—
	A, mem	A ← (mem)	2	2	3		x	x	x	x
	XA, mem	XA ← (mem)	2	2	3		x	x	x	x
	mem, A	(mem) ← A	2	2	3		x	x	x	x
	mem, XA	(mem) ← XA	2	2	3		x	x	x	x
	A, reg	A ← (reg)	2	2			x	x	x	—
	XA, rp'	XA ← rp'	2	2			x	x	x	—
	reg1, A	reg1 ← A	2	2			x	x	x	—
	rp'1, XA	rp'1 ← XA	2	2			x	x	x	—
XCH	A, @HL	A ↔ (HL)	1	1	1		x	x	x	x
	A, @HL+	A ↔ (HL), then L←L+1	1	2+S	1	L = 0	x	x	—	—
	A, @HL–	A ↔ (HL), then L←L–1	1	2+S	1	L = FH	x	x	—	—
	A, @rpa1	A ↔ (rpa1)	1	1	2		x	x	x	—
	XA, @HL	XA ↔ (HL)	2	2	1		x	x	x	—
	A, mem	A ↔ (mem)	2	2	3		x	x	x	x
	XA, mem	XA ↔ (mem)	2	2	3		x	x	x	x
	A, reg1	A ↔ (reg1)	1	1			x	x	x	x
	XA, rp'	XA ↔ rp'	2	2			x	x	x	—
MOVT	XA, @PCDE	XA ← $(PC_{14-8}+DE)_{ROM}$	1	3			x	x	x	—
	XA, @PCXA	XA ← $(PC_{14-8}+XA)_{ROM}$	1	3			x	x	x	x
	XA, @BCDE	XA ← $(B_{2-0}+CDE)_{ROM}$	1	3	6		x	—	—	—
	XA, @BCXA	XA ← $(B_{2-0}+CXA)_{ROM}$	1	3	6	Note 1	x	—	—	—

† MC: Machine Cycle
AA: Addressing Area
EHE: Expanded High-End
HE: High End
Std: Standard
LE: Low End
x = Instruction available
— = Instruction not available

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Instruction Set (cont)

Mnemonic	Operand	Operation	Bytes	MC†	AA†	Skip Condition	EHE† CPU	HE† CPU	Std† CPU	LE† CPU
Transfer (cont)										
MOV1	CY, fmem.bit	CY ← (fmem.bit)	2	2	4		x	x	—	—
	CY, pmem.@L	CY ← ($pmem_{7-2}$+ L_{3-2} .bit(L_{1-0}))	2	2	5		x	x	—	—
	CY, @H+ mem.bit	CY ← (H+ mem_{3-0}.bit)	2	2	1		x	x	—	—
	fmem.bit, CY	(fmem.bit) ← CY	2	2	4		x	x	—	—
	pmem.@L, CY	($pmem_{7-2}$+ L_{3-2}.bit (L_{1-0})) ← CY	2	2	5		x	x	—	—
	CY, @H+ mem.bit	(H+ mem_{3-0}.bit) ← CY	2	2	1		x	x	—	—
Arithmetic										
ADDS	A, #n4	A ← A+ n4	1	1+S		Carry	x	x	x	x
	XA, #n8	XA ← XA+ n8	2	2+S		Carry	x	x	—	—
	A, @HL	A ← A+ (HL)	1	1+S	1	Carry	x	x	x	x
	XA, rp'	XA ← XA+ rp'	2	2+S		Carry	x	x	—	—
	rp'1, XA	rp'1 ← rp'1+ XA	2	2+S		Carry	x	x	—	—
ADDC	A, @HL	A, CY ← A+ (HL)+ CY	1	1	1		x	x	x	x
	XA, rp'	XA, CY ← XA+ rp'+ CY	2	2			x	x	—	—
	rp'1, XA	rp'1, CY ← rp'1+ XA+ CY	2	2			x	x	—	—
SUBS	A, @HL	A ← A–(HL)	1	1+S	1	Borrow	x	x	x	—
	XA, rp'	XA ← XA–rp'	2	2+S		Borrow	x	x	—	—
	rp'1, XA	rp'1 ← rp'1–XA	2	2+S		Borrow	x	x	—	—
SUBC	A, @HL	A, CY ← A – (HL) – CY	1	1	1		x	x	x	—
	XA, rp'	XA, CY ← XA–rp'–CY	2	2			x	x	—	—
	rp'1, XA	rp'1, CY ← rp'1–XA–CY	2	2			x	x	—	—
AND	A, #n4	A←A ∧ n4	2	2			x	x	x	—
	A, @HL	A←A ∧ (HL)	1	1	1		x	x	x	x
	XA, rp'	XA ← XA ∧ rp'	2	2			x	x	—	—
	rp'1, XA	rp'1 ← rp'1 ∧ XA	2	2			x	x	—	—
OR	A, #n4	A ← A ∨ n4	2	2			x	x	x	—
	A, @HL	A ←A ∨ (HL)	1	1	1		x	x	x	x
	XA, rp'	XA ← XA ∨ rp'	2	2			x	x	—	—
	rp'1, XA	rp'1 ← rp'1 ∨ XA	2	2			x	x	—	—
XOR	A, #n4	A ← A ∀ n4	2	2			x	x	x	—
	A, @HL	A ← A ∀ (HL)	1	1	1		x	x	x	x
	XA, rp'	XA ← XA ∀ rp'	2	2			x	x	—	—
	rp'1, XA	rp'1 ← rp'1 ∀ XA	2	2			x	x	—	—

† MC: Machine Cycle
AA: Addressing Area
EHE: Expanded High-End

HE: High End
Std: Standard
LE: Low End

x = Instruction available
— = Instruction not available

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Instruction Set (cont)

Mnemonic	Operand	Operation	Bytes	MC†	AA†	Skip Condition	EHE† CPU	HE† CPU	Std† CPU	LE† CPU
Accumulator Manipulation										
RORC	A	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n	1	1			x	x	x	x
NOT	A	A ← $\overline{A}$	2	2			x	x	x	x
Increment/Decrement										
INCS	reg	reg ← reg+1	1	1+S		reg = 0	x	x	x	x
	rp1	rp1 ← rp1+1	1	1+S		rp1 = 00H	x	x	—	—
	@HL	(HL) ← (HL)+1	2	2+S	1	(HL) = 0	x	x	x	—
	mem	(mem) ← (mem)+1	2	2+S	3	(mem) = 0	x	x	x	x
DECS	reg	reg ← reg–1	1	1+S		reg = FH	x	x	x	x
	rp'	rp' ← rp'–1	2	2+S		rp' = FFH	x	x	—	—
Comparison										
SKE	reg, #n4	skip if reg = n4	2	2+S		reg = n4	x	x	x	x
	@HL, #n4	skip if (HL) = n4	2	2+S	1	(HL) = n4	x	x	x	—
	A, @HL	skip if A = (HL)	1	1+S	1	A = (HL)	x	x	x	x
	XA, @HL	skip if XA = (HL)	2	2+S	1	XA = (HL)	x	x	—	—
	A, reg	skip if A = reg	2	2+S		A = reg	x	x	x	—
	XA, rp'	skip if XA = rp'	2	2+S		XA = rp'	x	x	—	—
Carry Flag Manipulation										
SET1	CY	CY ← 1	1	1			x	x	x	x
CLR1	CY	CY ← 0	1	1			x	x	x	x
SKT	CY	skip if CY = 1	1	1+S		CY = 1	x	x	x	x
NOT1	CY	CY ← $\overline{CY}$	1	1			x	x	x	x
Memory Bit Manipulation										
SET1	mem.bit	(mem.bit) ← 1	2	2	3		x	x	x	x
	fmem.bit	(fmem.bit) ← 1	2	2	4		x	x	x	x
	pmem.@L	($pmem_{7-2}$+L_{3-2}.bit (L_{1-0})) ← 1	2	2	5		x	x	x	—
	@H+ mem.bit	(H + mem_{3-0}.bit) ← 1	2	2	1		x	x	x	—
CLR1	mem.bit	(mem.bit) ← 0	2	2	3		x	x	x	x
	fmem.bit	(fmem.bit) ← 0	2	2	4		x	x	x	x
	pmem.@L	($pmem_{7-2}$+L_{3-2}.bit (L_{1-0})) ← 0	2	2	5		x	x	x	—
	@H+ mem.bit	(H + mem_{3-0}.bit) ← 0	2	2	1		x	x	x	—

† MC: Machine Cycle
AA: Addressing Area
EHE: Expanded High-End
HE: High End
Std: Standard
LE: Low End
x = Instruction available
— = Instruction not available

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Instruction Set (cont)

Mnemonic	Operand	Operation	Bytes	MC†	AA†	Skip Condition	EHE† CPU	HE† CPU	Std† CPU	LE† CPU
Memory Bit Manipulation (cont)										
SKT	mem.bit	skip if (mem.bit) = 1	2	2+S	1	(mem.bit) = 1	x	x	x	x
	fmem.bit	skip if (fmem.bit) = 1	2	2+S	4	(fmem.bit) = 1	x	x	x	x
	pmem.@L	skip if ($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0})) = 1	2	2+S	5	(pmem.@L = 1)	x	x	x	—
	@H+ mem.bit	skip if (H+ mem_{3-0}.bit) = 1	2	2+S	1	(@H+ mem.bit) = 1	x	x	x	—
SKF	mem.bit	skip if (mem.bit) = 0	2	2+S	3	(mem.bit) = 0	x	x	x	x
	fmem.bit	skip if (fmem.bit) = 0	2	2+S	4	(fmem.bit) = 0	x	x	x	x
	pmem.@L	skip if ($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0})) = 0	2	2+S	5	(pmem.@L = 0)	x	x	x	—
	@H+ mem.bit	skip if (H+ mem_{3-0}.bit) = 0	2	2+S	1	(@H+ mem.bit) = 0	x	x	x	—
SKTCLR	fmem.bit	skip if (fmem.bit) = 1 and clear	2	2+S	4	(fmem.bit) = 1	x	x	x	x
	pmem.@L	skip if ($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0})) = 1 and clear	2	2+S	5	(pmem.@L = 1)	x	x	x	—
	@H+ mem.bit	skip if (H+ mem_{3-0}.bit) = 1 and clear	2	2+S	1	(@H+ mem.bit) = 1	x	x	x	—
AND1	CY, fmem.bit	CY ← CY ∧ (fmem.bit)	2	2	4		x	x	x	x
	CY, pmem.@L	CY ← CY ∧ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	2	2	5		x	x	x	—
	CY, @H+ mem.bit	CY ← CY ∧ (H+ mem_{3-0}.bit)	2	2	1		x	x	x	—
OR1	CY, fmem.bit	CY ← CY ∨ (fmem.bit)	2	2	4		x	x	x	x
	CY, pmem.@L	CY ← CY ∨ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	2	2	5		x	x	x	—
	CY, @H+ mem.bit	CY ← CY ∨ (H+ mem_{3-0}.bit)	2	2	1		x	x	x	—
XOR1	CY, fmem.bit	CY ← CY ⊻ (fmem.bit)	2	2	4		x	x	x	x
	CY, pmem.@L	CY ← CY ⊻ ($pmem_{7-2}$+ L_{3-2}.bit (L_{1-0}))	2	2	5		x	x	x	—
	CY, @H+ mem.bit	CY ← CY ⊻ (H+ mem_{3-0}.bit)	2	2	1		x	x	x	—
Branch										
BR (Note 2)	addr	PC_{13-0} ← $addr_{13-0}$	–	–	6		x	x	x	x
	!addr (Note 2)	PC_{14} ← 0, PC_{13-0} ← addr	3	3	6		x	x	x	—
	$addr (Note 2)	PC ← addr	1	2	7		x	x	x	x

† MC: Machine Cycle
AA: Addressing Area
EHE: Expanded High-End
HE: High End
Std: Standard
LE: Low End
x = Instruction available
— = Instruction not available

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Instruction Set (cont)

Mnemonic	Operand	Operation	Bytes	MC†	AA†	Skip Condition	EHE† CPU	HE† CPU	Std† CPU	LE† CPU
Branch (cont)										
BRCB	!caddr (Note 2)	$PC_{14-12} \leftarrow PC_{14-12}$, $PC_{11-0} \leftarrow caddr_{11-0}$	2	2	8		x	x	x	x
BR	PCDE	$PC_{14-8} \leftarrow PC_{14-8}$, $PC_{7-0} \leftarrow DE$	2	3	11		x	x	—	—
	PCXA	$PC_{14-8} \leftarrow PC_{14-8}$, $PC_{7-0} \leftarrow XA$	2	3	11		x	x	—	—
	BCDE (Note 3)	$PC_{14-12} \leftarrow B_{2-0}$, $PC_{11-0} \leftarrow CDE$	2	3	11		x	—	—	—
	BCXA (Note 3)	$PC_{14-12} \leftarrow B_{2-0}$, $PC_{11-0} \leftarrow CXA$	2	3	11		x	—	—	—
BRA (Note 2)	!addr1	PC ← addr1	3	3	11		x	—	—	—
Subroutine Stack Control										
CALL (Note 4)	!addr	(SP–4)(SP–1)(SP–2) ← PC_{11-0} (SP–3) ← (MBE, RBE, $PC_{13,12}$) PC_{13-0} ← addr, SP ← (SP–4)	3	3	6		x	x	x	—
CALLA (Notes 4, 5)	!addr	(SP–1) ← *, *, *, *, (SP–2) ← *, *, MBE, RBE, (SP–3)(SP–4)(SP–5)(SP–6) ← PC_{14-0}, SP ← SP–6	3	3	11		x	—	—	—
CALLF	!faddr	(SP–4)(SP–1)(SP–2) ← PC_{11-0} (SP–3) ← (MBE, RBE, $PC_{13,12}$) PC_{13-0} ← 000, faddr, SP ← (SP–4)	2	2	9		x	x	x	x
CALLF (Notes 5, 6)	!faddr	(SP–1) ← *, *, *, *, (SP–2) ← *, *, MBE, RBE, (SP–3)(SP–4)(SP–5)(SP–6) ← PC_{14-0}, PC_{14-0} ← 0000, faddr, SP ← SP–6	2	3	9		x	—	—	—
RET		(MBE, RBE, $PC_{13,12}$) ← (SP+1) PC_{11-0} ← (SP), (SP+3)(SP+2) SP ← (SP+4)	1	3			—	x	x	x
RET (Notes 5, 6)		PC_{11-0} ← (SP) (SP+2)(SP+3) *, PC_{14-12} ← (SP+1), *, *, MBE, RBE ← (SP+4) SP ← SP+6	1	3			x	—	—	—
RETS		(MBE, RBE, $PC_{13,12}$) ← (SP+1) PC_{11-0} ← (SP) (SP+3)(SP+2) SP ← (SP+4), then skip unconditionally	1	3+S		Unconditional	—	x	x	x
RETS (Notes 5, 6)		PC_{11-0} ← (SP) (SP+3) (SP+2) *, PC_{14-12} ← (SP+1) *, *, MBE, RBE ← (SP+4) SP ← SP+6, then skip unconditionally	1	3+S		No condition	x	—	—	—

† MC: Machine Cycle
AA: Addressing Area
EHE: Expanded High-End
HE: High End
Std: Standard
LE: Low End
x = Instruction available
— = Instruction not available

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Instruction Set (cont)

Mnemonic	Operand	Operation	Bytes	MC†	AA†	Skip Condition	EHE† CPU	HE† CPU	Std† CPU	LE† CPU
Subroutine Stack Control (cont)										
RETI		MBE, RBE, PC_{13} PC_{12} ← (SP+1) PC_{11-0} ← (SP), (SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← (SP+6)	1	3			—	x	x	x
RETI (Notes 5, 6)		PC_{11-0} ← (SP), (SP+3)(SP+2) *, PC_{14-12} ← (SP+1) PSW ← (SP+4)(SP+5) SP ← SP+6	1	3			x	—	—	—
PUSH	rp	(SP–1)(SP–2) ← rp, SP ← (SP–2)	1	1			x	x	x	x
	BS	(SP–1) ← MBS, (SP–2) ← RBS, SP ← (SP–2)	2	2			x	x	x	—
POP	rp	rp ← (SP+1)(SP), SP ← (SP+2)	1	1			x	x	x	x
	BS	MBS ← (SP+1), RBS ← (SP), SP ← (SP+2)	2	2			x	x	x	—
Interrupt Control										
EI		IME ← 1	2	2			x	x	x	x
	IExxx	IExxx ← 1	2	2			x	x	x	x
DI		IME ← 0	2	2			x	x	x	x
	IExxx	IExxx ← 0	2	2			x	x	x	x
Input/Output (Note 7)										
IN	A, $PORT_n$	A ← $PORT_n$	2	2			x	x	x	x
	XA, $PORT_n$	XA ← $PORT_{n+1}$, $PORT_n$	2	2			x	x	x	—
OUT	$PORT_n$, A	$PORT_n$ ← A	2	2			x	x	x	x
	$PORT_n$, XA	$PORT_{n+1}$, $PORT_n$ ← XA	2	2			x	x	x	—
CPU Control										
HALT		Set HALT mode (PCC.2 ← 1)	2	2			x	x	x	x
STOP		Set STOP mode (PCC.3 ← 1)	2	2			x	x	x	x
NOP		No operation	1	1			x	x	x	x
Special										
SEL	RB_n	RBS ← n; (n = 0-3)	2	2			x	x	—	—
	MB_n	MBS ← n	2	2			x	x	x	—

† MC: Machine Cycle
AA: Addressing Area
EHE: Expanded High-End
HE: High End
Std: Standard
LE: Low End
x = Instruction available
— = Instruction not available

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Instruction Set (cont)

Mnemonic	Operand	Operation	Bytes	MC†	AA†	Skip Condition	EHE† CPU	HE† CPU	Std† CPU	LE† CPU
GETI (Notes 8, 9)	taddr	For BR instructions: (TBR in GETI table) $PC_{13-0} \leftarrow (taddr)_{5-0}$, (taddr+1)	1	3	10	Depends on the referenced instruction	—	x	x	—
		For CALL instructions: (TCALL in GETI table) (SP–4), (SP–1), (SP–2) $\leftarrow PC_{11-0}$; (SP–3) ← MBE, RBE, $PC_{13,12}$; $PC_{13-0} \leftarrow (taddr)_{5-0}$, (taddr+1), SP ← SP–4	1	3	10	Depends on the referenced instruction	—	x	x	—
		For instructions other than TBR or TCALL, the instruction at (taddr) and (taddr+1) is executed.	1	3	10	Depends on the referenced instruction	—	x	x	—

Notes:

(1) Available on all expanded high-end CPUs except μPD75217.

(2) Optimum instruction is selected by the assembler from BRA !addr, BR !addr, BRCB !caddr, and BR $addr.

(3) Can be used for expanded high-end CPU except μPD75217

(4) For parts that contain the expanded high-end CPU and use the 32K mode, the CALL instruction operates the same as the CALLA instruction except the CALL takes 4 machine cycles and the CALLA takes 3 machine cycles.

(5) * = undefined value.

(6) This operation is only for parts with expanded high-end CPU operating in the 32K mode, or for parts with the expanded high-end CPU and no 32K mode.

(7) When executing the IN/OUT instruction, either MBE must be reset to 0, or MBE and MBS must be set to 1 and 15, respectively.

(8) TBR and TCALL are GETI table pseudoinstructions.

(9) The GETI instruction shown applies to the high-end and standard CPUs. The GETI instruction is not available in the low-end CPU. For parts with the expanded high-end CPU, see the User's Manual.

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SOLDERING

Packaging and Soldering Information

Part Number	Package	Package Drawing	Recommended Soldering Code
μPD75304GF-xxx-3B9 μPD75306GF-xxx-3B9 μPD75308GF-xxx-3B9 μPD75312GF-xxx-3B9 μPD75316GF-xxx-3B9	80-pin plastic QFP (14 x 20 mm)	P80GF-80-3B9-1	IR30-00-1, VP15-00-1, WS60-00-1
μPD75P308GF	80-pin plastic QFP (14 x 20 mm)	P80GF-80-3B9-1	IR30-162-1, VP15-162-1, WS60-162-1
μPD75P316AGF	80-pin plastic QFP (14 x 20 mm)	P80GF-80-3B9-1	IR30-207-1, VP15-207-1, WS60-207-1
μPD75P308K μPD75P316AK	80-pin ceramic LCC w/window	X80KW-80A	Soldering not recommended

Soldering Conditions

Method (Note 1)	Code (Note 2)	Soldering Conditions	Exposure Limit (Note 3)
Infrared reflow	IR30-00-1	Package peak temp: 230°C Time: 30 sec max (210°C min)	No limit
	IR30-162-1		Max no. of days: 2 (thereafter, 16 hours baking at 125°C is required)
	IR30-207-1		Max no. of days: 7 (thereafter, 20 hours baking at 125°C is required)
Vapor phase	VP15-00-1	Package peak temp: 215°C Time: 40 sec max (200°C min)	No limit
	VP15-162-1		Max no. of days: 2 (thereafter, 16 hours baking at 125°C is required)
	VP15-207-1		Max no. of days: 7 (thereafter, 20 hours baking at 125°C is required)
Wave soldering	WS60-00-1	Solder bath temp: 260°C max Time: 10 sec max	No limit
	WS60-162-1		Max no. of days: 2 (thereafter, 16 hours baking at 125°C is required)
	WS60-207-1		Max no. of days: 7 (thereafter, 20 hours baking at 125°C is required)
Pin partial heating		Pin partial temp: 300°C max Time: 3 sec max (per device side)	

Notes:

(1) Do not use different soldering methods together. However, on all devices the pin partial heating soldering method can be used alone or in combination with other soldering methods.

(2) The maximum number of soldering operations is one or two as indicated by the last digit of the soldering code: -1 or -2.

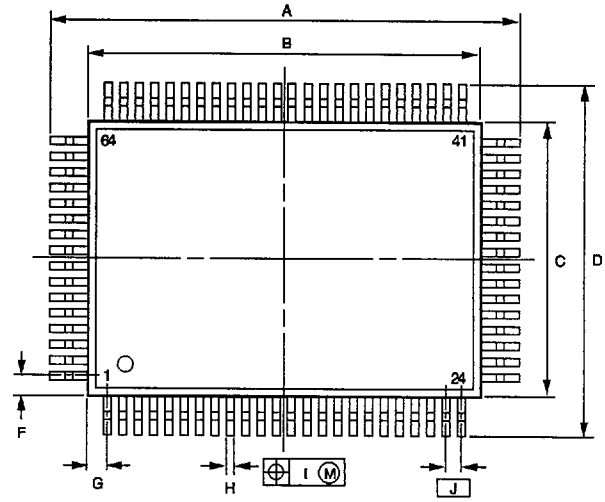
(3) Maximum no. of days refers to the number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

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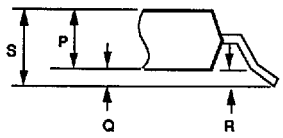
PACKAGE DRAWINGS

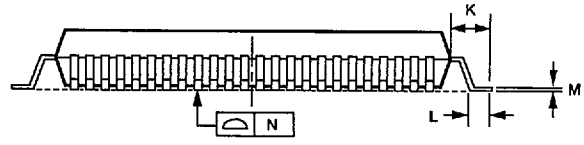
80-Pin Plastic QFP, 14 x 20 mm (Dwg P80GF-80-3B9-1)

Item	Millimeters	Inches
A	23.6 ±0.4	.929 ±.016
B	20.0 ±0.2	.787 +.009 −.008
C	14.0 ±0.2	.551 +.009 −.008
D	17.6 ±0.4	.693 ±.016
F	1.0	.039
G	0.8	.031
H	0.35 ±0.10	.014 +.004 −.005
I	0.15	.006
J	0.8 (TP)	.031 (TP)
K	1.8 ±0.2	.071 +.009 −.008
L	0.8 ±0.2	.031 +.009 −.008
M	0.15 +0.10 −0.05	.006 +.004 −.002
N	0.15	.006
P	2.7	.106
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	3.0 max	.118 max



Pin Detail





P80GF-80-3B9-2

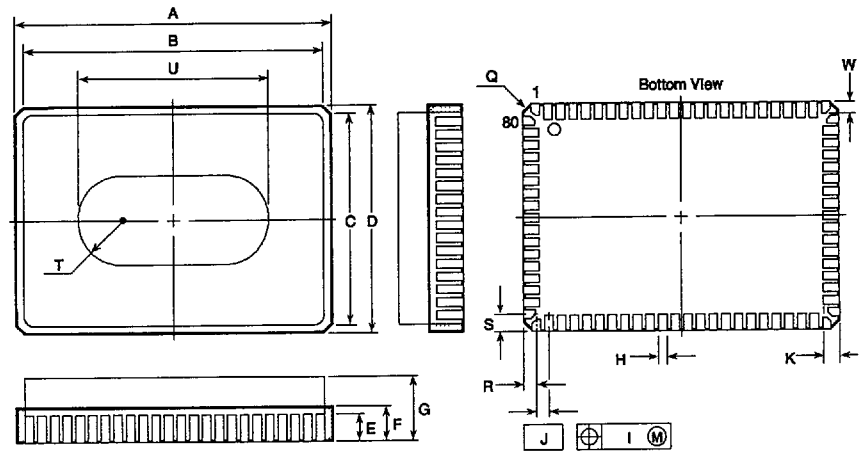
83IH-5543B (5/94)

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PACKAGE DRAWINGS (cont)

80-Pin Ceramic LCC With Window (Dwg x80KW-80A)

Item	Millimeters	Inches
A	20.0 ± 0.4	.787 $^{+.017}_{-.016}$
B	19.0	.748
C	13.2	.520
D	14.2 ± 0.4	.559 ± .016
E	1.64	.065
F	2.14	.084
G	4.064 max	.160 max
H	0.51 ± 0.10	.020 ± .004
I	0.08	.003
J	0.8 (TP)	.031 (TP)
K	1.0 ± 0.2	.039 $^{+.009}_{-.008}$
Q	0.5 cor	.020 cor
R	0.8	.031
S	1.1	.043
T	3.0 rad	.118 rad
U	12.0	.472
W	0.75 ± 0.2	.030 $^{+.008}_{-.009}$



X80KW-80A

49NR-817B (11/89)

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PACKAGE DRAWINGS (cont)

80-Pin Ceramic QFP For Engineering Samples

Item	Millimeters	Inches
A	20.0	.787
B	18.4	.724
C	12.0	.472
D	14.2	.559
H	0.32	.013
J	0.8	.031
N	0.15	.006
S	2.25	.089

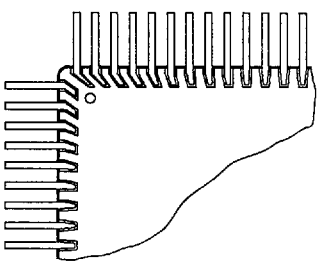
Notes:

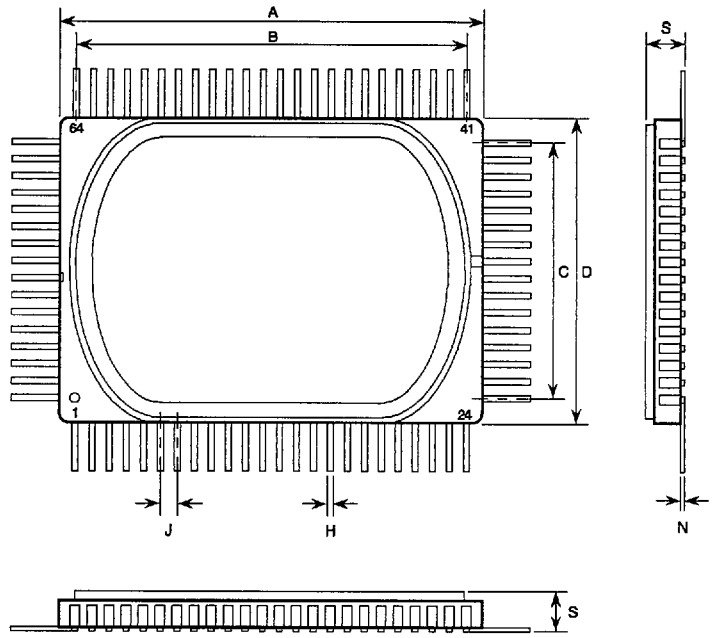
(1) The metal cover is connected to pin 33 (V_{SS})

(2) The leads on the bottom surface are formed obliquely.

(3) The length of the leads is not defined since the cutting of the lead tips is not controlled during the manufacturing process.

Enlarged detail of bottom





83YL-9299B (2/94)

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