## Description

The μPD71055 is a low-power CMOS programmable parallel interface unit for use in microcomputer systems. Typically, the unit's three I/O ports interface peripheral devices to the system bus.

## Features

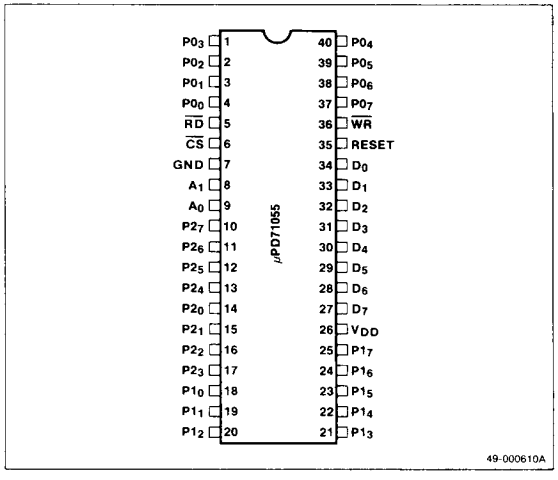
- ☐ Three 8-bit I/O ports
- ☐ Three programmable operation modes
- ☐ Bit manipulation command
- ☐ Microcomputer compatible
- ☐ CMOS technology
- ☐ Single +5 V ±10% power supply
- ☐ Industrial temperature range: −40 to +85 °C
- ☐ 8 MHz and 10 MHz

## Ordering Information

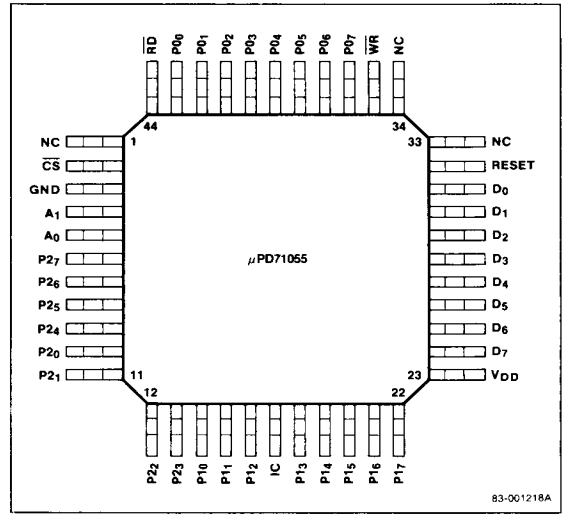
| Part Number | Clock (MHz) | Package |
|---|---|---|
| μPD71055C-8 | 8 | 40-pin plastic DIP |
| C-10 | 10 | |
| G-8 | 8 | 44-pin plastic QFP (P44G-80-22) |
| GB-8 | 8 | 44-pin plastic QFP (P44GB-80-3B4) |
| GB-10 | 10 | |
| L-8 | 8 | 44-pin PLCC |
| L-10 | 10 | |

## Pin Configurations

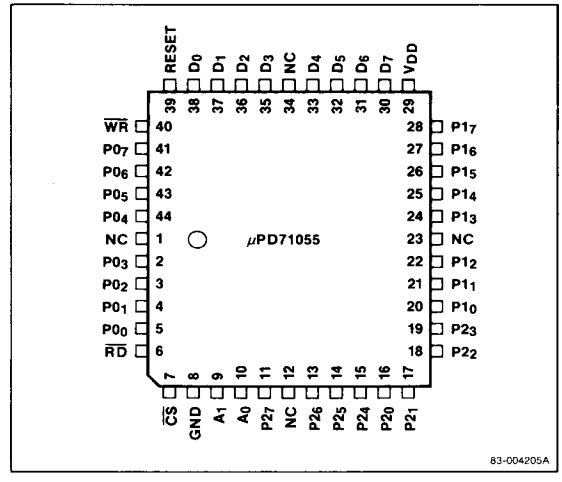
### 40-Pin Plastic DIP




### 44-Pin Plastic QFP




### 44-Pin Plastic Leaded Chip Carrier (PLCC)




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## Pin Identification

| Symbol | Function |
|---|---|
| $\overline{CS}$ | Chip select input |
| GND | Ground |
| $A_1$, $A_0$ | Address inputs 1 and 0 |
| $P0_7$-$P0_0$ | I/O port 0, bits 7-0 |
| $P1_7$-$P1_0$ | I/O port 1, bits 7-0 |
| $P2_7$-$P2_0$ | I/O port 2, bits 7-0 |
| IC | Internally connected |
| $V_{DD}$ | +5 V |
| $D_7$-$D_0$ | I/O data bus |
| RESET | Reset input |
| $\overline{WR}$ | Write strobe input |
| $\overline{RD}$ | Read strobe input |
| NC | No connection |

## Pin Functions

### $D_7$-$D_0$ [Data Bus]

$D_7$-$D_0$ make up an 8-bit, three-state, bidirectional data bus. The bus is connected to the system data bus. It is used to send commands to the μPD71055 and to send data to and from the μPD71055.

### $\overline{CS}$ [Chip Select]

The $\overline{CS}$ input is used to select the μPD71055. When $\overline{CS} = 0$, the μPD71055 is selected and the states of the $D_7$-$D_0$ pins are determined by the $\overline{RD}$ and $\overline{WR}$ inputs. When $\overline{CS} = 1$, the μPD71055 is not selected and its data bus is high-impedance.

### $\overline{RD}$ [Read Strobe]

The $\overline{RD}$ input is set low when data is being read from the μPD71055 data bus.

### $\overline{WR}$ [Write Strobe]

The $\overline{WR}$ input should be set low when data is to be written to the μPD71055 data bus. The contents of the data bus are written to the μPD71055 at the rising edge (low to high) of the $\overline{WR}$ signal.

### $A_1$, $A_0$ [Address]

The $A_1$ and $A_0$ inputs are used in combination with the $\overline{RD}$ and $\overline{WR}$ signals to select one of the three ports or the command register. $A_1$ and $A_0$ are usually connected to the lower two bits of the system address bus (table 1).

### $\overline{WR}$ [Write Strobe]

The $\overline{WR}$ input should be set low when data is to be written to the μPD71055 data bus. The contents of the data bus are written to the μPD71055 at the rising edge (low to high) of the $\overline{WR}$ signal.

### $A_1$, $A_0$ [Address]

The $A_1$ and $A_0$ inputs are used in combination with the $\overline{RD}$ and $\overline{WR}$ signals to select one of the three ports or the command register. $A_1$ and $A_0$ are usually connected to the lower two bits of the system address bus (table 1).

*Table 1. Control Signals and Operation*

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | $A_1$ | $A_0$ | Operation | μPD71055 Operation |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | Port 0 to data bus | Input |
| 0 | 0 | 1 | 0 | 1 | Port 1 to data bus | Input |
| 0 | 0 | 1 | 1 | 0 | Port 2 to data bus | Input |
| 0 | 0 | 1 | 1 | 1 | Use prohibited | |
| 0 | 0 | 0 | x | x | | |
| 0 | 1 | 0 | 0 | 0 | Data bus to port 0 | Output |
| 0 | 1 | 0 | 0 | 1 | Data bus to port 1 | Output |
| 0 | 1 | 0 | 1 | 0 | Data bus to port 2 | Output |
| 0 | 1 | 0 | 1 | 1 | Data bus to command register | Output |
| 0 | 1 | 1 | x | x | Data bus high impedance | |
| 1 | x | x | x | x | | |

### RESET [Reset]

When the RESET input is high, the μPD71055 is reset. The group 0 and the group 1 ports are set to mode 0 (basic I/O port mode). All port bits are cleared to zero and all ports are set for input.

### $P0_7$-$P0_0$, $P1_7$-$P1_0$, $P2_7$-$P2_0$ [Ports 0, 1, 2]

Pins $P0_7$-$P0_0$, $P1_7$-$P1_0$, and $P2_7$-$P2_0$ are the port 0, 1, and 2 I/O pins, bits 7-0, respectively.

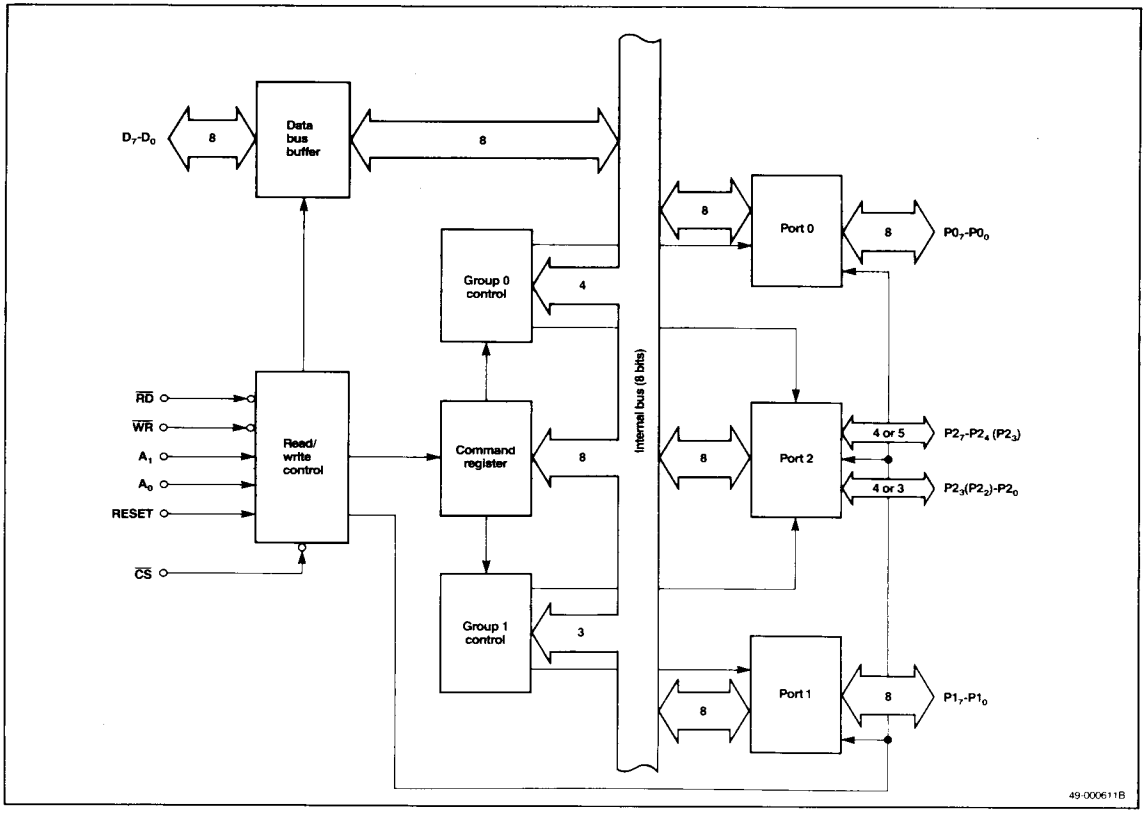
### IC [Internally Connected]

Pins marked IC are used internally and must be left unconnected.



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## Block Diagram




## Functional Description

### Ports 0, 1, 2

The μPD71055 has three 8-bit I/O ports, referred to as port 0, port 1, and port 2. These ports are divided into two groups, group 0 and group 1. The groups can be in one of three modes, mode 0, mode 1, and mode 2. Modes can be set independently for each group.

When port 0 is in mode 0, port 0 and the four upper bits of port 2 belong to group 0, and port 1 and the four lower bits of port 2 belong to group 1. When port 0 is in mode 1 or 2, port 0 and the 5 upper bits of port 2 belong to group 0 and port 1 and the three lower bits of port 2 belong to group 1.

### Command Register

The host writes command words to the μPD71055 in this register. These commands control group 0 and group 1. Note that the contents of this register cannot be read.

### Group 0 Control and Group 1 Control

These blocks control the operation of group 0 and group 1.

### Read/Write Control

The read/write control controls the read/write operations for the ports and the data bus in response to the $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, and address signals. It also handles RESET signals and the $A_0$, $A_1$ address inputs.

### Data Bus Buffer

The data bus buffer latches information going to or from the system data bus.

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## Absolute Maximum Ratings

($T_A = 25°C$)

| | |
|---|---|
| Power supply voltage, $V_{DD}$ | −0.5 to +7.0 V |
| Input voltage, $V_I$ | −0.5 to $V_{DD}$ + 0.3 V |
| Output voltage, $V_O$ | −0.5 to $V_{DD}$ + 0.3 V |
| Power dissipation, $PD_{MAX}$ | 500 mW |
| Operating temperature, $T_{opt}$ | −40 to +85°C |
| Storage temperature, $T_{stg}$ | −65 to +150°C |

**Comment:** These devices are not meant to be operated outside the limits specified above. Exposure to stresses beyond those listed in Absolute Maximum Ratings could cause damage. Exposure to an absolute maximum rating for extended periods may affect reliability.

## Capacitance

($T_A = 25°C$, $V_{DD} = GND = 0$ V)

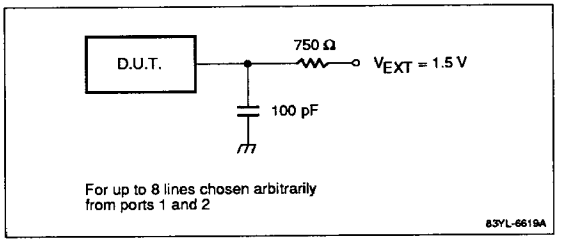
| Parameter | Symbol | Limits Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input capacitance | $C_I$ | | | 10 | pF | fc = 1 MHz Unmeasured pins returned to 0 V |
| I/O capacitance | $C_{IO}$ | | | 20 | pF | |

## DC Characteristics

($T_A = -40$ to +85°C, $V_{DD} = 5$ V ±10%)

| Parameter | Symbol | Limits Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input voltage high | $V_{IH}$ | 2.2 | | $V_{DD}$ + 0.3 | V | |
| Input voltage low | $V_{IL}$ | −0.5 | | 0.8 | V | |
| Output voltage high | $V_{OH}$ | 0.7 $V_{DD}$ | | | V | $I_{OH} = -400\ \mu A$ |
| Output voltage low | $V_{OL}$ | | | 0.4 | V | $I_{OL} = 2.5$ mA |
| Darlington drive current | $I_{DAR}$ | −1.0 | | −4.0 | mA | See test setup diagram |
| Input leakage current high | $I_{LIH}$ | | | 10 | μA | $V_I = V_{DD}$ |
| Input leakage current low | $I_{LIL}$ | | | −10 | μA | $V_I = 0$ V |
| Output leakage current high | $I_{LOH}$ | | | 10 | μA | $V_O = V_{DD}$ |
| Output leakage current low | $I_{LOL}$ | | | −10 | μA | $V_O = 0$ V |
| Supply current (dynamic) μPD71055 | $I_{DD1}$ | | | 10 | mA | Normal operation |
| μPD71055-10 | $I_{DD1}$ | | 5 | 10 | mA | Normal operation |
| Supply current (standby) | $I_{DD2}$ | | 2 | 50 | μA | Inputs: RESET = 0.1 V, others = $V_{DD}$ − 0.1 V Outputs: Open |

### *Test Setup for $I_{DAR}$ Measurement*






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## AC Characteristics

($T_A$ = −40 to +85°C, $V_{DD}$ = 5 V ±10%)

| Parameter | Symbol | 8 MHz Limits Min | 8 MHz Limits Max | 10 MHz Limits Min | 10 MHz Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Read Timing** | | | | | | | |
| $A_1$, $A_0$, $\overline{CS}$ set-up to $\overline{RD}$ ↓ | $t_{SAR}$ | 0 | | 0 | | ns | |
| $A_1$, $A_0$, $\overline{CS}$ hold from $\overline{RD}$ ↑ | $t_{HRA}$ | 0 | | 0 | | ns | |
| $\overline{RD}$ pulse width | $t_{RRL}$ | 160 | | 150 | | ns | |
| Data delay from $\overline{RD}$ ↓ | $t_{DRD}$ | | 120 | | 100 | ns | $C_L$ = 150 pF |
| Data float from $\overline{RD}$ ↑ | $t_{FRD}$ | 10 | 85 | 10 | 60 | ns | $C_L$ = 20 pF; $R_L$ = 2 kΩ |
| Read recovery time | $t_{RV}$ | 200 | | 150 | | ns | |
| **Write Timing** | | | | | | | |
| $A_1$, $A_0$, $\overline{CS}$ set-up to $\overline{WR}$ ↓ | $t_{SAW}$ | 0 | | 0 | | ns | |
| $A_1$, $A_0$, $\overline{CS}$ hold from $\overline{WR}$ ↑ | $t_{HWA}$ | 0 | | 0 | | ns | |
| $\overline{WR}$ pulse width | $t_{WWL}$ | 120 | | 100 | | ns | |
| Data set-up to $\overline{WR}$ ↑ | $t_{SDW}$ | 100 | | 100 | | ns | |
| Data hold from $\overline{WR}$ ↑ | $t_{HWD}$ | 0 | | 0 | | ns | |
| Write recovery time | $t_{RV}$ | 200 | | 150 | | ns | |
| **Other Timing** | | | | | | | |
| Port set-up time to $\overline{RD}$ ↓ | $t_{SPR}$ | 0 | | 0 | | ns | |
| Port hold time from $\overline{RD}$ ↑ | $t_{HRP}$ | 0 | | 0 | | ns | |
| Port set-up time to $\overline{STB}$ ↓ | $t_{SPS}$ | 0 | | 0 | | ns | |
| Port hold time from $\overline{STB}$ ↑ | $t_{HSP}$ | 150 | | 150 | | ns | |
| Port delay time from $\overline{WR}$ ↑ | $t_{DWP}$ | | 350 | | 200 | ns | $C_L$ = 150 pF |
| $\overline{STB}$ pulse width | $t_{SSL}$ | 350 | | 100 | | ns | |
| $\overline{DAK}$ pulse width | $t_{DADAL}$ | 300 | | 100 | | ns | |
| Port delay time from $\overline{DAK}$ ↓(mode 2) | $t_{DDAP}$ | | 300 | | 150 | ns | CL = 150 pF |
| Port float time from $\overline{DAK}$ ↑(mode 2) | $t_{FDAP}$ | 20 | 250 | 20 | 250 | ns | $C_L$ = 20 pF; $R_L$ = 2 kΩ |
| $\overline{OBF}$ set delay from $\overline{WR}$ ↑ | $t_{DWOB}$ | | 300 | | 150 | ns | $C_L$ = 150 pF |
| $\overline{OBF}$ clear delay from $\overline{DAK}$ ↓ | $t_{DDAOB}$ | | 350 | | 150 | ns | |
| IBF set delay from $\overline{STB}$ ↓ | $t_{DSIB}$ | | 300 | | 150 | ns | |
| IBF clear delay from $\overline{RD}$ ↑ | $t_{DRIB}$ | | 300 | | 150 | ns | |
| INT set delay from $\overline{DAK}$ ↑ | $t_{DDAI}$ | | 350 | | 150 | ns | |
| INT clear delay from $\overline{WR}$ ↓ | $t_{DWI}$ | | 450 | | 200 | ns | |
| INT set delay from $\overline{STB}$ ↑ | $t_{DSI}$ | | 300 | | 150 | ns | |
| INT clear delay from $\overline{RD}$ ↓ | $t_{DRI}$ | | 400 | | 200 | ns | |
| RESET pulse width | $t_{RESET1}$ | 50 | | 50 | | μs | During right after power-on |
| | $t_{RESET2}$ | 500 | | 500 | | ns | During operation |

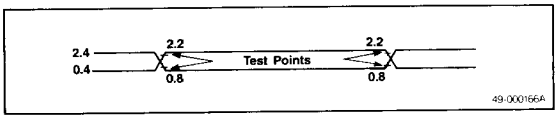
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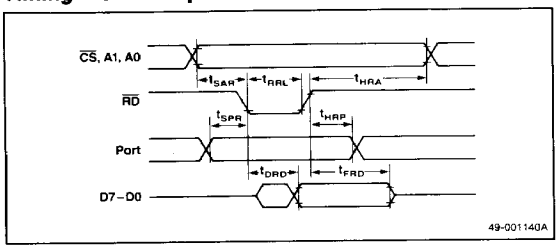
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## Timing Waveforms

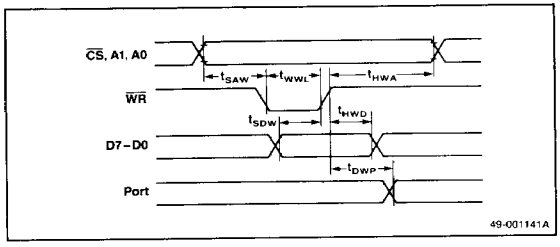
### AC Test Waveform



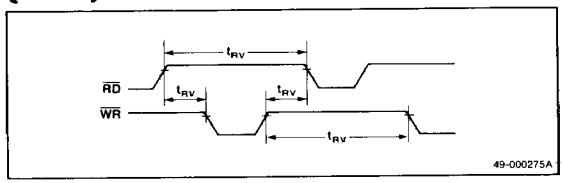

### Timing Mode 0: Input



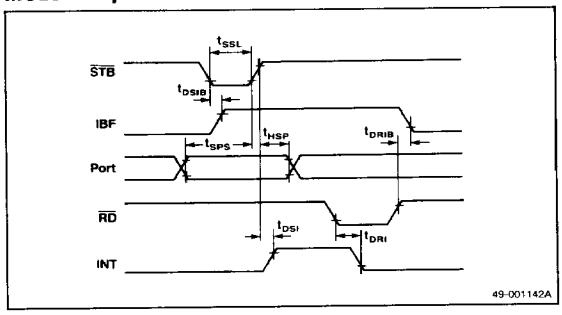

### Mode 0: Output



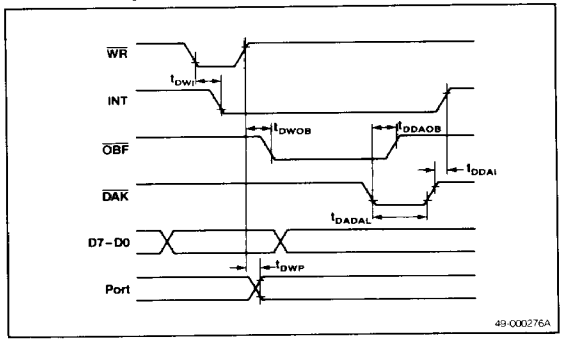

### Recovery Time




### Mode 1: Input




### Mode 1: Output

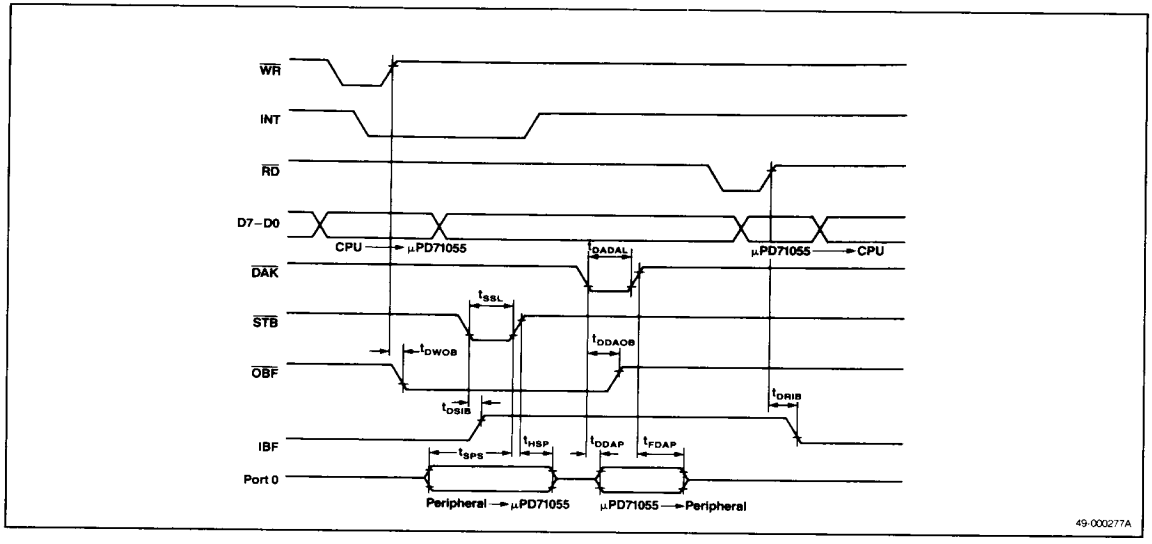





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## Timing Waveforms (cont)

*Mode 2*




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### μPD71055 Commands

Two commands control μPD71055 operation. The mode select command determines the operation of group 0 and group 1 ports. The bit manipulation command sets or resets the bits of port 2. These commands are executed by writing an 8-bit command word to the command register ($A_1A_0 = 11$).

#### Mode Select

The μPD71055 port groups have three modes. Modes 0 and 1 can be specified for groups 0 and 1, but mode 2 can only be specified for group 0. The bits of all ports are cleared when a mode is selected or when the μPD71055 is reset.

**Mode 0.** Basic input/output port operation.

**Mode 1.** Strobed input/output operation controlled by three or four bits of port 2 used as control/status signals.

**Mode 2.** (Only available for group 0). Port 0 is the bidirectional I/O port and the higher 5 bits of port 2 are used for status and control signals.

To specify the mode, set the command word as shown in figure 1 and write it to the command register.

#### Bit Manipulation Command

This command (figure 2) affects only port 2. It is mainly used in mode 1 and mode 2 to control the port 2 bits which are used as control/status signals. It is also used to enable and disable μPD71055-generated interrupts and to set and reset port 2 general input/output pins.

For example, to set bit 2 of port 2 to 1 ($P2_2 = 1$), set the command word as shown in figure 3 (05H) in the command register.

### Operation in Each Mode

The operation mode for each group in the μPD71055 can be set according to the application. Group 0 can be in modes 0, 1, or 2, while group 1 is in mode 0 or 1. Group 1 cannot be used in mode 2.

The $\overline{RD}$ and $\overline{WR}$ signals that appear in the descriptions of each mode refer to the port in question as addressed by $A_1$ and $A_0$. These signals only affect the port addressed by $A_1$ and $A_0$.

Where the port addressed may not be clear, 0 or 1 is appended to the signal name to indicate the port.

#### Mode 0

In this mode the ports of the μPD71055 are used to perform basic I/O operations. Each port operates with a buffered input and a buffered latched output. See figure 4.

Depending on the control word sent to the μPD71055 from the system bus, ports 0, 1, and 2 can be independently specified for input or output.

#### Input Port Operation

While the $\overline{RD}$ signal is low, data from the port selected by the $A_1A_0$ signals is put on the data bus. See figure 5.

#### Output Port Operation

When the μPD71055 is written to ($\overline{WR} = 0$), the data on the data bus will be latched in the port selected by the $A_1A_0$ signals at the rising edge of $\overline{WR}$ and output to the port pins (figure 6). Following the programming of mode 0, all outputs are at a low level.

By reading a port which is set for output, the output value of the port can be obtained.

Note: When group 0 is in mode 1 or mode 2, only bits $P2_2$-$P2_0$ of port 2 can be used by group 1. Bit $P2_3$ belongs to group 0.

#### Mode 0 Example

This is an example of a CPU connected to an A/D converter via a μPD71055 (figure 7). Here both group 0 and group 1 are set to mode 0 and port 2 is used to start conversion and detect the end of the conversion process.

Figure 8 is a subroutine that reads the converted data from an A/D converter.



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***Figure 1. Mode Select Command Word***

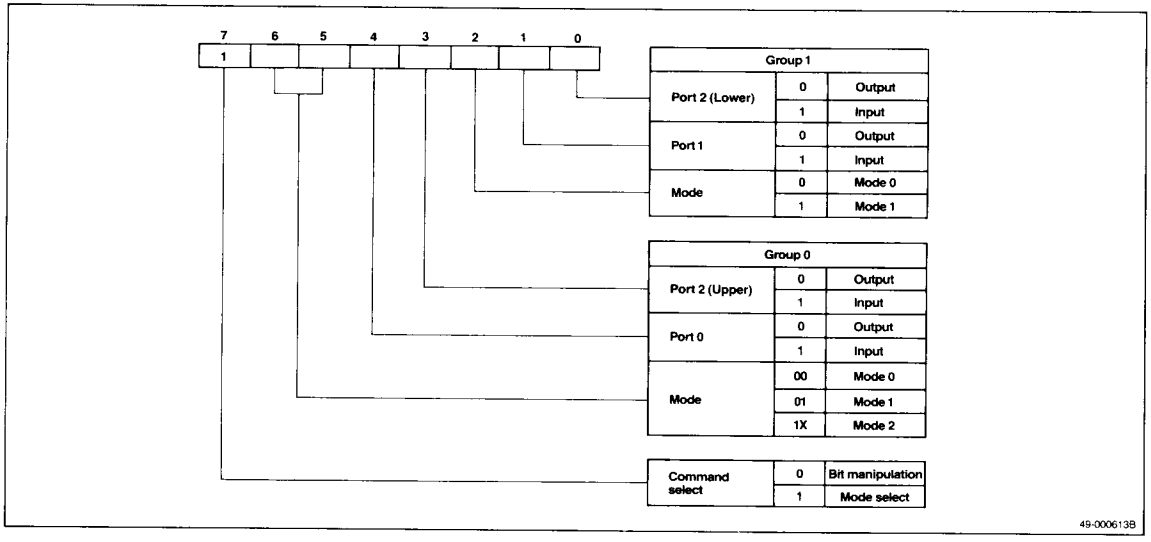



***Figure 2. Bit Manipulation Command Word***

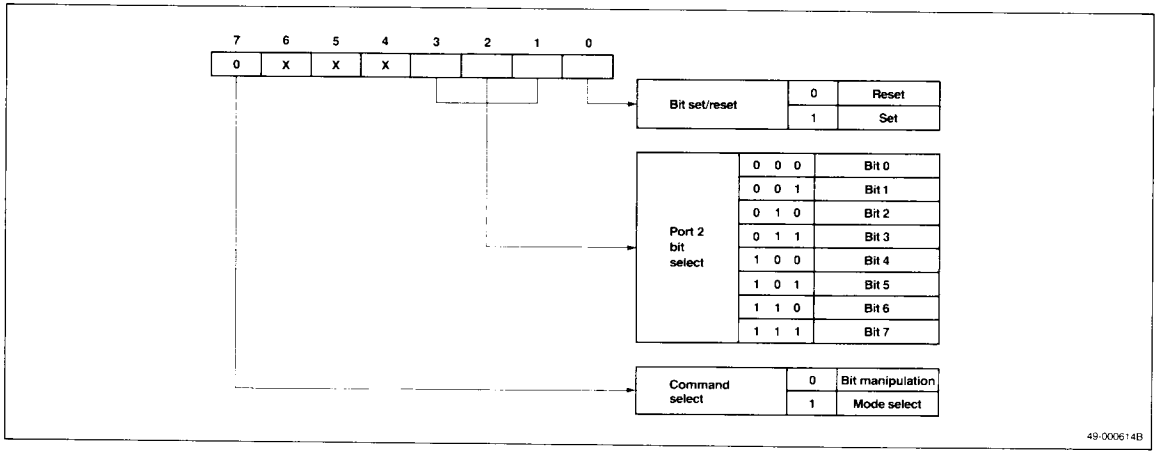
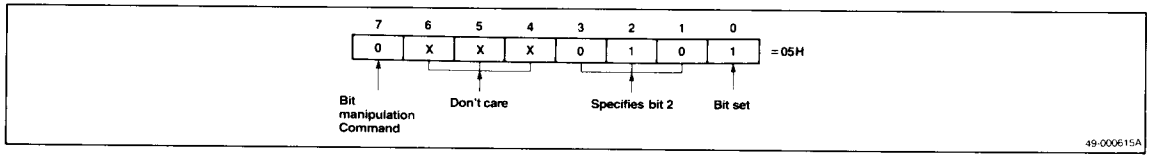



***Figure 3. Bit Manipulation Command Example***




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*Figure 4. Mode 0*

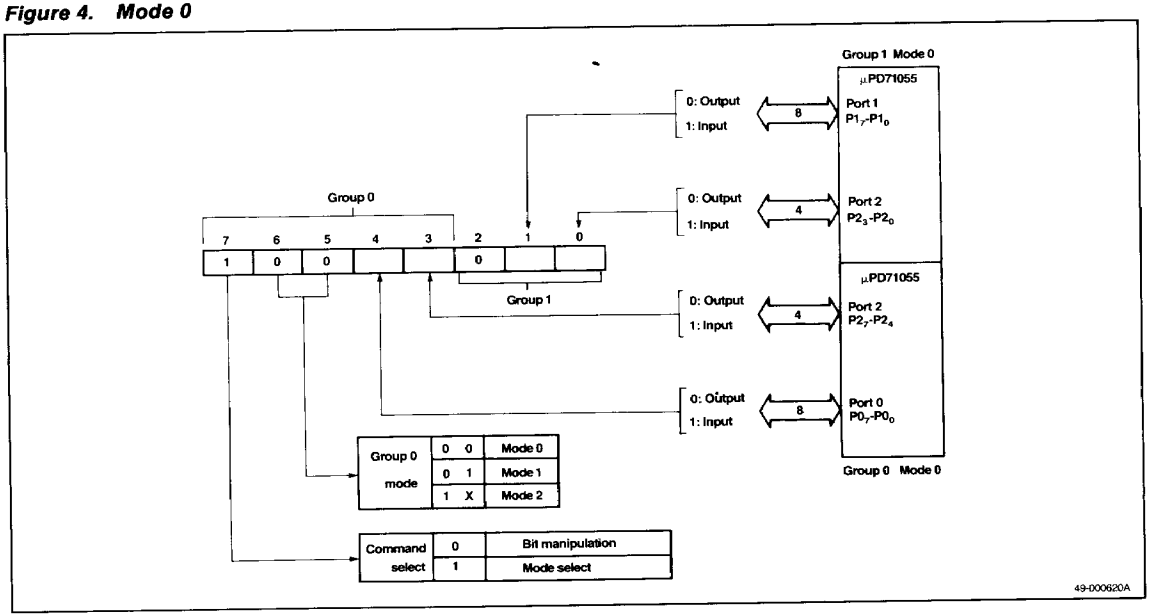



*Figure 5. Mode 0 Input Timing*

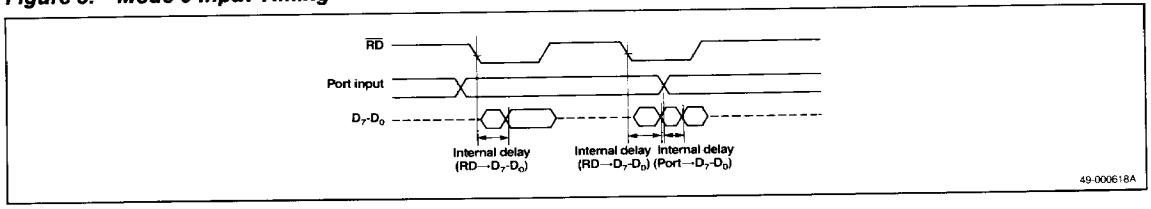
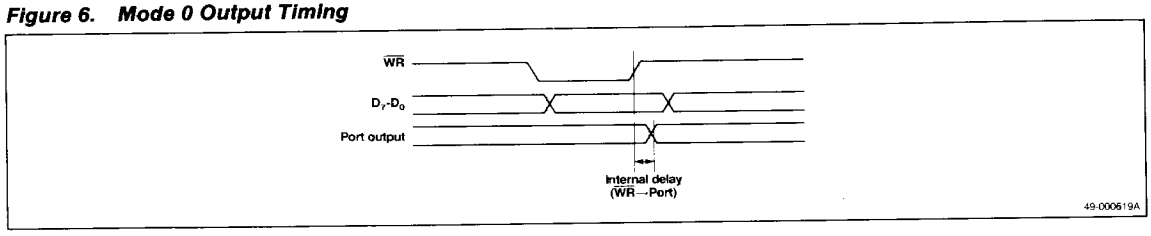



*Figure 6. Mode 0 Output Timing*






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*Figure 7. A/D Converter Connection Example*

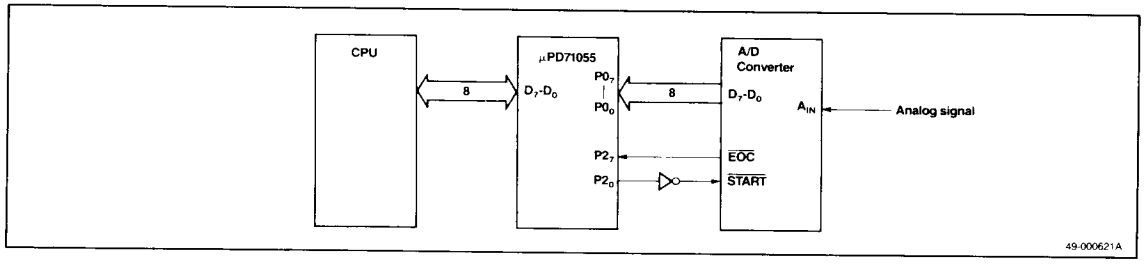



*Figure 8. A/D Converter Example*

```
READ_A/D:   MOV     AL,10011000B    ;μPD71055 Mode Setting:
            OUT     CTRLPORT,AL     ;Group 0, group 1 in mode 0
                                    ;Port 0 & port 2 (upper) are inputs
                                    ;Port 1 & port 2 (lower) are outputs
            MOV     AL,00000001B
            OUT     CTRLPORT,AL     ;Conversion starts by setting P2₀ high
WAIT_EOC:   IN      AL,PORT2        ;End of conversion wait loop
            TEST1   AL,7            ;Conversion ends when P2₇ = 0
            BNZ     WAIT_EOC
            IN      AL,PORT0        ;Read A/D converted values
            RET
```

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## Mode 1

In this mode, the control and status signals control the I/O data. In group 0, port 0 functions as the data port and the upper five bits of port 2 function as control/status. In group 1, port 1 functions as the data port and the lower three bits of port 2 function as control/status.

In mode 1, the bit manipulation command is used to write the bits of port 2.

### Group 0 Mode 1

When group 0 is used in mode 1, the upper five bits of port 2 become part of group 0. Of these five bits, three are used for control/status and the remaining two can be used for I/O (using the bit manipulation command). See figure 9.

### Group 1 Mode 1

When group 1 is used in mode 1, the lower three or four bits of port 2 become part of group 1. Of these four bits, three are used for control/status. The remaining bit, $P2_3$, can be used for I/O only if group 0 is in mode 0. Otherwise, $P2_3$ belongs to group 0 as a control/status bit. See figure 9 and table 4.

### Mode 1 Input Operation

In mode 1, port 0 is the data port for group 0, and port 1 for group 1. The control/status bits (port 2) are used as listed below. Figure 10 shows the signal timing.

**$\overline{STB}$ [Strobe].** The data input at port 0 is latched in port 0 when the $\overline{STB0}$ input is brought low. The data input at port 1 is latched in port 1 by $\overline{STB1}$.

**IBF [Input Buffer Full F/F].** The IBF output goes high to indicate that the input buffer has become full. IBF goes high when the $\overline{STB}$ signal goes low. IBF goes low at the rising edge of the $\overline{RD}$ signal when $\overline{STB} = 1$.

The IBF F/F is cleared when mode 1 is programmed.

**INT [Interrupt Request].** INT goes high when the data is latched in the input port, when RIE is 1 and $\overline{STB}$, IBF and $\overline{RD}$ are all high. INT goes low at the falling edge of the $\overline{RD}$ signal. It can function as a data read request interrupt signal to a CPU.

INT is cleared when mode 1 is programmed.



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**Figure 9. Mode 1 Input**

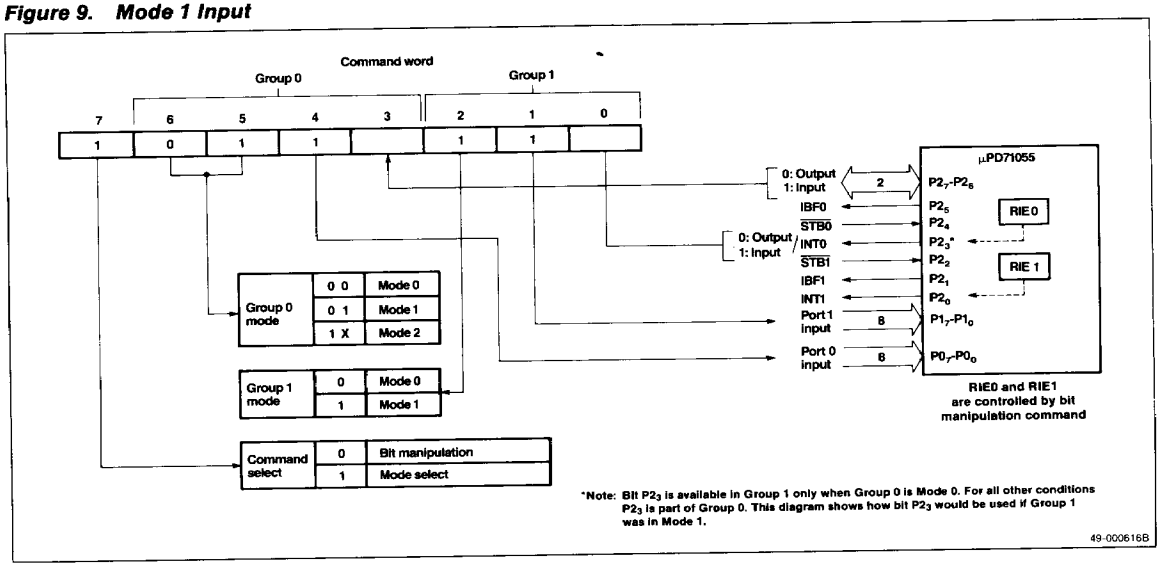
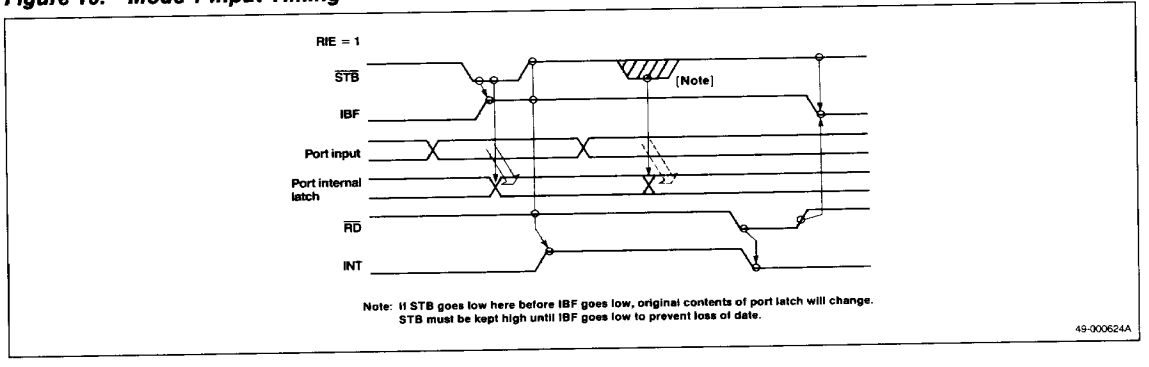



**Figure 10. Mode 1 Input Timing**






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**RIE [Read Interrupt Enable Flag].** RIE controls the interrupt output. Interrupts can be enabled by using the bit manipulation command to set this bit to 1, and disabled by resetting it to 0. This signal is internal to the μPD71055 and is not an output. The state of RIE does not affect the function of $\overline{STB0}$ or $\overline{STB1}$, which are inputs to the same bits ($P2_4$ and $P2_2$) of port 2.

When input is specified in mode 1, the status of IBF, INT and RIE can be read by reading the contents of port 2.

## Mode 1 Output Operation

In mode 1 output operation (figure 11), the status/control bits (port 2) are used as listed below. Figure 12 shows the signal timing.

**$\overline{OBF}$ [Output Buffer Full F/F].** $\overline{OBF}$ goes low when data is received by the μPD71055 and is latched in output ports 1 or 0. $\overline{OBF}$ functions as a data receive flag. $\overline{OBF}$ goes low at the rising edge of $\overline{WR}$ when $\overline{DAK} = 1$ (write complete). It goes high when the $\overline{DAK}$ signal goes low.

***Figure 11. Mode 1 Output***

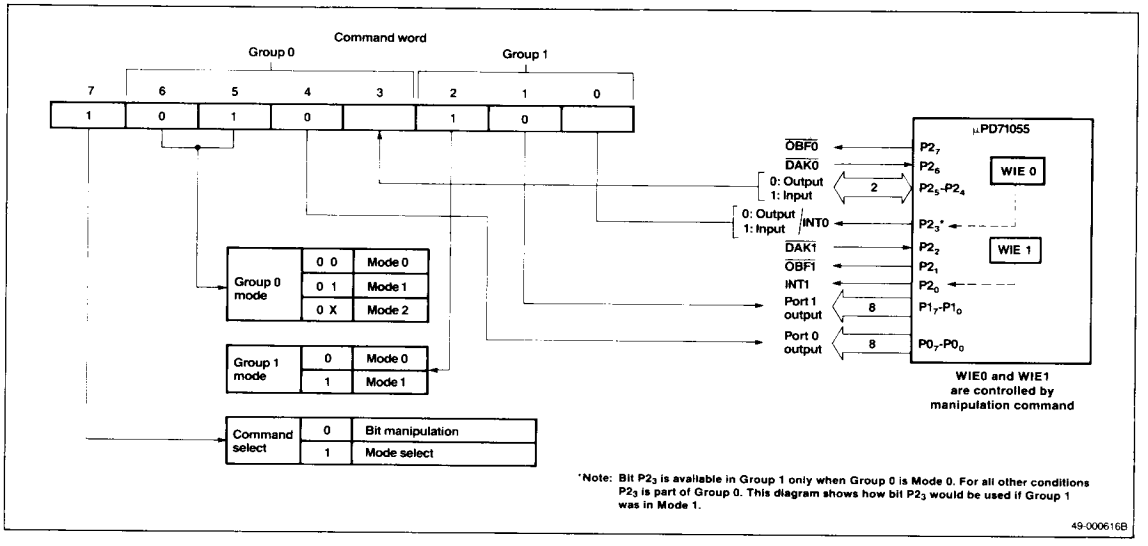
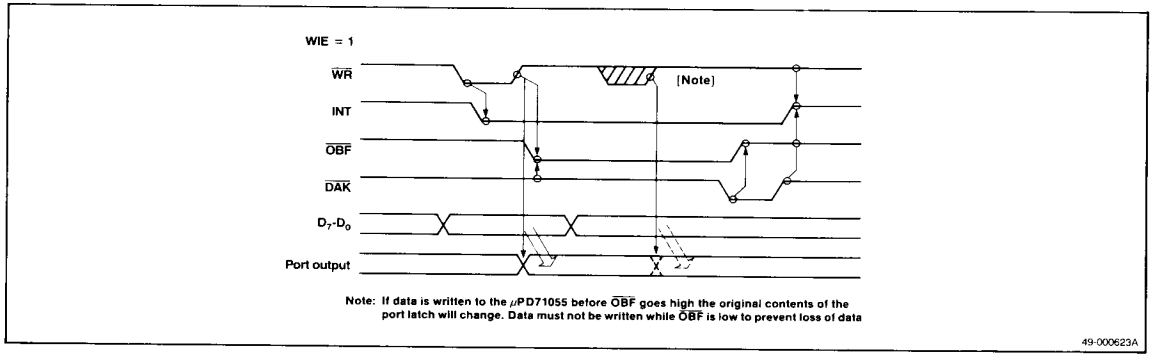



***Figure 12. Mode 1 Output Timing***






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$\overline{DAK}$ **[Data Acknowledge].** When this input is low, it signals the μPD71055 that output port data has been taken from the 71055.

**INT [Interrupt Request].** INT goes high when the output data is taken when WIE is set to 1 and $\overline{WR}$, $\overline{OBF}$ and $\overline{DAK}$ are all high. It goes low at the falling edge of the $\overline{WR}$ signal. INT therefore functions as a write request signal, indicating that new data should be sent to the μPD71055.

**WIE [Write Interrupt Enable Flag].** WIE controls the interrupt output. Interrupts can be enabled by using the bit manipulation command to set this bit to 1 and disabled by resetting it to 0. This signal is internal to the μPD71055 and is not an output. The state of WIE does not affect the function of $\overline{DAK}$ addressed to the same bits of port 2.

When output is specified in mode 1, the status of $\overline{OBF}$, INT and WIE can be obtained by reading the contents of port 2.

Table 2 shows a summary of these signals.

***Table 2. Functions of Port 2 Bits in Mode 1***

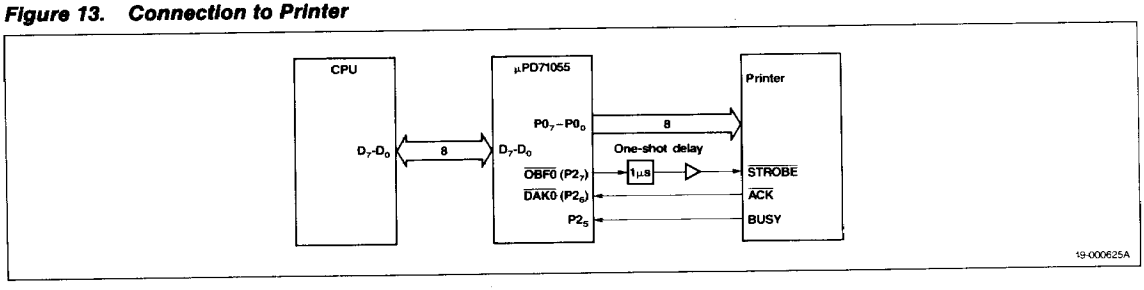
| Group | Bit | Data Input | Data Output |
|---|---|---|---|
| 1 | $P2_0$ | INT1 (Interrupt request) | INT1 (Interrupt request) |
| | $P2_1$ | IBF1 (Input buffer full f/f) | $\overline{OBF1}$ (Output buffer full f/f) |
| | $P2_2$ | $\overline{STB1}$ (Strobe input)<br>RIE1 (Read interrupt enable flag) | $\overline{DAK1}$ (Data acknowledge input)<br>WIE1 (Write interrupt enable flag) |
| | $P2_3$ | I/O (Note) | I/O (Note) |
| 0 | $P2_3$ | INT0 (Interrupt request) | INT0 (Interrupt request) |
| | $P2_4$ | $\overline{STB0}$ (Strobe input)<br>RIE0 (Read interrupt enable flag) | I/O |
| | $P2_5$ | IBF0 (Input buffer full f/f) | I/O |
| | $P2_6$ | I/O | $\overline{DAK0}$ (Data acknowledge input)<br>WIE0 (Write interrupt enable flag) |
| | $P2_7$ | I/O | $\overline{OBF0}$ (Output buffer full f/f) |

**Note:** Can be used with group 1 only when group 0 is set to mode 0. In other modes, $P2_3$ belongs to group 0.

## Mode 1 Example

This example (figure 13) demonstrates connecting a printer to the μPD71055. Group 0 is used in mode 1 output. Group 1 can operate in mode 0 or 1; in this example it is set to mode 0.

***Figure 13. Connection to Printer***






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*Figure 14. Printer Example Subroutine*

```
;This subroutine sends character strings to the printer
INIT:       MOV     AL,10101000B        ;μPD71055 Mode Setting:
                                        ;Group 0: mode 1 output
                                        ;Group 1: mode 0
            OUT     CTRLPORT,AL
            RET
SENDPRN:    MOV     BW,DATA             ;Output data address
PRNLOOP:    MOV     AL,[BW]
            CMP     AL,0FFH             ;End if data = 0FFH
            BNZ     WAIT
            RET
WAIT:       IN      AL,PORT2
            TEST1   AL,7                ;Wait until output buffer is empty
            BZ      WAIT
            TEST1   AL,5                ;Wait until printer can accept data
            BNZ     WAIT
            MOV     AL,[BW]             ;Send data to printer
            OUT     PORT0,AL
            INC     BW
            BR      PRNLOOP
```

5e

## Mode 2

Mode 2 can only be used by group 0. In this mode, port 0 functions as a bidirectional 8-bit data port operating under the control of the upper five bits of port 2 as control/status signals. In this mode, port 0 combines the input and output operations of mode 1. See figures 15 and 16.

In mode 2, the status of the following signals can be determined by reading port 2: $\overline{OBF0}$, IBF0, INT0, WIE0, and RIE0.

The $\overline{DAK0}$ and $\overline{STB0}$ signals are used to select input or output for port 0. By using these signals, bidirectional operation between the μPD71055 and peripheral can be realized.

In mode 2, the bit manipulation command is used to write to port 2.

### Control/Status Port Operation

The following control/status signals are used for output:

**$\overline{OBF0}$ [Output Buffer Full].** $\overline{OBF0}$ goes low when data is received from the $D_0$-$D_7$ data bus and is latched in the port 0 output buffer. It therefore functions as a receive request signal to the peripheral. $\overline{OBF0}$ goes low at the rising edge of the $\overline{WR0}$ signal (end of data write). It goes high when $\overline{DAK0}$ is low (output data from port 0 received).

**$\overline{DAK0}$ [Data Acknowledge].** $\overline{DAK0}$ is sent to the μPD71055 in response to the $\overline{OBF0}$ signal. It should be set low when data is received from port 0 of the μPD71055.

**WIE0 [Write Interrupt Enable Flag].** WIE0 controls the write interrupt request output. Interrupts are enabled by using the bit manipulation command to set this bit to 1 and disabled by setting it to 0. The state of WIE does not affect the $\overline{DAK}$ function of this pin.

The following control/status signals are used for input:

**$\overline{STB0}$ [Strobe Input].** When $\overline{STB0}$ goes low, the data being sent to the μPD71055 is latched in port 0.

**IBF0 [Input Buffer Full F/F].** When IBF0 goes high, it indicates that the input buffer is full. It functions as a signal which can be used to prohibit further data transfer. IBF0 goes high when $\overline{STB0}$ goes low. It goes low at the rising edge of $\overline{RD0}$ when $\overline{STB0}$ = 1 (read complete).



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***Figure 15. Mode 2***

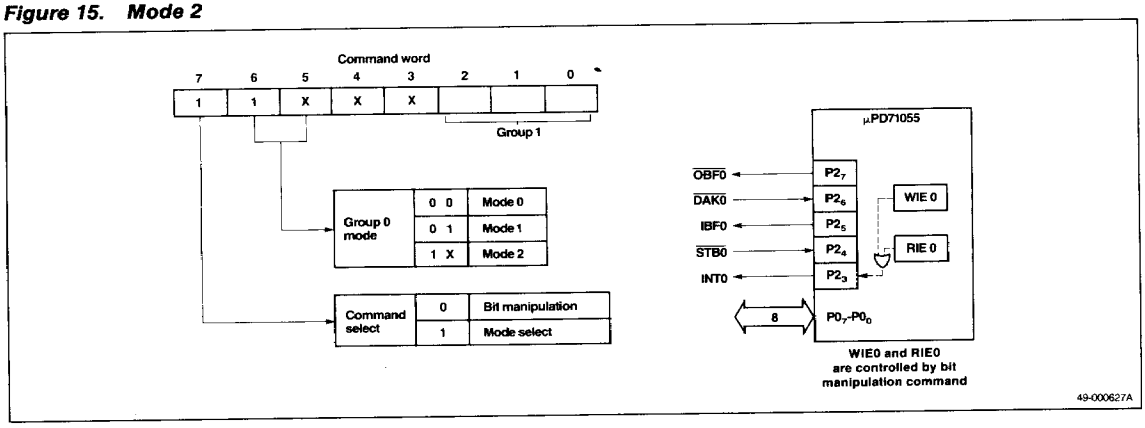
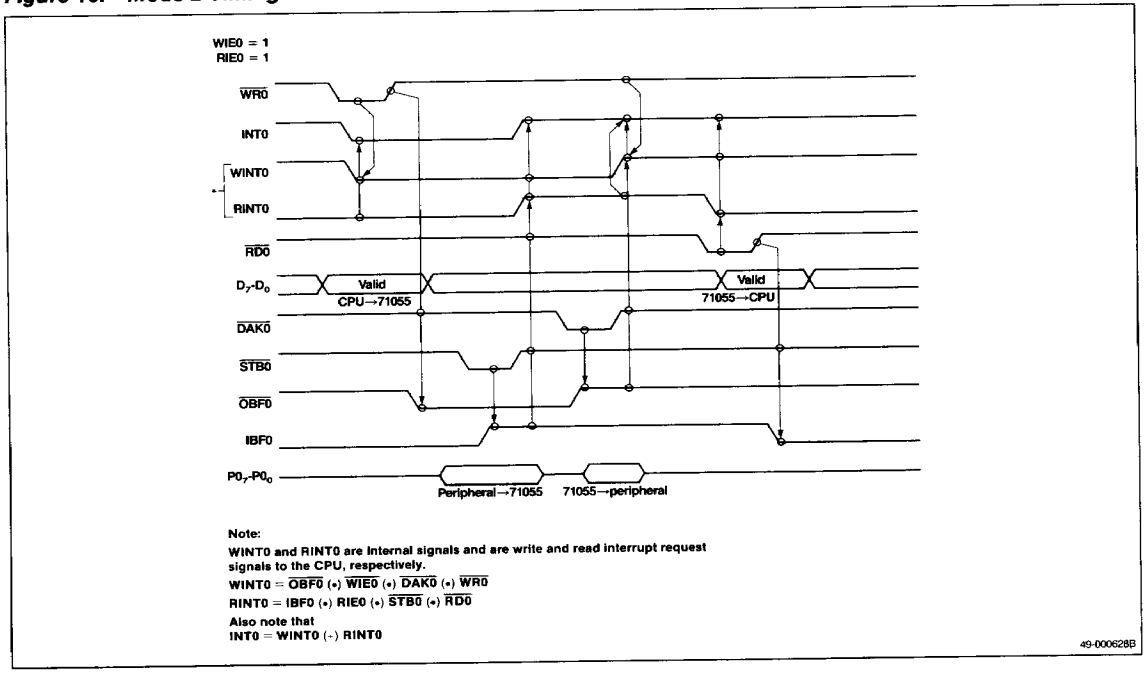



***Figure 16. Mode 2 Timing***






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**RIE0 [Read Interrupt Enable Flag].** RIE0 controls the read interrupt request output. Interrupts are enabled by using the bit manipulation command to set this bit to 1 and disabled by setting it to 0. The state of RIE0 does not affect the $\overline{STB0}$ function of this pin.

This control/status signal is used for both input and output:

**INT0 [Interrupt Request].** During input operations, INT0 functions as a read request interrupt signal. During output, it functions as a write request interrupt signal. This signal is the logical OR of the INT signal for data read (RINT0) and the INT signal for write (WINT0) in mode 1 (RINT0 OR WINT0).

In mode 2, the status of $\overline{OBF0}$, IBF0, INT0, WIE0, and RIE0 can be determined by reading port 2.

Table 3 is a summary of these signals.

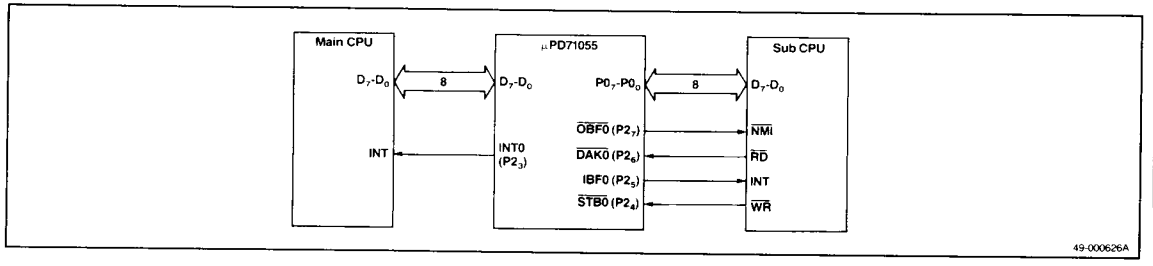
***Table 3. Functions of Port 2 in Mode 2***

| Bit | Function |
|---|---|
| $P2_3$ | INT0 (Interrupt request) |
| $P2_4$ | $\overline{STB0}$ (Strobe input)<br>RIE0 (Read interrupt enable flag) |
| $P2_5$ | IBF0 (Input buffer full f/f) |
| $P2_6$ | $\overline{DAK0}$ (Data acknowledge input)<br>WIE0 (Write interrupt enable flag) |
| $P2_7$ | $\overline{OBF0}$ (Output buffer full f/f) |

## Mode 2 Example

Figures 17, 18, and 19 show data transfer between two CPUs.

***Figure 17. Connecting Two CPUs***

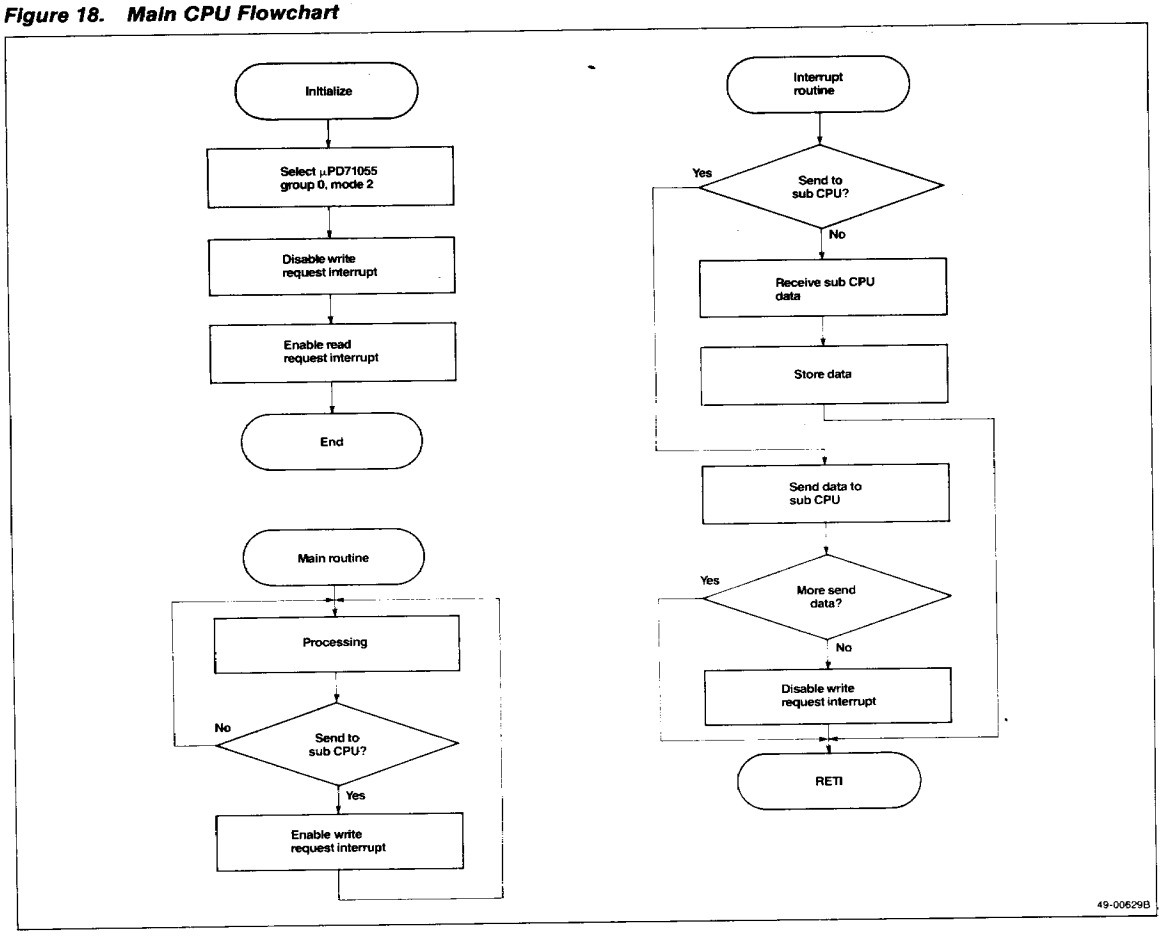



5e



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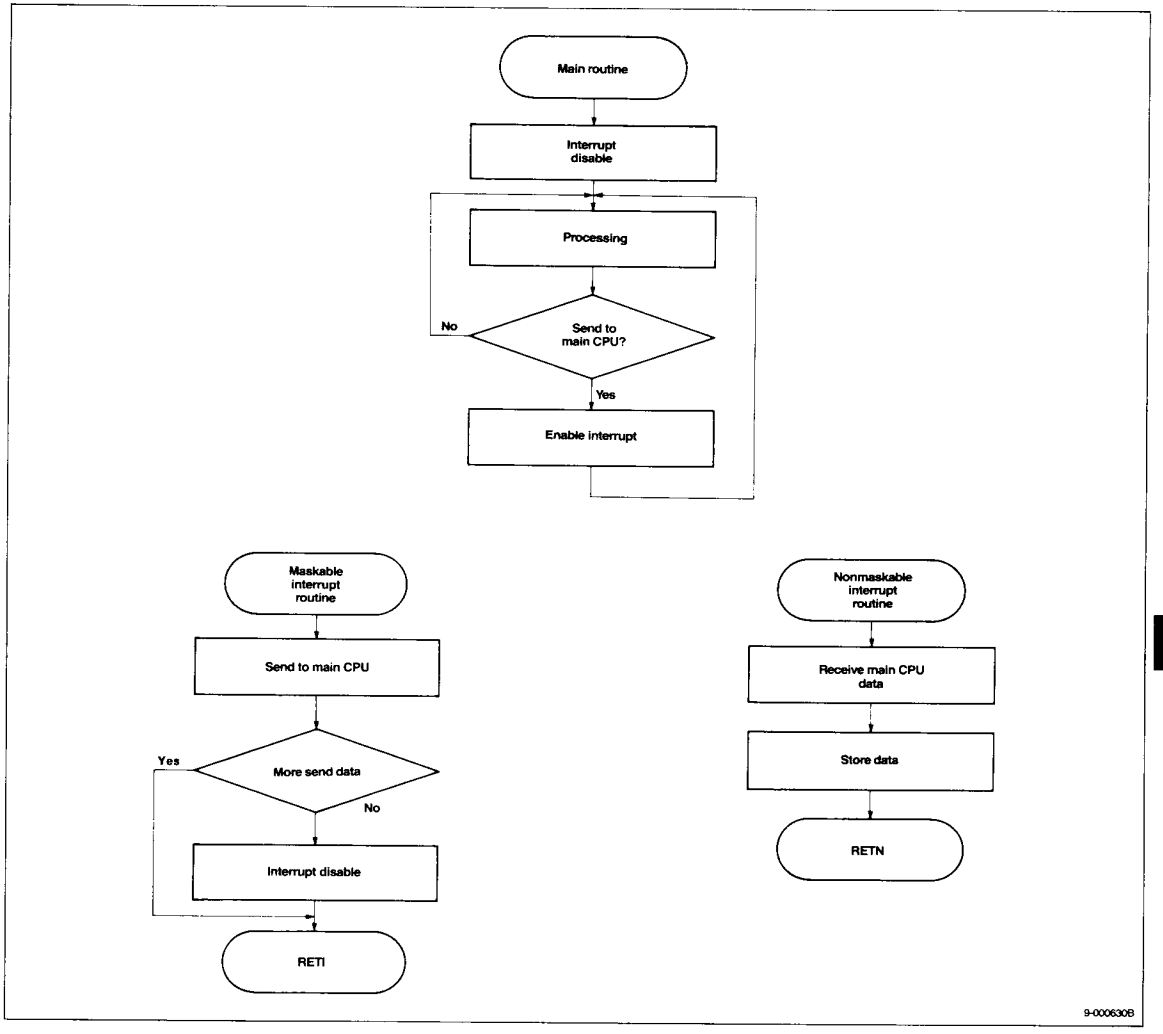
*Figure 18. Main CPU Flowchart*






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*Figure 19. Sub CPU Flowchart*








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## Mode Combinations

Table 4 is a complete list of all the combinations of modes and groups, and the function of the port 2 bits in each mode.

***Table 4. Mode Combinations and Port 2 Bit Functions***

| Group 0 | | | | | | | Group 1 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode | $P0_7$-$P0_0$ | $P2_7$ | $P2_6$ | $P2_5$ | $P2_4$ | $P2_3$ | Mode | $P1_7$-$P1_0$ | $P2_3$ | $P2_2$ | $P2_1$ | $P2_0$ |
| 0 | In | D | D | D | D | NA | 0 | In | D | D | D | D |
| 0 | In | D | D | D | D | NA | 0 | Out | D | D | D | D |
| 0 | In | D | D | D | D | NA | 1 | In | B | $\overline{STB1}$ (RIE1) | IBF1 | INT1 |
| 0 | In | D | D | D | D | NA | 1 | Out | B | $\overline{DAK1}$ (WIE1) | $\overline{OBF1}$ | INT1 |
| 0 | Out | D | D | D | D | NA | 0 | In | D | D | D | D |
| 0 | Out | D | D | D | D | NA | 0 | Out | D | D | D | D |
| 0 | Out | D | D | D | D | NA | 1 | In | B | $\overline{STB1}$ (RIE1) | IBF1 | INT1 |
| 0 | Out | D | D | D | D | NA | 1 | Out | B | $\overline{DAK1}$ (WIE1) | $\overline{OBF1}$ | INT1 |
| 1 | In | B | B | IBF0 | $\overline{STB0}$ (RIE0) | INT0 | 0 | In | NA | D | D | D |
| 1 | In | B | B | IBF0 | $\overline{STB0}$ (RIE0) | INT0 | 0 | Out | NA | D | D | D |
| 1 | In | B | B | IBF0 | $\overline{STB0}$ (RIE0) | INT0 | 1 | In | NA | $\overline{STB1}$ (RIE1) | IBF1 | INT1 |
| 1 | In | B | B | IBF0 | $\overline{STB0}$ (RIE0) | INT0 | 1 | Out | NA | $\overline{DAK1}$ (WIE1) | $\overline{OBF1}$ | INT1 |
| 1 | Out | $\overline{OBF0}$ | $\overline{DAK0}$ (WIE0) | B | B | INT0 | 0 | In | NA | D | D | D |
| 1 | Out | $\overline{OBF0}$ | $\overline{DAK0}$ (WIE0) | B | B | INT0 | 0 | Out | NA | D | D | D |
| 1 | Out | $\overline{OBF0}$ | $\overline{DAK0}$ (WIE0) | B | B | INT0 | 1 | In | NA | $\overline{STB1}$ (RIE1) | IBF1 | INT1 |
| 1 | Out | $\overline{OBF0}$ | $\overline{DAK0}$ (WIE0) | B | B | INT0 | 1 | Out | NA | $\overline{DAK1}$ (WIE1) | $\overline{OBF1}$ | INT1 |
| 2 | I/O | $\overline{OBF0}$ | $\overline{DAK0}$ (WIE0) | IBF0 | $\overline{STB0}$ (RIE0) | INT0 | 0 | In | NA | D | D | D |
| 2 | I/O | $\overline{OBF0}$ | $\overline{DAK0}$ (WIE0) | IBF0 | $\overline{STB0}$ (RIE0) | INT0 | 0 | Out | NA | D | D | D |
| 2 | I/O | $\overline{OBF0}$ | $\overline{DAK0}$ (WIE0) | IBF0 | $\overline{STB0}$ (RIE0) | INT0 | 1 | In | NA | $\overline{STB1}$ (RIE1) | IBF1 | INT1 |
| 2 | I/O | $\overline{OBF0}$ | $\overline{DAK0}$ (WIE0) | IBF0 | $\overline{STB0}$ (RIE0) | INT0 | 1 | Out | NA | $\overline{DAK1}$ (WIE1) | $\overline{OBF1}$ | INT1 |

**Note:**

(1) In this chart, "NA" indicates that the bit cannot be used by this group.

(2) The symbol "B" indicates bits that can only be rewritten by the bit manipulation command.

(3) In this chart, "D" indicates that is used by the user.

(4) Symbols in parentheses are internal flags. They are not output to port 2 pins and they cannot be read by the host.

(5) In indicates Input, Out indicates Output, and I/O indicates Input/Output.



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