

# MOS INTEGRATED CIRCUIT

# $\mu$ PD70F3003A, 70F3025A

## V853™

## 32-/16-BIT SINGLE-CHIP MICROCONTROLLER

### DESCRIPTION

The  $\mu$ PD70F3003A and  $\mu$ PD70F3025A have a flash memory instead of the internal mask ROM of the  $\mu$ PD703003A/703004A and  $\mu$ PD703025A, respectively. This model is useful for small-scale production of a variety of application sets or early start of production since the program can be written and erased by the user even with the  $\mu$ PD70F3003 mounted on the board.

Functions in detail are described in the following user's manuals. Be sure to read these manuals when you design your systems.

V853 User's Manual-Hardware : U10913E

V850 Family™ User's Manual-Architecture: U10243E

### FEATURES

- Compatible with  $\mu$ PD703003A, 703004A and 703025A
  - Can be replaced with mask ROM model for mass production of application set
    - $\mu$ PD70F3003A  $\rightarrow$   $\mu$ PD703003A, 703004A
    - $\mu$ PD70F3025A  $\rightarrow$   $\mu$ PD703025A
- Internal memory      Flash memory: 128K bytes ( $\mu$ PD70F3003A)  
256K bytes ( $\mu$ PD70F3025A)

**Remark** For differences among the products, refer to **1. DIFFERENCES AMONG PRODUCT.**

### ORDERING INFORMATION

| Part Number                               | Package                                        | Maximum Operating Frequency (MHz) |
|-------------------------------------------|------------------------------------------------|-----------------------------------|
| $\mu$ PD70F3003AGC-25-8EU                 | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) | 25                                |
| $\mu$ PD70F3003AGC-33-8EU                 | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) | 33                                |
| $\mu$ PD70F3025AGC-25-8EU <sup>Note</sup> | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) | 25                                |
| $\mu$ PD70F3025AGC-33-8EU <sup>Note</sup> | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) | 33                                |

**Note** Under development

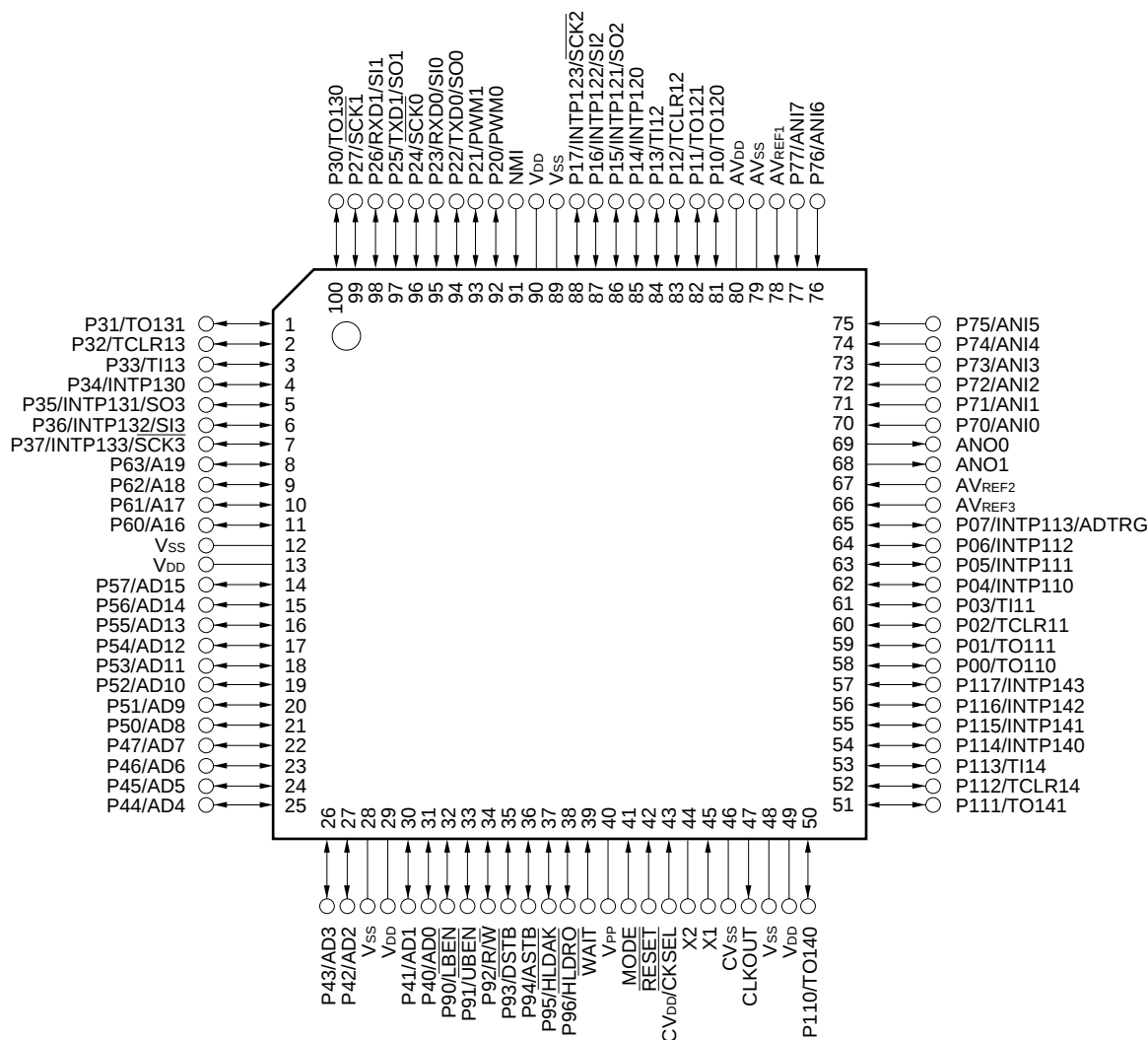
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

# PIN CONFIGURATION (Top View)

- 100-Pin Plastic LQFP (fine pitch) (14 × 14 mm)

μPD70F3003AGC-25-8EU    μPD70F3025AGC-25-8EU

μPD70F3003AGC-33-8EU    μPD70F3025AGC-33-8EU

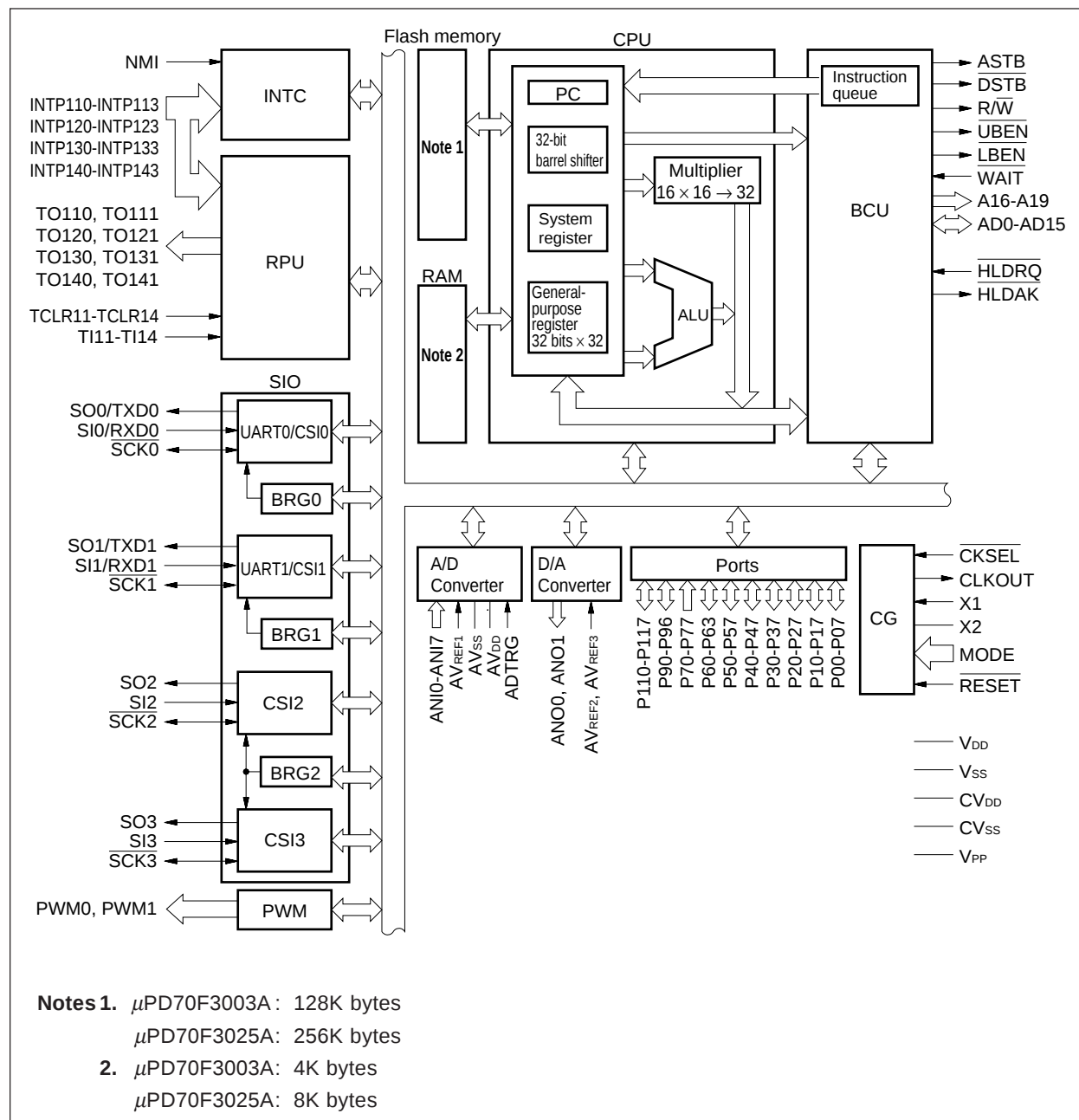


**Caution** Connect VPP pin to VSS pin except the case that μPD70F3003A or 70F3025A is used in flash memory programming mode.

# PIN NAMES

|                                        |                                      |                 |                            |
|----------------------------------------|--------------------------------------|-----------------|----------------------------|
| A16-A19                                | : Address Bus                        | P40-P47         | : Port4                    |
| AD0-AD15                               | : Address/Data Bus                   | P50-P57         | : Port5                    |
| ADTRG                                  | : AD Trigger Input                   | P60-P63         | : Port6                    |
| ANI0-ANI7                              | : Analog Input                       | P70-P77         | : Port7                    |
| ANO0, ANO1                             | : Analog Output                      | P90-P96         | : Port9                    |
| ASTB                                   | : Address Strobe                     | P110-P117       | : Port11                   |
| AV <sub>DD</sub>                       | : Analog V <sub>DD</sub>             | PWM0, PWM1      | : Pulse Width Modulation   |
| AV <sub>REF1</sub> -AV <sub>REF3</sub> | : Analog Reference Voltage           | RESET           | : Reset                    |
| AV <sub>SS</sub>                       | : Analog V <sub>SS</sub>             | R/W             | : Read/Write Status        |
| CV <sub>DD</sub>                       | : Power Supply for Clock Generator   | RXD0, PXD1      | : Receive Data             |
| CV <sub>SS</sub>                       | : Ground for Clock Generator         | SCK0-SCK3       | : Serial Clock             |
| CKSEL                                  | : Clock Select                       | SI0-SI3         | : Serial Input             |
| CLKOUT                                 | : Clock Output                       | SO0-SO3         | : Serial Output            |
| DSTB                                   | : Data Strobe                        | TO110, TO111,   | : Timer Output             |
| HLD <sub>AK</sub>                      | : Hold Acknowledge                   | TO120, TO121,   |                            |
| HLD <sub>RQ</sub>                      | : Hold Request                       | TO130, TO131,   |                            |
| INTP110-INTP113,                       | : Interrupt Request from Peripherals | TO140, TO141    |                            |
| INTP120-INTP123,                       |                                      | TCLR11-TCLR14   | : Timer Clear              |
| INTP130-INTP133,                       |                                      | TI11-TI14       | : Timer Input              |
| INTP140-INTP143                        |                                      | TXD0, TXD1      | : Transmit Data            |
| LBEN                                   | : Lower Byte Enable                  | UBEN            | : Upper Byte Enable        |
| MODE                                   | : Mode                               | WAIT            | : Wait                     |
| NMI                                    | : Non-maskable Interrupt Request     | X1, X2          | : Crystal                  |
| P00-P07                                | : Port0                              | V <sub>DD</sub> | : Power Supply             |
| P10-P17                                | : Port1                              | V <sub>PP</sub> | : Programming Power Supply |
| P20-P27                                | : Port2                              | V <sub>SS</sub> | : Ground                   |
| P30-P37                                | : Port3                              |                 |                            |

# INTERNAL BLOCK DIAGRAM



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## 1. DIFFERENCES AMONG PRODUCTS

| Parameter                   |                               |                  | μPD703003                                                                               | μPD703003A                     | μPD703004A | μPD703025A | μPD70F3003   | μPD70F3003A                    | μPD70F3025A |
|-----------------------------|-------------------------------|------------------|-----------------------------------------------------------------------------------------|--------------------------------|------------|------------|--------------|--------------------------------|-------------|
| Internal ROM                |                               |                  | Mask ROM                                                                                |                                |            |            | Flash memory |                                |             |
|                             |                               |                  | 128K bytes                                                                              |                                | 96K bytes  | 256K bytes | 128K bytes   |                                | 256K bytes  |
| Internal RAM                |                               |                  | 4K bytes                                                                                |                                |            | 8K bytes   | 4K bytes     |                                | 8K bytes    |
| Operation mode              | Normal operation mode         | Single chip mode | Provided                                                                                |                                |            |            |              |                                |             |
|                             |                               | ROM-less mode    | Provided                                                                                | None                           |            |            | Provided     | None                           |             |
|                             | Flash memory programming mode |                  | None                                                                                    |                                |            |            | Provided     |                                |             |
| V <sub>PP</sub> pin         |                               |                  | None                                                                                    |                                |            |            | Provided     |                                |             |
| CKC register value at reset |                               |                  | 00H                                                                                     | MODE = 0: 03H<br>MODE = 1: 00H |            |            | 00H          | MODE = 0: 03H<br>MODE = 1: 00H |             |
| Electrical specifications   |                               |                  | Current consumption, etc. differs. (Refer to each product data sheets.)                 |                                |            |            |              |                                |             |
| Others                      |                               |                  | Noise immunity and noise radiation differ because circuit scale and mask layout differ. |                                |            |            |              |                                |             |

## 2. PIN FUNCTIONS

### 2.1 Port Pins

(1/2)

| Pin Name | I/O | Function                                                                        | Shared with:  |
|----------|-----|---------------------------------------------------------------------------------|---------------|
| P00      | I/O | Port 0<br>8-bit I/O port.<br>Can be set in input or output mode in 1-bit units. | TO110         |
| P01      |     |                                                                                 | TO111         |
| P02      |     |                                                                                 | TCLR11        |
| P03      |     |                                                                                 | TI11          |
| P04      |     |                                                                                 | INTP110       |
| P05      |     |                                                                                 | INTP111       |
| P06      |     |                                                                                 | INTP112       |
| P07      |     |                                                                                 | INTP113/ADTRG |
| P10      | I/O | Port 1<br>8-bit I/O port.<br>Can be set in input or output mode in 1-bit units. | TO120         |
| P11      |     |                                                                                 | TO121         |
| P12      |     |                                                                                 | TCLR12        |
| P13      |     |                                                                                 | TI12          |
| P14      |     |                                                                                 | INTP120       |
| P15      |     |                                                                                 | INTP121/SO2   |
| P16      |     |                                                                                 | INTP122/SI2   |
| P17      |     |                                                                                 | INTP123/SCK2  |
| P20      | I/O | Port 2<br>8-bit I/O port.<br>Can be set in input or output mode in 1-bit units. | PWM0          |
| P21      |     |                                                                                 | PWM1          |
| P22      |     |                                                                                 | TXD0/SO0      |
| P23      |     |                                                                                 | RXD0/SI0      |
| P24      |     |                                                                                 | SCK0          |
| P25      |     |                                                                                 | TXD1/SO1      |
| P26      |     |                                                                                 | RXD1/SI1      |
| P27      |     |                                                                                 | SCK1          |
| P30      | I/O | Port 3<br>8-bit I/O port.<br>Can be set in input or output mode in 1-bit units. | TO130         |
| P31      |     |                                                                                 | TO131         |
| P32      |     |                                                                                 | TCLR13        |
| P33      |     |                                                                                 | TI13          |
| P34      |     |                                                                                 | INTP130       |
| P35      |     |                                                                                 | INTP131/SO3   |
| P36      |     |                                                                                 | INTP132/SI3   |
| P37      |     |                                                                                 | INTP133/SCK3  |
| P40-P47  | I/O | Port 4<br>8-bit I/O port.<br>Can be set in input or output mode in 1-bit units. | AD0-AD7       |
| P50-P57  | I/O | Port 5<br>8-bit I/O port.<br>Can be set in input or output mode in 1-bit units. | AD8-AD15      |

(2/2)

| Pin Name | I/O   | Function                                                                         | Shared with:                |
|----------|-------|----------------------------------------------------------------------------------|-----------------------------|
| P60-P63  | I/O   | Port 6<br>4-bit I/O port.<br>Can be set in input or output mode in 1-bit units.  | A16-A19                     |
| P70-P77  | Input | Port 7<br>8-bit input port.                                                      | ANI0-ANI7                   |
| P90      | I/O   | Port 9<br>7-bit I/O port.<br>Can be set in input or output mode in 1-bit units.  | $\overline{\text{LBEN}}$    |
| P91      |       |                                                                                  | $\overline{\text{UBEN}}$    |
| P92      |       |                                                                                  | $\overline{\text{R/W}}$     |
| P93      |       |                                                                                  | $\overline{\text{DSTB}}$    |
| P94      |       |                                                                                  | $\overline{\text{ASTB}}$    |
| P95      |       |                                                                                  | $\overline{\text{HLD\!AK}}$ |
| P96      |       |                                                                                  | $\overline{\text{HLD\!RQ}}$ |
| P110     | I/O   | Port 11<br>8-bit I/O port.<br>Can be set in input or output mode in 1-bit units. | TO140                       |
| P111     |       |                                                                                  | TO141                       |
| P112     |       |                                                                                  | TCLR14                      |
| P113     |       |                                                                                  | TI14                        |
| P114     |       |                                                                                  | INTP140                     |
| P115     |       |                                                                                  | INTP141                     |
| P116     |       |                                                                                  | INTP142                     |
| P117     |       |                                                                                  | INTP143                     |

## 2.2 Pins Other Than Port Pins

(1/2)

| Pin Name | I/O    | Function                                                                                | Shared with: |
|----------|--------|-----------------------------------------------------------------------------------------|--------------|
| TO110    | Output | Pulse signal output of timer 11-14                                                      | P00          |
| TO111    |        |                                                                                         | P01          |
| TO120    |        |                                                                                         | P10          |
| TO121    |        |                                                                                         | P11          |
| TO130    |        |                                                                                         | P30          |
| TO131    |        |                                                                                         | P31          |
| TO140    |        |                                                                                         | P110         |
| TO141    |        |                                                                                         | P111         |
| TCLR11   | Input  | External clear signal of timer 11-14                                                    | P02          |
| TCLR12   |        |                                                                                         | P12          |
| TCLR13   |        |                                                                                         | P32          |
| TCLR14   |        |                                                                                         | P112         |
| TI11     | Input  | External count clock of timer 11-14                                                     | P03          |
| TI12     |        |                                                                                         | P13          |
| TI13     |        |                                                                                         | P33          |
| TI14     |        |                                                                                         | P113         |
| INTP110  | Input  | External maskable interrupt reuest input and external capture trigger input of timer 11 | P04          |
| INTP111  |        |                                                                                         | P05          |
| INTP112  |        |                                                                                         | P06          |
| INTP113  |        |                                                                                         | P07/ADTRG    |
| INTP120  | Input  | External maskable interrupt reuest input and external capture trigger input of timer 12 | P14          |
| INTP121  |        |                                                                                         | P15/SO2      |
| INTP122  |        |                                                                                         | P16/S12      |
| INTP123  |        |                                                                                         | P17/SCK2     |
| INTP130  | Input  | External maskable interrupt reuest input and external capture trigger input of timer 13 | P34          |
| INTP131  |        |                                                                                         | P35/SO3      |
| INTP132  |        |                                                                                         | P36/SI3      |
| INTP133  |        |                                                                                         | P37/SCK3     |
| INTP140  | Input  | External maskable interrupt reuest input and external capture trigger input of timer 14 | P114         |
| INTP141  |        |                                                                                         | P115         |
| INTP142  |        |                                                                                         | P116         |
| INTP143  |        |                                                                                         | P117         |
| SO0      | Output | Serial transmit data output of CSI0-CSI3 (3 wire)                                       | P22/TXD0     |
| SO1      |        |                                                                                         | P25/TXD1     |
| SO2      |        |                                                                                         | P15/INTP121  |
| SO3      |        |                                                                                         | P35/INTP131  |
| SI0      | Input  | Serial receive data output of CSI0-CSI3 (3 wire)                                        | P23/RXD0     |
| SI1      |        |                                                                                         | P26/RXD1     |
| SI2      |        |                                                                                         | P16/INTP122  |
| SI3      |        |                                                                                         | P36/INTP132  |

(2/2)

| Pin Name                       | I/O    | Function                                                                                | Shared with:              |
|--------------------------------|--------|-----------------------------------------------------------------------------------------|---------------------------|
| $\overline{\text{SCK0}}$       | I/O    | Serial clock I/O of CSI0-CSI3 (3 wire)                                                  | P24                       |
| $\overline{\text{SCK1}}$       |        |                                                                                         | P27                       |
| $\overline{\text{SCK2}}$       |        |                                                                                         | P17/INTP123               |
| $\overline{\text{SCK3}}$       |        |                                                                                         | P37/INTP133               |
| TXD0                           | Output | Serial transmit data output of UART0-UART1                                              | P22/SO0                   |
| TXD1                           |        |                                                                                         | P25/SO1                   |
| RXD0                           | Input  | Serial receive data input of UART0-UART1                                                | P23/SI0                   |
| RXD1                           |        |                                                                                         | P26/SI1                   |
| PWM0                           | Output | Pulse signal output of PWM                                                              | P20                       |
| PWM1                           |        |                                                                                         | P21                       |
| AD0-AD7                        | I/O    | 16-bit multiplexed address/data bus when external memory is connected                   | P40-P47                   |
| AD8-AD15                       |        |                                                                                         | P50-P57                   |
| A16-A19                        | Output | High-order address bus when external memory is connected                                | P60-P63                   |
| $\overline{\text{LBEN}}$       | Output | Low-order byte enable signal output of external data bus                                | P90                       |
| $\overline{\text{UBEN}}$       |        | High-order byte enable signal output of external data bus                               | P91                       |
| $\text{R}/\overline{\text{W}}$ | Output | External read/write status output                                                       | P92                       |
| $\overline{\text{DSTB}}$       |        | External data strobe signal output                                                      | P93                       |
| ASTB                           |        | External address strobe signal output                                                   | P94                       |
| $\overline{\text{HLD\!AK}}$    | Output | Bus hold acknowledge output                                                             | P95                       |
| $\overline{\text{HLDRQ}}$      | Input  | Bus hold request input                                                                  | P96                       |
| ANI0-ANI7                      | Input  | Analog input to A/D converter                                                           | P70-P77                   |
| ANO0, ANO1                     | Output | Analog output of D/A converter                                                          | —                         |
| NMI                            | Input  | Non-maskable interrupt request input                                                    | —                         |
| CLKOUT                         | Output | System clock output                                                                     | —                         |
| $\overline{\text{CKSEL}}$      | Input  | Input specifying operation mode of clock generator                                      | CV <sub>DD</sub>          |
| $\overline{\text{WAIT}}$       | Input  | Control signal input inserting wait state in bus cycle                                  | —                         |
| MODE                           | Input  | Operation mode specification                                                            | —                         |
| $\overline{\text{RESET}}$      | Input  | System reset input                                                                      | —                         |
| X1                             | Input  | System clock resonator connection. Input external clock to X1 to supply external clock. | —                         |
| X2                             | —      |                                                                                         | —                         |
| ADTRG                          | Input  | A/D converter external trigger input                                                    | P07/INTP113               |
| AV <sub>REF1</sub>             | Input  | Reference voltage input for A/D converter                                               | —                         |
| AV <sub>REF2</sub>             | Input  | Reference voltage input for D/A converter                                               | —                         |
| AV <sub>REF3</sub>             |        |                                                                                         | —                         |
| AV <sub>DD</sub>               | —      | Positive power supply for A/D converter                                                 | —                         |
| AV <sub>SS</sub>               | —      | Ground potential for A/D converter                                                      | —                         |
| CV <sub>DD</sub>               | —      | Positive power supply for internal clock generator                                      | $\overline{\text{CKSEL}}$ |
| CV <sub>SS</sub>               | —      | Ground potential for internal clock generator                                           | —                         |
| V <sub>DD</sub>                | —      | Positive power supply                                                                   | —                         |
| V <sub>SS</sub>                | —      | Ground potential                                                                        | —                         |
| V <sub>PP</sub>                | —      | High voltage application pin when program is written/verified                           | —                         |

### 2.3 I/O Circuits of Pins and Recommended Connections of Unused Pins

Table 2-1 shows the I/O circuit type of each pin, and the recommended connections of the unused pins. Figure 2-1 shows a partially simplified diagram of each circuit.

When connecting a pin to  $V_{DD}$  or  $V_{SS}$  via resistor, use of a resistor of 1 to 10 k $\Omega$  is recommended.

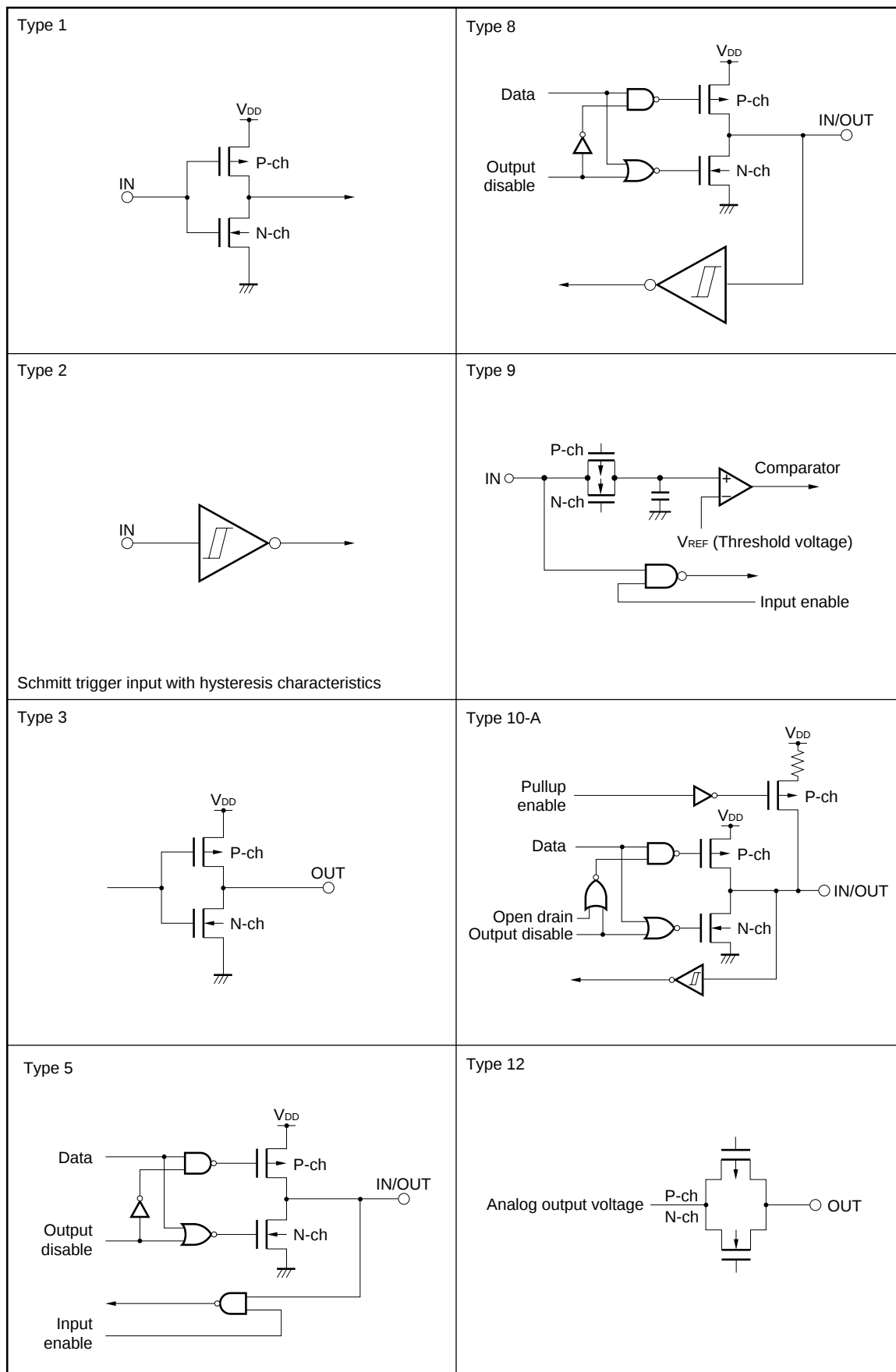
**Table 2-1. I/O Circuit Types of Each Pin and Recommended Connections of Unused Pins (1/2)**

| Pin                                                                                                                                                                                             | I/O Circuit Type | Recommended Connections                                                                           |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------------------------------------------------------------------------------------------------|
| P00/TO110, P01/TO111                                                                                                                                                                            | 5                | Input : Individually connect to $V_{DD}$ or $V_{SS}$ via resistor.<br>Output : Leave unconnected. |
| P02/TCLR11, P03/TI11,<br>P04/INTP110-P07/INTP113/ADTRG                                                                                                                                          | 8                |                                                                                                   |
| P10-TO120, P11/TO121                                                                                                                                                                            | 5                |                                                                                                   |
| P12/TCLR12, P13/TI12<br>P14/INTP120<br>P15/INTP121/SO2<br>P16/INTP122/SI2<br>P17/INTP123/ $\overline{SCK2}$                                                                                     | 8                |                                                                                                   |
| P20/PWM0, P21/PWM1<br>P22/TXD0/SO0                                                                                                                                                              | 5                |                                                                                                   |
| P23/RXD0/SI0, P24/ $\overline{SCK0}$                                                                                                                                                            | 8                |                                                                                                   |
| P25/TXD1/SO1                                                                                                                                                                                    | 5                |                                                                                                   |
| P26/RXD1/SI1, P27/ $\overline{SCK1}$                                                                                                                                                            | 8                |                                                                                                   |
| P30/TO130, P31/TO131                                                                                                                                                                            | 5                |                                                                                                   |
| P32/TCLR13, P33/TI13<br>P34/INTP130                                                                                                                                                             | 8                |                                                                                                   |
| P35/INTP131/SO3<br>P36/INTP132/SI3<br>P37/INTP133/ $\overline{SCK3}$                                                                                                                            | 10-A             |                                                                                                   |
| P40/AD0-P47/AD7<br>P50/AD8-P57/AD15<br>P60/A16-P63/A19                                                                                                                                          | 5                |                                                                                                   |
| P70/ANI0-P77/ANI7                                                                                                                                                                               | 9                |                                                                                                   |
| P90/ $\overline{LBEN}$<br>P91/ $\overline{UBEN}$<br>P92/ $\overline{R/W}$<br>P93/ $\overline{DSTB}$<br>P94/ASTB<br>P95/HLDA $\overline{K}$<br>P96/HLDR $\overline{Q}$<br>P110/TO140, P111/TO141 | 5                |                                                                                                   |
| P112/TCLR14, P113/TI14<br>P114/INTP140-P117/INTP143                                                                                                                                             | 8                |                                                                                                   |

Table 2-1. I/O Circuit Types of Each Pin and Recommended Connections of Unused Pins (2/2)

| Pin                                                       | I/O Circuit Type | Recommended Connections               |
|-----------------------------------------------------------|------------------|---------------------------------------|
| ANO0, ANO1                                                | 12               | Leave unconnected.                    |
| NMI                                                       | 2                | Directly connect to V <sub>SS</sub> . |
| CLKOUT                                                    | 3                | Leave unconnected.                    |
| $\overline{\text{WAIT}}$                                  | 1                | Directly connect to V <sub>DD</sub> . |
| MODE                                                      | 2                | —                                     |
| $\overline{\text{RESET}}$                                 |                  | —                                     |
| CV <sub>DD</sub> /CKSEL                                   |                  | —                                     |
| AV <sub>REF1</sub> -AV <sub>REF3</sub> , AV <sub>SS</sub> | —                | Directly connect to V <sub>SS</sub> . |
| AV <sub>DD</sub>                                          | —                | Directly connect to V <sub>DD</sub> . |
| V <sub>PP</sub>                                           | —                | Connect to V <sub>SS</sub> .          |

Figure 2-1. I/O Circuits of Pins



### 3. ELECTRICAL SPECIFICATIONS

#### 3.1 Normal Operation Mode

##### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

| Parameter                      | Symbol     | Condition                                                                          |                       | Ratings                 | Unit             |
|--------------------------------|------------|------------------------------------------------------------------------------------|-----------------------|-------------------------|------------------|
| Supply voltage                 | $V_{DD}$   | $V_{DD}$ pin                                                                       |                       | -0.5 to +7.0            | V                |
|                                | $CV_{DD}$  | $CV_{DD}$ pin                                                                      |                       | -0.5 to $V_{DD} + 0.3$  | V                |
|                                | $CV_{SS}$  | $CV_{SS}$ pin                                                                      |                       | -0.5 to +0.5            | V                |
|                                | $AV_{DD}$  | $AV_{DD}$ pin                                                                      |                       | -0.5 to $V_{DD} + 0.3$  | V                |
|                                | $AV_{SS}$  | $AV_{SS}$ pin                                                                      |                       | -0.5 to +0.5            | V                |
| Input voltage                  | $V_{I1}$   | <b>Note</b> , $V_{DD} = 5.0\text{ V} \pm 10\%$                                     |                       | -0.5 to $V_{DD} + 0.3$  | V                |
|                                | $V_{I2}$   | $V_{PP}$ pin in flash memory programming mode,<br>$V_{DD} = 5.0\text{ V} \pm 10\%$ |                       | -0.5 to +11.0           | V                |
| Clock input voltage            | $V_K$      | X1 pin, $V_{DD} = 5.0\text{ V} \pm 10\%$                                           |                       | -0.5 to $V_{DD} + 1.0$  | V                |
| Output current, low            | $I_{CL}$   | 1 pin                                                                              |                       | 4.0                     | mA               |
|                                |            | Total of all pins                                                                  |                       | 100                     | mA               |
| Output current, high           | $I_{CH}$   | 1 pin                                                                              |                       | -4.0                    | mA               |
|                                |            | Total of all pins                                                                  |                       | -100                    | mA               |
| Output voltage                 | $V_O$      | $V_{DD} = 5.0\text{ V} \pm 10\%$                                                   |                       | -0.5 to $V_{DD} + 0.3$  | V                |
| Analog input voltage           | $V_{IAN}$  | P70/ANI0-P77/ANI7                                                                  | $AV_{DD} > V_{DD}$    | -0.5 to $V_{DD} + 0.3$  | V                |
|                                |            |                                                                                    | $V_{DD} \geq AV_{DD}$ | -0.5 to $AV_{DD} + 0.3$ | V                |
| Analog reference input voltage | $AV_{REF}$ | $AV_{REF1}-AV_{REF3}$                                                              | $AV_{DD} > V_{DD}$    | -0.5 to $V_{DD} + 0.3$  | V                |
|                                |            |                                                                                    | $V_{DD} \geq AV_{DD}$ | -0.5 to $AV_{DD} + 0.3$ | V                |
| Operating ambient temperature  | $T_A$      |                                                                                    |                       | -40 to +85              | $^\circ\text{C}$ |
| ★ Storage temperature          | $T_{stg}$  |                                                                                    |                       | -65 to +125             | $^\circ\text{C}$ |

**Note** Except X1, P70/AN0-P77/AN7,  $AV_{REF1}-AV_{REF3}$

- Cautions**
1. Do not directly connect the output (or I/O) pins of two or more IC products, and do not directly connect them to  $V_{DD}$ ,  $V_{CC}$ , or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.
  2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the program may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.  
The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

**Capacitance ( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{SS} = 0\text{ V}$ )**

| Parameter          | Symbol   | Condition                                               | MIN. | TYP. | MAX. | Unit |
|--------------------|----------|---------------------------------------------------------|------|------|------|------|
| Input capacitance  | $C_i$    | $f_c = 1\text{ MHz}$<br>Pins other than tested pin: 0 V |      |      | 15   | pF   |
| I/O capacitance    | $C_{IO}$ |                                                         |      |      | 15   | pF   |
| Output capacitance | $C_o$    |                                                         |      |      | 15   | pF   |

★ **Operating Conditions**

| Operation Mode           | Internal Operating Clock Frequency ( $\phi$ ) | Operating Temperature ( $T_A$ ) | Supply Voltage ( $V_{DD}$ ) |
|--------------------------|-----------------------------------------------|---------------------------------|-----------------------------|
| Direct mode,<br>PLL mode | 2 to 33 MHz <sup>Note 1</sup>                 | $-40$ to $+85^\circ\text{C}$    | $5.0\text{ V} \pm 10\%$     |
|                          | 5 to 33 MHz <sup>Note 2</sup>                 | $-40$ to $+85^\circ\text{C}$    | $5.0\text{ V} \pm 10\%$     |

- Notes 1.** When A/D converter not used.  
**2.** When A/D converter used.

**DC Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )**

(1/2)

| Parameter                               | Symbol          | Condition                                                | MIN.           | TYP. | MAX.           | Unit          |
|-----------------------------------------|-----------------|----------------------------------------------------------|----------------|------|----------------|---------------|
| Input voltage, high                     | $V_{IH}$        | Except X1 and <b>Note 1</b>                              | 2.2            |      | $V_{DD} + 0.3$ | V             |
|                                         |                 | <b>Note 1</b>                                            | $0.8 V_{DD}$   |      | $V_{DD} + 0.3$ | V             |
| Input voltage, low                      | $V_{IL}$        | Except X1 and <b>Note 1</b>                              | $-0.5$         |      | +0.8           | V             |
|                                         |                 | <b>Note 1</b>                                            | $-0.5$         |      | $0.2 V_{DD}$   | V             |
| Clock input voltage, high               | $V_{XH}$        | X1                                                       | $0.8 V_{DD}$   |      | $V_{DD} + 0.5$ | V             |
| Clock input voltage, low                | $V_{XL}$        | X1                                                       | $-0.5$         |      | 0.6            | V             |
| Schmitt trigger input threshold voltage | $V_T^+$         | <b>Note 1</b> , rising                                   |                | 3.0  |                | V             |
|                                         | $V_T^-$         | <b>Note 1</b> , falling                                  |                | 2.0  |                | V             |
| Schmitt trigger input hysteresis width  | $V_T^+ - V_T^-$ | <b>Note 1</b>                                            | 0.5            |      |                | V             |
| Output voltage, high                    | $V_{OH}$        | $I_{OH} = -2.5\text{ mA}$                                | $0.7 V_{DD}$   |      |                | V             |
|                                         |                 | $I_{OH} = -100\text{ }\mu\text{A}$                       | $V_{DD} - 0.4$ |      |                | V             |
| Output voltage, low                     | $V_{OL}$        | $I_{OC} = 2.5\text{ mA}$                                 |                |      | 0.45           | V             |
| Input leakage current, high             | $I_{LIH}$       | $V_i = V_{DD}$                                           |                |      | 10             | $\mu\text{A}$ |
| Input leakage current, low              | $I_{LIL}$       | $V_i = 0\text{ V}$                                       |                |      | -10            | $\mu\text{A}$ |
| Output leakage current, high            | $I_{LOH}$       | $V_o = V_{DD}$                                           |                |      | 10             | $\mu\text{A}$ |
| Output leakage current, low             | $I_{LOL}$       | $V_o = 0\text{ V}$                                       |                |      | -10            | $\mu\text{A}$ |
| Software pull-up resistor               | R               | P35/INTP131/SO3,<br>P36/INTP132/SI3,<br>P37/INTP133/SCK3 | 15             | 40   | 90             | k $\Omega$    |

(2/2)

| Parameter      |                  |              | Symbol           | Condition                     | MIN. | TYP.                     | MAX.                     | Unit    |
|----------------|------------------|--------------|------------------|-------------------------------|------|--------------------------|--------------------------|---------|
| Supply current | $\mu$ PD70F3003A | Operating    | I <sub>DD1</sub> | Direct mode <sup>Note 2</sup> |      | $2.2 \times \phi + 7.5$  | $2.5 \times \phi + 22$   | mA      |
|                |                  |              |                  | PLL mode <sup>Note 2</sup>    |      | $2.3 \times \phi + 9.5$  | $2.6 \times \phi + 25$   | mA      |
|                |                  | In HALT mode | I <sub>DD2</sub> | Direct mode <sup>Note 2</sup> |      | $1.2 \times \phi + 7.5$  | $1.3 \times \phi + 15$   | mA      |
|                |                  |              |                  | PLL mode <sup>Note 2</sup>    |      | $1.3 \times \phi + 9.5$  | $1.4 \times \phi + 17$   | mA      |
|                |                  | In IDLE mode | I <sub>DD3</sub> | Direct mode <sup>Note 2</sup> |      | $8 \times \phi + 300$    | $10 \times \phi + 500$   | $\mu$ A |
|                |                  |              |                  | PLL mode <sup>Note 2</sup>    |      | $0.1 \times \phi + 2$    | $0.2 \times \phi + 3$    | mA      |
|                |                  | In STOP mode | I <sub>DD4</sub> | CESEL = 0, <b>Note 3</b>      |      | 2                        | 50                       | $\mu$ A |
|                |                  |              |                  | CESEL = 0, <b>Note 4</b>      |      | 2                        | 200                      | $\mu$ A |
|                |                  |              |                  | CESEL = 1, <b>Note 3</b>      |      | 30                       | 200                      | $\mu$ A |
|                |                  |              |                  | CESEL = 1, <b>Note 4</b>      |      | 30                       | 500                      | $\mu$ A |
|                | $\mu$ PD70F3025A | Operating    | I <sub>DD1</sub> | Direct mode <sup>Note 2</sup> |      | $2.5 \times \phi + 8$    | $2.8 \times \phi + 22.5$ | mA      |
|                |                  |              |                  | PLL mode <sup>Note 2</sup>    |      | $2.6 \times \phi + 10$   | $2.9 \times \phi + 25.5$ | mA      |
|                |                  | In HALT mode | I <sub>DD2</sub> | Direct mode <sup>Note 2</sup> |      | $1.3 \times \phi + 7.5$  | $1.4 \times \phi + 15$   | mA      |
|                |                  |              |                  | PLL mode <sup>Note 2</sup>    |      | $1.3 \times \phi + 12.5$ | $1.4 \times \phi + 20$   | mA      |
|                |                  | In IDLE mode | I <sub>DD3</sub> | Direct mode <sup>Note 2</sup> |      | $8 \times \phi + 300$    | $10 \times \phi + 500$   | $\mu$ A |
|                |                  |              |                  | PLL mode <sup>Note 2</sup>    |      | $0.1 \times \phi + 2$    | $0.2 \times \phi + 3$    | mA      |
|                |                  | In STOP mode | I <sub>DD4</sub> | CESEL = 0, <b>Note 3</b>      |      | 2                        | 50                       | $\mu$ A |
|                |                  |              |                  | CESEL = 0, <b>Note 4</b>      |      | 2                        | 200                      | $\mu$ A |
|                |                  |              |                  | CESEL = 1, <b>Note 3</b>      |      | 60                       | 300                      | $\mu$ A |
|                |                  |              |                  | CESEL = 1, <b>Note 4</b>      |      | 60                       | 500                      | $\mu$ A |

**Notes 1.** P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE

**2.** When A/D converter used :  $\phi = 5$  to 33 MHz

When A/D converter not used:  $\phi = 2$  to 33 MHz

**3.**  $-40^{\circ}\text{C} \leq T_A \leq +50^{\circ}\text{C}$

**4.**  $50^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$

**Remarks 1.** TYP. value is a value for your reference at  $T_A = 25^{\circ}\text{C}$  and  $V_{DD} = 5.0\text{ V}$ . The supply current does not include  $AV_{REF1}$ - $AV_{REF3}$  and the current running through the software pull-up resistor.

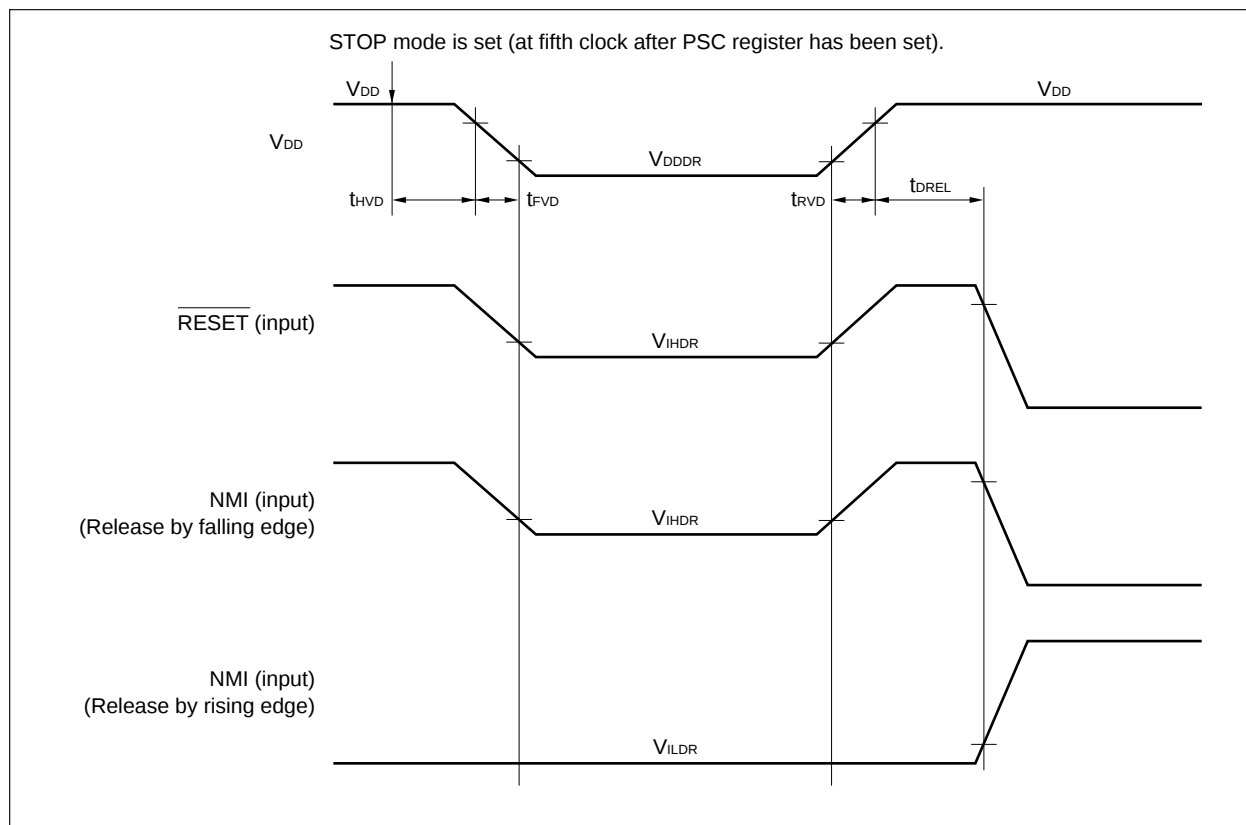
**2.**  $\phi$ : Internal system clock frequency

**Data Retention Characteristics (T<sub>A</sub> = -40 to +85°C)**

| Parameter                                           | Symbol            | Condition                                                          | MIN.                  | TYP.                  | MAX.                  | Unit |
|-----------------------------------------------------|-------------------|--------------------------------------------------------------------|-----------------------|-----------------------|-----------------------|------|
| Data hold voltage                                   | V <sub>DDDR</sub> | STOP mode                                                          | 1.5                   |                       | 5.5                   | V    |
| Data hold current                                   | I <sub>DDDR</sub> | V <sub>DD</sub> = V <sub>DDDR</sub> -40°C ≤ T <sub>A</sub> ≤ +50°C |                       | 0.2 V <sub>DDDR</sub> | 50                    | μA   |
|                                                     |                   | 50°C < T <sub>A</sub> ≤ 85°C                                       |                       | 0.2 V <sub>DDDR</sub> | 200                   | μA   |
| Supply voltage rise time                            | t <sub>RVD</sub>  |                                                                    | 200                   |                       |                       | μs   |
| Supply voltage fall time                            | t <sub>FVD</sub>  |                                                                    | 200                   |                       |                       | μs   |
| Supply voltage hold time<br>(vs. STOP mode setting) | t <sub>HVD</sub>  |                                                                    | 0                     |                       |                       | ms   |
| STOP mode release signal input time                 | t <sub>DREL</sub> |                                                                    | 0                     |                       |                       | ns   |
| Data hold input voltage, high                       | V <sub>IHDR</sub> | Note                                                               | 0.9 V <sub>DDDR</sub> |                       | V <sub>DDDR</sub>     | V    |
| Data hold input voltage, low                        | V <sub>ILDR</sub> | Note                                                               | 0                     |                       | 0.1 V <sub>DDDR</sub> | V    |

**Note** P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE, X1

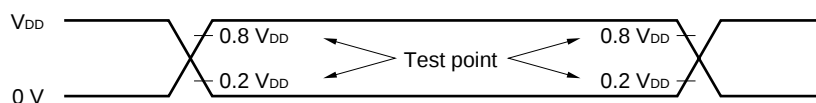
**Remark** TYP. value is a value for your reference at T<sub>A</sub> = 25°C and V<sub>DD</sub> = 5.0 V.



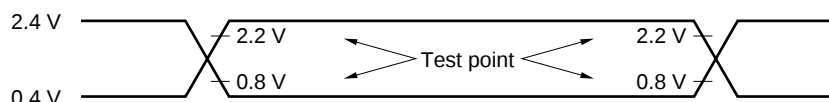
AC Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )

AC test input wave

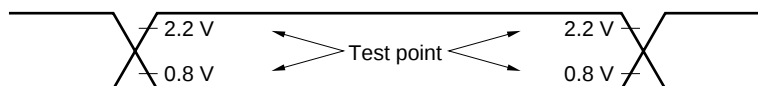
- (a) P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112, TCLR14, P113/TI14, P114/INTP140-P117/INTP143, RESET, NMI, MODE, X1



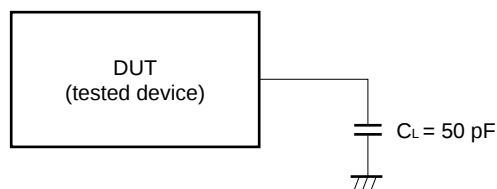
- (b) Other than (a)



AC test output test point



Load condition



**Caution** If the load capacitance exceeds  $50\text{ pF}$  due to the circuit configuration, decrease the load capacitance of this device to less than  $50\text{ pF}$  by using a buffer.

## (1) Clock timing

| Parameter                 | Symbol |           | Condition                     | 25 MHz Model  |               | 33 MHz Model  |               | Unit |
|---------------------------|--------|-----------|-------------------------------|---------------|---------------|---------------|---------------|------|
|                           |        |           |                               | MIN.          | MAX.          | MIN.          | MAX.          |      |
| ★ X1 input cycle          | <1>    | $t_{CYX}$ | Direct mode                   | 20            | <b>Note 1</b> | 15            | <b>Note 1</b> | ns   |
|                           |        |           | PLL mode<br>(PLL lock status) | 200           | <b>Note 1</b> | 151           | <b>Note 1</b> | ns   |
| X1 input width, high      | <2>    | $t_{WXH}$ | Direct mode                   | 7             |               | 6             |               | ns   |
|                           |        |           | PLL mode                      | 80            |               | 60            |               | ns   |
| X1 input width, low       | <3>    | $t_{WXL}$ | Direct mode                   | 7             |               | 6             |               | ns   |
|                           |        |           | PLL mode                      | 80            |               | 60            |               | ns   |
| X1 input rise time        | <4>    | $t_{XR}$  | Direct mode                   |               | 7             |               | 7             | ns   |
|                           |        |           | PLL mode                      |               | 15            |               | 10            | ns   |
| X1 input fall time        | <5>    | $t_{XF}$  | Direct mode                   |               | 7             |               | 7             | ns   |
|                           |        |           | PLL mode                      |               | 15            |               | 10            | ns   |
| ★ CPU operating frequency | —      | $\phi$    |                               | <b>Note 2</b> | 25            | <b>Note 2</b> | 33            | MHz  |
| CLKOUT output cycle       | <6>    | $t_{CYK}$ |                               | 40            | <b>Note 3</b> | 30            | <b>Note 3</b> | ns   |
| CLKOUT width, high        | <7>    | $t_{WKH}$ |                               | 0.5 T – 5     |               | 0.5 T – 5     |               | ns   |
| CLKOUT width, low         | <8>    | $t_{WKL}$ |                               | 0.5 T – 5     |               | 0.5 T – 5     |               | ns   |
| CLKOUT rise time          | <9>    | $t_{XR}$  |                               |               | 5             |               | 5             | ns   |
| CLKOUT fall time          | <10>   | $t_{XF}$  |                               |               | 5             |               | 5             | ns   |
| X1 ↓ → CLKOUT delay time  | <11>   | $t_{DXK}$ | Direct mode                   | 3             | 17            | 3             | 17            | ns   |

**Notes 1.** When A/D converter used: 100 ns

★ When A/D converter not used: 250 ns

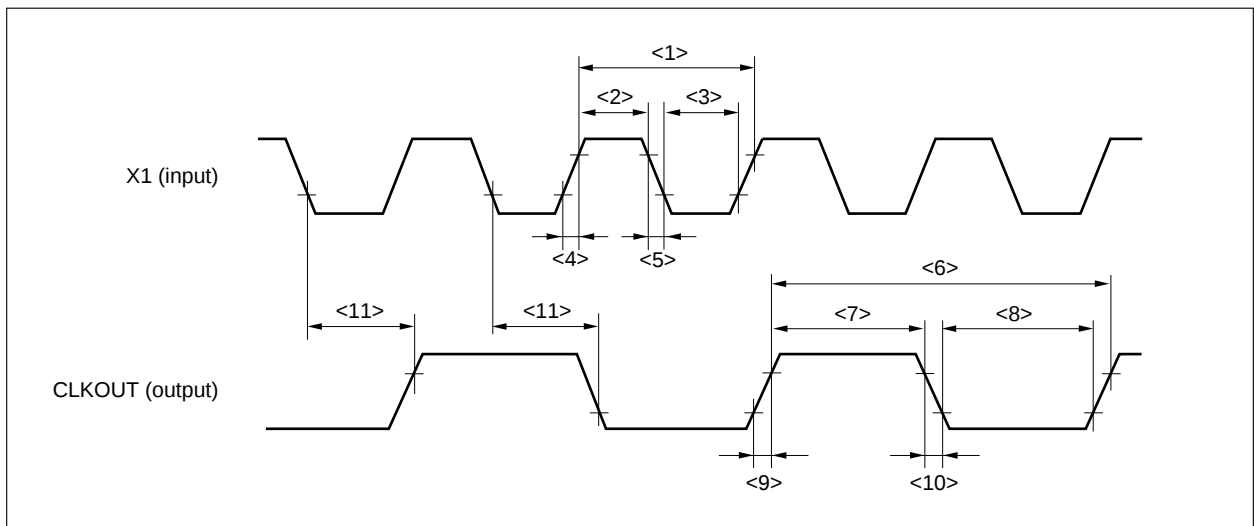
**2.** When A/D converter used: 5 MHz

★ When A/D converter not used: 2 MHz

**3.** When A/D converter used: 200 ns

★ When A/D converter not used: 500 ns

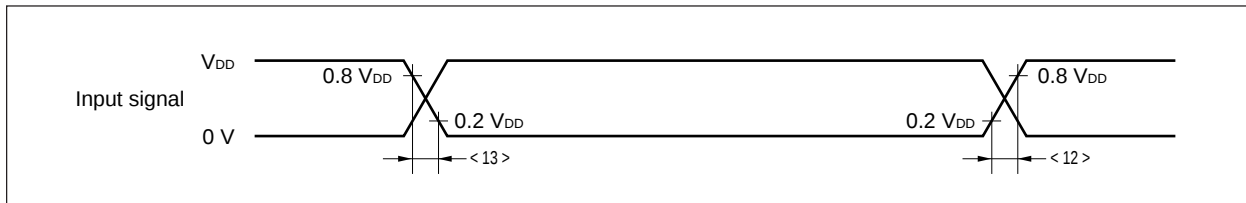
**Remark** T =  $t_{CYK}$



## (2) Input wave

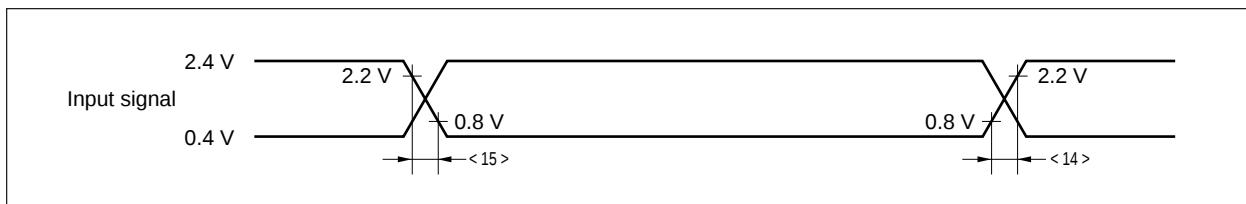
- (a) P02/TCLR11, P03/TI11, P04/INTP110-P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/ $\overline{\text{SCK2}}$ , P23/RXD0/SI0, P24/ $\overline{\text{SCK0}}$ , P26/RXD1/SI1, P27/ $\overline{\text{SCK1}}$ , P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/ $\overline{\text{SCK3}}$ , P112/TCLR14, P113/TI14, P114/INTP140-P117/INTP143,  $\overline{\text{RESET}}$ , NMI, MODE

| Parameter       | Symbol         | Condition | 25 MHz Model |      | 33 MHz Model |      | Unit |
|-----------------|----------------|-----------|--------------|------|--------------|------|------|
|                 |                |           | MIN.         | MAX. | MIN.         | MAX. |      |
| Input rise time | <12> $t_{IR2}$ |           |              | 20   |              | 20   | ns   |
| Input fall time | <13> $t_{IF2}$ |           |              | 20   |              | 20   | ns   |



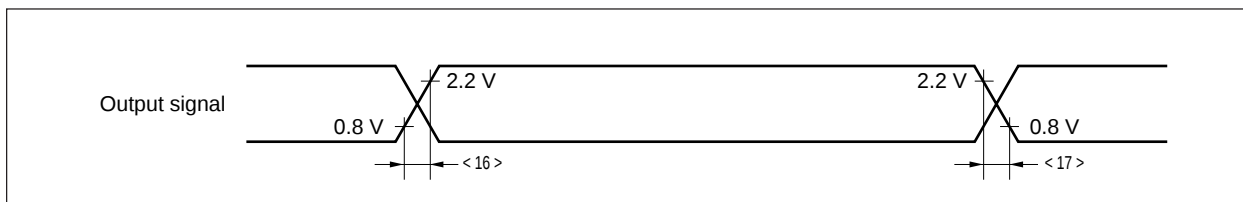
## (b) Other than (a)

| Parameter       | Symbol         | Condition | 25 MHz Model |      | 33 MHz Model |      | Unit |
|-----------------|----------------|-----------|--------------|------|--------------|------|------|
|                 |                |           | MIN.         | MAX. | MIN.         | MAX. |      |
| Input rise time | <14> $t_{IR1}$ |           |              | 10   |              | 10   | ns   |
| Input fall time | <15> $t_{IF1}$ |           |              | 10   |              | 10   | ns   |



(3) Output wave (other than CLKOUT)

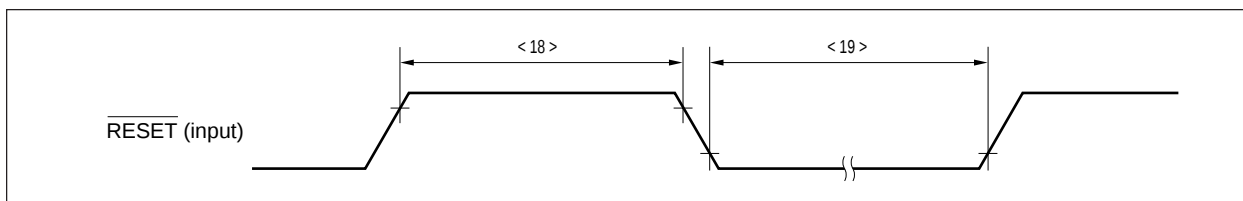
| Parameter        | Symbol        | Condition | 25 MHz Model |      | 33 MHz Model |      | Unit |
|------------------|---------------|-----------|--------------|------|--------------|------|------|
|                  |               |           | MIN.         | MAX. | MIN.         | MAX. |      |
| Output rise time | <16> $t_{OR}$ |           |              | 10   |              | 10   | ns   |
| Output fall time | <17> $t_{OF}$ |           |              | 10   |              | 10   | ns   |



(4) Reset timing

| Parameter         | Symbol          | Condition                                                     | 25 MHz Model    |      | 33 MHz Model    |      | Unit |
|-------------------|-----------------|---------------------------------------------------------------|-----------------|------|-----------------|------|------|
|                   |                 |                                                               | MIN.            | MAX. | MIN.            | MAX. |      |
| RESET width, high | <18> $t_{WRSH}$ |                                                               | 500             |      | 500             |      | ns   |
| RESET width, low  | <19> $t_{WRSL}$ | On power application, or on releasing STOP mode               | $500 + T_{OST}$ |      | $500 + T_{OST}$ |      | ns   |
|                   |                 | Except on power application, or except on releasing STOP mode | 500             |      | 500             |      | ns   |

**Remark**  $T_{OST}$ : oscillation stabilization time



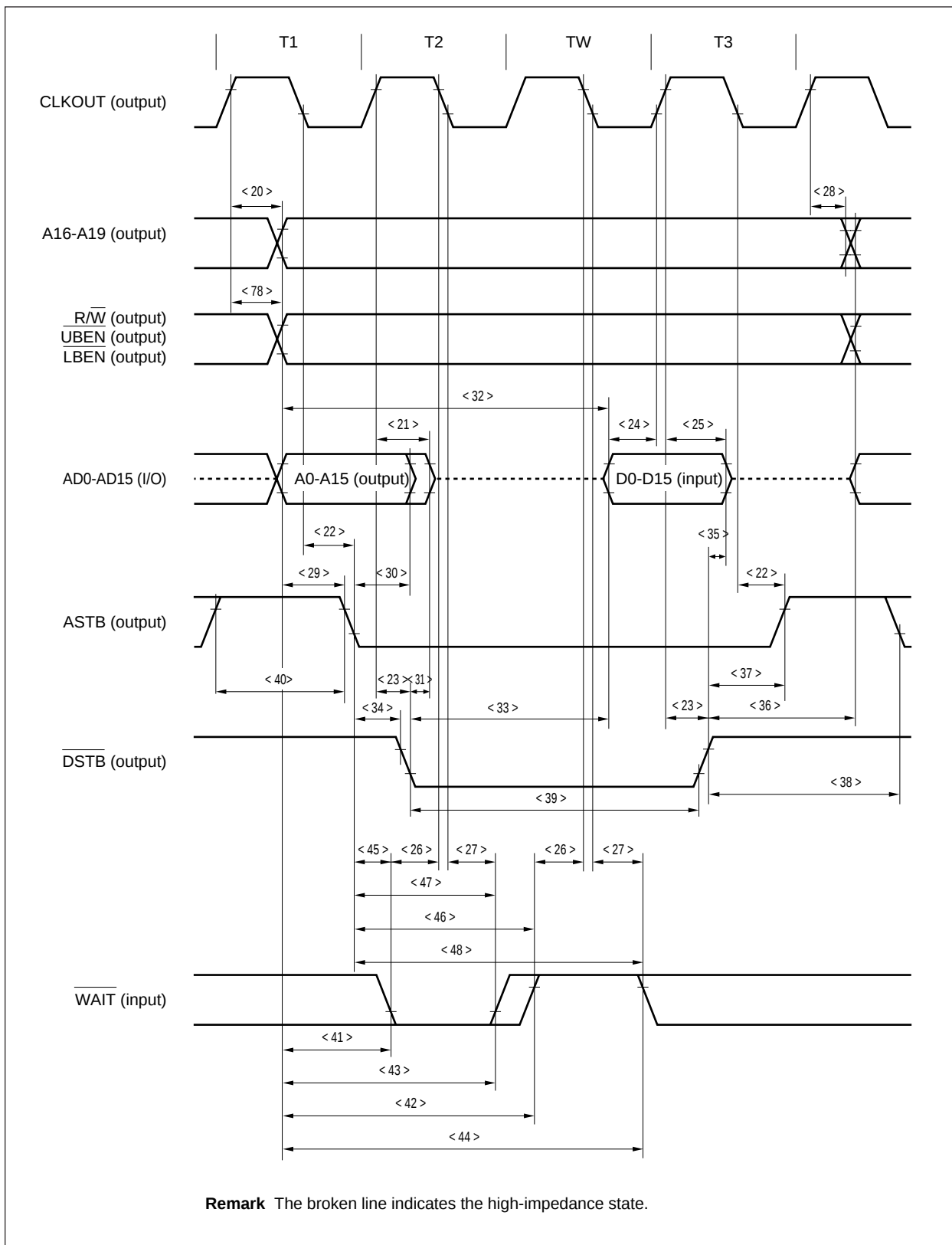
## (5) Read timing (1/2)

| Parameter                                                                                         | Symbol |                     | Condition                                            | 25 MHz Model     |                  | 33 MHz Model     |                  | Unit |
|---------------------------------------------------------------------------------------------------|--------|---------------------|------------------------------------------------------|------------------|------------------|------------------|------------------|------|
|                                                                                                   |        |                     |                                                      | MIN.             | MAX.             | MIN.             | MAX.             |      |
| CLKOUT $\uparrow \rightarrow$ address delay time                                                  | <20>   | t <sub>DKA</sub>    |                                                      | 3                | 20               | 3                | 20               | ns   |
| CLKOUT $\uparrow \rightarrow$ R/W, $\overline{\text{UBEN}}$ , $\overline{\text{LBEN}}$ delay time | <78>   | t <sub>DKA2</sub>   |                                                      | -2               | +13              | -2               | +13              | ns   |
| CLKOUT $\uparrow \rightarrow$ address float delay time                                            | <21>   | t <sub>FKA</sub>    |                                                      | 3                | 15               | 3                | 15               | ns   |
| CLKOUT $\downarrow \rightarrow$ ASTB delay time                                                   | <22>   | t <sub>DKST</sub>   |                                                      | 3                | 15               | 3                | 15               | ns   |
| CLKOUT $\downarrow \rightarrow$ $\overline{\text{DSTB}}$ delay time                               | <23>   | t <sub>DKD</sub>    |                                                      | 3                | 15               | 3                | 15               | ns   |
| Data input setup time (vs. CLKOUT $\uparrow$ )                                                    | <24>   | t <sub>SIDK</sub>   |                                                      | 5                |                  | 5                |                  | ns   |
| Data input hold time (vs. CLKOUT $\uparrow$ )                                                     | <25>   | t <sub>HKID</sub>   |                                                      | 5                |                  | 5                |                  | ns   |
| $\overline{\text{WAIT}}$ setup time (vs. CLKOUT $\downarrow$ )                                    | <26>   | t <sub>SWTK</sub>   |                                                      | 5                |                  | 5                |                  | ns   |
| $\overline{\text{WAIT}}$ hold time (vs. CLKOUT $\downarrow$ )                                     | <27>   | t <sub>HKWT</sub>   |                                                      | 5                |                  | 5                |                  | ns   |
| Address hold time (vs. CLKOUT $\uparrow$ )                                                        | <28>   | t <sub>HKA</sub>    |                                                      | 0                |                  | 0                |                  | ns   |
| Address setup time (vs. ASTB $\downarrow$ )                                                       | <29>   | t <sub>SAST</sub>   | -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C             | 0.5 T - 10       |                  | 0.5 T - 10       |                  | ns   |
|                                                                                                   |        |                     | 70°C < T <sub>A</sub> $\leq$ 85°C                    | 0.5 T - 12       |                  | 0.5 T - 12       |                  | ns   |
| Address hold time (vs. ASTB $\downarrow$ )                                                        | <30>   | t <sub>HSTA</sub>   |                                                      | 0.5 T - 10       |                  | 0.5 T - 10       |                  | ns   |
| $\overline{\text{DSTB}}$ $\downarrow \rightarrow$ address float delay time                        | <31>   | t <sub>FDA</sub>    |                                                      |                  | 0                |                  | 0                | ns   |
| Data input setup time (vs. address)                                                               | <32>   | t <sub>SAID</sub>   | -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C             |                  | (2 + n) T - 22   |                  | (2 + n) T - 22   | ns   |
|                                                                                                   |        |                     | 70°C < T <sub>A</sub> $\leq$ 85°C                    |                  | (2 + n) T - 25   |                  | (2 + n) T - 25   | ns   |
| Data input setup time (vs. $\overline{\text{DSTB}}$ $\downarrow$ )                                | <33>   | t <sub>SDID</sub>   | -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C             |                  | (1 + n) T - 20   |                  | (1 + n) T - 20   | ns   |
|                                                                                                   |        |                     | 70°C < T <sub>A</sub> $\leq$ 85°C                    |                  | (1 + n) T - 24   |                  | (1 + n) T - 24   | ns   |
| ASTB $\downarrow \rightarrow$ $\overline{\text{DSTB}}$ $\downarrow$ delay time                    | <34>   | t <sub>DSTD</sub>   |                                                      | 0.5 T - 10       |                  | 0.5 T - 10       |                  | ns   |
| Data input hold time (vs. $\overline{\text{DSTB}}$ $\uparrow$ )                                   | <35>   | t <sub>HDID</sub>   |                                                      | 0                |                  | 0                |                  | ns   |
| $\overline{\text{DSTB}}$ $\uparrow \rightarrow$ address output delay time                         | <36>   | t <sub>DDA</sub>    |                                                      | (1 + i) T        |                  | (1 + i) T        |                  | ns   |
| $\overline{\text{DSTB}}$ $\uparrow \rightarrow$ ASTB $\uparrow$ delay time                        | <37>   | t <sub>DDSTH</sub>  |                                                      | 0.5 T - 10       |                  | 0.5 T - 10       |                  | ns   |
| $\overline{\text{DSTB}}$ $\uparrow \rightarrow$ ASTB $\downarrow$ delay time                      | <38>   | t <sub>DDSTL</sub>  |                                                      | (1.5 + i) T - 10 |                  | (1.5 + i) T - 10 |                  | ns   |
| $\overline{\text{DSTB}}$ width, low                                                               | <39>   | t <sub>WDL</sub>    | -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C             | (1 + n) T - 10   |                  | (1 + n) T - 10   |                  | ns   |
|                                                                                                   |        |                     | 70°C < T <sub>A</sub> $\leq$ 85°C                    | (1 + n) T - 13   |                  | (1 + n) T - 13   |                  | ns   |
| ASTB width, high                                                                                  | <40>   | t <sub>WSTH</sub>   |                                                      | T - 10           |                  | T - 10           |                  | ns   |
| $\overline{\text{WAIT}}$ setup time (vs. address)                                                 | <41>   | t <sub>SAWT1</sub>  | n $\geq$ 1, -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C |                  | 1.5 T - 20       |                  | 1.5 T - 20       | ns   |
|                                                                                                   |        |                     | n $\geq$ 1, 70°C < T <sub>A</sub> $\leq$ 85°C        |                  | 1.5 T - 24       |                  | 1.5 T - 24       | ns   |
|                                                                                                   | <42>   | t <sub>SAWT2</sub>  | n $\geq$ 1, -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C |                  | (1.5 + n) T - 20 |                  | (1.5 + n) T - 20 | ns   |
|                                                                                                   |        |                     | n $\geq$ 1, 70°C < T <sub>A</sub> $\leq$ 85°C        |                  | (1.5 + n) T - 24 |                  | (1.5 + n) T - 24 | ns   |
| $\overline{\text{WAIT}}$ hold time (vs. address)                                                  | <43>   | t <sub>HAWT1</sub>  | n $\geq$ 1                                           | (0.5 + n) T      |                  | (0.5 + n) T      |                  | ns   |
|                                                                                                   | <44>   | t <sub>HAWT2</sub>  | n $\geq$ 1                                           | (1.5 + n) T      |                  | (1.5 + n) T      |                  | ns   |
| $\overline{\text{WAIT}}$ setup time (vs. ASTB $\downarrow$ )                                      | <45>   | t <sub>SSTWT1</sub> | n $\geq$ 1, -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C |                  | T - 18           |                  | T - 18           | ns   |
|                                                                                                   |        |                     | n $\geq$ 1, 70°C < T <sub>A</sub> $\leq$ 85°C        |                  | T - 20           |                  | T - 20           | ns   |
|                                                                                                   | <46>   | t <sub>SSTWT2</sub> | n $\geq$ 1                                           |                  | (1 + n) T - 15   |                  | (1 + n) T - 15   | ns   |
| $\overline{\text{WAIT}}$ hold time (vs. ASTB $\downarrow$ )                                       | <47>   | t <sub>HSTWT1</sub> | n $\geq$ 1                                           | nT               |                  | nT               |                  | ns   |
|                                                                                                   | <48>   | t <sub>HSTWT2</sub> | n $\geq$ 1                                           | (1 + n) T        |                  | (1 + n) T        |                  | ns   |

Remarks 1. T = t<sub>cyk</sub>

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.
3. i indicates the number of idle states (0 or 1) to be inserted in the read cycle.
4. Be sure to observe at least one of data input hold times t<sub>HKID</sub> (<25>) and t<sub>HDID</sub> (<35>).

(5) Read Timing (2/2): 1 wait



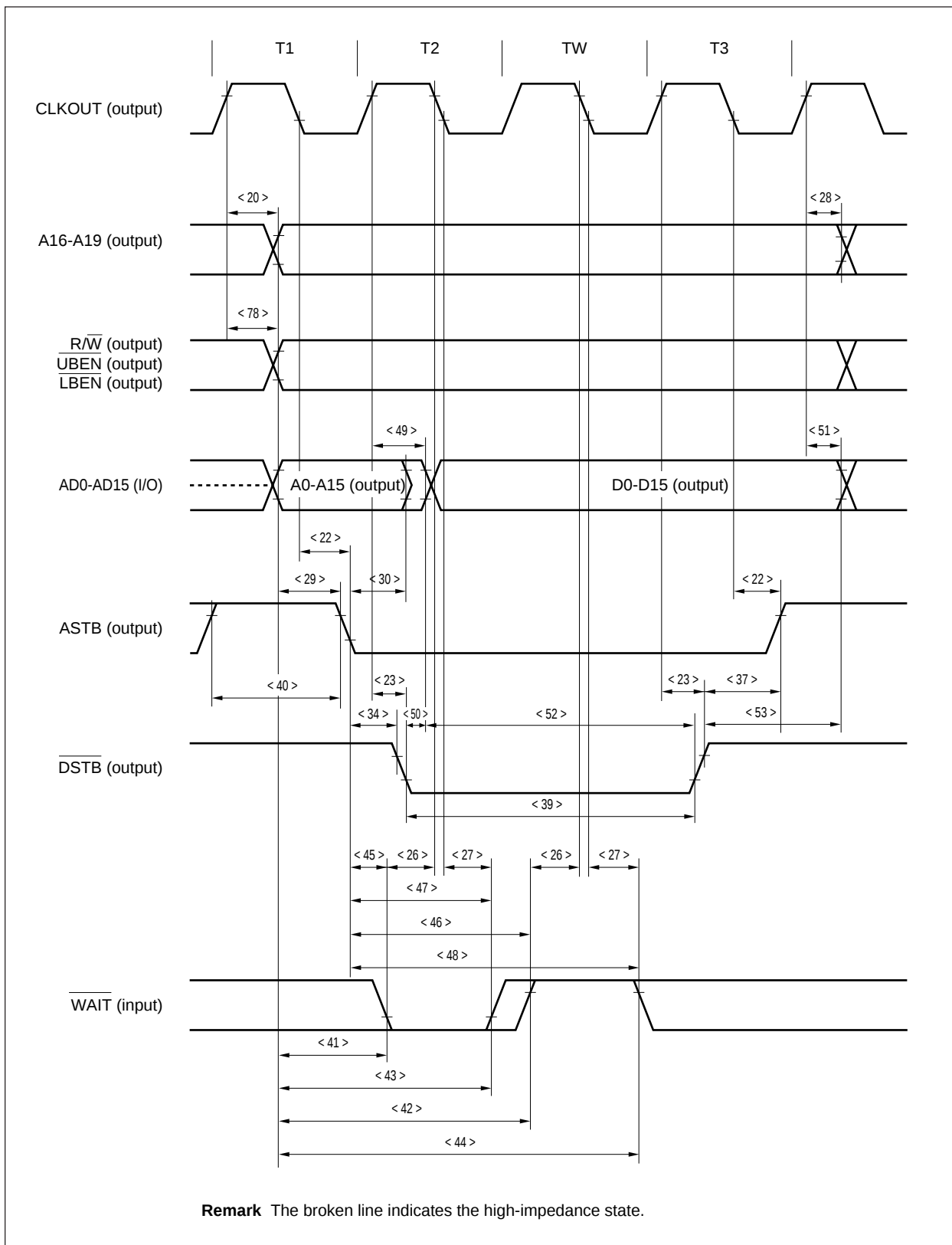
## (6) Write timing (1/2)

| Parameter                                                                           | Symbol |                     | Condition                                            | 25 MHz Model     |      | 33 MHz Model     |      | Unit |
|-------------------------------------------------------------------------------------|--------|---------------------|------------------------------------------------------|------------------|------|------------------|------|------|
|                                                                                     |        |                     |                                                      | MIN.             | MAX. | MIN.             | MAX. |      |
| CLKOUT $\uparrow \rightarrow$ address delay time                                    | <20>   | t <sub>DKA</sub>    |                                                      | 3                | 20   | 3                | 20   | ns   |
| CLKOUT $\uparrow \rightarrow$ R/W, $\overline{UBEN}$ , $\overline{LBEN}$ delay time | <78>   | t <sub>DKA2</sub>   |                                                      | -2               | +13  | -2               | +13  | ns   |
| CLKOUT $\downarrow \rightarrow$ ASTB delay time                                     | <22>   | t <sub>DKST</sub>   |                                                      | 3                | 15   | 3                | 15   | ns   |
| CLKOUT $\uparrow \rightarrow$ $\overline{DSTB}$ delay time                          | <23>   | t <sub>DKD</sub>    |                                                      | 3                | 15   | 3                | 15   | ns   |
| WAIT setup time (vs. CLKOUT $\downarrow$ )                                          | <26>   | t <sub>SWTK</sub>   |                                                      | 5                |      | 5                |      | ns   |
| WAIT hold time (vs. CLKOUT $\downarrow$ )                                           | <27>   | t <sub>HKWT</sub>   |                                                      | 5                |      | 5                |      | ns   |
| Address hold time (vs. CLKOUT $\uparrow$ )                                          | <28>   | t <sub>HKA</sub>    |                                                      | 0                |      | 0                |      | ns   |
| Address setup time (vs. ASTB $\downarrow$ )                                         | <29>   | t <sub>SAST</sub>   | -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C             | 0.5 T - 10       |      | 0.5 T - 10       |      | ns   |
|                                                                                     |        |                     | 70°C < T <sub>A</sub> $\leq$ 85°C                    | 0.5 T - 12       |      | 0.5 T - 12       |      | ns   |
| Address hold time (vs. ASTB $\downarrow$ )                                          | <30>   | t <sub>HSTA</sub>   |                                                      | 0.5 T - 10       |      | 0.5 T - 10       |      | ns   |
| ASTB $\downarrow \rightarrow$ $\overline{DSTB}$ $\downarrow$ delay time             | <34>   | t <sub>DSTD</sub>   |                                                      | 0.5 T - 10       |      | 0.5 T - 10       |      | ns   |
| $\overline{DSTB}$ $\uparrow \rightarrow$ ASTB $\uparrow$ delay time                 | <37>   | t <sub>DDSTH</sub>  |                                                      | 0.5 T - 10       |      | 0.5 T - 10       |      | ns   |
| $\overline{DSTB}$ width, low                                                        | <39>   | t <sub>WDL</sub>    | -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C             | (1 + n) T - 10   |      | (1 + n) T - 10   |      | ns   |
|                                                                                     |        |                     | 70°C < T <sub>A</sub> $\leq$ 85°C                    | (1 + n) T - 13   |      | (1 + n) T - 13   |      | ns   |
| ASTB width, high                                                                    | <40>   | t <sub>WSTH</sub>   |                                                      | T - 10           |      | T - 10           |      | ns   |
| WAIT setup time (vs. address)                                                       | <41>   | t <sub>SAWT1</sub>  | n $\geq$ 1, -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C | 1.5 T - 20       |      | 1.5 T - 20       |      | ns   |
|                                                                                     |        |                     | n $\geq$ 1, 70°C < T <sub>A</sub> $\leq$ 85°C        | 1.5 T - 24       |      | 1.5 T - 24       |      | ns   |
|                                                                                     | <42>   | t <sub>SAWT2</sub>  | n $\geq$ 1, -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C | (1.5 + n) T - 20 |      | (1.5 + n) T - 20 |      | ns   |
|                                                                                     |        |                     | n $\geq$ 1, 70°C < T <sub>A</sub> $\leq$ 85°C        | (1.5 + n) T - 24 |      | (1.5 + n) T - 24 |      | ns   |
| WAIT hold time (vs. address)                                                        | <43>   | t <sub>HAWT1</sub>  | n $\geq$ 1                                           | (0.5 + n) T      |      | (0.5 + n) T      |      | ns   |
|                                                                                     | <44>   | t <sub>HAWT2</sub>  | n $\geq$ 1                                           | (1.5 + n) T      |      | (1.5 + n) T      |      | ns   |
| WAIT setup time (vs. ASTB $\downarrow$ )                                            | <45>   | t <sub>SSTWT1</sub> | n $\geq$ 1, -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C | T - 18           |      | T - 18           |      | ns   |
|                                                                                     |        |                     | n $\geq$ 1, 70°C < T <sub>A</sub> $\leq$ 85°C        | T - 20           |      | T - 20           |      | ns   |
|                                                                                     | <46>   | t <sub>SSTWT2</sub> | n $\geq$ 1                                           | (1 + n) T - 15   |      | (1 + n) T - 15   |      | ns   |
| WAIT hold time (vs. ASTB $\downarrow$ )                                             | <47>   | t <sub>HSTWT1</sub> | n $\geq$ 1                                           | nT               |      | nT               |      | ns   |
|                                                                                     | <48>   | t <sub>HSTWT2</sub> | n $\geq$ 1                                           | (1 + n) T        |      | (1 + n) T        |      | ns   |
| CLKOUT $\uparrow \rightarrow$ data output delay time                                | <49>   | t <sub>DKOD</sub>   | -40°C $\leq$ T <sub>A</sub> $\leq$ +70°C             |                  | 20   |                  | 20   | ns   |
|                                                                                     |        |                     | 70°C < T <sub>A</sub> $\leq$ 85°C                    |                  | 23   |                  | 23   | ns   |
| $\overline{DSTB}$ $\downarrow \rightarrow$ data output delay time                   | <50>   | t <sub>DDOD</sub>   |                                                      |                  | 10   |                  | 10   | ns   |
| Data output hold time (vs. CLKOUT $\uparrow$ )                                      | <51>   | t <sub>HKOD</sub>   |                                                      | 0                |      | 0                |      | ns   |
| Data output setup time (vs. $\overline{DSTB}$ $\uparrow$ )                          | <52>   | t <sub>SODD</sub>   |                                                      | (1 + n) T - 15   |      | (1 + n) T - 15   |      | ns   |
| Data output hold time (vs. $\overline{DSTB}$ $\uparrow$ )                           | <53>   | t <sub>HDOD</sub>   |                                                      | T - 10           |      | T - 10           |      | ns   |

Remarks 1. T = t<sub>cyk</sub>

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait



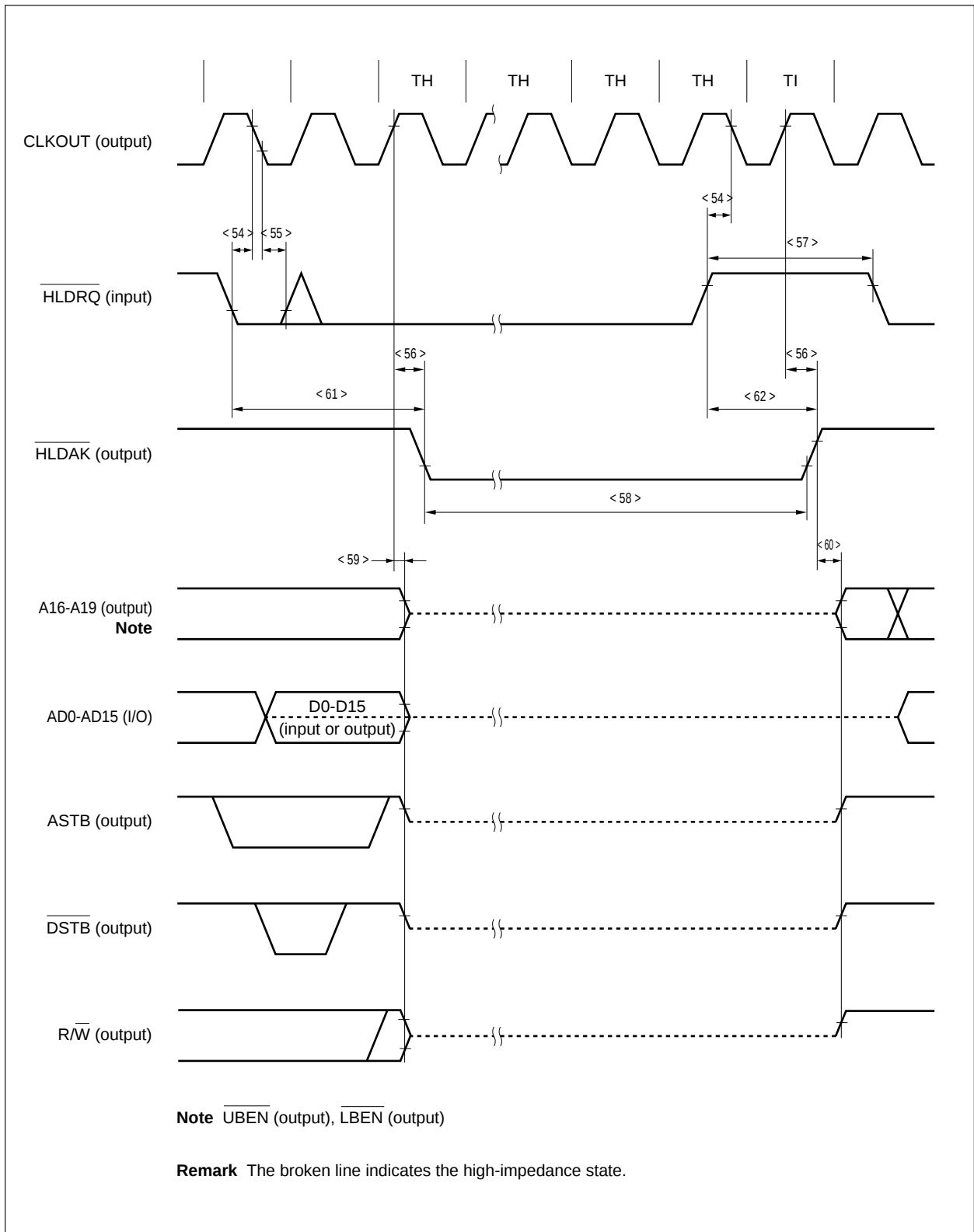
## (7) Bus hold timing (1/2)

| Parameter                                                                                              | Symbol |                     | Condition                                               | 25 MHz Model |                    | 33 MHz Model |                    | Unit |
|--------------------------------------------------------------------------------------------------------|--------|---------------------|---------------------------------------------------------|--------------|--------------------|--------------|--------------------|------|
|                                                                                                        |        |                     |                                                         | MIN.         | MAX.               | MIN.         | MAX.               |      |
| $\overline{\text{HLDRQ}}$ setup time (vs. CLKOUT $\downarrow$ )                                        | <54>   | t <sub>SHOK</sub>   |                                                         | 5            |                    | 5            |                    | ns   |
| $\overline{\text{HLDRQ}}$ hold time (vs. CLKOUT $\downarrow$ )                                         | <55>   | t <sub>HKHQ</sub>   |                                                         | 5            |                    | 5            |                    | ns   |
| CLKOUT $\uparrow \rightarrow$ $\overline{\text{HLD\!AK}}$ delay time                                   | <56>   | t <sub>DKHA</sub>   |                                                         |              | 20                 |              | 20                 | ns   |
| $\overline{\text{HLDRQ}}$ width, high                                                                  | <57>   | t <sub>WHQH</sub>   |                                                         | T + 10       |                    | T + 10       |                    | ns   |
| $\overline{\text{HLD\!AK}}$ width, low                                                                 | <58>   | t <sub>WHAL</sub>   | $-40^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ | T – 10       |                    | T – 10       |                    | ns   |
|                                                                                                        |        |                     | $70^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$      | T – 12       |                    | T – 12       |                    | ns   |
| CLKOUT $\uparrow \rightarrow$ Bus float delay time                                                     | <59>   | t <sub>DKF</sub>    |                                                         |              | 20                 |              | 20                 | ns   |
| $\overline{\text{HLD\!AK}}$ $\uparrow \rightarrow$ bus output delay time                               | <60>   | t <sub>DHAC</sub>   |                                                         | –3           |                    | –3           |                    | ns   |
| $\overline{\text{HLDRQ}}$ $\downarrow \rightarrow$ $\overline{\text{HLD\!AK}}$ $\downarrow$ delay time | <61>   | t <sub>DHQHA1</sub> |                                                         |              | (2 n + 7.5) T + 20 |              | (2 n + 7.5) T + 20 | ns   |
| $\overline{\text{HLDRQ}}$ $\uparrow \rightarrow$ $\overline{\text{HLD\!AK}}$ $\uparrow$ delay time     | <62>   | t <sub>DHQHA2</sub> |                                                         | 0.5 T        | 1.5 T + 20         | 0.5 T        | 1.5 T + 20         | ns   |

**Remarks 1.** T = t<sub>CYK</sub>

- 2.** n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

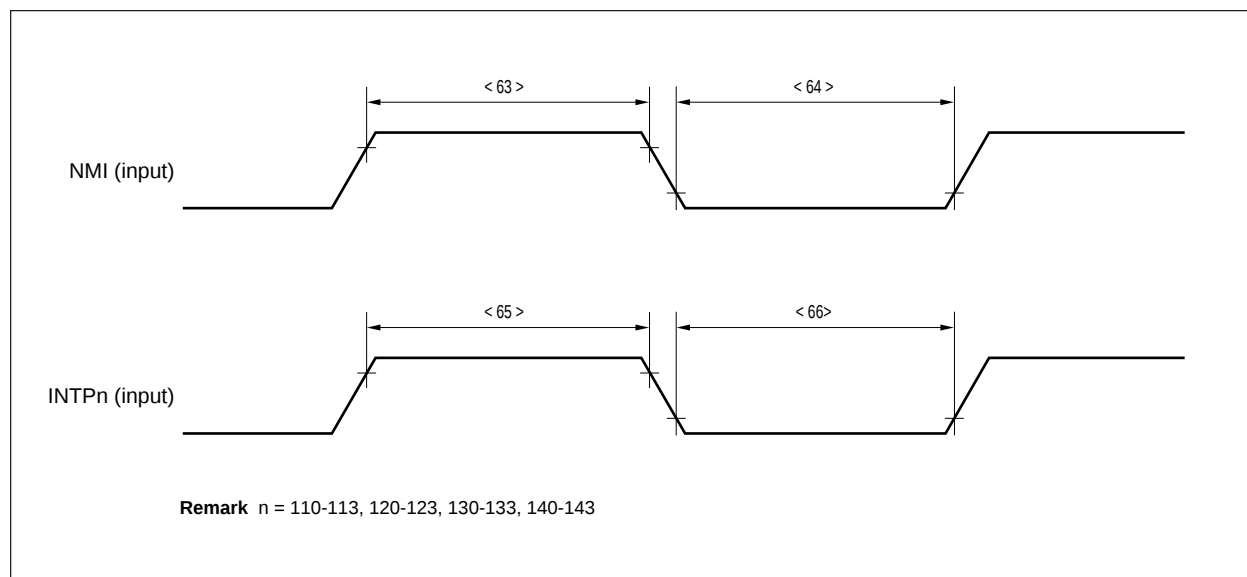
(7) Bus hold timing (2/2)



## (8) Interrupt timing

| Parameter         | Symbol |            | Condition                                       | 25 MHz Model |      | 33 MHz Model |      | Unit |
|-------------------|--------|------------|-------------------------------------------------|--------------|------|--------------|------|------|
|                   |        |            |                                                 | MIN.         | MAX. | MIN.         | MAX. |      |
| NMI width, high   | <63>   | $t_{WNIH}$ |                                                 | 500          |      | 500          |      | ns   |
| NMI width, low    | <64>   | $t_{WNIL}$ |                                                 | 500          |      | 500          |      | ns   |
| INTPn width, high | <65>   | $t_{WITH}$ | n = 110-113,<br>120-123,<br>130-133,<br>140-143 | 3 T + 10     |      | 3 T + 10     |      | ns   |
| INTPn width, low  | <66>   | $t_{WITL}$ | n = 110-113,<br>120-123,<br>130-133,<br>140-143 | 3 T + 10     |      | 3 T + 10     |      | ns   |

**Remark** T =  $t_{CYK}$



[MEMO]

## (9) CSI timing (1/2)

## (a) Master mode

## (i) CSI0-CSI2 timing

| Parameter                                                        | Symbol                   | Condition | 25 MHz Model                |      | 33 MHz Model                |      | Unit |
|------------------------------------------------------------------|--------------------------|-----------|-----------------------------|------|-----------------------------|------|------|
|                                                                  |                          |           | MIN.                        | MAX. | MIN.                        | MAX. |      |
| $\overline{\text{SCKn}}$ cycle                                   | <67> $t_{\text{CYSK1}}$  | Output    | 160                         |      | 120                         |      | ns   |
| $\overline{\text{SCKn}}$ width, high                             | <68> $t_{\text{WSKH1}}$  | Output    | $0.5 t_{\text{CYSK1}} - 20$ |      | $0.5 t_{\text{CYSK1}} - 20$ |      | ns   |
| $\overline{\text{SCKn}}$ width, low                              | <69> $t_{\text{WSKL1}}$  | Output    | $0.5 t_{\text{CYSK1}} - 20$ |      | $0.5 t_{\text{CYSK1}} - 20$ |      | ns   |
| SIn setup time (vs. $\overline{\text{SCKn}} \uparrow$ )          | <70> $t_{\text{SSISK1}}$ |           | 30                          |      | 30                          |      | ns   |
| SIn hold time (vs. $\overline{\text{SCKn}} \uparrow$ )           | <71> $t_{\text{HSKSI1}}$ |           | 0                           |      | 0                           |      | ns   |
| SOn output delay time (vs. $\overline{\text{SCKn}} \downarrow$ ) | <72> $t_{\text{DSKSO1}}$ |           |                             | 18   |                             | 18   | ns   |
| SOn output hold time (vs. $\overline{\text{SCKn}} \uparrow$ )    | <73> $t_{\text{HSKSO1}}$ |           | $0.5 t_{\text{CYSK1}} - 5$  |      | $0.5 t_{\text{CYSK1}} - 5$  |      | ns   |

**Remark** n = 0-2

## (ii) CSI3 timing

| Parameter                                                        | Symbol                   | Condition                               | 25 MHz Model                |      | 33 MHz Model                |      | Unit |
|------------------------------------------------------------------|--------------------------|-----------------------------------------|-----------------------------|------|-----------------------------|------|------|
|                                                                  |                          |                                         | MIN.                        | MAX. | MIN.                        | MAX. |      |
| $\overline{\text{SCK3}}$ cycle                                   | <67> $t_{\text{CYSK3}}$  | Output $R_L = 1.5$<br>k $\Omega$        | 500                         |      | 500                         |      | ns   |
| $\overline{\text{SCK3}}$ width, high                             | <68> $t_{\text{WSKH3}}$  | Output $C_L = 50$<br>pF                 | $0.5 t_{\text{CYSK3}} - 70$ |      | $0.5 t_{\text{CYSK3}} - 70$ |      | ns   |
| $\overline{\text{SCK3}}$ width, low                              | <69> $t_{\text{WSKL3}}$  | Output                                  | $0.5 t_{\text{CYSK3}} - 70$ |      | $0.5 t_{\text{CYSK3}} - 70$ |      | ns   |
| SI3 setup time (vs. $\overline{\text{SCK3}} \uparrow$ )          | <70> $t_{\text{SSISK3}}$ |                                         | 100                         |      | 100                         |      | ns   |
| SI3 hold time (vs. $\overline{\text{SCK3}} \uparrow$ )           | <71> $t_{\text{HSKSI3}}$ |                                         | 50                          |      | 50                          |      | ns   |
| SO3 output delay time (vs. $\overline{\text{SCK3}} \downarrow$ ) | <72> $t_{\text{DSKSO3}}$ | $R_L = 1.5$ K $\Omega$<br>$C_L = 50$ pF |                             | 150  |                             | 150  | ns   |
| SO3 output hold time (vs. $\overline{\text{SCK3}} \uparrow$ )    | <73> $t_{\text{HSKSO3}}$ |                                         | $0.5 t_{\text{CYSK3}} - 5$  |      | $0.5 t_{\text{CYSK3}} - 5$  |      | ns   |

**Remark**  $R_L$  and  $C_L$  are the load resistance and load capacitance respectively of the  $\overline{\text{SCK3}}$  and SO3 output lines.

## (b) Slave mode

## (i) CSI0-CSI2 timing

| Parameter                                                        | Symbol                   | Condition | 25 MHz Model       |      | 33 MHz Model       |      | Unit |
|------------------------------------------------------------------|--------------------------|-----------|--------------------|------|--------------------|------|------|
|                                                                  |                          |           | MIN.               | MAX. | MIN.               | MAX. |      |
| $\overline{\text{SCKn}}$ cycle                                   | <67> $t_{\text{CYSK2}}$  | Input     | 160                |      | 120                |      | ns   |
| $\overline{\text{SCKn}}$ width, high                             | <68> $t_{\text{WSKH2}}$  | Input     | 50                 |      | 30                 |      | ns   |
| $\overline{\text{SCKn}}$ width, low                              | <69> $t_{\text{WSKL2}}$  | Input     | 50                 |      | 30                 |      | ns   |
| SIn setup time (vs. $\overline{\text{SCKn}} \uparrow$ )          | <70> $t_{\text{SSISK2}}$ |           | 10                 |      | 10                 |      | ns   |
| SIn hold time (vs. $\overline{\text{SCKn}} \uparrow$ )           | <71> $t_{\text{HSKSI2}}$ |           | 10                 |      | 10                 |      | ns   |
| SOn output delay time (vs. $\overline{\text{SCKn}} \downarrow$ ) | <72> $t_{\text{DSKSO2}}$ |           |                    | 30   |                    | 30   | ns   |
| SOn output hold time (vs. $\overline{\text{SCKn}} \uparrow$ )    | <73> $t_{\text{HSKSO2}}$ |           | $t_{\text{WSKH2}}$ |      | $t_{\text{WSKH2}}$ |      | ns   |

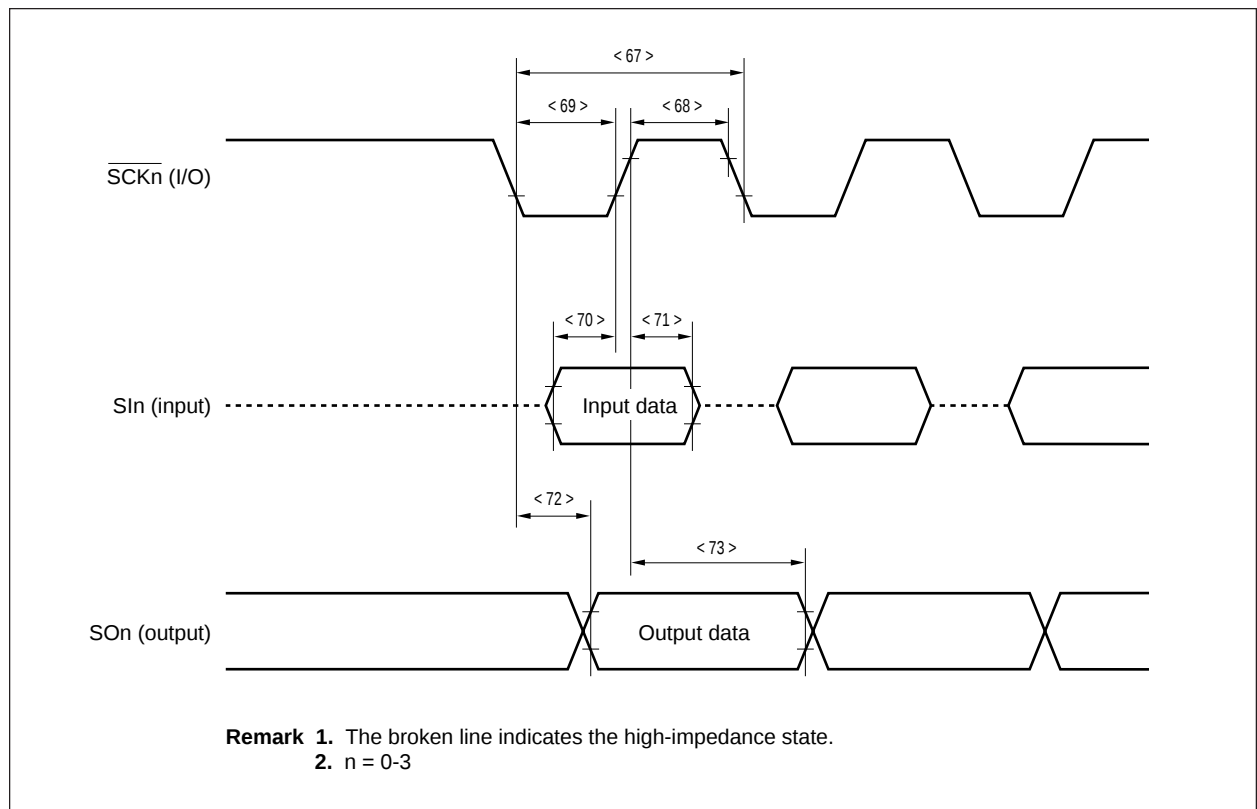
**Remark** n = 0-2

## (9) CSI timing (2/2)

## (ii) CSI3 timing

| Parameter                                                          | Symbol |                     | Condition                   | 25 MHz Model       |      | 33 MHz Model       |      | Unit |
|--------------------------------------------------------------------|--------|---------------------|-----------------------------|--------------------|------|--------------------|------|------|
|                                                                    |        |                     |                             | MIN.               | MAX. | MIN.               | MAX. |      |
| $\overline{\text{SCK3}}$ cycle                                     | <67>   | $t_{\text{CYSK4}}$  | Input                       | 500                |      | 500                |      | ns   |
| $\overline{\text{SCK3}}$ width, high                               | <68>   | $t_{\text{WSKH4}}$  | Input                       | 180                |      | 180                |      | ns   |
| $\overline{\text{SCK3}}$ width, low                                | <69>   | $t_{\text{WSKL4}}$  | Input                       | 180                |      | 180                |      | ns   |
| SI3 setup time (vs. $\overline{\text{SCK3}}$ $\uparrow$ )          | <70>   | $t_{\text{SSISK4}}$ |                             | 100                |      | 100                |      | ns   |
| SI3 hold time (vs. $\overline{\text{SCK3}}$ $\uparrow$ )           | <71>   | $t_{\text{HSKSI4}}$ |                             | 50                 |      | 50                 |      | ns   |
| SO3 output delay time (vs. $\overline{\text{SCK3}}$ $\downarrow$ ) | <72>   | $t_{\text{DSKSO4}}$ | $R_L = 1.5 \text{ k}\Omega$ |                    | 150  |                    | 150  | ns   |
| SO3 output hold time (vs. $\overline{\text{SCK3}}$ $\uparrow$ )    | <73>   | $t_{\text{HSKSO4}}$ | $C_L = 50 \text{ pF}$       | $t_{\text{WSKH4}}$ |      | $t_{\text{WSKH4}}$ |      | ns   |

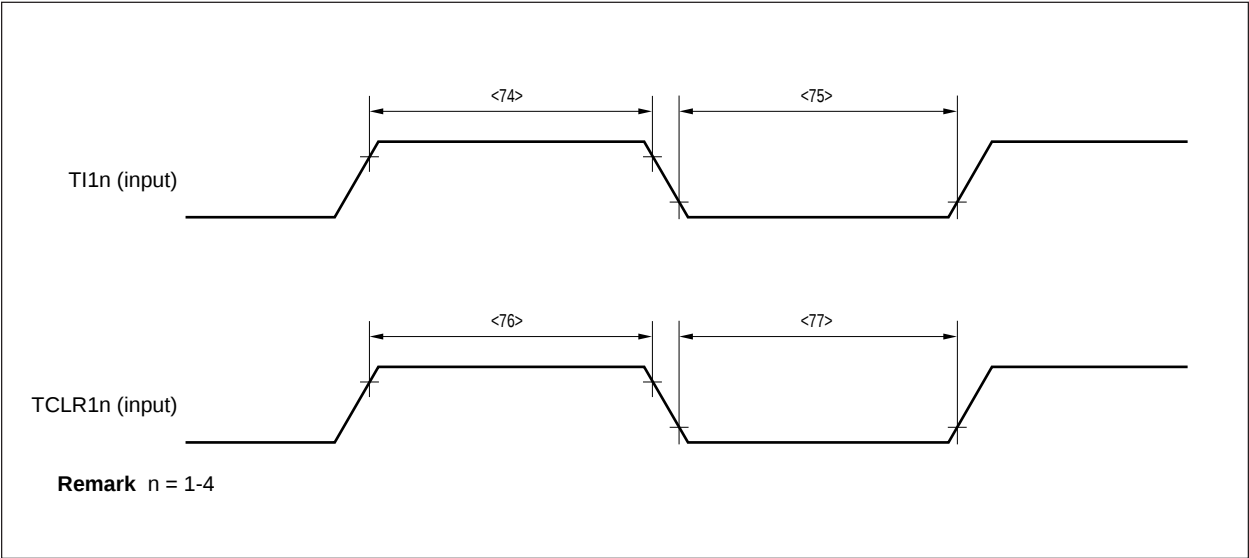
**Remark**  $R_L$  and  $C_L$  are the load resistance and load capacitance respectively of the  $\overline{\text{SCK3}}$  and SO3 output lines.



(10) RPU timing

| Parameter          | Symbol |                   | Condition | 25 MHz Model |      | 33 MHz Model |      | Unit |
|--------------------|--------|-------------------|-----------|--------------|------|--------------|------|------|
|                    |        |                   |           | MIN.         | MAX. | MIN.         | MAX. |      |
| TI1n width, high   | <74>   | t <sub>WTIH</sub> |           | 3 T + 10     |      | 3 T + 10     |      | ns   |
| TI1n width, low    | <75>   | t <sub>WTIL</sub> |           | 3 T + 10     |      | 3 T + 10     |      | ns   |
| TCLR1n width, high | <76>   | t <sub>WTCH</sub> |           | 3 T + 10     |      | 3 T + 10     |      | ns   |
| TCLR1n width, low  | <77>   | t <sub>WTCL</sub> |           | 3 T + 10     |      | 3 T + 10     |      | ns   |

Remark T = t<sub>CYK</sub>



**A/D Converter Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = V_{SS} = 0\text{ V}$ )**

| Parameter                              | Symbol      | Conditions                                 | 25 MHz Model |           |                 | 33 MHz Model |           |                 | Unit      |
|----------------------------------------|-------------|--------------------------------------------|--------------|-----------|-----------------|--------------|-----------|-----------------|-----------|
|                                        |             |                                            | MIN.         | TYP.      | MAX.            | MIN.         | TYP.      | MAX.            |           |
| Resolution                             | —           |                                            | 10           | 10        | 10              | 10           | 10        | 10              | bit       |
| Overall error <sup>Note 1</sup>        | —           | $4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ |              |           | $\pm 0.4$       |              |           | $\pm 0.4$       | %FSR      |
|                                        | —           | $3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ |              |           | $\pm 0.7$       |              |           | $\pm 0.7$       | %FSR      |
| Quantize error                         | —           |                                            |              |           | $\pm 1/2$       |              |           | $\pm 1/2$       | LSB       |
| Conversion time                        | $t_{CONV}$  | $4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ | 48           |           |                 | 60           |           |                 | $t_{CYK}$ |
|                                        |             | $3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ | 48           |           |                 | 60           |           |                 | $t_{CYK}$ |
| Sampling time                          | $t_{SAMP}$  | $4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ | 8            |           |                 | 10           |           |                 | $t_{CYK}$ |
|                                        |             | $3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ | 8            |           |                 | 10           |           |                 | $t_{CYK}$ |
| Zero-scale error <sup>Note 1</sup>     | —           | $4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ |              | $\pm 1.5$ | $\pm 3.5$       |              | $\pm 1.5$ | $\pm 3.5$       | LSB       |
|                                        | —           | $3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ |              | $\pm 1.5$ | $\pm 4.5$       |              | $\pm 1.5$ | $\pm 4.5$       | LSB       |
| Full-scale error <sup>Note 1</sup>     | —           | $4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ |              | $\pm 1.5$ | $\pm 2.5$       |              | $\pm 1.5$ | $\pm 2.5$       | LSB       |
|                                        | —           | $3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ |              | $\pm 1.5$ | $\pm 4.5$       |              | $\pm 1.5$ | $\pm 4.5$       | LSB       |
| Non-linear error <sup>Note 1</sup>     | —           | $4.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ |              | $\pm 1.5$ | $\pm 2.5$       |              | $\pm 1.5$ | $\pm 2.5$       | LSB       |
|                                        | —           | $3.5\text{ V} \leq AV_{REF1} \leq AV_{DD}$ |              | $\pm 1.5$ | $\pm 4.5$       |              | $\pm 1.5$ | $\pm 4.5$       | LSB       |
| Analog input voltage <sup>Note 2</sup> | $V_{IAN}$   |                                            | $-0.3$       |           | $AV_{DD} + 0.3$ | $-0.3$       |           | $AV_{DD} + 0.3$ | V         |
| Reference voltage                      | $AV_{REF1}$ |                                            | 3.5          |           | $AV_{DD}$       | 3.5          |           | $AV_{DD}$       | V         |
| $AV_{REF1}$ current                    | $AI_{REF1}$ |                                            |              | 1.2       | 3.0             |              | 1.2       | 3.0             | mA        |
| $AV_{DD}$ supply current               | $AI_{DD}$   |                                            |              | 2.3       | 6.0             |              | 2.3       | 6.0             | mA        |

**Notes** 1. Except quantize error2. The conversion result is 000H when  $V_{IAN} = 0$ .Converted with 10-bit resolution when  $0 < V_{IAN} < AV_{REF1}$ .The conversion result is 3FFH when  $AV_{REF1} \leq V_{IAN} \leq AV_{DD}$ .

D/A Converter Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                              | Symbol      | Conditions                                                                             | 25 MHz Model  |      |               | 33 MHz Model  |      |               | Unit |
|----------------------------------------|-------------|----------------------------------------------------------------------------------------|---------------|------|---------------|---------------|------|---------------|------|
|                                        |             |                                                                                        | MIN.          | TYP. | MAX.          | MIN.          | TYP. | MAX.          |      |
| Resolution                             | —           |                                                                                        | 8             | 8    | 8             | 8             | 8    | 8             | bit  |
| Overall error                          | —           | Load conditions: 2 MΩ, 30 pF<br>$AV_{REF2} = V_{DD}$<br>$AV_{REF3} = 0$                |               |      | 0.8           |               |      | 0.8           | %    |
|                                        | —           | Load conditions: 2 MΩ, 30 pF<br>$AV_{REF2} = 0.75 V_{DD}$<br>$AV_{REF3} = 0.25 V_{DD}$ |               |      | 1.0           |               |      | 1.0           | %    |
|                                        | —           | Load conditions: 4 MΩ, 30 pF<br>$AV_{REF2} = V_{DD}$<br>$AV_{REF3} = 0$                |               |      | 0.6           |               |      | 0.6           | %    |
|                                        | —           | Load conditions: 4 MΩ, 30 pF<br>$AV_{REF2} = 0.75 V_{DD}$<br>$AV_{REF3} = 0.25 V_{DD}$ |               |      | 0.8           |               |      | 0.8           | %    |
| Settling time                          | —           | Load conditions: 2 MΩ, 30 pF                                                           |               |      | 10            |               |      | 10            | μs   |
| Output resistance                      | RO          |                                                                                        |               | 8    |               |               | 8    |               | kΩ   |
| $AV_{REF2}$ input voltage              | $AV_{REF2}$ |                                                                                        | $0.75 V_{DD}$ |      | $V_{DD}$      | $0.75 V_{DD}$ |      | $V_{DD}$      | V    |
| $AV_{REF3}$ input voltage              | $AV_{REF3}$ |                                                                                        | 0             |      | $0.25 V_{DD}$ | 0             |      | $0.25 V_{DD}$ | V    |
| $AV_{REF2}-AV_{REF3}$ resistance value | $R_{AIREF}$ | DACS0, DACS1 = 55H                                                                     | 2             | 4    |               | 2             | 4    |               | kΩ   |

### 3.2 Flash Memory Programming Mode

★ **Basic Characteristics** ( $T_A = 10$  to  $40^\circ\text{C}$  (when rewiring),  $T_A = -40$  to  $+85^\circ\text{C}$  (when not rewriting))

| Parameter                         | Symbol    | Conditions                          | MIN.         | TYP. | MAX.                   | Unit  |
|-----------------------------------|-----------|-------------------------------------|--------------|------|------------------------|-------|
| Operating frequency               | $f_x$     |                                     | 10           |      | 33                     | MHz   |
| Supply voltage                    | $V_{DD}$  |                                     | 4.5          |      | 5.5                    | V     |
|                                   | $V_{PPL}$ | $V_{PP}$ low level detection        | -0.5         |      | $0.2 V_{DD}$           | V     |
|                                   | $V_{PPM}$ | $V_{PP}$ , $V_{DD}$ level detection | $0.8 V_{DD}$ |      | $1.2 V_{DD}$           | V     |
|                                   | $V_{PPH}$ | $V_{PP}$ high voltage detection     | 9.7          | 10.3 | 10.6                   | V     |
| $V_{DD}$ supply current           | $I_{DO}$  |                                     |              |      | $3.0 \times \phi + 25$ | mA    |
| $V_{PP}$ supply current           | $I_{PP}$  | $V_{PP} = 10.3$ V                   |              |      | 200                    | mA    |
| Number of rewrite <sup>Note</sup> | $C_{WRT}$ |                                     | 20           |      |                        | times |

**Note** Operation is not guaranteed when rewrite is performed more than 20 times.

**Cautions** 1.  $V_{PP}$  pull-down resistance value ( $R_{VPP}$ ) is recommended to be in the range 5 k $\Omega$  to 15 k $\Omega$ .

2. Set the transfer rate between programmer and device as follows.

CSIO : 0.2 to 1 MHz

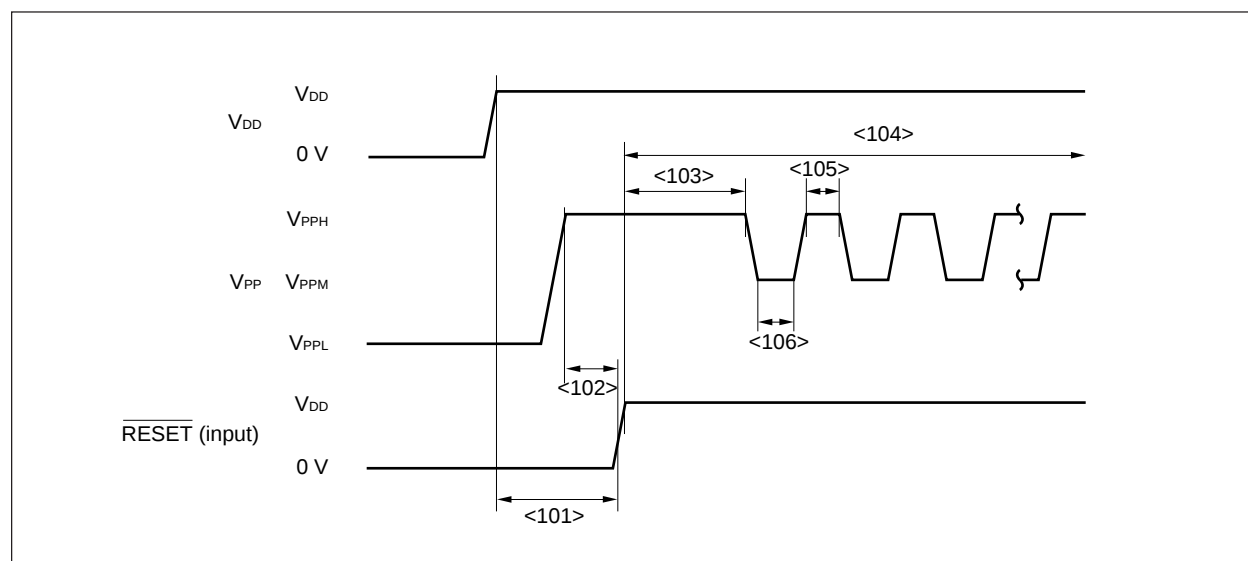
UART0: 4800 to 76800 bps

**Remark**  $\phi$ : Internal system clock frequency

## Serial Write Operation Characteristics

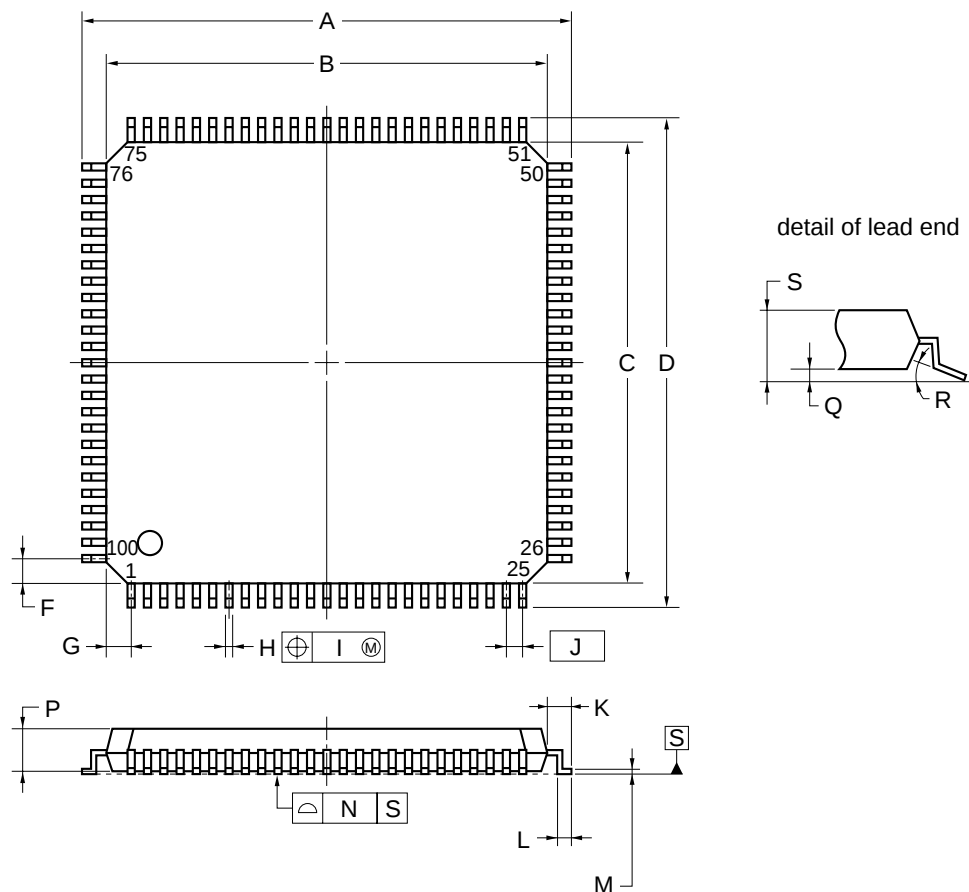
| Parameter                                                                 | Symbol                   | Conditions | MIN.       | TYP. | MAX. | Unit          |
|---------------------------------------------------------------------------|--------------------------|------------|------------|------|------|---------------|
| $V_{DD} \uparrow \rightarrow \overline{\text{RESET}} \uparrow$ setup time | <101> $t_{\text{DRRR}}$  |            | 10         |      |      | ms            |
| $V_{PP} \uparrow \rightarrow \overline{\text{RESET}} \uparrow$ setup time | <102> $t_{\text{PSRR}}$  |            | 1.0        |      |      | $\mu\text{s}$ |
| $\overline{\text{RESET}} \uparrow \rightarrow V_{PP}$ count start time    | <103> $t_{\text{RRCF}}$  |            | $5T + 500$ |      |      | ns            |
| Count end time                                                            | <104> $t_{\text{COUNT}}$ |            |            |      | 10   | ms            |
| $V_{PP}$ counter width, high                                              | <105> $t_{\text{CH}}$    |            | 1.0        |      |      | $\mu\text{s}$ |
| $V_{PP}$ counter width, low                                               | <106> $t_{\text{CL}}$    |            | 1.0        |      |      | $\mu\text{s}$ |

**Remark**  $T = t_{\text{CYK}}$



★ 4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



**NOTE**

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            |
|------|----------------------------------------|
| A    | 16.00±0.20                             |
| B    | 14.00±0.20                             |
| C    | 14.00±0.20                             |
| D    | 16.00±0.20                             |
| F    | 1.00                                   |
| G    | 1.00                                   |
| H    | 0.22 <sup>+0.05</sup> <sub>-0.04</sub> |
| I    | 0.08                                   |
| J    | 0.50 (T.P.)                            |
| K    | 1.00±0.20                              |
| L    | 0.50±0.20                              |
| M    | 0.17 <sup>+0.03</sup> <sub>-0.07</sub> |
| N    | 0.08                                   |
| P    | 1.40±0.05                              |
| Q    | 0.10±0.05                              |
| R    | 3° <sup>+7°</sup> <sub>-3°</sub>       |
| S    | 1.60 MAX.                              |

S100GC-50-8EU, 8EA-2

## 5. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

**Table 5-1. Soldering Conditions**

$\mu$ PD70F3003AGC-25-8EU : 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

$\mu$ PD70F3003AGC-33-8EU : 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

$\mu$ PD70F3025AGC-25-8EU : 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

$\mu$ PD70F3025AGC-33-8EU : 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

| Soldering Method | Soldering Condition                                                                                                                                                                         | Symbol of Recommended Soldering Condition |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| Infrared reflow  | Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 3 max., Number of days: 3 <sup>Note</sup> (after that, prebaking is necessary at 125°C for 10 hours.) | IR35-103-3                                |
| VPS              | Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 3 max., Number of days: 3 <sup>Note</sup> (after that, prebaking is necessary at 125°C for 10 hours.) | VP15-103-3                                |
| Partial heating  | Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)                                                                                                                      | —                                         |

**Note** The number of days for storage at 25°C, 65% RH MAX after the dry pack has been opened.

**Caution** Do not use two or more soldering methods in combination (except partial heating method).

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## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V<sub>DD</sub> or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Related document** : μPD703003 Data Sheet (U12261E)  
 μPD703003A, 703004A, 703025A Data Sheet (U13188E)  
 μPD70F3003 Data Sheet (U12036E)

**Reference document:** Concept of Electrical Characteristics - Microcomputers (IEI-601) (Japanese version)

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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