DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD16732A, 16732B

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD16732A, 16732B are a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.1 V to V_{DD2} – 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 65 MHz when driving at 3.0 V, 45 MHz when driving at 2.3 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels by input display signal 2 systems (Clock divide).

FEATURES

- CMOS level input (2.3 V to 3.6 V)
- 384 Outputs
- Input of 6 bits (gradation data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter (R-DAC)
- High-speed data transfer: $f_{MAX.}$ = 65 MHz (internal data transfer speed when operating at V_{DD1} = 3.0 V)
- Output dynamic range V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output Voltage polarity inversion function (POL)
- Display data inversion function (POL2)
- Low power control function (LPC)
- Logic power supply voltage (V_{DD1}) : 2.3 V to 3.6 V
- Driver power supply voltage (V_{DD2}) : 8.5 ± 0.5 V
- Different point between μPD16732A, 16732B : The ladder resistors value(Refer to **5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE**)

ORDERING INFORMATION

Part Number	Package
μPD16732AN-×××	TCP (TAB package)
μPD16732BN-×××	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact an NEC salesperson.

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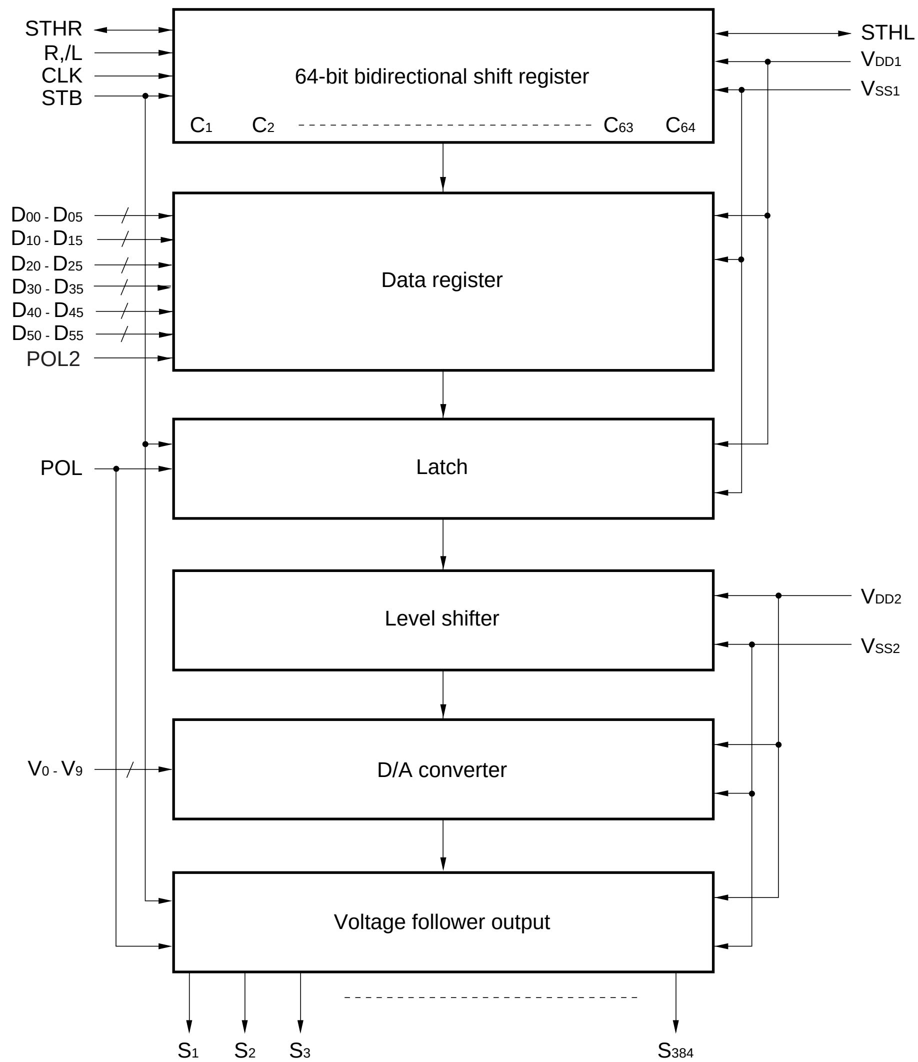
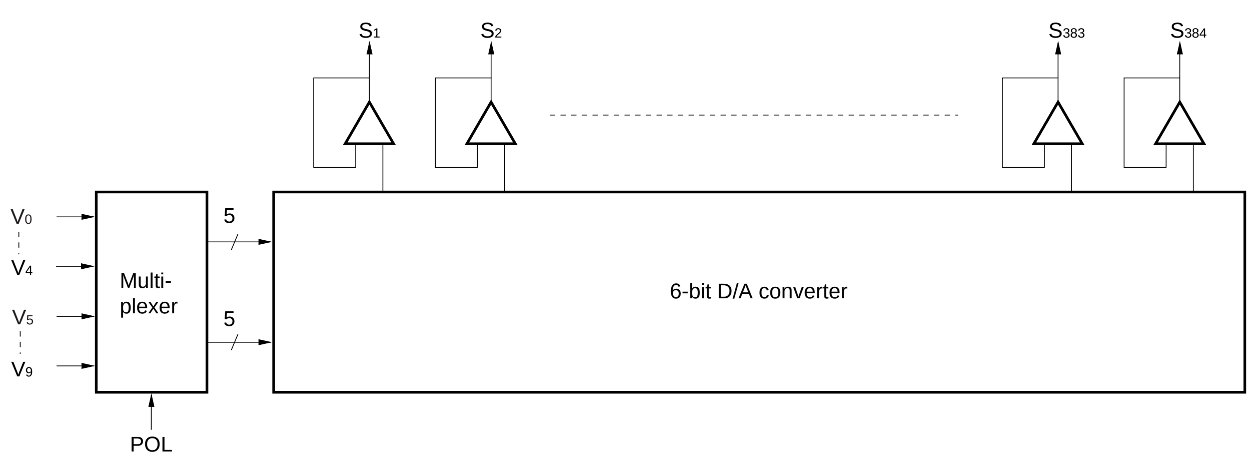
The mark ★ shows major revised points.

1. BLOCK DIAGRAM

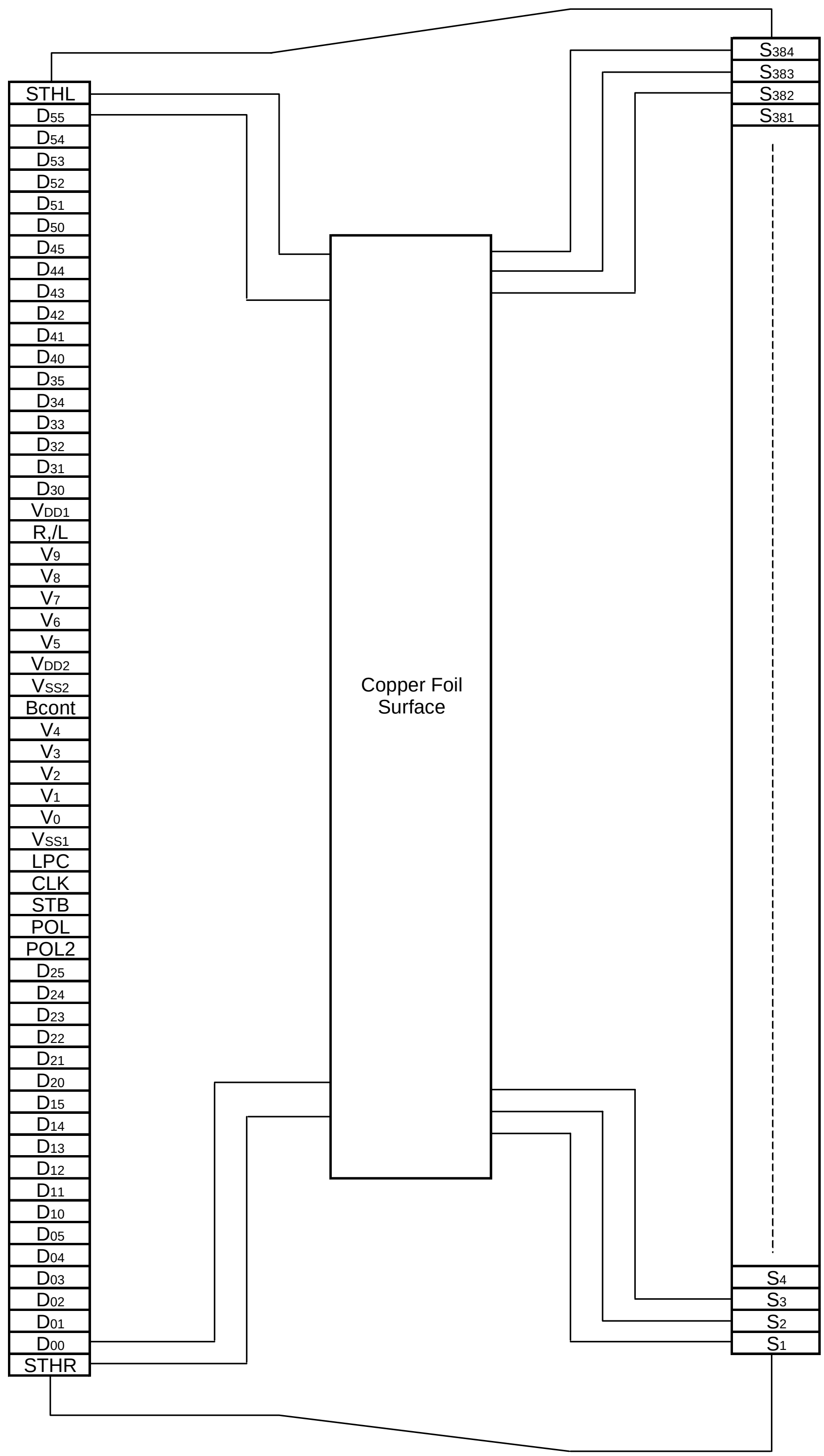


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16732AN-xxx, μPD16732BN-xxx : TCP (TAB package))



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	Description
S_1 to S_{384}	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05} D_{10} to D_{15} D_{20} to D_{25} D_{30} to D_{35} D_{40} to D_{45} D_{50} to D_{55}	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H : STHR input, $S_1 \rightarrow S_{384}$, STHL output R,/L = L : STHL input, $S_{384} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H : Becomes the start pulse output pin. R,/L = L : Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L : The S_{2n-1} output uses V_0 to V_4 as the reference supply. The S_{2n} output uses V_5 to V_9 as the reference supply. POL = H: The S_{2n-1} output uses V_5 to V_9 as the reference supply. The S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL\text{-}STB}$) with respect to STB's rising edge.
POL2	Data inversion	POL2 = H : Display data is inverted. POL2 = L : Display data is not inverted
★ LPC	Low power control input	The current consumption is lowered by controlling the constant current source of the output amplifier. In low power mode (LPC = "L"), the V_{DD2} of static current consumption can be reduced to two thirds of the normal current consumption. This pin is pulled up to the V_{DD1} power supply inside the IC. LPC = H or Open : Normal power mode LPC = L : Low power mode

(2/2)

Pin Symbol	Pin Name	Description
Bcont	Bias control	This pin can be used to finely control the bias current inside the output amplifier. In cases when fine-control is necessary, connect this pin to the stabilized ground potential (V_{SS2}) via an external resistor of 10 to 100kΩ (per IC). When this fine-control function is not required, leave this pin open. Refer to **9. CURRENT CONSUMPTION REDUCTION FUNCTION**
V_0 to V_9	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\ V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\ V$
V_{DD1}	Logic power supply	2.3 V to 3.6 V
V_{DD2}	Driver power supply	8.5 V ± 0.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2, ⋯, V_9) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ -compensated voltages to V_0' to V_{63}' and V_0'' to V_{63}'' is almost equivalent. For the 2 sets of five γ-compensated power supplies, V_0 to V_4 and V_5 to V_9, respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the γ -compensated power supplies V_1 to V_3 and V_6 to V_8.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of V_{DD2} – 0.1 V> V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1 V.

Figures 5–2 and 5–3 show the relationship between the input data and the output data. This driver IC is designed for only single-sided mounting. Therefore, please do not use it for γ-corrected power supply level inversion in double-sided mounting.

Figure 5–1. Relationship between Input Data and γ- corrected Power Supply

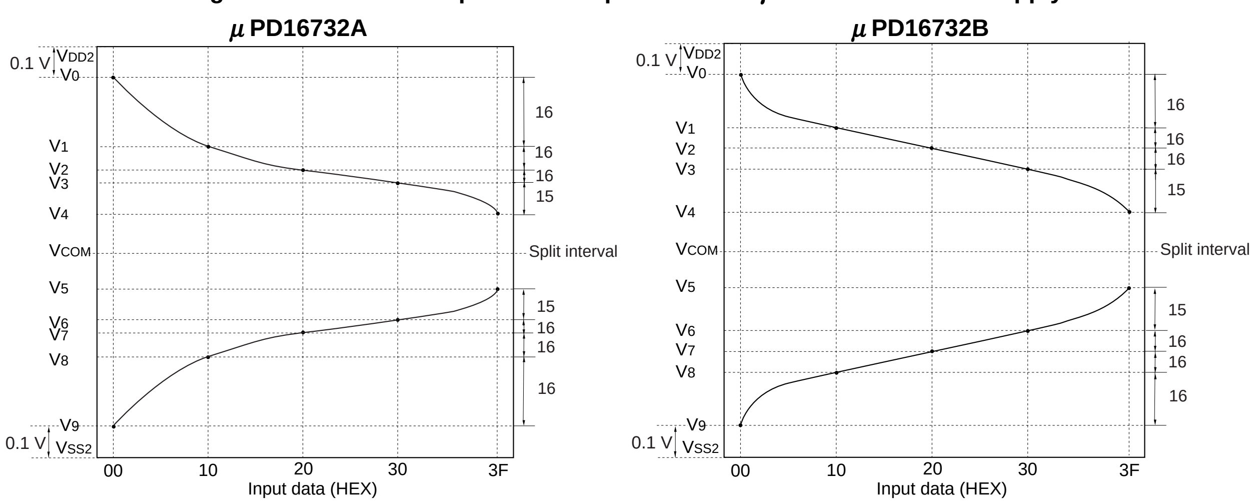
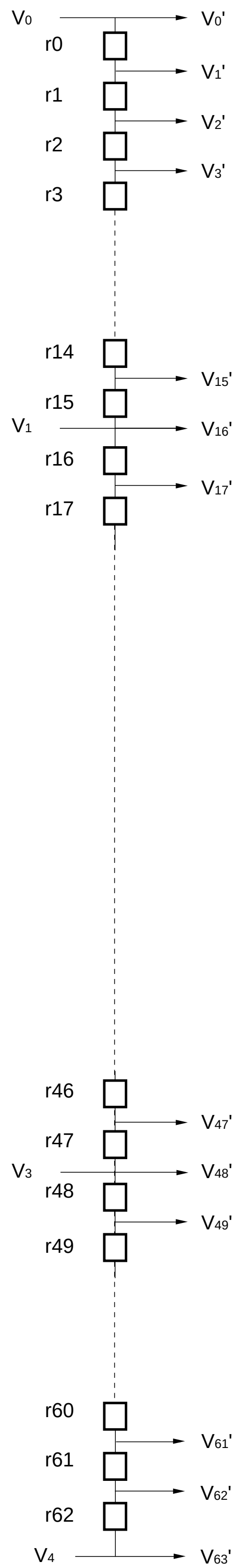


Figure 5–2. Relationship between Input Data and Output Voltage (1/2)

V_{DD2} – 0.1 V> V_0 > V_1 > V_2 > V_3 > V_4 > V_5, POL2 = L



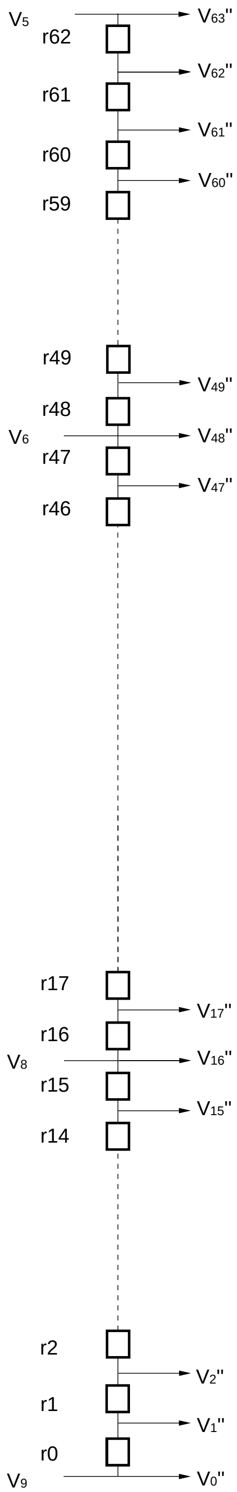
Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage		732A	732B
00H	0	0	0	0	0	0	V_0'	V_0		
01H	0	0	0	0	0	1	V_1'	$V_1+(V_0-V_1)\times$	7250/8050	4585/6351
02H	0	0	0	0	1	0	V_2'	$V_1+(V_0-V_1)\times$	6500/8050	3849/6351
03H	0	0	0	0	1	1	V_3'	$V_1+(V_0-V_1)\times$	5800/8050	3283/6351
04H	0	0	0	1	0	0	V_4'	$V_1+(V_0-V_1)\times$	5150/8050	2774/6351
05H	0	0	0	1	0	1	V_5'	$V_1+(V_0-V_1)\times$	4550/8050	2378/6351
06H	0	0	0	1	1	0	V_6'	$V_1+(V_0-V_1)\times$	4000/8050	2038/6351
07H	0	0	0	1	1	1	V_7'	$V_1+(V_0-V_1)\times$	3450/8050	1755/6351
08H	0	0	1	0	0	0	V_8'	$V_1+(V_0-V_1)\times$	2950/8050	1472/6351
09H	0	0	1	0	0	1	V_9'	$V_1+(V_0-V_1)\times$	2450/8050	1246/6351
0AH	0	0	1	0	1	0	V_{10}'	$V_1+(V_0-V_1)\times$	2050/8050	1020/6351
0BH	0	0	1	0	1	1	V_{11}'	$V_1+(V_0-V_1)\times$	1650/8050	850/6351
0CH	0	0	1	1	0	0	V_{12}'	$V_1+(V_0-V_1)\times$	1300/8050	680/6351
0DH	0	0	1	1	0	1	V_{13}'	$V_1+(V_0-V_1)\times$	950/8050	510/6351
0EH	0	0	1	1	1	0	V_{14}'	$V_1+(V_0-V_1)\times$	600/8050	340/6351
0FH	0	0	1	1	1	1	V_{15}'	$V_1+(V_0-V_1)\times$	300/8050	170/6351
10H	0	1	0	0	0	0	V_{16}'	V_1		
11H	0	1	0	0	0	1	V_{17}'	$V_2+(V_1-V_2)\times$	2450/2750	2280/2432
12H	0	1	0	0	1	0	V_{18}'	$V_2+(V_1-V_2)\times$	2200/2750	2128/2432
13H	0	1	0	0	1	1	V_{19}'	$V_2+(V_1-V_2)\times$	1950/2750	1976/2432
14H	0	1	0	1	0	0	V_{20}'	$V_2+(V_1-V_2)\times$	1700/2750	1824/2432
15H	0	1	0	1	0	1	V_{21}'	$V_2+(V_1-V_2)\times$	1500/2750	1672/2432
16H	0	1	0	1	1	0	V_{22}'	$V_2+(V_1-V_2)\times$	1300/2750	1520/2432
17H	0	1	0	1	1	1	V_{23}'	$V_2+(V_1-V_2)\times$	1100/2750	1368/2432
18H	0	1	1	0	0	0	V_{24}'	$V_2+(V_1-V_2)\times$	950/2750	1216/2432
19H	0	1	1	0	0	1	V_{25}'	$V_2+(V_1-V_2)\times$	800/2750	1064/2432
1AH	0	1	1	0	1	0	V_{26}'	$V_2+(V_1-V_2)\times$	650/2750	912/2432
1BH	0	1	1	0	1	1	V_{27}'	$V_2+(V_1-V_2)\times$	500/2750	760/2432
1CH	0	1	1	1	0	0	V_{28}'	$V_2+(V_1-V_2)\times$	400/2750	608/2432
1DH	0	1	1	1	0	1	V_{29}'	$V_2+(V_1-V_2)\times$	300/2750	456/2432
1EH	0	1	1	1	1	0	V_{30}'	$V_2+(V_1-V_2)\times$	200/2750	304/2432
1FH	0	1	1	1	1	1	V_{31}'	$V_2+(V_1-V_2)\times$	100/2750	152/2432
20H	1	0	0	0	0	0	V_{32}'	V_2		
21H	1	0	0	0	0	1	V_{33}'	$V_3+(V_2-V_3)\times$	1500/1600	2340/2496
22H	1	0	0	0	1	0	V_{34}'	$V_3+(V_2-V_3)\times$	1400/1600	2184/2496
23H	1	0	0	0	1	1	V_{35}'	$V_3+(V_2-V_3)\times$	1300/1600	2028/2496
24H	1	0	0	1	0	0	V_{36}'	$V_3+(V_2-V_3)\times$	1200/1600	1872/2496
25H	1	0	0	1	0	1	V_{37}'	$V_3+(V_2-V_3)\times$	1100/1600	1716/2496
26H	1	0	0	1	1	0	V_{38}'	$V_3+(V_2-V_3)\times$	1000/1600	1560/2496
27H	1	0	0	1	1	1	V_{39}'	$V_3+(V_2-V_3)\times$	900/1600	1404/2496
28H	1	0	1	0	0	0	V_{40}'	$V_3+(V_2-V_3)\times$	800/1600	1248/2496
29H	1	0	1	0	0	1	V_{41}'	$V_3+(V_2-V_3)\times$	700/1600	1092/2496
2AH	1	0	1	0	1	0	V_{42}'	$V_3+(V_2-V_3)\times$	600/1600	936/2496
2BH	1	0	1	0	1	1	V_{43}'	$V_3+(V_2-V_3)\times$	500/1600	780/2496
2CH	1	0	1	1	0	0	V_{44}'	$V_3+(V_2-V_3)\times$	400/1600	624/2496
2DH	1	0	1	1	0	1	V_{45}'	$V_3+(V_2-V_3)\times$	300/1600	468/2496
2EH	1	0	1	1	1	0	V_{46}'	$V_3+(V_2-V_3)\times$	200/1600	312/2496
2FH	1	0	1	1	1	1	V_{47}'	$V_3+(V_2-V_3)\times$	100/1600	156/2496
30H	1	1	0	0	0	0	V_{48}'	V_3		
31H	1	1	0	0	0	1	V_{49}'	$V_4+(V_3-V_4)\times$	3350/3450	4397/4572
32H	1	1	0	0	1	0	V_{50}'	$V_4+(V_3-V_4)\times$	3250/3450	4222/4572
33H	1	1	0	0	1	1	V_{51}'	$V_4+(V_3-V_4)\times$	3150/3450	4047/4572
34H	1	1	0	1	0	0	V_{52}'	$V_4+(V_3-V_4)\times$	3050/3450	3872/4572
35H	1	1	0	1	0	1	V_{53}'	$V_4+(V_3-V_4)\times$	2950/3450	3697/4572
36H	1	1	0	1	1	0	V_{54}'	$V_4+(V_3-V_4)\times$	2800/3450	3465/4572
37H	1	1	0	1	1	1	V_{55}'	$V_4+(V_3-V_4)\times$	2650/3450	3233/4572
38H	1	1	1	0	0	0	V_{56}'	$V_4+(V_3-V_4)\times$	2500/3450	3001/4572
39H	1	1	1	0	0	1	V_{57}'	$V_4+(V_3-V_4)\times$	2300/3450	2769/4572
3AH	1	1	1	0	1	0	V_{58}'	$V_4+(V_3-V_4)\times$	2100/3450	2480/4572
3BH	1	1	1	0	1	1	V_{59}'	$V_4+(V_3-V_4)\times$	1850/3450	2135/4572
3CH	1	1	1	1	0	0	V_{60}'	$V_4+(V_3-V_4)\times$	1600/3450	1733/4572
3DH	1	1	1	1	0	1	V_{61}'	$V_4+(V_3-V_4)\times$	1300/3450	1331/4572
3EH	1	1	1	1	1	0	V_{62}'	$V_4+(V_3-V_4)\times$	800/3450	872/4572
3FH	1	1	1	1	1	1	V_{63}'	V_4		

rn	(Ω) 732A	732B
r0	800	1766
r1	750	736
r2	700	566
r3	650	509
r4	600	396
r5	550	340
r6	550	283
r7	500	283
r8	500	226
r9	400	226
r10	400	170
r11	350	170
r12	350	170
r13	350	170
r14	300	170
r15	300	170
r16	300	152
r17	250	152
r18	250	152
r19	250	152
r20	200	152
r21	200	152
r22	200	152
r23	150	152
r24	150	152
r25	150	152
r26	150	152
r27	100	152
r28	100	152
r29	100	152
r30	100	152
r31	100	152
r32	100	156
r33	100	156
r34	100	156
r35	100	156
r36	100	156
r37	100	156
r38	100	156
r39	100	156
r40	100	156
r41	100	156
r42	100	156
r43	100	156
r44	100	156
r45	100	156
r46	100	156
r47	100	156
r48	100	175
r49	100	175
r50	100	175
r51	100	175
r52	100	175
r53	150	232
r54	150	232
r55	150	232
r56	200	232
r57	200	289
r58	250	345
r59	250	402
r60	300	402
r61	500	459
r62	800	872
rtotal	15850	15851

Caution There is no connection between V_4 and V_5 terminal in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage (2/2)

$V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1$ V, POL2 = L



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage				rn	(Ω)	
									732A	732B		732A	732B
00H	0	0	0	0	0	0	V_0''	V_9			r0	800	1766
01H	0	0	0	0	0	1	V_1''	$V_9+(V_8-V_9)\times$	800/8050	1766/6351	r1	750	736
02H	0	0	0	0	1	0	V_2''	$V_9+(V_8-V_9)\times$	1550/8050	2502/6351	r2	700	566
03H	0	0	0	0	1	1	V_3''	$V_9+(V_8-V_9)\times$	2250/8050	3068/6351	r3	650	509
04H	0	0	0	1	0	0	V_4''	$V_9+(V_8-V_9)\times$	2900/8050	3577/6351	r4	600	396
05H	0	0	0	1	0	1	V_5''	$V_9+(V_8-V_9)\times$	3500/8050	3973/6351	r5	550	340
06H	0	0	0	1	1	0	V_6''	$V_9+(V_8-V_9)\times$	4050/8050	4313/6351	r6	550	283
07H	0	0	0	1	1	1	V_7''	$V_9+(V_8-V_9)\times$	4600/8050	4596/6351	r7	500	283
08H	0	0	1	0	0	0	V_8''	$V_9+(V_8-V_9)\times$	5100/8050	4879/6351	r8	500	226
09H	0	0	1	0	0	1	V_9''	$V_9+(V_8-V_9)\times$	5600/8050	5105/6351	r9	400	226
0AH	0	0	1	0	1	0	V_{10}''	$V_9+(V_8-V_9)\times$	6000/8050	5331/6351	r10	400	170
0BH	0	0	1	0	1	1	V_{11}''	$V_9+(V_8-V_9)\times$	6400/8050	5501/6351	r11	350	170
0CH	0	0	1	1	0	0	V_{12}''	$V_9+(V_8-V_9)\times$	6750/8050	5671/6351	r12	350	170
0DH	0	0	1	1	0	1	V_{13}''	$V_9+(V_8-V_9)\times$	7100/8050	5841/6351	r13	350	170
0EH	0	0	1	1	1	0	V_{14}''	$V_9+(V_8-V_9)\times$	7450/8050	6011/6351	r14	300	170
0FH	0	0	1	1	1	1	V_{15}''	$V_9+(V_8-V_9)\times$	7750/8050	6181/6351	r15	300	170
10H	0	1	0	0	0	0	V_{16}''	V_8			r16	300	152
11H	0	1	0	0	0	1	V_{17}''	$V_8+(V_7-V_8)\times$	300/2750	152/2432	r17	250	152
12H	0	1	0	0	1	0	V_{18}''	$V_8+(V_7-V_8)\times$	550/2750	304/2432	r18	250	152
13H	0	1	0	0	1	1	V_{19}''	$V_8+(V_7-V_8)\times$	800/2750	456/2432	r19	250	152
14H	0	1	0	1	0	0	V_{20}''	$V_8+(V_7-V_8)\times$	1050/2750	608/2432	r20	200	152
15H	0	1	0	1	0	1	V_{21}''	$V_8+(V_7-V_8)\times$	1250/2750	760/2432	r21	200	152
16H	0	1	0	1	1	0	V_{22}''	$V_8+(V_7-V_8)\times$	1450/2750	912/2432	r22	200	152
17H	0	1	0	1	1	1	V_{23}''	$V_8+(V_7-V_8)\times$	1650/2750	1064/2432	r23	150	152
18H	0	1	1	0	0	0	V_{24}''	$V_8+(V_7-V_8)\times$	1800/2750	1216/2432	r24	150	152
19H	0	1	1	0	0	1	V_{25}''	$V_8+(V_7-V_8)\times$	1950/2750	1368/2432	r25	150	152
1AH	0	1	1	0	1	0	V_{26}''	$V_8+(V_7-V_8)\times$	2100/2750	1520/2432	r26	150	152
1BH	0	1	1	0	1	1	V_{27}''	$V_8+(V_7-V_8)\times$	2250/2750	1672/2432	r27	100	152
1CH	0	1	1	1	0	0	V_{28}''	$V_8+(V_7-V_8)\times$	2350/2750	1824/2432	r28	100	152
1DH	0	1	1	1	0	1	V_{29}''	$V_8+(V_7-V_8)\times$	2450/2750	1976/2432	r29	100	152
1EH	0	1	1	1	1	0	V_{30}''	$V_8+(V_7-V_8)\times$	2550/2750	2128/2432	r30	100	152
1FH	0	1	1	1	1	1	V_{31}''	$V_8+(V_7-V_8)\times$	2650/2750	2280/2432	r31	100	152
20H	1	0	0	0	0	0	V_{32}''	V_7			r32	100	156
21H	1	0	0	0	0	1	V_{33}''	$V_7+(V_6-V_7)\times$	100/1600	156/2496	r33	100	156
22H	1	0	0	0	1	0	V_{34}''	$V_7+(V_6-V_7)\times$	200/1600	312/2496	r34	100	156
23H	1	0	0	0	1	1	V_{35}''	$V_7+(V_6-V_7)\times$	300/1600	468/2496	r35	100	156
24H	1	0	0	1	0	0	V_{36}''	$V_7+(V_6-V_7)\times$	400/1600	624/2496	r36	100	156
25H	1	0	0	1	0	1	V_{37}''	$V_7+(V_6-V_7)\times$	500/1600	780/2496	r37	100	156
26H	1	0	0	1	1	0	V_{38}''	$V_7+(V_6-V_7)\times$	600/1600	936/2496	r38	100	156
27H	1	0	0	1	1	1	V_{39}''	$V_7+(V_6-V_7)\times$	700/1600	1092/2496	r39	100	156
28H	1	0	1	0	0	0	V_{40}''	$V_7+(V_6-V_7)\times$	800/1600	1248/2496	r40	100	156
29H	1	0	1	0	0	1	V_{41}''	$V_7+(V_6-V_7)\times$	900/1600	1404/2496	r41	100	156
2AH	1	0	1	0	1	0	V_{42}''	$V_7+(V_6-V_7)\times$	1000/1600	1560/2496	r42	100	156
2BH	1	0	1	0	1	1	V_{43}''	$V_7+(V_6-V_7)\times$	1100/1600	1716/2496	r43	100	156
2CH	1	0	1	1	0	0	V_{44}''	$V_7+(V_6-V_7)\times$	1200/1600	1872/2496	r44	100	156
2DH	1	0	1	1	0	1	V_{45}''	$V_7+(V_6-V_7)\times$	1300/1600	2028/2496	r45	100	156
2EH	1	0	1	1	1	0	V_{46}''	$V_7+(V_6-V_7)\times$	1400/1600	2184/2496	r46	100	156
2FH	1	0	1	1	1	1	V_{47}''	$V_7+(V_6-V_7)\times$	1500/1600	2340/2496	r47	100	156
30H	1	1	0	0	0	0	V_{48}''	V_6			r48	100	175
31H	1	1	0	0	0	1	V_{49}''	$V_6+(V_5-V_6)\times$	100/3450	175/4572	r49	100	175
32H	1	1	0	0	1	0	V_{50}''	$V_6+(V_5-V_6)\times$	200/3450	350/4572	r50	100	175
33H	1	1	0	0	1	1	V_{51}''	$V_6+(V_5-V_6)\times$	300/3450	525/4572	r51	100	175
34H	1	1	0	1	0	0	V_{52}''	$V_6+(V_5-V_6)\times$	400/3450	700/4572	r52	100	175
35H	1	1	0	1	0	1	V_{53}''	$V_6+(V_5-V_6)\times$	500/3450	875/4572	r53	150	232
36H	1	1	0	1	1	0	V_{54}''	$V_6+(V_5-V_6)\times$	650/3450	1107/4572	r54	150	232
37H	1	1	0	1	1	1	V_{55}''	$V_6+(V_5-V_6)\times$	800/3450	1339/4572	r55	150	232
38H	1	1	1	0	0	0	V_{56}''	$V_6+(V_5-V_6)\times$	950/3450	1571/4572	r56	200	232
39H	1	1	1	0	0	1	V_{57}''	$V_6+(V_5-V_6)\times$	1150/3450	1803/4572	r57	200	289
3AH	1	1	1	0	1	0	V_{58}''	$V_6+(V_5-V_6)\times$	1350/3450	2092/4572	r58	250	345
3BH	1	1	1	0	1	1	V_{59}''	$V_6+(V_5-V_6)\times$	1600/3450	2437/4572	r59	250	402
3CH	1	1	1	1	0	0	V_{60}''	$V_6+(V_5-V_6)\times$	1850/3450	2839/4572	r60	300	402
3DH	1	1	1	1	0	1	V_{61}''	$V_6+(V_5-V_6)\times$	2150/3450	3241/4572	r61	500	459
3EH	1	1	1	1	1	0	V_{62}''	$V_6+(V_5-V_6)\times$	2650/3450	3700/4572	r62	800	872
3FH	1	1	1	1	1	1	V_{63}''	V_5			rtotal	15850	15851

Caution There is no connection between V_4 and V_5 terminal in the chip.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)
Input width: 36 bits (2-pixel data)

R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

R,/L = L (Left shift)

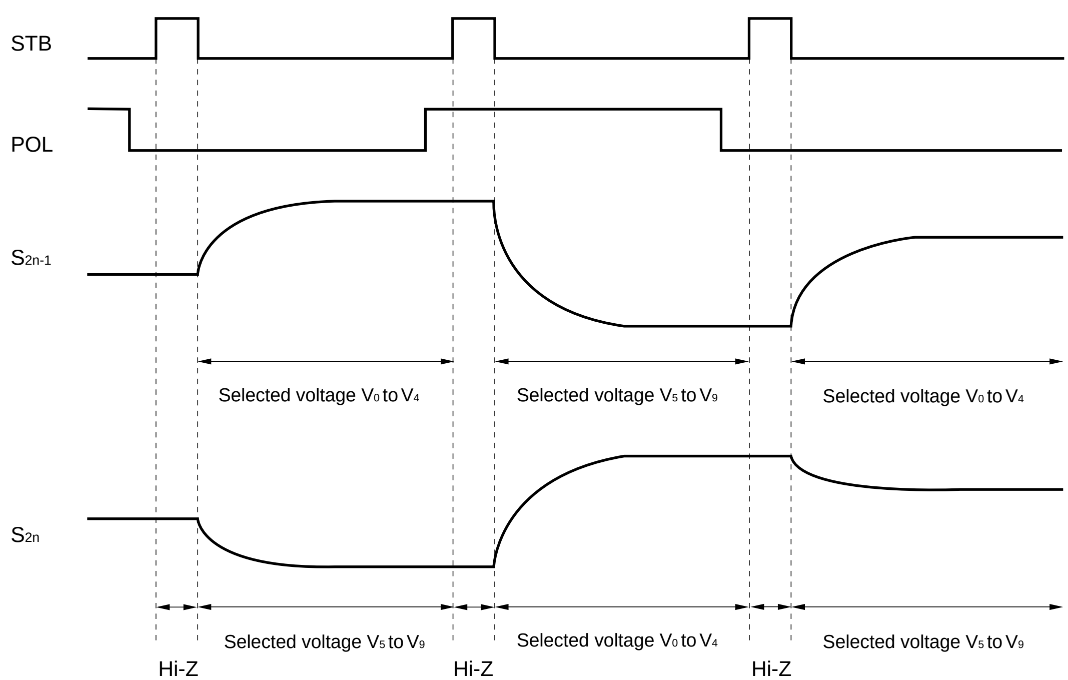
Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Note S_{2n-1} (Odd output), S_{2n} (Even output)

★ 7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. RELATIONSHIP BETWEEN STB, CLK, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

Figure 8–1. Output Circuit Block Diagram

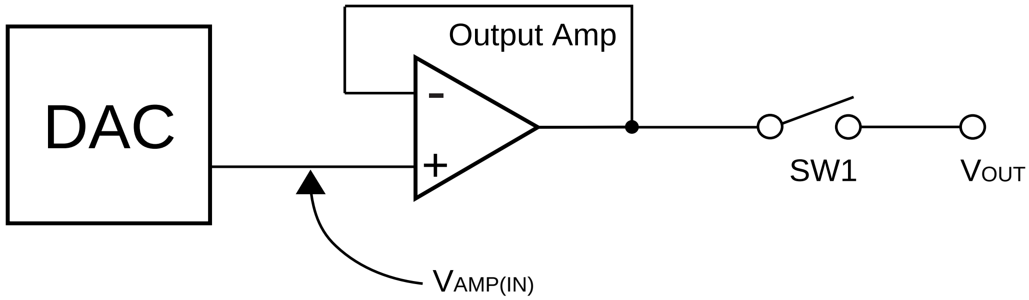
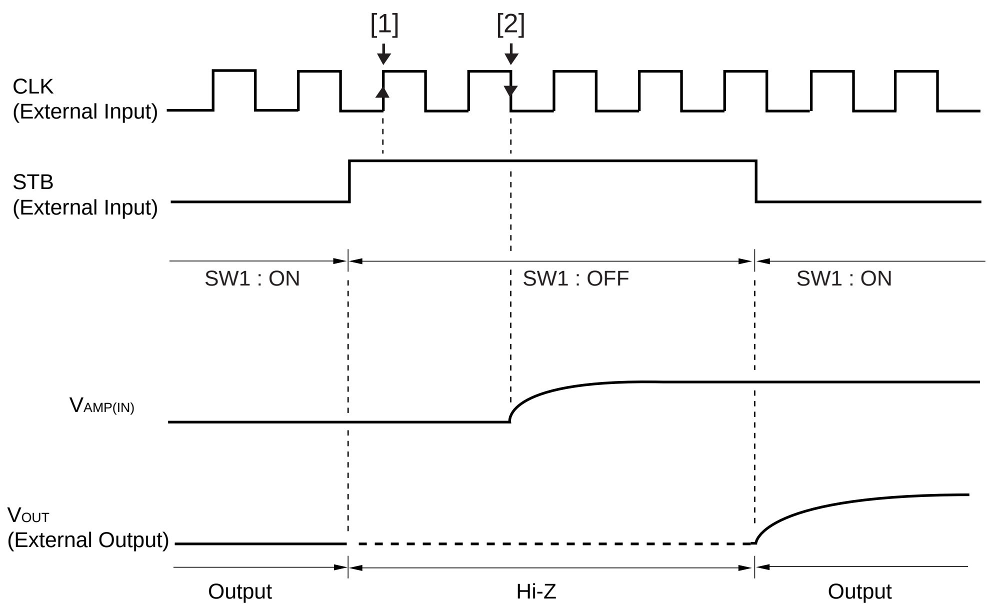


Figure 8–2. Output Circuit Timing Waveform



Remarks 1. STB = L : SW1 = ON

STB = H : SW1 = OFF

2. STB = “H” is acknowledged at timing [1].

3. The display data latch is completed at timing [2] and the input voltage (Vamp (in) : gray-scale level voltage) of the output amplifier changes.

9. CURRENT CONSUMPTION REDUCTION FUNCTION

The μPD16732A and 16732B have a low power control function (LPC) which can switch the bias current of the output amplifier between two levels and a bias control function (Bcont) which can be used to finely control the bias current.

<Low power control function (LPC)>

The bias current of the output amplifier can be switched between two levels using this pin. (Bcont: Open)

LPC = H or Open: Normal power mode

LPC = L: Low power mode

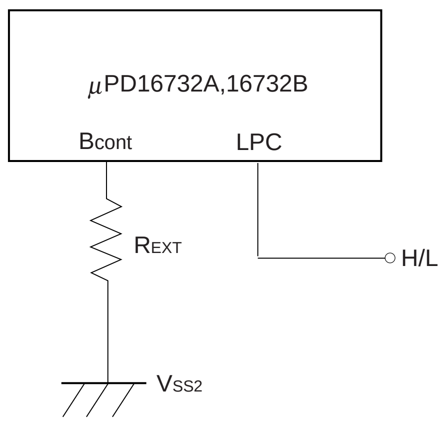
★ The V_{DD2} of static current consumption can be reduced to two thirds of that in normal mode. Input a stable DC current (V_{DD1}/V_{SS1}) to this pin.

<Bias Current Control Function (Bcont)>

It is possible to fine-control the current consumption by using the bias current control function (Bcont pin). When using this function, connect this pin to the stabilized ground potential (V_{SS2}) via an external resistor (R_{EXT}). When not using this function, leave this pin open.

Refer to the table below for the percentage of current regulation when using the bias current control function.

Figure9–1. Bias Current Control Function (Bcont)



Refer to the table below for the percentage of current regulation when using the bias current control function.

★ **Talbe9–1. Current Consumption Regulation Percentage Compared to Normal Mode**

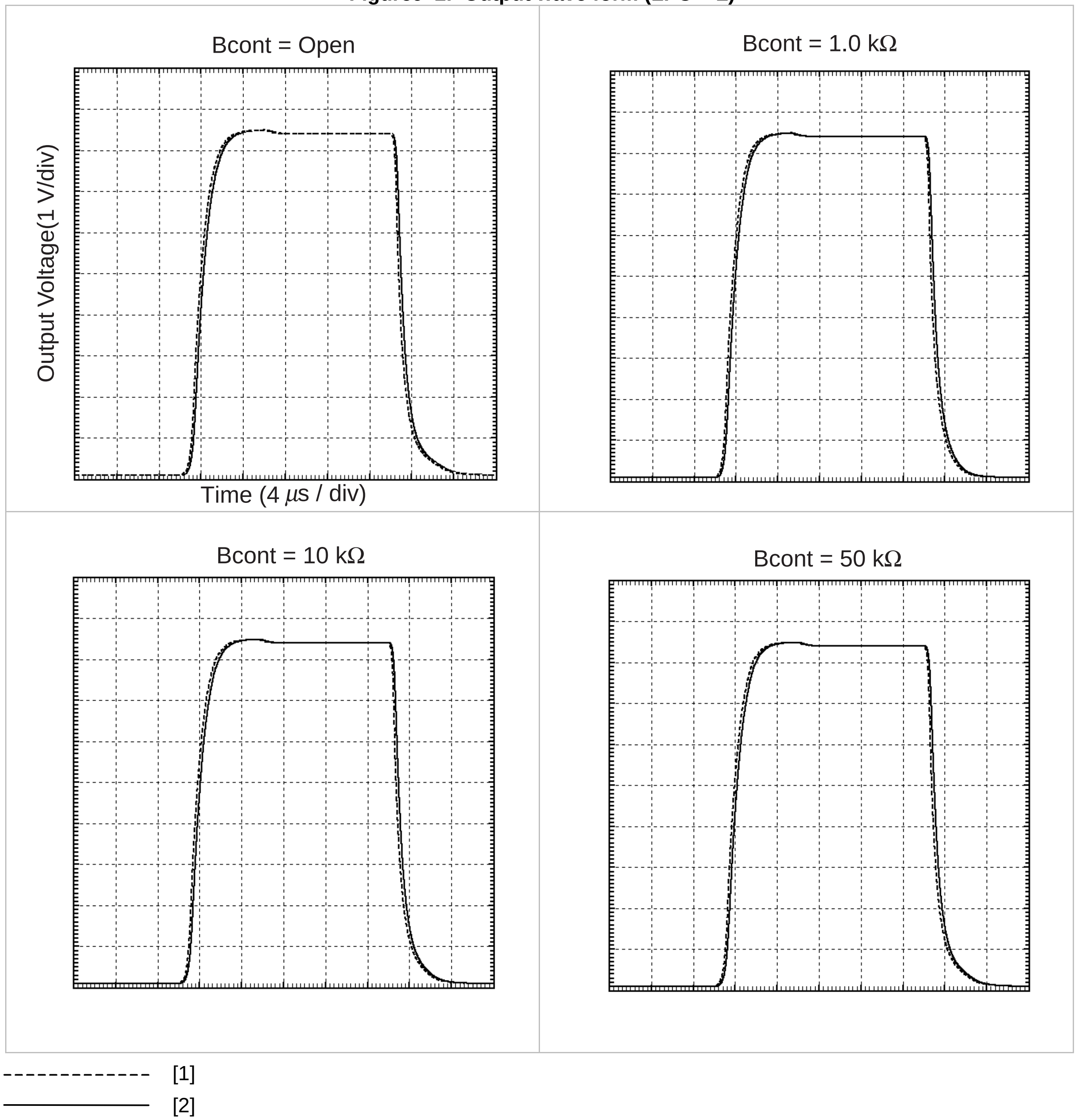
R_{EXT}	Current Consumption Regulation Percentage	
	LPC = H	LPC = L
∞ (Open)	100 %	65 %
50 kΩ	110 %	70 %
20 kΩ	115 %	80 %
10 kΩ	120 %	85 %

V_{DD1} = 3.3 V
V_{DD2} = 8.7 V
LPC = 3.3 V/0 V

Remark The above current consumption regulation percentages are not product-characteristic guaranteed as they are based on the results of simulation.

Caution Because the low-power and bias-current control functions control the bias current in the output amplifier and regulate the over-all current consumption of the driver IC, when this occurs, the characteristics of the output amplifier will simultaneously change. Therefore, when using these functions, be sure to sufficiently evaluate the picture quality.

Figure9–2. Output wave form (LPC = L)



<Test Condition>

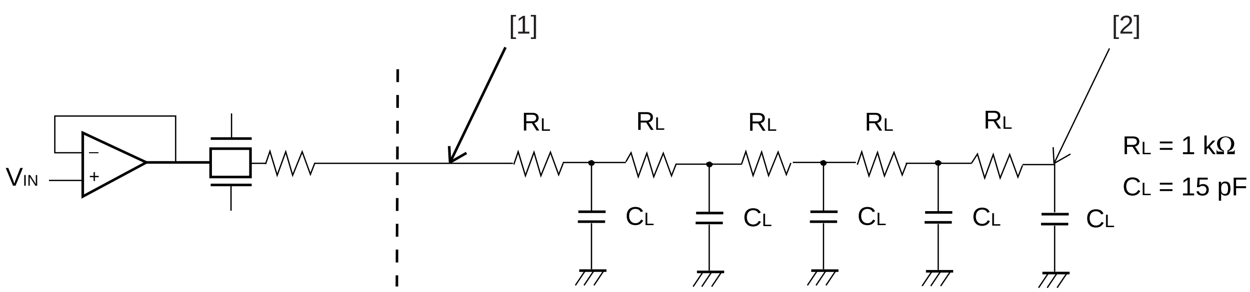
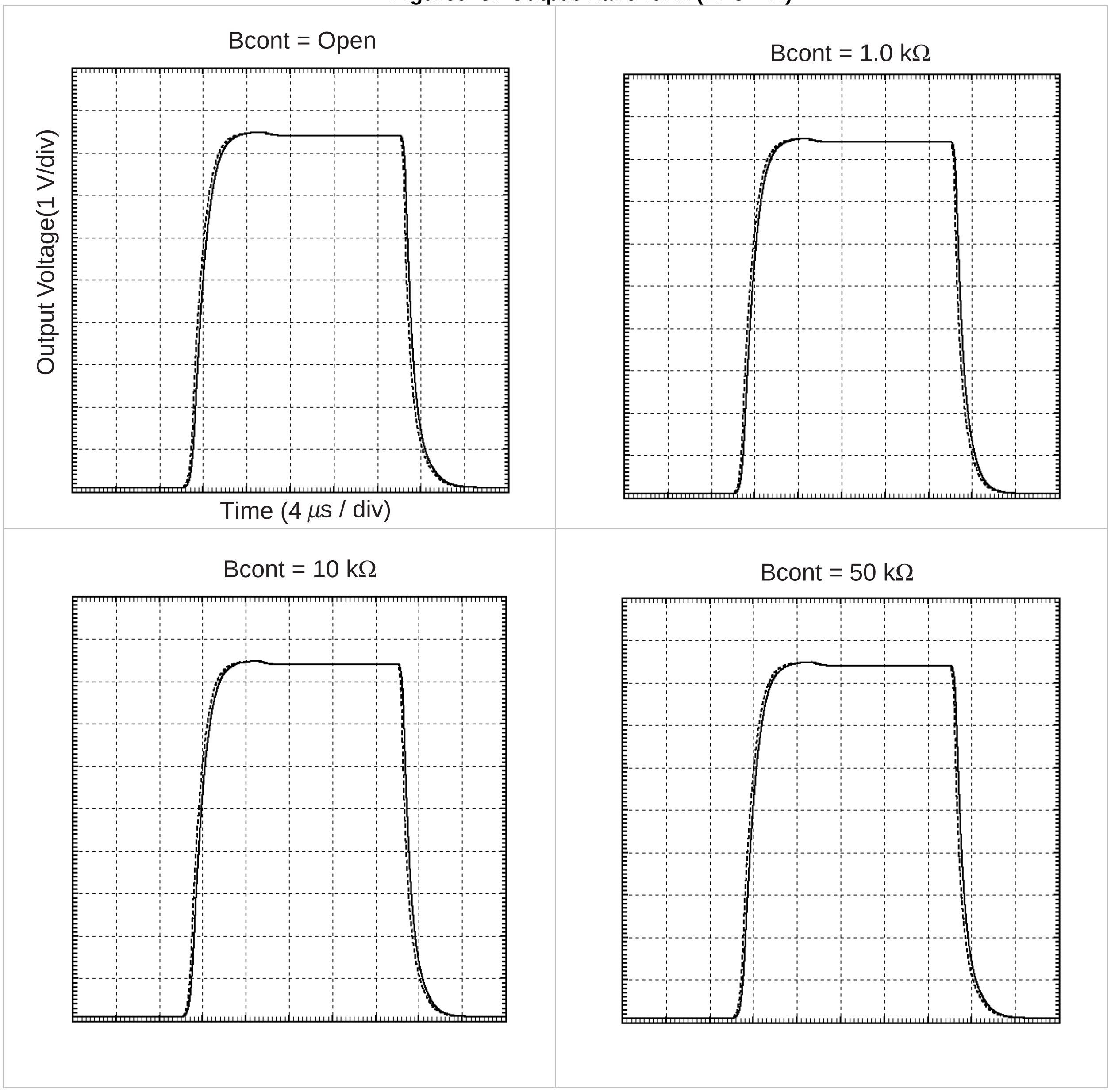


Figure9–3. Output wave form (LPC = H)



10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.3		3.6	V
Driver Part Supply Voltage	V_{DD2}		8.0	8.5	9.0	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_9		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Driver Part Output Voltage	V_O		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum Clock Frequency	$f_{MAX.}$	V_{DD1} = 2.3 V to 3.6 V	45			MHz
		V_{DD1} = 3.0 V to 3.6 V	65			MHz

Electrical Characteristics (T_A = –10 to +75 °C, V_{DD1} = 2.3 V to 3.6 V, V_{DD2} = 8.5 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V, Unless otherwise specified, the input level is defined to be LPC = H or Open, Bcont = Open)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}				±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA	V_{DD1} – 0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA			0.1	V
γ-Corrected Supply Current	I_γ	V_0 to V_4 = V_5 to V_9 = 4.0 V; V_0 pin, V_5 pin	126	252	504	μA
		V_4 pin, V_9 pin	–504	–252	–126	μA
Driver Output Current	I_{VOH}	V_X = 7.0 V, V_{OUT} = 6.5 V [Note]			–30	μA
	I_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V [Note]	30			μA
Output Voltage Deviation	ΔV_O	V_{DD1} = 3.3 V, V_{DD2} = 8.5 V, V_{OUT} = 2.0 V, 4.25 V, 6.5 V		±7	±20	mV
Output swing difference deviation	ΔV_{P-P}			±2	±15	mV
Output Voltage Range	V_O	All Input data	0.1		V_{DD2} – 0.1	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}, with no load		3.0	6.0	mA
Driver Part Dynamic Current Consumption	I_{DD21}	V_{DD2} = 8.5 V ± 0.5 V, with no load LPC = H, Bcont = Open		3.0	6.0	mA
	I_{DD22}	V_{DD2} = 8.5 V ± 0.5 V, with no load LPC = L, Bcont = Open		2.0	4.0	mA

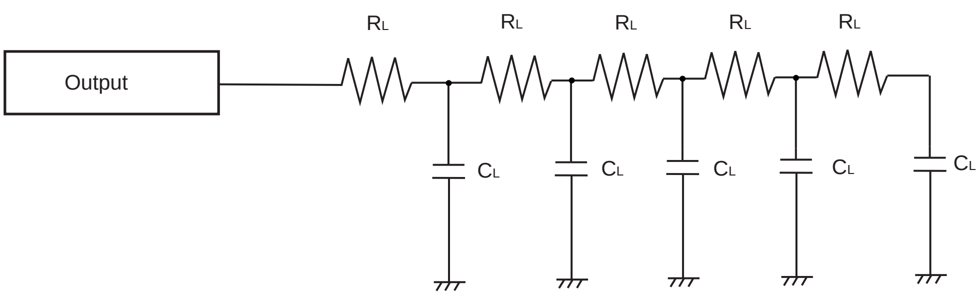
Notes1. V_X refers to the output voltage of analog output pins S_1 to S_{384}.
2. V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

Cautions 1. The STB cycle is defined to be 20 μs at f_{CLK} = 40 MHz.
2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (T_A = –10 to +75 °C, V_{DD1} = 2.3 V to 3.6 V, V_{DD2} = 8.5 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V, Unless otherwise specified, the input level is defined to be LPC = H or Open, Bcont = Open)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 10 pF, V_{DD1} = 2.3 V to 3.6 V		10	17	ns
		C_L = 10 pF, V_{DD1} = 3.0 V to 3.6 V		7	10.5	ns
Driver Output Delay Time	t_{PLH2}	C_L = 75 pF, R_L = 5 kΩ		2.5	5	μs
	t_{PLH3}			5	8	μs
	t_{PHL2}			2.5	5	μs
	t_{PHL3}			5	8	μs
Input Capacitance	C_{I1}	STHR (STHL) excluded, T_A = +25°C		5	10	pF
	C_{I2}	STHR (STHL), T_A = +25°C		8	10	pF

<Measurement Condition>



R_L= 1 kΩ

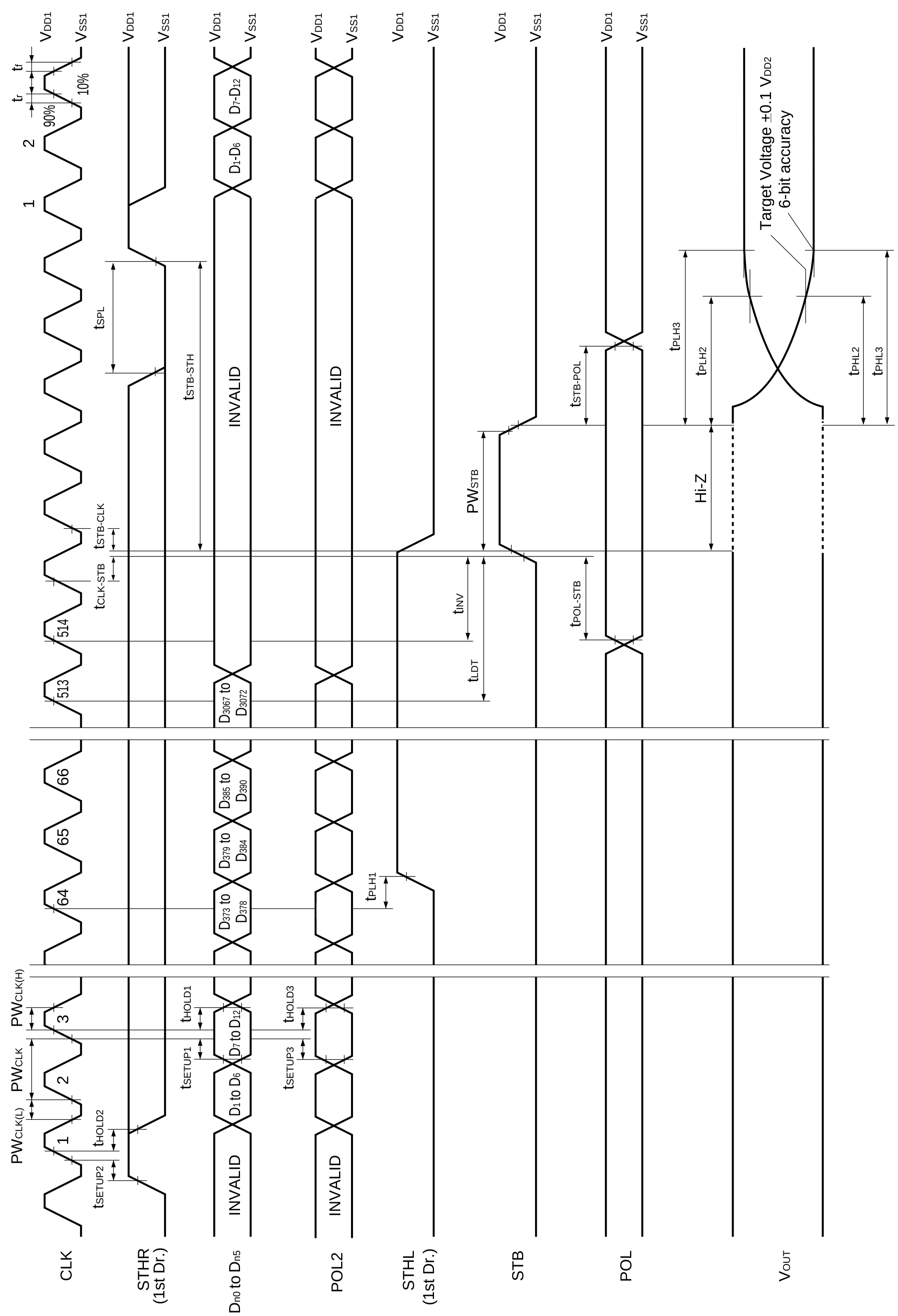
C_L= 15 pF

Timing Requirement (T_A = –10 to +75 °C, V_{DD1} = 2.3 V to 3.6 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 8.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}	V_{DD1} = 2.3 V to 3.6 V	22			ns
		V_{DD1} = 3.0 V to 3.6 V	15			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$	V_{DD1} = 2.3 V to 3.6 V	6			ns
		V_{DD1} = 3.0 V to 3.6 V	4			ns
Data Setup Time	t_{SETUP1}		4			ns
Data Hold Time	t_{HOLD1}		0			ns
Start Pulse Setup Time	t_{SETUP2}		4			ns
Start Pulse Hold Time	t_{HOLD2}		0			ns
POL2 Setup Time	t_{SETUP3}		4			ns
POL2 Hold Time	t_{HOLD3}		0			ns
Start Pulse Low Period	t_{SPL}		6			ns
STB Pulse Width	PW_{STB}		2			CLK
					4	μs
Data Invalid Period	t_{INV}		1			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK\text{-}STB}$	CLK ↑ → STB ↑	6			ns
STB-CLK Time	$t_{STB\text{-}CLK}$	STB ↑ → CLK ↑ V_{DD1} = 2.3 V to 3.6 V	9			ns
		STB ↑ → CLK ↑ V_{DD1} = 3.0 V to 3.6 V	6			ns
Time Between STB and Start Pulse	$t_{STB\text{-}STH}$	STB ↑ → STHR(STHL) ↑	2			CLK
POL-STB Time	$t_{POL\text{-}STB}$	POL ↑ or ↓ → STB ↑	–5			ns
★ STB-POL Time	$t_{STB\text{-}POL}$	STB ↓ → POL ↓ or ↑	6			ns

★ 11. SWITCHING CHARACTERISTICS WAVEFORM

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7\ V_{DD1}$, $V_{IL} = 0.3\ V_{DD1}$.



12. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16732A, 16732B.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

μPD16732AN-xxx, μPD16732BN-××× : TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2 : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2 : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)