Battery Protection IC for 2-Serial to 4-serial-Cell Pack (Secondary Protection)

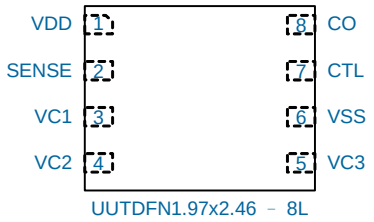
General Description

The uP8206 series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit. Short-circuits between cells accommodate series connection of two to four cells.

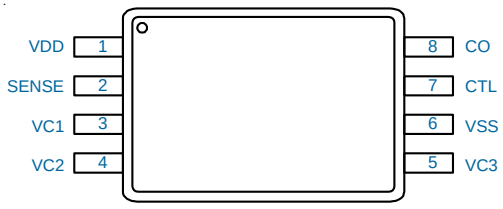
Applications

- **Lithium-ion Rechargeable Battery Packs (for Secondary Protection)**
- **Notebook Computers**
- **Portable Instrumentation**
- **Portable Equipment**

Pin Configuration



UUTDFN1.97x2.46 – 8L



TSSOP – 8L

Features

- **High-Accuracy Voltage Detection Circuit for Each Cell**
  - **Overcharge Detection Voltage n (n = 1 to 4)**
    4.0V to 4.6V (in 50 mV steps)
    Accuracy :±25 mV (+25°C),
    Accuracy : ±30 mV (-5°C to +55°C)
  - **Overcharge Hysteresis Voltage n (n = 1 to 4)**
    0.38 ±0.15V
- **Delay Time for Overcharge Detection Can be Set by an Internal Circuit Only (External Capacitors are Unnecessary)**
- **Output Control Function via CTL Pin**
- **High Withstand Voltage Devices Absolute Maximum Rating: 28V**
- **Wide Operating Voltage Range 4V to 24V**
- **Wide Operating Temperature Range -40°C to +85°C**
- **Low Current Consumption**
  - **At 3.5V for Each Cell 5.0uA Max. (+25°C)**
  - **At 2.3V for Each Cell 4.0uA Max. (+25°C)**
- **RoHS Compliant and Halogen-Free**

Ordering Information

Order Number	Package	Top Marking	Note
uP8206PDX8-XY	UUTDFN1.97x2.46-8L	ECPXY	Code X: Over-Charge Detection Voltage A: 4.30V; B: 4.35V; C: 4.40V; D: 4.45V; E: 4.50V F: 4.55V;G: 4.60V Code Y: Over-Charge Detection Delay Time 1: 6.5s; 2: 3.5s; 3: 4s
uP8206ATA8-XY	TSSOP-8L	8206AXY	

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Marking Rule

Line1: Product Code
-ECP: Product Code
-XY: Version Code
Line2: Lot Number

UUTDFN1.97x2.46 - 8L

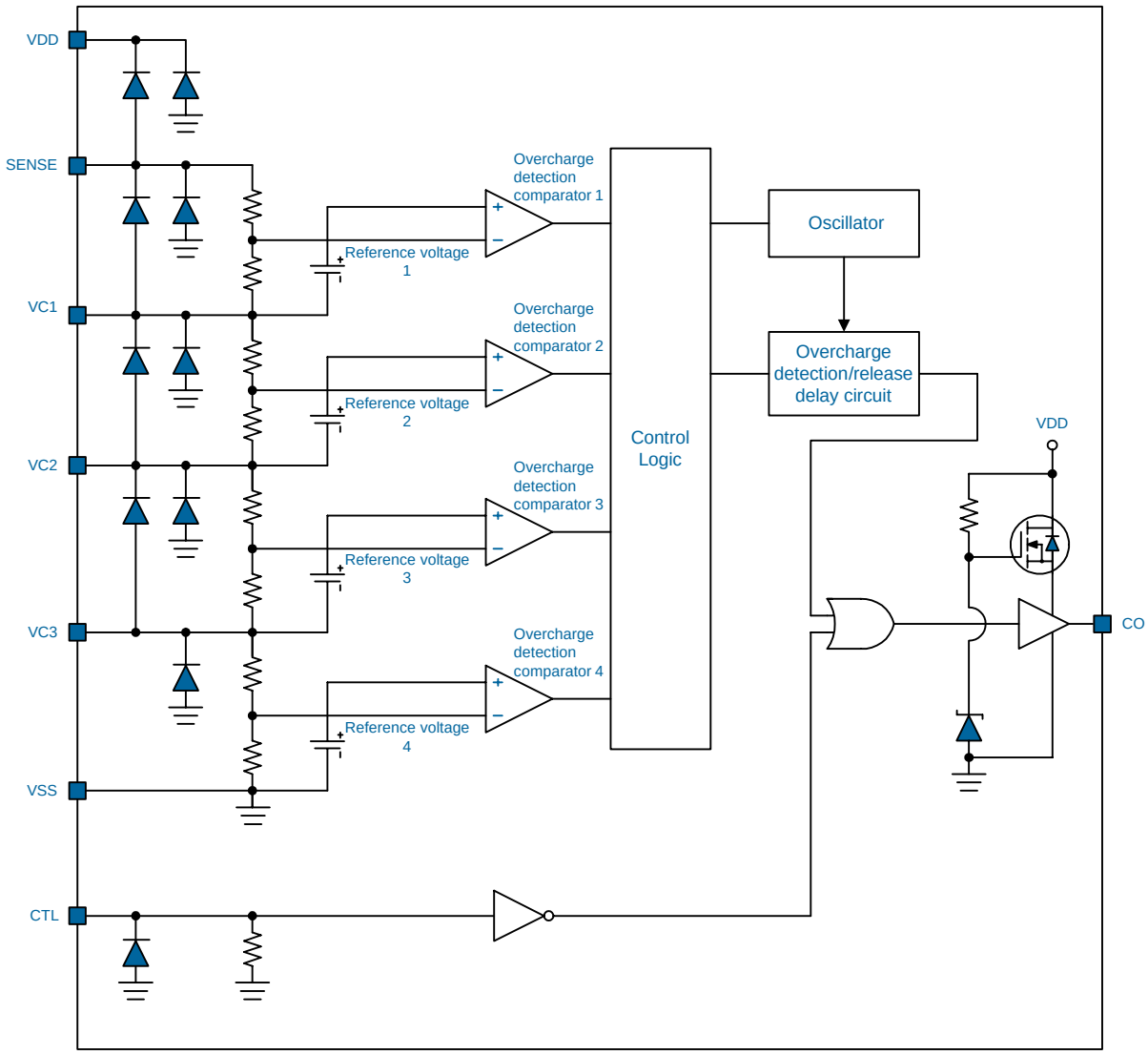
Line1: Product Code
-8206A: Product Code
-XY: Version Code
Line2: Lot Number

TSSOP - 8L

Functional Pin Description

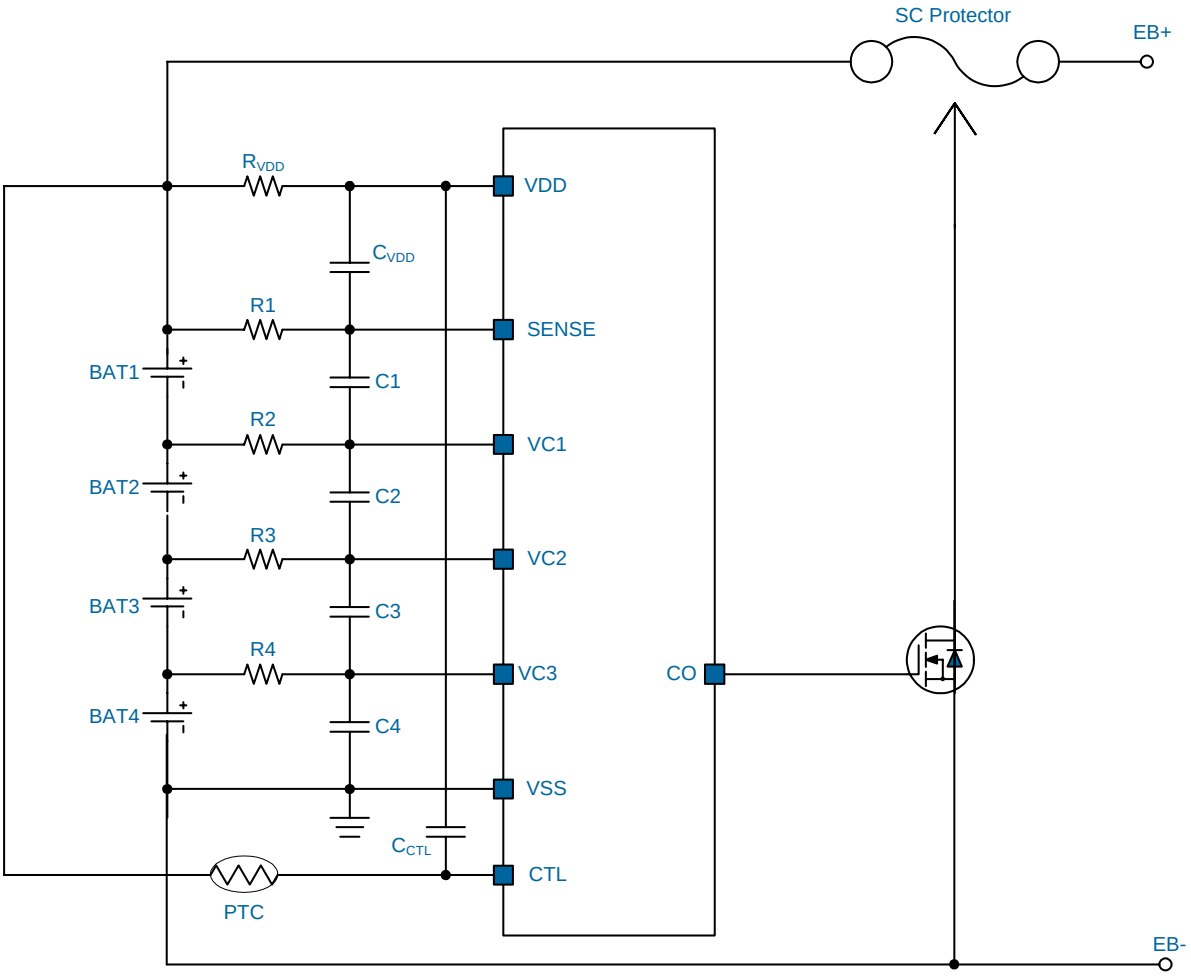
Pin No.	Pin Name	Pin Function
1	VDD	**Positive Power Input Pin.**
2	SENSE	**Positive Voltage Connection Pin of Battery 1.**
3	VC1	**Negative Voltage Connection Pin of Battery 1.** **Positive Voltage Connection Pin of Battery 2.**
4	VC2	**Negative Voltage Connection Pin of Battery 2.** **Positive Voltage Connection Pin of Battery 3.**
5	VC3	**Negative Voltage Connection Pin of Battery 3.** **Positive Voltage Connection Pin of Battery 4.**
6	VSS	**Negative Power Input Pin.** **Negative Voltage Connection Pin of Battery 4.**
7	CTL	**CO Output Control Pin.**
8	CO	**FET Gate Connection Pin for Charge.**

Functional Block Diagram



Example of Application Circuit

1. Overheat Protection Via PTC



Cautions

1. The above connection example will not guarantee successful operation. Perform thorough evaluation using the actual application.
2. A pull-down resistor is included in the CTL pin. To perform overheat protection via the PTC in the uP8206A/P Series, connect the PTC before connecting batteries.
3. When the power fluctuation is large, connect the power supply of the PTC to the VDD pin of the uP8206A/P Series.
4. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

   4-series cell configuration

   BAT4 → BAT3 → BAT2 → BAT1

   3-series cell configuration

   BAT3 → BAT2 → BAT1

   2-series cell configuration

   BAT2 → BAT1

Test Circuit

(1) Test Condition 1, Test Circuit 1

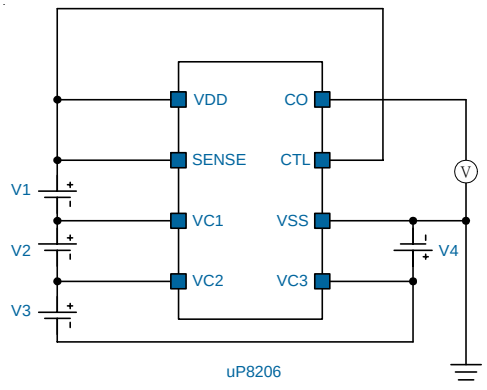
Set V1, V2, V3, and V4 to 3.5V. Overcharge detection voltage 1 (V_{CU1}) is the V1 voltage when CO is *H* after the voltage of V1 has been gradually increased. The overcharge hysteresis voltage (V_{HC1}) is the difference between V1 and V_{CU1} when CO is *L* after the voltage of V1 has been gradually decreased. Overcharge detection voltage V_{CUn} (n = 2 to 4) and overcharge hysteresis V_{HCn} (n = 2 to 4) can be determined in the same way as when n = 1.

(2) Test Condition 2, Test Circuit 1

Set V1, V2, V3, and V4 to 3.5V and in a moment of time (within 10us) increase V1 up to 5.0V. The overcharge detection delay time (t_{CU}) is the period from when V1 reached 5.0V to when CO becomes *H*. After that, in a moment of time (within 10us) decrease V1 down to 3.5V. The overcharge release delay time (t_{CL}) is the period from when V1 has reached 3.5V to when CO becomes *L*.

(3) Test Condition 3, Test Circuit 1

Set V1, V2, V3, and V4 to 3.5V and in a moment of time (within 10us) increase V1 up to 5.0V. This is defined as the first rise. Within t_{CU} 20 ms after the first rise, in a moment of time (within 10us) decrease V1 down to 3.5V and then in a moment of time (within 10us) restore up to 5.0V. This is defined as the second rise. When the period from when V1 was fallen to the second rise is short, CO becomes *H* after t_{CU} has elapsed since the first rise. If the period from when V1 falls to the second rise is gradually made longer, CO becomes *H* when t_{CU} has elapsed since the second rise. The overcharge timer reset delay time (t_{TR}) is the period from V1 fall till the second rise at that time.



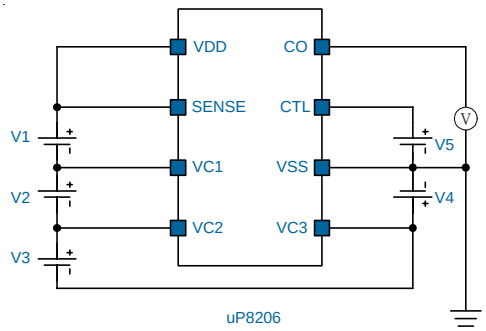
Test Circuit 1

(4) Test Condition 4, Test Circuit 2

In the uP8206A/P Series, set V1, V2, V3, and V4 to 3.5V and V5 to 14V. The CTL pin response time (t_{CTL}) is the period from when V5 reaches 0 V after V5 is in a moment of time (within 10us) decreased down to 0V to when CO becomes *H*.

(5) Test Condition 6, Test Circuit 2

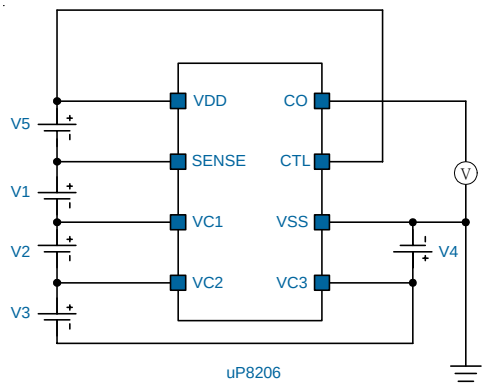
Set V1, V2, V3, and V4 to 3.5V and V5 to 0V. The CTL input *H* voltage (V_{CTLH}) is the maximum voltage of V5 when CO is *L* after V5 has been gradually increased. Next, set V5 to 14V. The CTL input *L* voltage (V_{CTLL}) is the minimum voltage of V5 when CO is *H* after V5 has been gradually decreased.



Test Circuit 2

(6) Test Condition 5, Test Circuit 3

After setting V1, V2, V3, and V4 to 3.5V and V5 to 0V, in a moment of time (within 10us) increase V5 up to 8.5V and decrease V5 again down to 0V. When the period from when V5 was raised to when it has fallen is short, if an overcharge detection operation is performed subsequently, the overcharge detection time is t_{CU}. However, when the period from when V5 is raised to when it is fallen is gradually made longer, the overcharge detection time during the subsequent overcharge detection operation is shorter than t_{CU}. The transition time to test mode (t_{TST}) is the period from when V5 was raised to when it has fallen at that time.

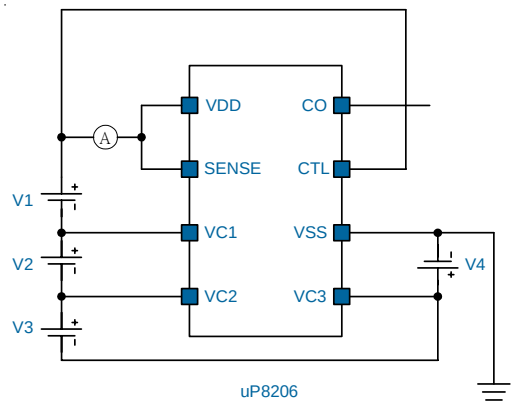


Test Circuit 3

(7) Test Condition 7, Test Circuit 4

The current consumption during operation (I_{OPE}) is the total of the currents that flow in the VDD pin and SENSE pin when V1, V2, V3, and V4 are set to 3.5V.

The current consumption during over discharge (I_{OPED}) is the total of the currents that flow in the VDD pin and SENSE pin when V1, V2, V3, and V4 are set to 2.3V.

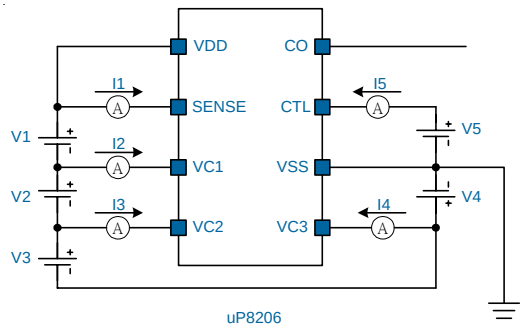


Test Circuit 4

(8) Test Condition 8, Test Circuit 5

The SENSE pin current (I_{SENSE}) is I1, the VC1 pin current (I_{VC1}) is I2, the VC2 pin current (I_{VC2}) is I3, the VC3 pin current (I_{VC3}) is I4, and the CTL pin *H* current (I_{CTLH}) is I5 when V1, V2, V3, and V4 are set to 3.5V, and V5 to 14V.

The CTL pin *L* current (I_{CTLL}) is I5 when V1, V2, V3, and V4 are set to 3.5V and V5 to 0V.



Test Circuit 5

Functional Description

Overcharge Detection

When the voltage of one of the batteries exceeds the overcharge detection voltage (V_{CU}) during charging under normal conditions and the state is retained for the overcharge detection delay time (t_{CU}) or longer, CO becomes *H*. This state is called overcharge. Attaching FET to the CO pin provides charge control and a second protection.

In the uP8206A/P Series, if the voltage of all the batteries decreases below the total of the overcharge detection voltage (V_{CU}) and the overcharge hysteresis voltage (V_{HC}) and the state is retained for the overcharge release delay time (t_{CL}) or longer, CO becomes *L*.

Overcharge Timer Reset

When an overcharge release noise that forces the voltage of the battery temporarily below the overcharge detection voltage (V_{CU}) is input during the overcharge detection delay time (t_{CU}) from when V_{CU} is exceeded to when charging is stopped, t_{CU} is continuously counted if the time the overcharge release noise persists is shorter than the overcharge timer reset delay time (t_{TR}). Under the same conditions, if the time the overcharge release noise persists t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CU} has been exceeded, counting t_{CU} resumes.

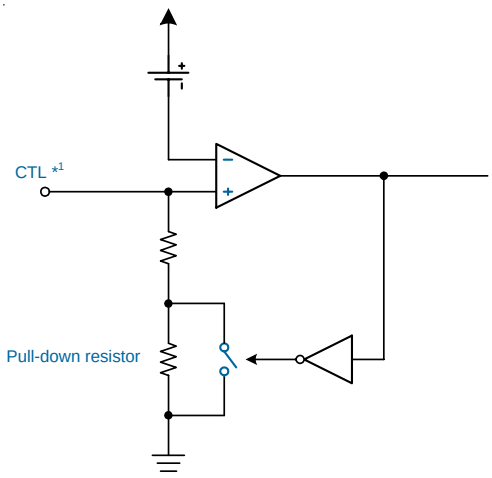
CTL Pin

The uP8206 Series has a control pin. The CTL pin is used to control the output voltage of the CO pin. In the uP8206A/P Series, the CTL pin takes precedence over the overcharge detection circuit.

Table 1. uP8206 Control via CTL Pin

CTL PIN	CO Pin
	uP8206A/P
"H"	Normal state*1
"Open"	"H"
"L"	"H"
"L" to "H"	--
"H" to "L"	--

***1.** The state is controlled by the overcharge detection circuit.



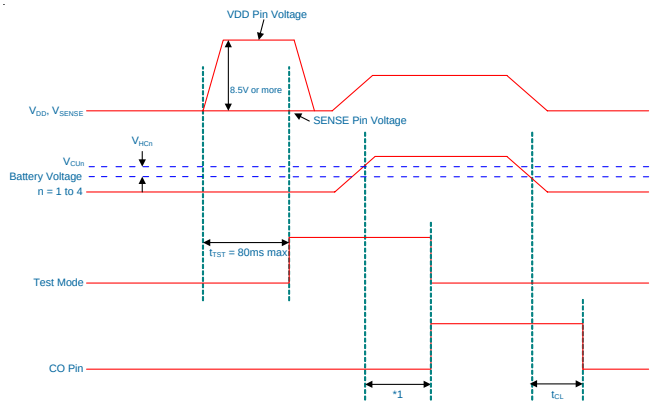
***1.** The reverse voltage *H* to *L* or *L* to *H* of CTL pin is VDD pin voltage -2.9V (Typ.), does not have the hysteresis.

Caution

1. Since the CTL pin implements high resistance of 8 MΩ to 12MΩ for pull down, be careful of external noise application. If an external noise is applied, CO may become *H*. Perform thorough evaluation using the actual application.

Test Mode

In the uP8206 Series, the overcharge detection delay time (t_{CU}) can be shortened by entering the test mode. The test mode can be set by retaining the VDD pin voltage 8.5V or higher than the SENSE pin voltage for at least 80 ms (V1 = V2 = V3 = V4 = 3.5V, T_A = 25°C). The status is retained by the internal latch and the test mode is retained even if the VDD pin voltage is decreased to the same voltage as that of the SENSE pin. When CO becomes "H" and when the delay time has elapsed after overcharge detection, the latch for retaining the test mode is reset and the uP8206 Series exits from the test mode.



***1.**

During normal mode, t_{CU} = 6.5s (Typ). In the product t_{CU} = 50ms(Typ.)

During normal mode, t_{CU} = 3.5s (Typ). In the product t_{CU} = 28ms(Typ.)

During normal mode, t_{CU} = 4.0s(Typ.). In the product t_{CU} = 32ms(Typ.)

Caution

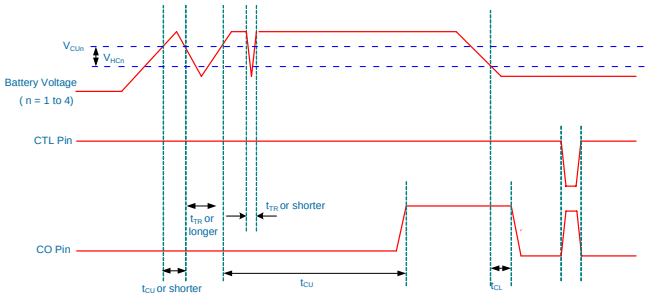
1. Set the test mode when no batteries are overcharged.

2. The overcharge release delay time (t_{CL}) is not shortened in the test mode.

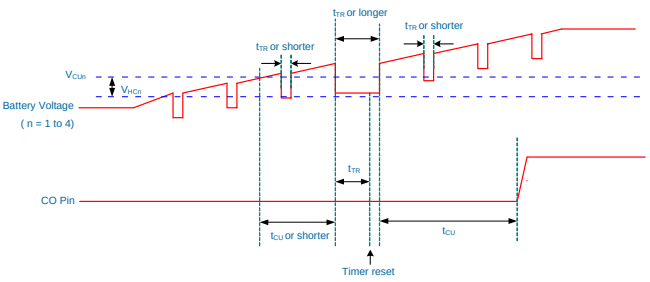
3. The overcharge timer resets delay time (t_{TR}) is not shortened in the test mode.

Timing Charts

1. Overcharge Detection Operation



2. Overcharge Timer Reset Operation



Battery Protection IC Connection Example

(1) 4-serial cell

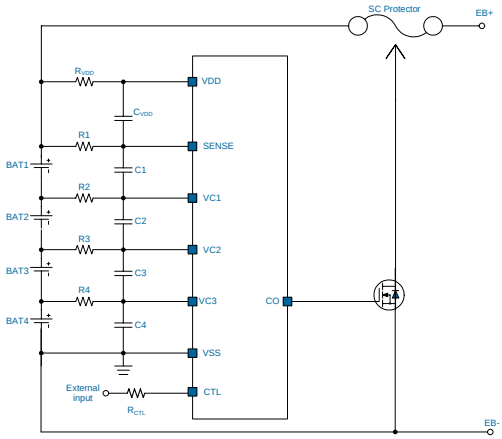


Table 2. Constants for 4-Serial cell External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R4	0.1	1	10	kΩ
2	C1 to C4, C_{VDD}	0.01	0.1	1	uF
3	R_{VDD}	50	100	500	Ω
4	R_{CTL}	0	100	500	Ω

Caution

1. The above constants are subject to change without prior notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

3. Set the same constants to R1 to R4 and to C1 to C4 and C_{VDD}.

4. Set R_{VDD}, C1 to C4, and C_{VDD} so that the condition (R_{VDD}) x (C1 to C4, C_{VDD}) ≥ $5x10^{-6}$ is satisfied.

5. Set R1 to R4, C1 to C4, and C_{VDD} so that the condition (R1 to R4) . (C1 to C4, C_{VDD}) ≥ $1x10^{-4}$is satisfied.

6. In the uP8206A/P Series, normally input *H* to the external input, and input *L* when setting CO to *H*.

7. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

4-series cell configuration

BAT4 → BAT3 → BAT2 → BAT1

(2) 3-serial cell

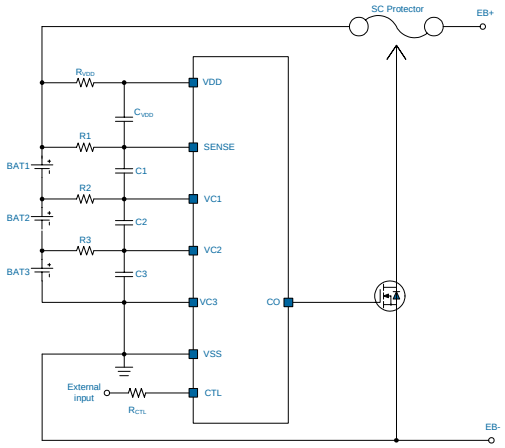


Table 3. Constants for 3-serial cell External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R3	0.1	1	10	kΩ
2	C1 to C3, C_{VDD}	0.01	0.1	1	uF
3	R_{VDD}	50	100	500	Ω
4	R_{CTL}	0	100	500	Ω

Caution

1. The above constants are subject to change without prior notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

3. Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.

4. Set R_{VDD}, C1 to C3, and C_{VDD} so that the condition (R_{VDD}) x (C1 to C3, C_{VDD}) ≥ $5x10^{-6}$ is satisfied.

5. Set R1 to R3, C1 to C3, and C_{VDD} so that the condition (R1 to R3) . (C1 to C3, C_{VDD}) ≥ $1x10^{-4}$is satisfied.

6. In the uP8206A/P Series, normally input *H* to the external input, and input *L* when setting CO to *H*.

7. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

3-series cell configuration

BAT3 → BAT2 → BAT1

(3) 2-serial cell

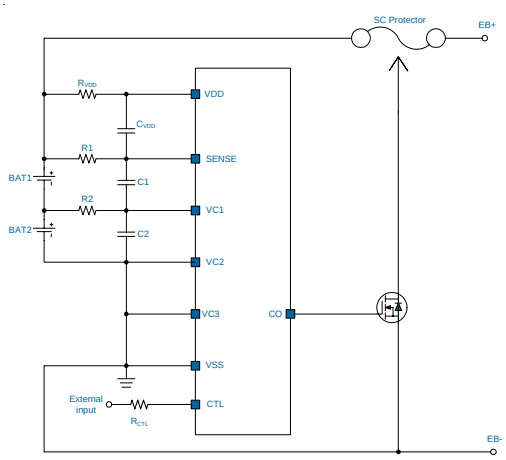


Table 4. Constants for 2-serial cell External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R2	0.1	1	10	kΩ
2	C1 to C2, C_{VDD}	0.01	0.1	1	uF
3	R_{VDD}	50	100	500	Ω
4	R_{CTL}	0	100	500	Ω

Caution

1. The above constants are subject to change without prior notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

3. Set the same constants to R1 to R2 and to C1 to C2 and C_{VDD}.

4. Set R_{VDD}, C1 to C2, and C_{VDD} so that the condition (R_{VDD}) x (C1 to C2, C_{VDD}) ≥ $5x10^{-6}$ is satisfied.

5. Set R1 to R2, C1 to C2, and C_{VDD} so that the condition (R1 to R2) . (C1 to C2, C_{VDD}) ≥ $1x10^{-4}$is satisfied.

6. In the uP8206A/P Series, normally input *H* to the external input, and input *L* when setting CO to *H*.

7. Cell connections: To prevent incorrect output activation, the VSS pin must be connected first. Connect sequences must be used as following:

2-series cell configuration

BAT2 → BAT1

Precautions

Do not connect batteries charged with V_{CU} + V_{HC} or more. If the connected batteries include a battery charged with V_{CU} + V_{HC} or more, *H* may be output at CO after all pins are connected.

In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.

Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figure in "**Battery Protection IC Connection Example**".

The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.

Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.

uPI claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

Absolute Maximum Rating

(Note 1)

Supply Voltage Range between VDD and VSS ---------- VSS -0.3V to +28V
Supply Input Voltage Range, SENSE, VC1, VC2, VC3 ---------- VSS -0.3V to +28V
CO Output Pin Voltage Range, CO ---------- -0.3V to +9V
Supply Input Voltage Range, SENSE to VC1, VC1 to VC2, VC2 to VC3, VC3 to VSS ---------- -0.3V to +8V
Other Pins, CTL ---------- -0.3V to 28V
Storage Temperature Range ---------- -45°C to +125°C
Junction Temperature ---------- 125°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 1kV

Thermal Information

Package Thermal Resistance (Note 3)

- UUTDFN1.97x2.46 - 8L θ_{JA} ---------- 102°C/W
- UUTDFN1.97x2.46 - 8L θ_{JC} ---------- 20°C/W
- TSSOP8 - 8L θ_{JA} ---------- 145°C/W
- TSSOP8 - 8L θ_{JC} ---------- 50°C/W

Power Dissipation, P_D @ T_A = 25°C

- UUTDFN1.97x2.46 - 8L ---------- 0.6W
- TSSOP8 - 8L ---------- 0.625W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{DD}, Vss ---------- 4V to +25V
Supply Input Voltage, VC1, VC2, VC3, CTL ---------- 0V to +25V
Input Voltage, VCn - VC(n-1), (n = 1,2,3), VC0 = Vss ---------- 0V to +5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Condtion	Test Circuit
DETECTION VOLTAGE								
Overcharge Detection Voltage(n = 1, 2, 3, 4)	V_{CUn}	4.20V to 4.80V, adjustable, T_A = 25°C	V_{CUn}-0.025	V_{CUn}	V_{CUn}+0.025	V	1	1
		4.20V to 4.80V, adjustable, T_A = -5°C to 55°C*1	V_{CUn}-0.030	V_{CUn}	V_{CUn}+0.030	V	1	1
Overcharge Hysteresis Voltage(n = 1, 2, 3, 4)	V_{HCn}		V_{HCn}-0.15	-0.38	V_{HCn}+0.15	V	1	1
Overcharge Detection Voltage	V_{CU}	uP8206XXX8-AY	4.275	4.30	4.325	V	1	1
		uP8206XXX8-BY	4.325	4.35	4.375		1	1
		uP8206XXX8-CY	4.375	4.40	4.425		1	1
		uP8206XXX8-DY	4.425	4.45	4.475		1	1
		uP8206XXX8-EY	4.475	4.50	4.525		1	1
		uP8206XXX8-FY	4.525	4.55	4.575		1	1
		uP8206XXX8-GY	4.575	4.60	4.625		1	1
Overcharge Hysteresis Voltage	V_{HC}		-0.53	-0.38	-0.23	V	1	1
INPUT VOLTAGE								
Supply Voltage between VDD and VSS	V_{DSOP}		4	--	24	V	--	--
CTL Input "H" Voltage	V_{CTLH}		V_{DD}·0.95	--	--	V	6	2
CTL Input "L" Voltage	V_{CTLL}		--	--	V_{DD}·0.4	V	6	2
INPUT CURRENT								
Current Consumption during Operation	I_{OPE}	V1 = V2 = V3 = V4 = 3.5V	--	2.5	5.0	uA	7	4
Current Consumption during Over Discharge	I_{OPED}	V1 = V2 = V3 = V4 = 2.3V	--	2.0	4.0	uA	7	4
SENSE Pin Current	I_{SENSE}	V1 = V2 = V3 = V4 = 3.5V	--	1.5	3.2	uA	8	5
VC1 Pin Current	I_{VC1}	V1 = V2 = V3 = V4 = 3.5V	-0.3	0	0.3	uA	8	5
VC2 Pin Current	I_{VC2}	V1 = V2 = V3 = V4 = 3.5V	-0.3	0	0.3	uA	8	5
VC3 Pin Current	I_{VC3}	V1 = V2 = V3 = V4 = 3.5V	-0.3	0	0.3	uA	8	5
CTL Pin "H" Current	I_{CTLH}	V1 = V2 = V3 = V4 = 3.5V, V_{CTL} = V_{DD}	1.1	1.5	1.8	uA	8	5
CTL Pin "L" Current	I_{CTLL}	V1 = V2 = V3 = V4 = 3.5V, V_{CTL} = 0V	-0.15	--	--	uA	8	5

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Current						
CO Pin Sink Current	I_{COL}	CO = 0.1V, VDD = SENSE, SENSE-VC1 = VC1-VC2 = VC2-VC3 = VC3-VSS = 3.5V	5	--	--	uA
CO Pin Source Current	I_{COH}	SENSE-VC1 or VC1-VC2 or VC2-VC3 or VC3-VSS = V_{CU}, V_{CO} = V_{COH} - 1V	1	--	--	mA
Output Voltage						
CO Pin Drive Voltage	V_{CO}	SENSE-VC1 or VC1-VC2 or VC2-VC3 or VC3-VSS = V_{CU} , VDD = 14V, I_{OH} = 0mA	6	7	9	V
		VDD = 4.3V, CTL = 0V	1.5	2.0	--	

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

Electrical Characteristics

T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Condtion	Test Circuit
DETECTION VOLTAGE								
Overcharge Detection Voltage(n = 1, 2, 3, 4)	V_{CUn}	4.20V to 4.80V, adjustable, T_A = 25°C	V_{CUn}-0.045	V_{CUn}	V_{CUn}+0.045	V	1	1
Overcharge Hysteresis Voltage(n = 1, 2, 3, 4)	V_{HCn}		V_{HCn}-0.19	-0.38	V_{HCn}+0.19	V	1	1
Overcharge Detection Voltage	V_{CU}	uP8206XXX8-AY	4.255	4.30	4.345	V	1	1
		uP8206XXX8-BY	4.305	4.35	4.395		1	1
		uP8206XXX8-CY	4.355	4.40	4.445		1	1
		uP8206XXX8-DY	4.405	4.45	4.495		1	1
		uP8206XXX8-EY	4.455	4.50	4.545		1	1
		uP8206XXX8-FY	4.505	4.55	4.595		1	1
		uP8206XXX8-GY	4.555	4.60	4.645		1	1
Overcharge Hysteresis Voltage	V_{HC}		-0.57	-0.38	-0.19	V	1	1
INPUT VOLTAGE								
Supply Voltage between VDD and VSS	V_{DSOP}		4	--	24	V	--	--
CTL Input "H" Voltage	V_{CTLH}		V_{DD}-0.95	--	--	V	6	2
CTL Input "L" Voltage	V_{CTLL}		--	--	V_{DD}-0.4	V	6	2
INPUT CURRENT								
Current Consumption during Operation	I_{OPE}	V1 = V2 = V3 = V4 = 3.5V	--	2.50	5.50	uA	7	4
Current Consumption during Over Discharge	I_{OPED}	V1 = V2 = V3 = V4 = 2.3V	--	2.00	4.10	uA	7	4
SENSE Pin Current	I_{SENSE}	V1 = V2 = V3 = V4 = 3.5V	--	1.50	3.74	uA	8	5
VC1 Pin Current	I_{VC1}	V1 = V2 = V3 = V4 = 3.5V	-0.42	0	0.42	uA	8	5
VC2 Pin Current	I_{VC2}	V1 = V2 = V3 = V4 = 3.5V	-0.42	0	0.42	uA	8	5
VC3 Pin Current	I_{VC3}	V1 = V2 = V3 = V4 = 3.5V	-0.42	0	0.42	uA	8	5
CTL Pin "H" Current	I_{CTLH}	V1 = V2 = V3 = V4 = 3.5V, V_{CTL} = V_{DD}	1.00	1.50	1.90	uA	8	5
CTL Pin "L" Current	I_{CTLL}	V1 = V2 = V3 = V4 = 3.5V, V_{CTL} = 0V	-0.18	--	--	uA	8	5

Electrical Characteristics

T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Current						
CO Pin Sink Current	I_{COL}	CO = 0.1V, VDD = SENSE, SENSE-VC1 = VC1-VC2 = VC2-VC3 = VC3-VSS = 3.5V	5.5	--	--	uA
CO Pin Source Current	I_{COH}	SENSE-VC1 or VC1-VC2 or VC2-VC3 or VC3-VSS = V_{CU}, V_{CO} = V_{COH} - 1V	1.1	--	--	mA
Output Voltage						
CO Pin Drive Voltage	V_{CO}	SENSE-VC1 or VC1-VC2 or VC2-VC3 or VC3-VSS = V_{CU} , VDD = 14V, I_{OH} = 0mA	5.94	7	9.04	V
		VDD = 4.3V, CTL = 0V	1.44	2	--	

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

Detection Delay Time

(1) uP8206PDX8-X1, uP8206ATA8-X1 (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Condition	Test Circuit
Delay Time								
Overcharge Detection Delay Time	t_{CU}		5.2	6.5	7.8	s	2	1
Overcharge Timer Reset Delay Time	t_{TR}		3.96	6.34	10.15	ms	3	1
Overcharge Release Delay Time	t_{CL}		40.65	50.78	60.94	ms	2	1
CTL Pin Response Time	t_{CTL}		--	--	2.5	ms	4	2
Transition Time to Test Mode	t_{TST}	V1 = V2 = V3 = V4 = 3.5V, V_{DD} >= V_{SENSE} + 8.5V	--	--	80	ms	5	3

(2) uP8206PDX8-X2, uP8206ATA8-X2

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Condition	Test Circuit
Delay Time								
Overcharge Detection Delay Time	t_{CU}		2.8	3.5	4.2	s	2	1
Overcharge Timer Reset Delay Time	t_{TR}		3.96	6.34	10.15	ms	3	1
Overcharge Release Delay Time	t_{CL}		1.37	1.71	2.05	ms	2	1
CTL Pin Response Time	t_{CTL}		--	--	2.5	ms	4	2
Transition Time to Test Mode	t_{TST}	V1 = V2 = V3 =V4 = 3.5V, V_{DD} >= V_{SENSE} + 8.5V	--	--	80	ms	5	3

(3) uP8206PDX8-X3, uP8206ATA8-X3

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Condition	Test Circuit
Delay Time								
Overcharge Detection Delay Time	t_{CU}		3.2	4	4.8	s	2	1
Overcharge Timer Reset Delay Time	t_{TR}		3.15	3.91	4.69	ms	3	1
Overcharge Release Delay Time	t_{CL}		25	31.25	37.5	ms	2	1
CTL Pin Response Time	t_{CTL}		--	--	2.5	ms	4	2
Transition Time to Test Mode	t_{TST}	V1 = V2 = V3 =V4 = 3.5V, V_{DD} >= V_{SENSE} + 8.5V	--	--	80	ms	5	3

Detection Delay Time

(1) uP8206PDX8-X1, uP8206ATA8-X1 (T_A = -40°C to 85°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Condition	Test Circuit
Delay Time								
Overcharge Detection Delay Time	t_{CU}		3.7	6.5	9.6	s	2	1
Overcharge Timer Reset Delay Time	t_{TR}		2	6.34	13.65	ms	3	1
Overcharge Release Delay Time	t_{CL}		36.85	50.78	65.34	ms	2	1
CTL Pin Response Time	t_{CTL}		--	--	3	ms	4	2
Transition Time to Test Mode	t_{TST}		--	--	120	ms	5	3

(2) uP8206PDX8-X2, uP8206ATA8-X2

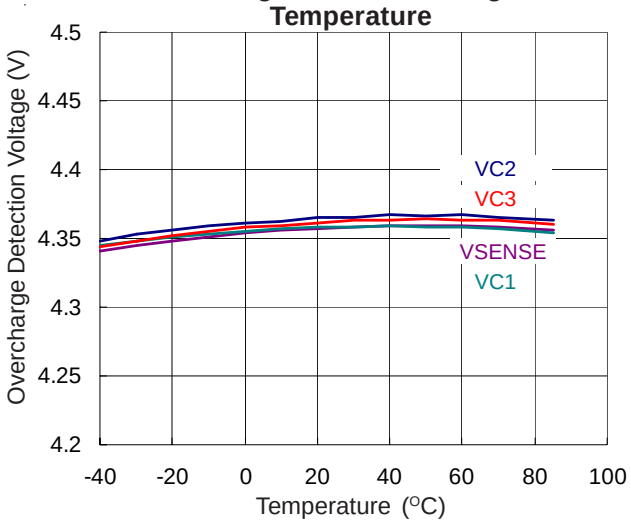
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Condition	Test Circuit
Delay Time								
Overcharge Detection Delay Time	t_{CU}		1.99	3.5	5.16	s	2	1
Overcharge Timer Reset Delay Time	t_{TR}		2	6.34	13.65	ms	3	1
Overcharge Release Delay Time	t_{CL}		1.24	1.71	2.20	ms	2	1
CTL Pin Response Time	t_{CTL}		--	--	3	ms	4	2
Transition Time to Test Mode	t_{TST}		--	--	120	ms	5	3

(3) uP8206PDX8-X3, uP8206ATA8-X3

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Test Condition	Test Circuit
Delay Time								
Overcharge Detection Delay Time	t_{CU}		2.28	4	5.89	s	2	1
Overcharge Timer Reset Delay Time	t_{TR}		1.23	3.91	8.40	ms	3	1
Overcharge Release Delay Time	t_{CL}		22.8	31.25	40	ms	2	1
CTL Pin Response Time	t_{CTL}		--	--	3	ms	4	2
Transition Time to Test Mode	t_{TST}		--	--	120	ms	5	3

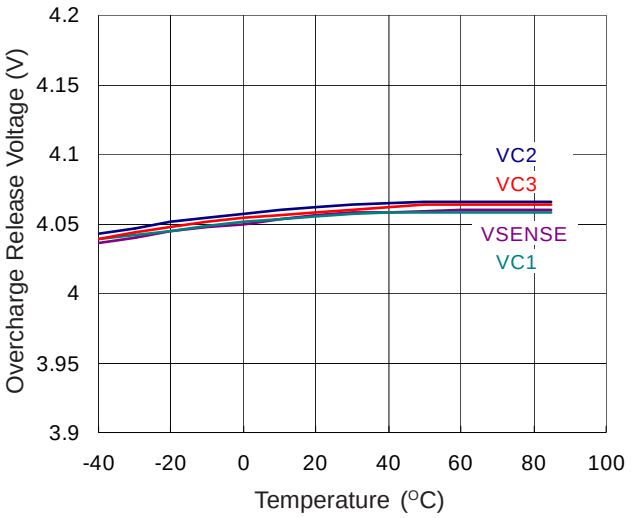
Typical Operation Characteristics

Overcharge Detection Voltage vs. Temperature



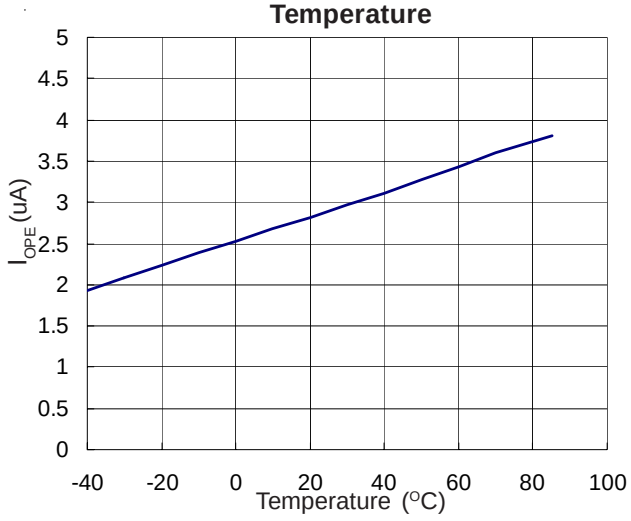
VSENSE = VC1 = VC2 = VC3 = 4.35V

Overcharge Release Voltage vs. Temperature



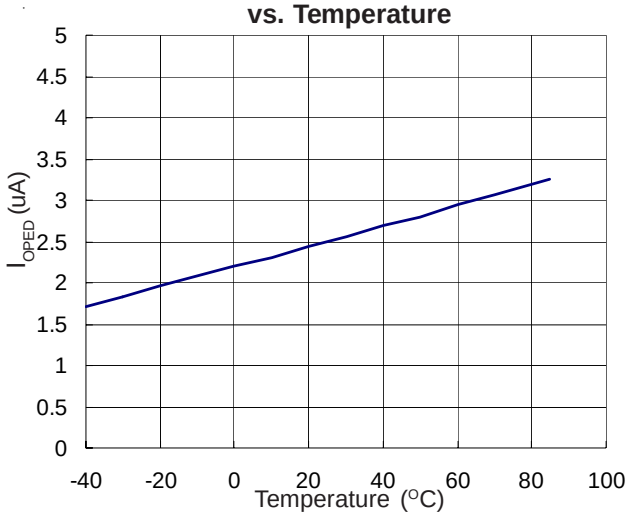
VSENSE = VC1 = VC2 = VC3 = 4.05V

Current Consumption during Operation vs. Temperature



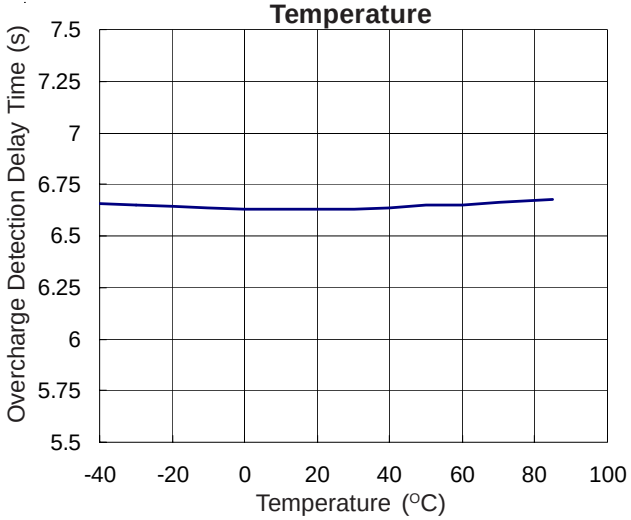
VSENSE = VC1 = VC2 = VC3 = 3.5V

Current Consumption during Over Discharge vs. Temperature



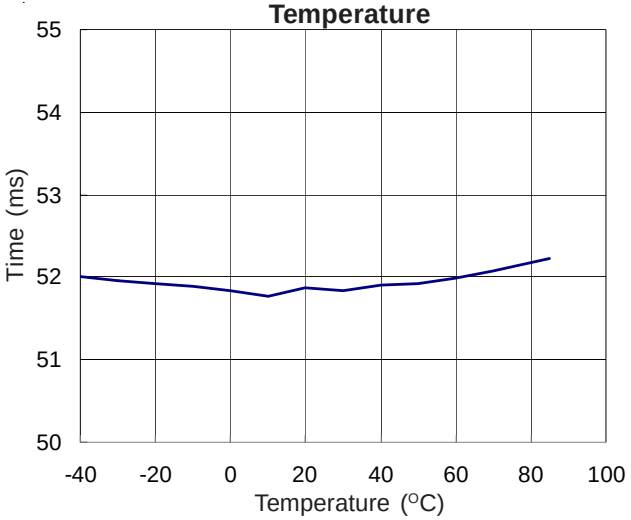
VSENSE = VC1 = VC2 = VC3 = 2.3V

Overcharge Detection Delay Time vs. Temperature



VSENSE = VC1 = VC2 = VC3 = 4.35V

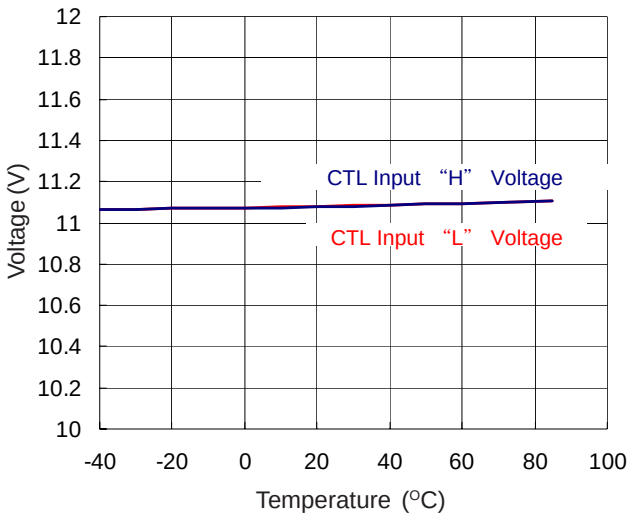
Overcharge Release Delay Time vs. Temperature



VSENSE = VC1 = VC2 = VC3 = 4.05V

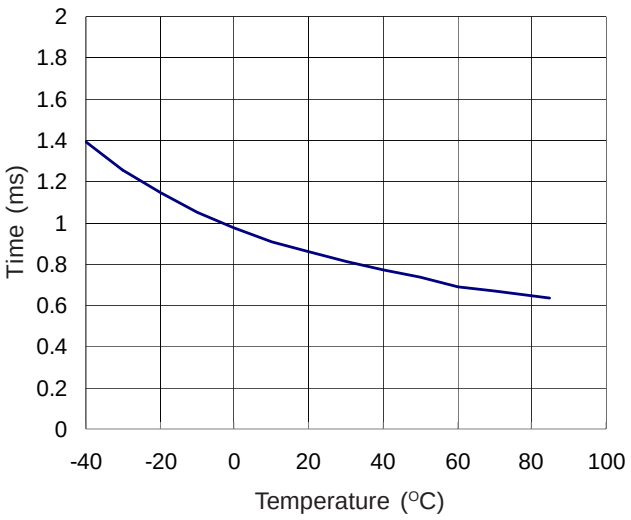
Typical Operation Characteristics

CTL Input Voltage vs. Temperature



VSENSE = VC1 = VC2 = VC3 = 3.5V, VCTL = 0V
increase and decrease

CTL Pin Response Time vs. Temperature



VSENSE = VC1 = VC2 = VC3 = 3.5V, VCTL = 14V

Battery Protection Connections

The following diagrams show the uP8206 package device in two to four cell configurations.

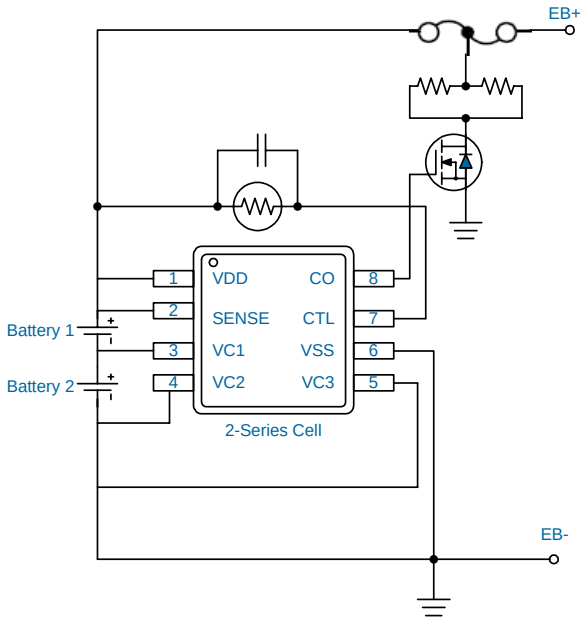


Figure 1. 2-Series Cell

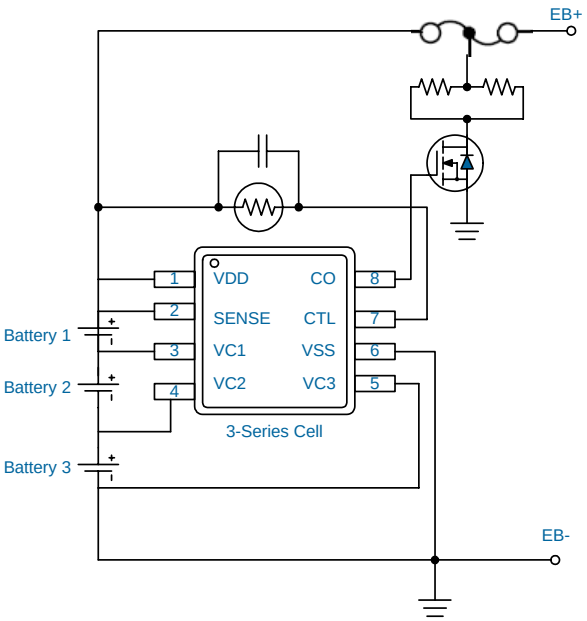


Figure 3. 3-Series Cell

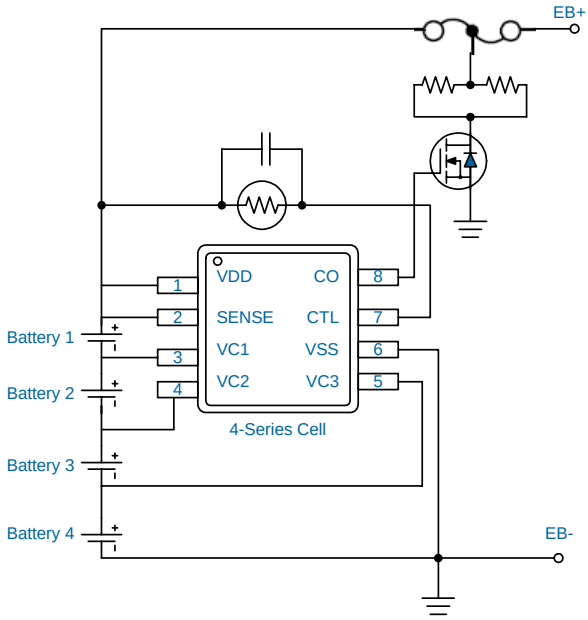
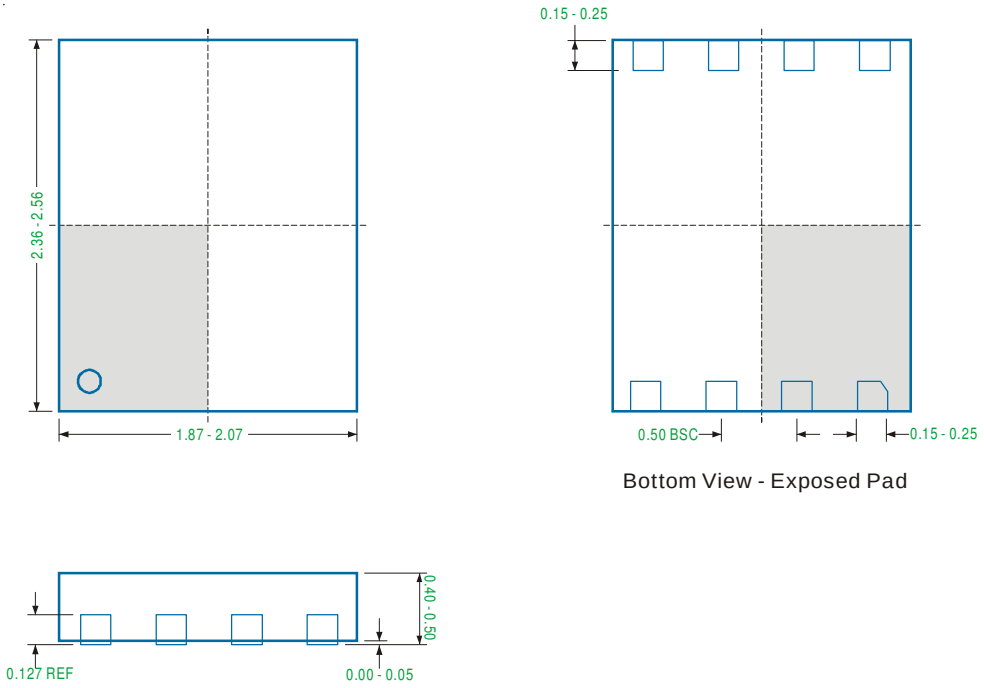


Figure 2. 4-Series Cell

Package Information

UUTDFN1.97x2.46 - 8L

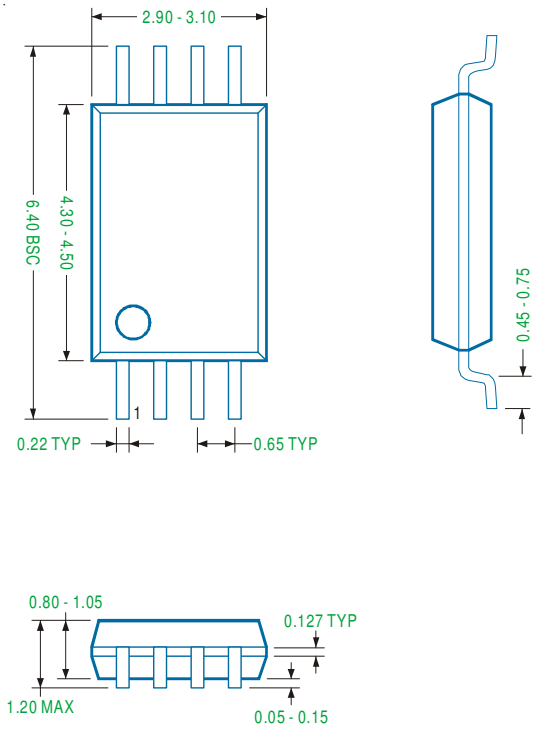


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

TSSOP - 8L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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