

**UCD4014B**

Preliminary

CMOS IC

**CMOS 8-STAGE STATIC SHIFT
REGISTERS**

■ DESCRIPTION

The **UTC UCD4014B** is a 8-stage synchronous parallel or serial input/serial output registers having common **CLOCK** and **PARALLEL/SERIAL CONTROL** inputs, a **SERIAL** data input, and individual parallel inputs to each register stage. Each register is a D-type master-slave flip-flop. Q6, Q7, and Q8 are outputs. With the positive clock line transition in the **UCD4014B** parallel/serial entry is made into the register synchronously.

In **UCD4014B** serial entry is controlled by the **PARALLEL/SERIAL CONTROL** input. When the **PARALLEL/SERIAL CONTROL** input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the **PARALLEL/SERIAL CONTROL** input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line.

■ FEATURES

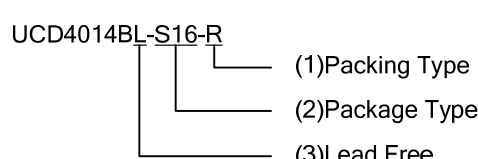
- * Up to 20V operation voltage
- * 12MHz (typ.) clock rate at 10V
- * Maximum input current of 1μA at 18V
- * Fully static operation
- * 8 master-slave flip-flops plus output buffering and control gating

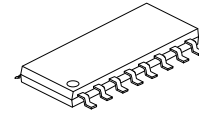
■ APPLICATIONS

- * General-purpose register
- * Parallel input/serial output data queueing
- * Parallel to serial data conversion

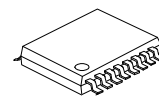
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4014BL-S16-R	UCD4014BG-S16-R	SOP-16	Tape Reel
UCD4014BL-S16-T	UCD4014BG-S16-T	SOP-16	Tube
UCD4014BL-P16-R	UCD4014BG-P16-R	TSSOP-16	Tape Reel
UCD4014BL-P16-T	UCD4014BG-P16-T	TSSOP-16	Tube

		(1) T: Tube, R: Tape Reel (2) S16: SOP-16, P16: TSSOP-16 (3) L: Lead Free, G: Halogen Free
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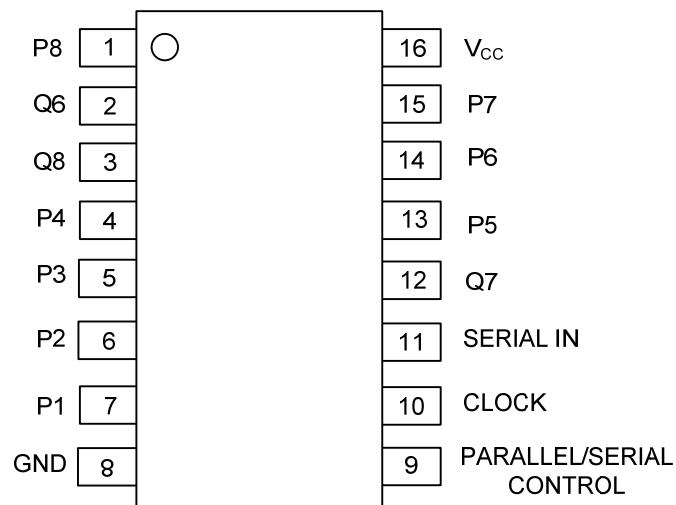


SOP-16



TSSOP-16

PIN CONFIGURATION



LOGIC DIAGRAM

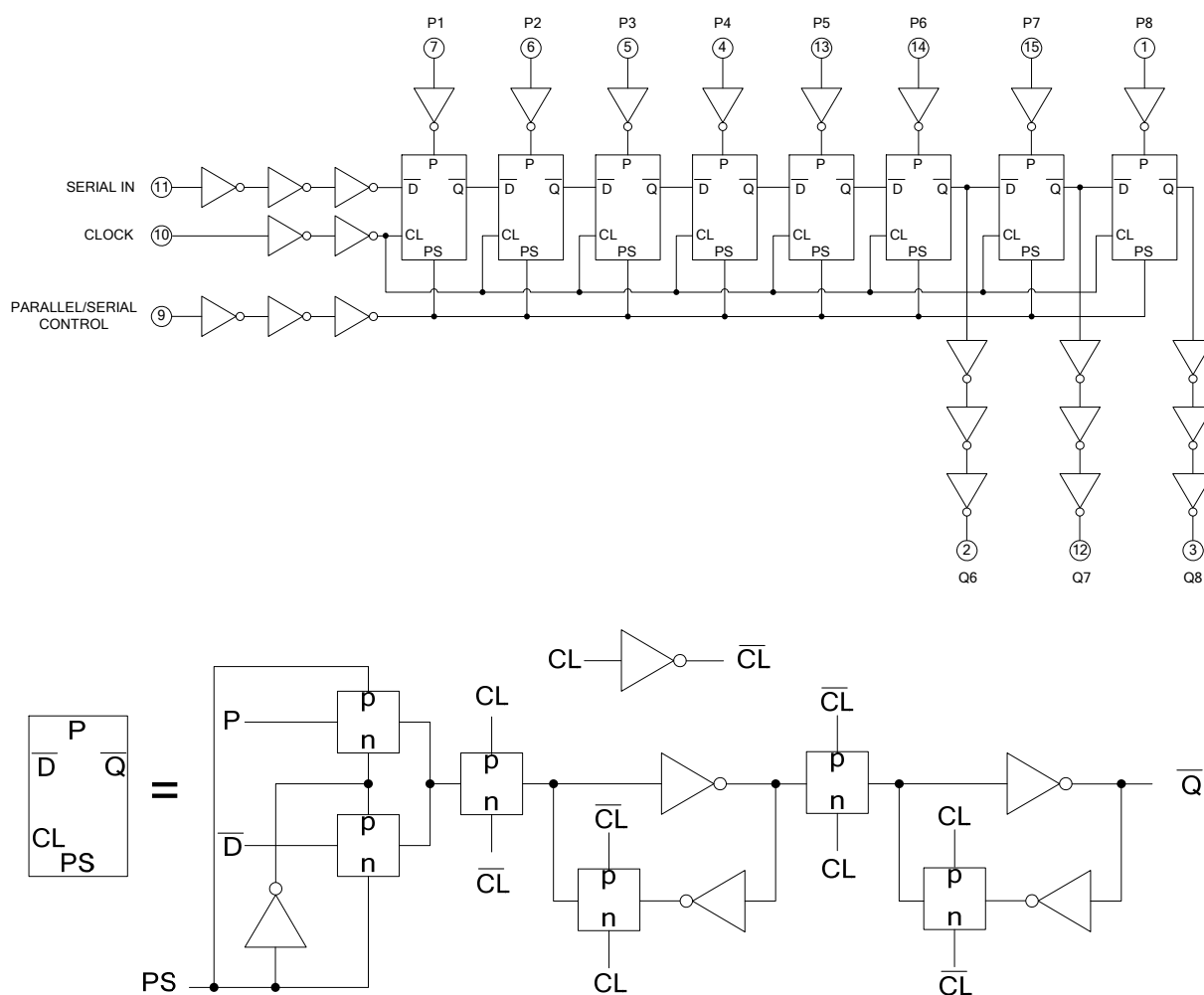


Fig.1 logic diagram

■ TRUE TABLE

CL	SER IN	PAR SER CONTROL	P ₁	P _n	Q ₁ (INTERNAL)	Q _n
	X	1	0	0	0	0
	X	1	1	0	1	0
	X	1	0	1	0	1
	X	1	1	1	1	1
	0	0	X	X	0	Q _{n-1}
	1	0	X	X	1	Q _{n-1}
	X	X	X	X	Q ₁ (NC)	Q _N (NC)

Note: X = Don't Care Case, NC = No Change

■ ABSOLUTE MAXIMUM RATING ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V _{CC}	-0.5 ~ 20	V
Input Voltage		V _{IN}	-0.5 ~ V _{CC} + 0.5	V
Output Voltage		V _{OUT}	-0.5 ~ V _{CC} + 0.5	V
Input Clamp Current (V _{IN} <0, or V _{IN} >V _{CC})		I _{IK}	±10	mA
Power Dissipation	T _A =-55°C~+100°C	P _D	500	mW
	T _A =+100°C~+125°C		200	mW
Storage Temperature		T _{STG}	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Supply Voltage	V _{CC}		3	18	V
Clock Pulse Width	t _W	V _{CC} = 5V	180	-	ns
		V _{CC} = 10V	80	-	
		V _{CC} = 15V	50	-	
Clock Frequency	f _{CL}	V _{CC} = 5V	-	3	MHz
		V _{CC} = 10V	-	6	
		V _{CC} = 15V	-	8.5	
Clock Rise and Fall Time	t _r , t _f	V _{CC} = 5V	-	15	μs
		V _{CC} = 10V	-	15	
		V _{CC} = 15V	-	15	
Set-up Time, Serial Input	t _S	V _{CC} = 5V	120	-	ns
		V _{CC} = 10V	80	-	
		V _{CC} = 15V	60	-	
Set-up Time, Parallel Input		V _{CC} = 5V	80	-	ns
		V _{CC} = 10V	50	-	
		V _{CC} = 15V	40	-	
Set-up Time, Parallel/Serial Control		V _{CC} = 5V	180	-	ns
		V _{CC} = 10V	80	-	
		V _{CC} = 15V	60	-	

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current	I_{CC}	$V_{IN}=0, 5V, V_{CC}=5V$		0.04	5	μA
		$V_{IN}=0, 10V, V_{CC}=10V$		0.04	10	
		$V_{IN}=0, 15V, V_{CC}=15V$		0.04	20	
		$V_{IN}=0, 20V, V_{CC}=20V$		0.08	100	
Output Low (Sink) Current	I_{OL}	$V_{OUT}=0.4V, V_{IN}=0.5V, V_{CC}=5V$	0.51	1		mA
		$V_{OUT}=0.5V, V_{IN}=0.10V, V_{CC}=10V$	1.3	2.6		
		$V_{OUT}=1.5V, V_{IN}=0.15V, V_{CC}=15V$	3.4	6.8		
Output High (Source) Current	I_{OH}	$V_{OUT}=4.6V, V_{IN}=0, 5V, V_{CC}=5V$	-0.51	-1		mA
		$V_{OUT}=2.5V, V_{IN}=0, 5V, V_{CC}=5V$	-1.6	-3.2		
		$V_{OUT}= 9.5V, V_{IN}=0.10V, V_{CC}=10V$	-1.3	-2.6		
		$V_{OUT}=13.5V, V_{IN}=0.15V, V_{CC}=15V$	-3.4	-6.8		
Output Voltage: Low-Level	V_{OL}	$V_{IN}=0.5V, V_{CC}=5V$		0	0.05	V
		$V_{IN}=0.10V, V_{CC}=10V$		0	0.05	
		$V_{IN}=0.15V, V_{CC}=15V$		0	0.05	

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage: High-Level	V_{OH}	$V_{IN} = 0, 5V, V_{CC} = 5V$	4.95	5		V
		$V_{IN} = 0, 10V, V_{CC} = 10V$	9.95	10		
		$V_{IN} = 0, 15V, V_{CC} = 15V$	14.95	15		
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5, 4.5V, V_{CC} = 5V$			1.5	V
		$V_{OUT} = 1, 9V, V_{CC} = 10V$			3	
		$V_{OUT} = 1.5, 13.5V, V_{CC} = 15V$			4	
Input High Voltage	V_{IH}	$V_{OUT} = 0.5, 4.5V, V_{CC} = 5V$	3.5			V
		$V_{OUT} = 1, 9V, V_{CC} = 10V$	7			
		$V_{OUT} = 1.5, 13.5V, V_{CC} = 15V$	11			
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN} = 0, 18V, V_{CC} = 18V$		$\pm 10^{-5}$	± 0.1	μA

■ SWITCHING CHARACTERISTICS ($T_A = 25^\circ C$, Input $t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 200K\Omega$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	t_{PLH} / t_{PHL}	$V_{CC}=5V$		160	320	ns
		$V_{CC}=10V$		80	160	
		$V_{CC}=15V$		60	120	
Transition Time	t_{THL} / t_{TLH}	$V_{CC}=5V$		100	200	ns
		$V_{CC}=10V$		50	100	
		$V_{CC}=15V$		40	80	
Maximum Clock Input Frequency	f_{CL}	$V_{CC}=5V$	3	6		MHz
		$V_{CC}=10V$	6	12		
		$V_{CC}=15V$	8.5	17		
Minimum Clock Pulse Width	t_W	$V_{CC}=5V$		90	180	ns
		$V_{CC}=10V$		40	80	
		$V_{CC}=15V$		25	50	
Clock Rise and Fall Time	t_r / t_f	$V_{CC}=5V$			15	μs
		$V_{CC}=10V$			15	
		$V_{CC}=15V$			15	
Minimum Setup Time, Serial Inputs	t_S	$V_{CC}=5V$		60	120	ns
		$V_{CC}=10V$		40	80	
		$V_{CC}=15V$		30	60	
Minimum Setup Time, Parallel Inputs	t_S	$V_{CC}=5V$		40	80	ns
		$V_{CC}=10V$		25	50	
		$V_{CC}=15V$		20	40	
Minimum Hold Time, Serial In, Parallel In, Parallel/Serial Control	t_H	$V_{CC}=5V$			0	ns
		$V_{CC}=10V$			0	
		$V_{CC}=15V$			0	
Average Input Capacitance	C_i	Any Input		5	7.5	pF

■ TEST CIRCUITS AND WAVEFORMS

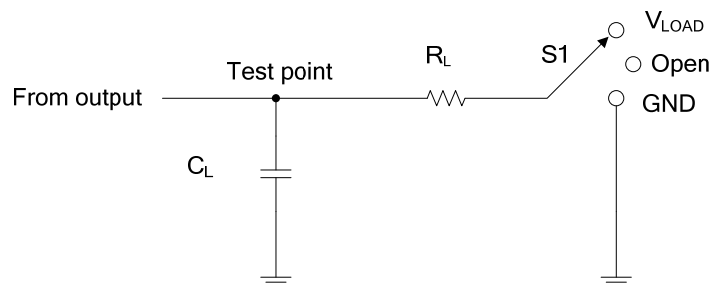


Fig 1. Test Circuit

Test	S1
t_{PLH}/t_{PHL}	GND

Inputs		V_M	V_{LOAD}	C_L	R_L
V_{IN}	t_r, t_f	$V_{CC}/2$	V_{CC}	50 pF	200 K Ω
V_{CC}	20 ns				

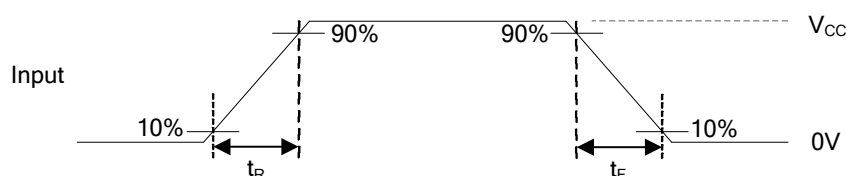


Fig 2. Voltage Waveforms Input Rise and Fall Times

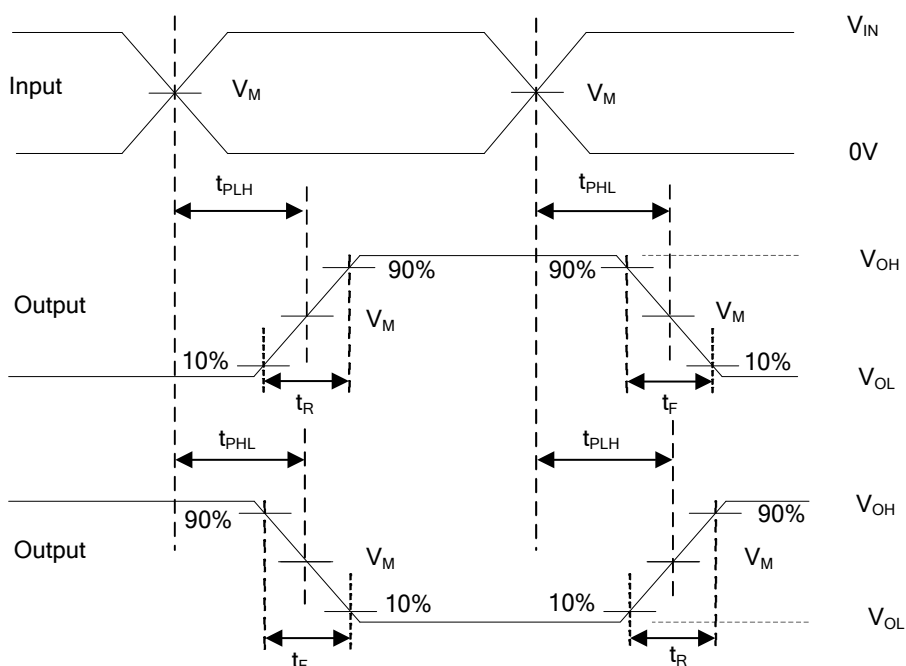


Fig 3. Voltage Waveforms Propagation Delay and Output Transition Times

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\Omega$.

■ TEST CIRCUITS AND WAVEFORMS(Cont.)

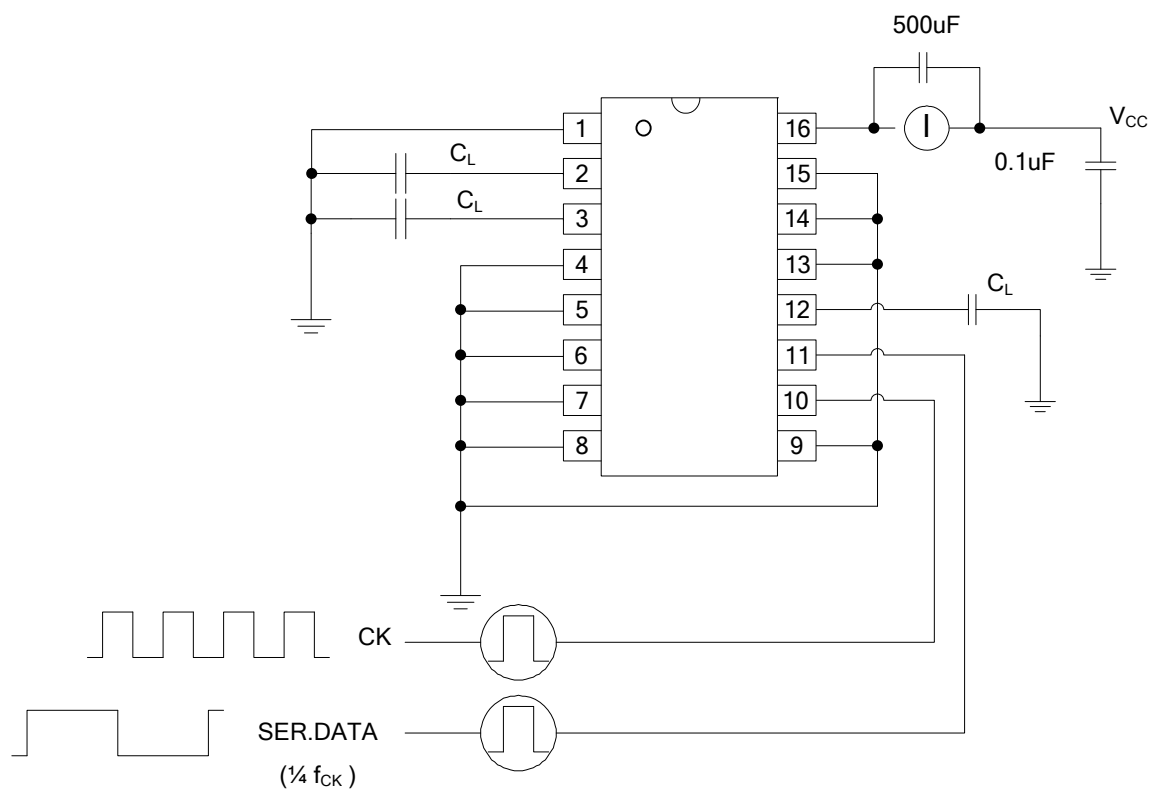


Fig 4. Dynamic power dissipation test circuit

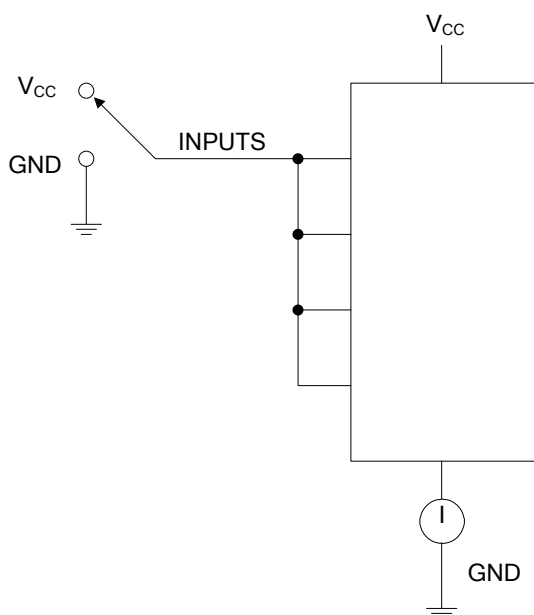


Fig 5. Quiescent device current test circuit

■ TEST CIRCUITS AND WAVEFORMS(Cont.)

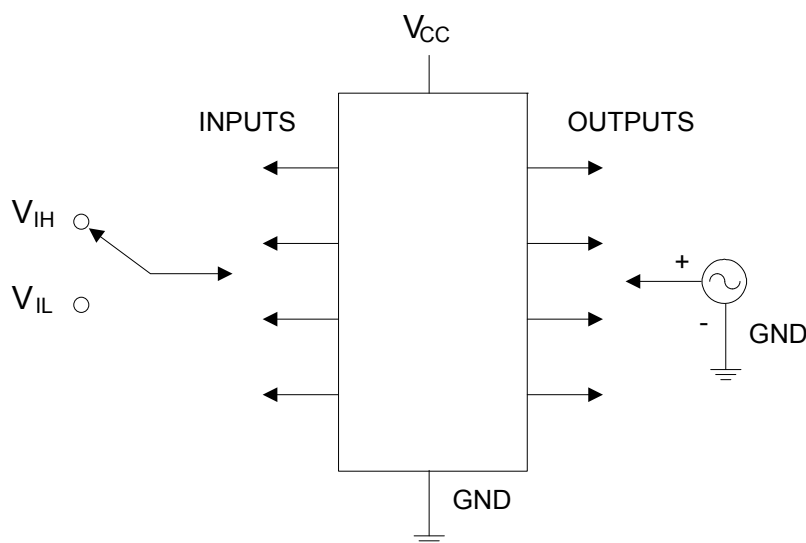


Fig 6. Input voltage test circuit

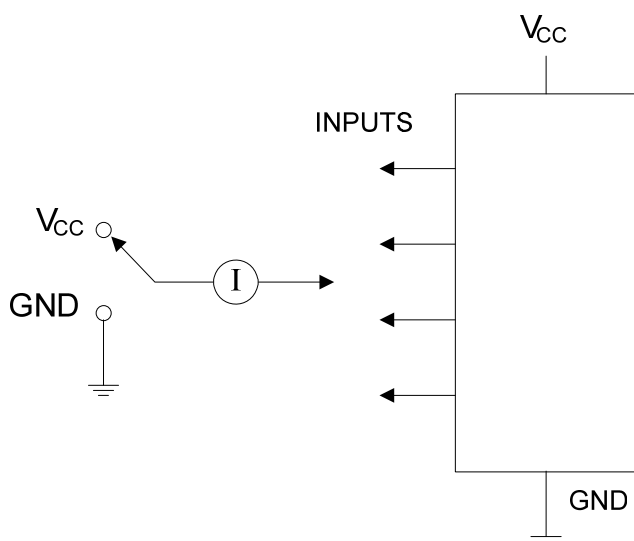


Fig 7. Input current test circuit

Note: measure inputs sequentially, to both V_{CC} and GND; connect all unused inputs to either V_{CC} or GND.

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