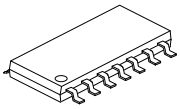
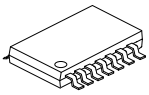
UCD40106B **Preliminary** ***CMOS IC***

HEX SCHMITT TRIGGERS



SOP-14



TSSOP-14

■ DESCRIPTION

The **UCD40106B** is a high speed Si-gate CMOS device which contains six independent Schmitt-trigger inverters and they perform the function $Y=\overline{A}$.

The device have different input threshold levels for positive-going (V_{T+}) and negative-going(V_{T-}) signals because of the Schmitt-trigger action in the input.

■ FEATURES

* High voltage type (20V rating)
* All inputs have Schmitt-trigger action
* Hysteresis Voltage(TYP): 0.9V at V_{CC}=5V
  2.3V at V_{CC}=10V
  3.5V at V_{CC}=15V
* Wide supply voltage range from 3V to 18V
* Inputs are TTL-Voltage compatible
* Noise immunity greater than 50%

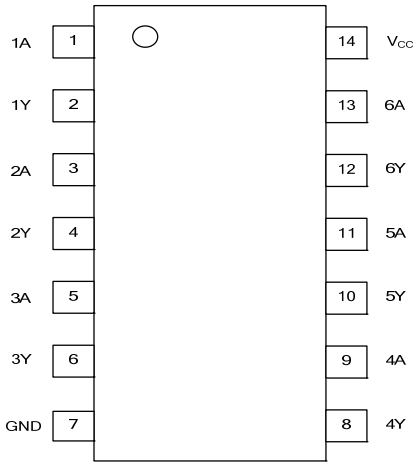
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD40106BL-S14-R	UCD40106BG-S14-R	SOP-14	Tape Reel
UCD40106BL-S14-T	UCD40106BG-S14-T	SOP-14	Tube
UCD40106BL-P14-R	UCD40106BG-P14-R	TSSOP-14	Tape Reel
UCD40106BL-P14-T	UCD40106BG-P14-T	TSSOP-14	Tube

UCD40106BG-S14-T
(1)Packing Type
(2)Package Type
(3)Halogen Free

(1) T: Tube, R: Tape Reel
(2) S14: SOP-14, P14: TSSOP-14
(3) L: Lead Free, G: Halogen Free

■ PIN CONFIGURATION

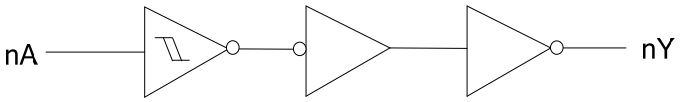


■ FUNCTION TABLE (each gate)

INPUT	OUTPUT
A	Y
L	H
H	L

Note: H: HIGH voltage level; L: LOW voltage level

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A =25°C, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 20	V
Input Voltage	V_{IN}	-0.5~ V_{CC}+0.5	V
DC Input Current, Any One Input	I_{IN}	±10	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	3		18	V
Input Voltage	V_{IN}		0		V_{CC}	V
Operating Temperature	T_{OPR}		-40		+85	°C

■ STATIC CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V_{T+}	V_{CC}=5V	2.2	2.9	3.6	V
		V_{CC}=10V	4.6	5.9	7.1	
		V_{CC}=15V	6.6	8.8	10.8	
Negative-Going Input Threshold Voltage	V_{T-}	V_{CC}=5V	0.9	1.9	2.8	V
		V_{CC}=10V	2.5	3.9	5.2	
		V_{CC}=15V	4.0.	5.8	7.4	
Hysteresis Voltage (V_{T+}-V_{T-}) (see figure 3)	ΔV_T	V_{CC}=5V	0.3	0.9	1.6	V
		V_{CC}=10V	1.2	2.3	3.6	
		V_{CC}=15V	1.6	3.5	5.0	
High-Level Output Voltage	V_{OH}	V_{CC}=5V, $\|I_O\|$ <1uA	4.95	5		V
		V_{CC}=10V, $\|I_O\|$ <1uA	9.95	10		
		V_{CC}=15V, $\|I_O\|$ <1uA	14.95	15		
Low-Level Output Voltage	V_{OL}	V_{CC}=5V, $\|I_O\|$ <1uA		0	0.05	V
		V_{CC}=10V, $\|I_O\|$ <1uA		0	0.05	
		V_{CC}=15V, $\|I_O\|$ <1uA		0	0.05	
High-level Output Current	I_{OH}	V_{CC}=5V, V_O=4.6V	-0.51	-1		mA
		V_{CC}=5V, V_O=2.5V	-1.6	-3.2		
		V_{CC}=10V, V_O=9.5V	-1.3	-2.6		
		V_{CC}=15V, V_O=13.5V	-3.4	-6.8		
Low-level Output Current	I_{OL}	V_{CC}=5V, V_O=0.4V	0.51	1.0		mA
		V_{CC}=10V, V_O=0.5V	1.3	2.6		
		V_{CC}=15V, V_O=1.5V	3.4	6.8		
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=18V, V_{IN}=V_{CC} or GND		±0.01	±100	nA
Quiescent Supply Current	I_{DD}	V_{CC}=5V, V_{IN}= V_{CC} or GND, I_{OUT}=0		0.02	1	uA
		V_{CC}=10V, V_{IN}= V_{CC} or GND, I_{OUT}=0		0.02	2	
		V_{CC}=15V, V_{IN}= V_{CC} or GND, I_{OUT}=0		0.02	4	
		V_{CC}=20V, V_{IN}= V_{CC} or GND, I_{OUT}=0		0.04	20	

■ DYNAMIC CHARACTERISTICS (T_A =25°C, unless otherwise specified; Input: t_R, t_F=20ns)

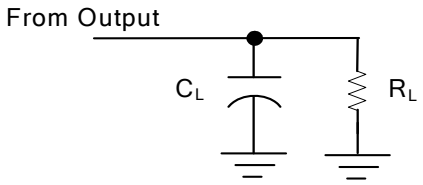
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH}/t_{PHL}	V_{CC}=5V, C_L=50Pf, R_L=200KΩ		140	280	ns
		V_{CC}=10V, C_L=50Pf, R_L=200KΩ		70	140	
		V_{CC}=15V, C_L=50Pf, R_L=200KΩ		60	120	
Output Transition Time	t_{TLH}/t_{THL}	V_{CC}=5V, C_L=50Pf, R_L=200KΩ		100	200	ns
		V_{CC}=10V, C_L=50Pf, R_L=200KΩ		50	100	
		V_{CC}=15V, C_L=50Pf, R_L=200KΩ		40	80	

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		5	7.5	pF
Power Dissipation Capacitance	C_{PD}	Any Gate		14		pF

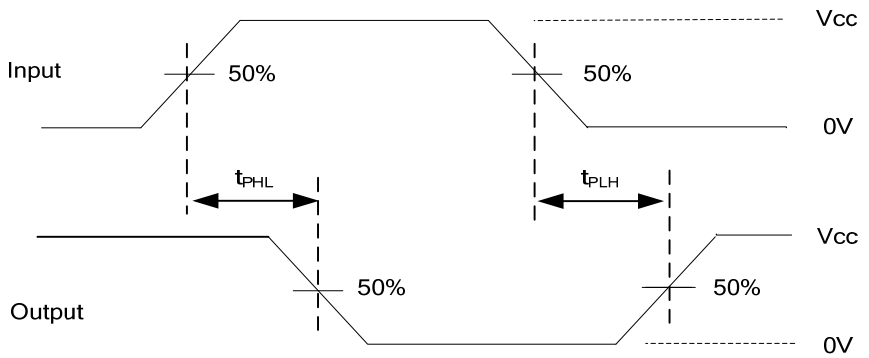
■ TEST CIRCUIT AND WAVEFORMS



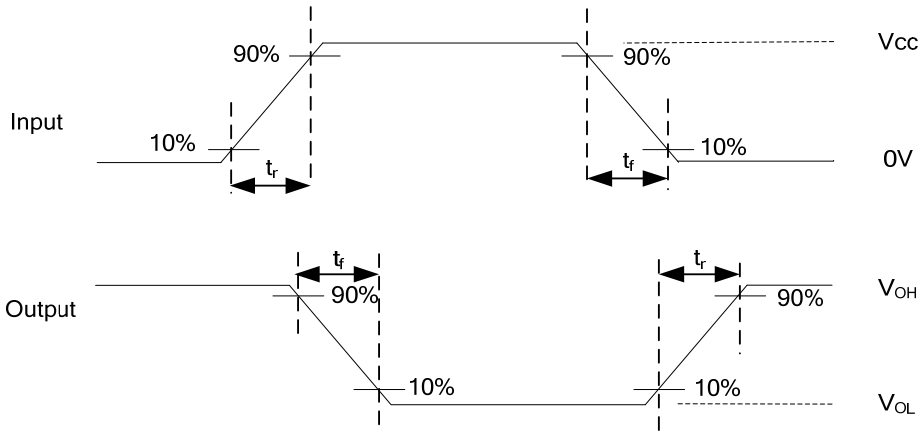
TEST CIRCUIT

Note: C_L includes probe and jig capacitance.

Fig. 1 Load circuitry for switching times.



PROPAGATION DELAY TIMES



Output Transition Time

Fig. 2 Propagation delay from input(A) to output(Y) and Output transition time.

■ TEST CIRCUIT AND WAVEFORMS(Cont.)

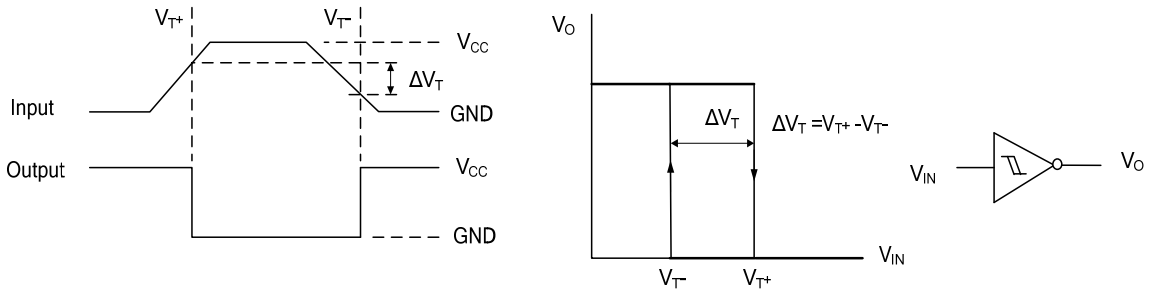


Fig. 3 Hysteresis definition, characteristics, and test setup