UCC2720xA 120-V Boot, 3-A Peak, High-Frequency, High-Side and Low-Side Driver

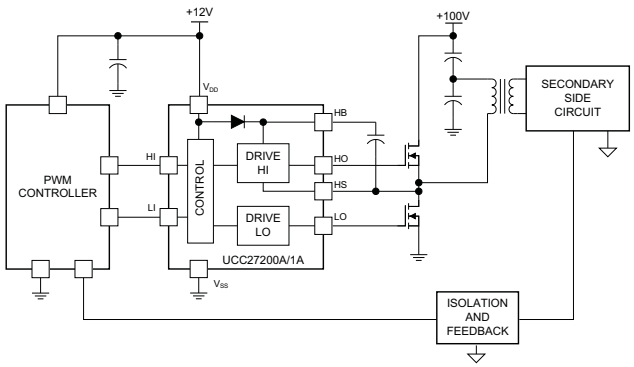
1 Features

- Drives Two N-Channel MOSFETs in High-Side and Low-Side Configuration
- Negative Voltage Handling on HS (–18V)
- Maximum Boot Voltage 120 V
- Maximum VDD Voltage 20 V
- On-Chip 0.65-V VF, 0.6-Ω RD Bootstrap Diode
- Greater than 1 MHz of Operation
- 20-ns Propagation Delay Times
- 3-A Sink, 3-A Source Output Currents
- 8-ns Rise/7-ns Fall Time with 1000-pF Load
- 1-ns Delay Matching
- Undervoltage Lockout for High-Side and Low-Side Driver
- Offered in 8-Pin SOIC (D), PowerPAD™ SOIC-8 (DDA), SON-8 (DRM), SON-9 (DRC) and SON-10 (DPR) Packages
- Specified from –40°C to 140°C

2 Applications

- Power Supplies for Telecom, Datacom, and Merchant Markets
- Half-Bridge Applications and Full-Bridge Converters
- Isolated Bus Architecture
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- High-Voltage Synchronous-Buck Converters
- Class-D Audio Amplifiers

Simplified Application Diagram



3 Description

The UCC2720xA family of high-frequency N-channel MOSFET drivers include a 120-V bootstrap diode and high-side/low-side driver with independent inputs for maximum control flexibility. This allows for N-channel MOSFET control in half-bridge, full-bridge, two-switch forward and active clamp forward converters. The low-side and the high-side gate drivers are independently controlled and matched to 1-ns between the turn-on and turn-off of each other. The UCC2720xA are based on the popular UCC27200/1 drivers, but offer some enhancements. In order to improve performance in noisy power supply environments the UCC2720xA has an enhanced ESD input structure and also has the ability to withstand a maximum of –18 V on its HS pin.

An on-chip bootstrap diode eliminates the external discrete diodes. Under-voltage lockout is provided for both the high-side and the low-side drivers forcing the outputs low if the drive voltage is below the specified threshold.

Two versions of the UCC27200A are offered. The UCC27200A has high-noise immune CMOS input thresholds while the UCC27201A has TTL-compatible thresholds.

Both devices are offered in an 8-pin SOIC (D), PowerPad SOIC-8 (DDA), SON-8 (DRM) package, a 9-pin SON-9 (DRC) package and a 10-pin SON-10 (DPR) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27200A, UCC27201A	SOIC (8)	4.90 mm × 3.91 mm
	HSOP (8)	4.89 mm × 3.90 mm
	VSON (9)	3.00 mm × 3.00 mm
	VSON (8)	4.00 mm × 4.00 mm
UCC27201A	WSON (10)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2011) to Revision B — **Page**

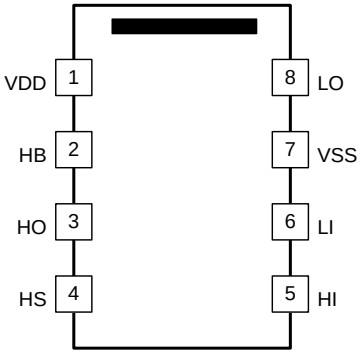
- Added Negative Voltage Handling on HS (–18 V) to Features List ... 1
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (February 2011) to Revision A — **Page**

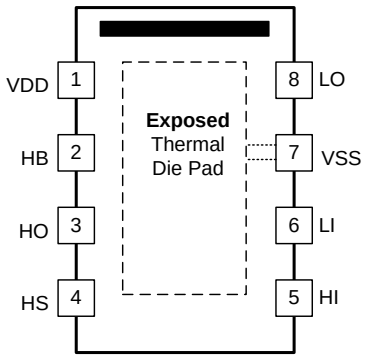
- Added SON-10 (DPR) Package to the List of FEATURES ... 1
- Added SON-10 (DPR) Package to the DESCRIPTION ... 1
- Changed the PIN FUNCTIONS table ... 4
- Added Additional PIN FUNCTIONS information ... 4
- Added ordering information for the SON-10 (DPR) ... 5
- Added note, "DPR(SON-10) package comes either in a small reel of 250 pieces as part number UCC27200ADPRT, or large reels pieces as part number UCC27200ADPRR." ... 5
- Added the SON-10 package to the ORDERING INFORMATION table ... 5
- Added the SON-10 package to the THERMAL INFORMATION table ... 5
- Changed the "Minimum input pulse width" value From: 50 ns Max To: 50 ns Typ ... 7

5 Pin Configuration and Functions

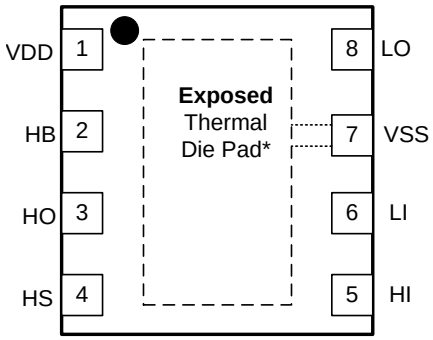
D Package
8-Pin SOIC
Top View



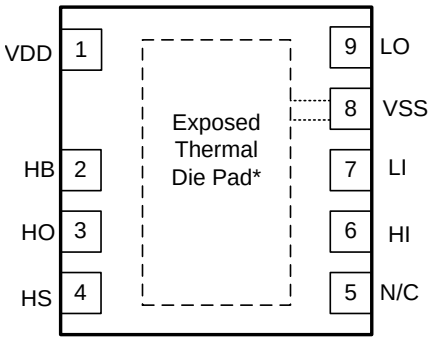
DDA Package
8-Pin SOIC With Exposed PowerPAD
Top View



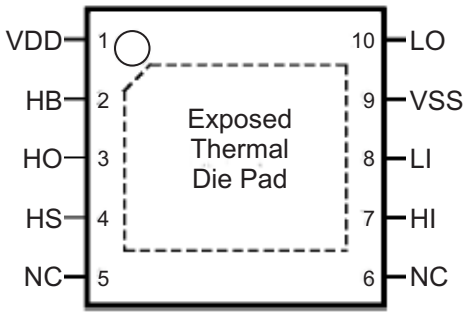
DRM Package
8-Pin SON
Top View



DRC Package
9-Pin SON
Top View



DPR Package
10-Pin SON
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DRM/D/DDA	DRC	DPR		
VDD	1	1	1	I	Positive supply to the lower gate driver. De-couple this pin to VSS (GND). Typical decoupling capacitor range is 0.22 µF to 1.0 µF.
HB	2	2	2	I	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF, the value is dependant on the gate charge of the high-side MOSFET however.
HO	3	3	3	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	4	4	I	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	5	6	7	I	High-side input.
LI	6	7	8	I	Low-side input.
VSS	7	8	9	O	Negative supply terminal for the device which is generally grounded.
LO	8	9	10	O	Low-side output. Connect to the gate of the low-side power MOSFET.
N/C	—	5	5/6	—	No connection. Pins labeled N/C have no connection.
PowerPAD(1)	—	—	—	—	Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) Pin VSS and the exposed thermal die pad are internally connected on the DDA and DRM packages only. Electrically referenced to VSS (GND).

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature, unless noted, all voltages are with respect to V_{SS} (1)

		MIN	MAX	UNIT
Supply voltage range, (2) V_{DD}		–0.3	20	V
Input voltages on LI and HI, V_{LI}, V_{HI}		–0.3	20	V
Output voltage on LO, V_{LO}	DC	–0.3	V_{DD} + 0.3	V
	Repetitive pulse <100 ns (3)	–2	V_{DD} + 0.3	
Output voltage on HO, V_{HO}	DC	V_{HS} – 0.3	V_{HB} + 0.3	V
	Repetitive pulse <100 ns (3)	V_{HS} – 2	V_{HB} + 0.3, (V_{HB} - V_{HS} <20)	
Voltage on HS, V_{HS}	DC	–1	120	V
	Repetitive pulse <100 ns (3)	–18	120	
Voltage on HB, V_{HB}		–0.3	120	V
Voltage On HB-HS		–0.3	120	V
Operating virtual junction temperature range, T_J		–40	150	°C
Lead temperature (soldering, 10 sec.)			300	°C
Power dissipation at T_A = 25°C (D package) (4)			1.3	W
Power dissipation at T_A = 25°C (DDA package) (4)			2.7	W
Power dissipation at T_A = 25°C (DRM package) (4)			3.3	W
Power dissipation at T_A = 25°C (DRC package) (4)			2.86	W
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to V_{ss}. Currents are positive into, negative out of the specified terminal.
(3) Values are verified by characterization and are not production tested.
(4) This data was taken using the JEDEC proposed high-K test PCB. See the THERMAL CHARACTERISTICS section for details.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	8	12	17	V
V_{HS}	Voltage on HS	–1		105	V
	Voltage on HS, (repetitive pulse <100 ns)	–15		110	V
V_{HB}	Voltage on HB	V_{HS} + 8, V_{DD} –1		V_{HS} + 17, 115	V
	Voltage slew rate on HS			50	V / ns
T_J	Operating junction temperature range	–40		140	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC27200A /UCC27201A	UCC27200A /UCC27201A	UCC27200A /UCC27201A	UCC27200A /UCC27201A	UCC27200A /UCC27201A	UNIT
		DRM (VSON)	DRC (VSON)	DPR (WSON)	D (SOIC)	DDA (HSOP)	
		8 PINS	9 PINS	10 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.2	43.7	34.8	106.5	40.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.6	49.9	32.1	52.9	49	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.2	19.1	11.9	46.6	10.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.6	0.2	9.6	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.4	19.3	12.2	46.1	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	3.8	1.3	—	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range, $V_{DD} = V_{HB} = 12$ V, $V_{HS} = V_{SS} = 0$ V, No load on LO or HO, $T_A = T_J = –40°C$ to +140°C, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I_{DD}	VDD quiescent current		$V_{LI} = V_{HI} = 0$		0.4	0.8	mA
I_{DDO}	VDD operating current	UCC27200A	f = 500 kHz, $C_{LOAD} = 0$		2.5	4	mA
		UCC27201A	f = 500 kHz, $C_{LOAD} = 0$		3.8	5.5	
I_{HB}	Boot voltage quiescent current		$V_{LI} = V_{HI} = 0$ V		0.4	0.8	mA
I_{HBO}	Boot voltage operating current		f = 500 kHz, $C_{LOAD} = 0$		2.5	4	mA
I_{HBS}	HB to V_{SS} quiescent current		$V_{HS} = V_{HB} = 110$ V		0.0005	1	uA
I_{HBSO}	HB to V_{SS} operating current		f = 500 kHz, $C_{LOAD} = 0$		0.1		mA
INPUT							
V_{HIT}	Input rising threshold		UCC27200A		5.8	8	V
V_{LIT}	Input falling threshold		UCC27200A	3	5.4		V
V_{IHYS}	Input voltage hysteresis		UCC27200A		0.4		V
V_{HIT}	Input voltage threshold		UCC27201A		1.7	2.5	V
V_{LIT}	Input voltage threshold		UCC27201A	0.8	1.6		V
V_{IHYS}	Input voltage Hysteresis		UCC27201A		100		mV
R_{IN}	Input pulldown resistance		UCC27201A	100	200	350	kΩ
UNDERVOLTAGE PROTECTION (UVLO)							
	VDD rising threshold			6.2	7.1	7.8	V
	VDD threshold hysteresis				0.5		V
	VHB rising threshold			5.8	6.7	7.2	V
	VHB threshold hysteresis				0.4		V
BOOTSTRAP DIODE							
V_F	Low-current forward voltage		I_{VDD} - HB = 100 µA		0.65	0.85	V
V_{FI}	High-current forward voltage		I_{VDD} - HB = 100 mA		0.85	1.1	V
R_D	Dynamic resistance, ΔVF/ΔI		I_{VDD} - HB = 100 mA and 80 mA		0.6	1.0	Ω

Electrical Characteristics (continued)

over operating free-air temperature range, $V_{DD} = V_{HB} = 12$ V, $V_{HS} = V_{SS} = 0$ V, No load on LO or HO, $T_A = T_J = –40°C$ to +140°C, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
LO GATE DRIVER							
V_{LOL}	Low level output voltage		I_{LO} = 100 mA		0.18	0.4	V
V_{LOH}	High level output voltage	T_J = -40 to 125°C	I_{LO} = –100 mA, $V_{LOH} = V_{DD} - V_{LO}$		0.25	0.4	V
		T_J = -40 to 140°C	I_{LO} = –100 mA, $V_{LOH} = V_{DD} - V_{LO}$		0.25	0.42	
	Peak pullup current		V_{LO} = 0 V		3		A
	Peak pulldown current		V_{LO} = 12 V		3		A
HO GATE DRIVER							
V_{HOL}	Low level output voltage		I_{HO} = 100 mA		0.18	0.4	V
V_{HOH}	High level output voltage	T_J = -40 to 125°C	I_{HO} = –100 mA, $V_{HOH} = V_{HB} - V_{HO}$		0.25	0.4	V
		T_J = -40 to 140°C	I_{HO} = –100 mA, $V_{HOH} = V_{HB} - V_{HO}$		0.25	0.42	
	Peak pullup current		V_{HO} = 0 V		3		A
	Peak pulldown current		V_{HO} = 12 V		3		A
PROPAGATION DELAYS							
t_{DLFF}	V_{LI} falling to V_{LO} falling	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	
t_{DHFF}	V_{HI} falling to V_{HO} falling	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	
t_{DLRR}	V_{LI} rising to V_{LO} rising	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	
t_{DHRR}	V_{HI} rising to V_{HO} rising	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	
DELAY MATCHING							
t_{MON}	LI ON, HI OFF				1	7	ns
t_{MOFF}	LI OFF, HI ON				1	7	ns
OUTPUT RISE AND FALL TIME							
t_R	LO, HO		C_{LOAD} = 1000 pF		8		ns
t_F	LO, HO		C_{LOAD} = 1000 pF		7		ns
t_R	LO, HO (3 V to 9 V)		C_{LOAD} = 0.1 µF		0.35	0.6	us
t_F	LO, HO (3 V to 9 V)		C_{LOAD} = 0.1 µF		0.3	0.6	us
MISCELLANEOUS							
	Minimum input pulse width that changes the output				50		ns
	Bootstrap diode turnoff time		I_F = 20 mA, I_{REV} = 0.5 A (1) (2)		20		ns

(1) Typical values for $T_A = 25°C$
(2) I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.

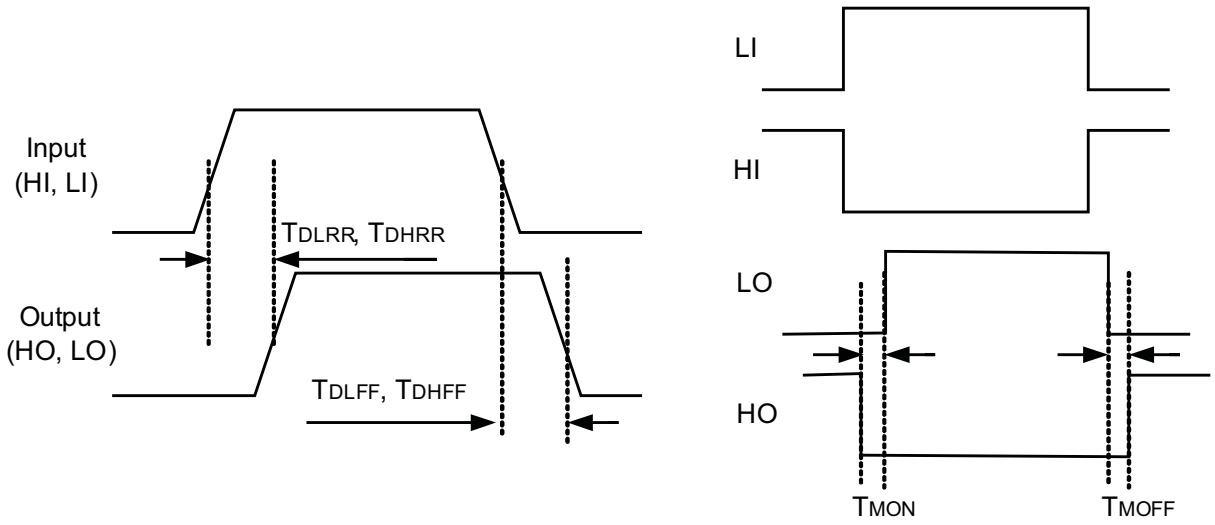


Figure 1. Timing Diagram

6.6 Typical Characteristics

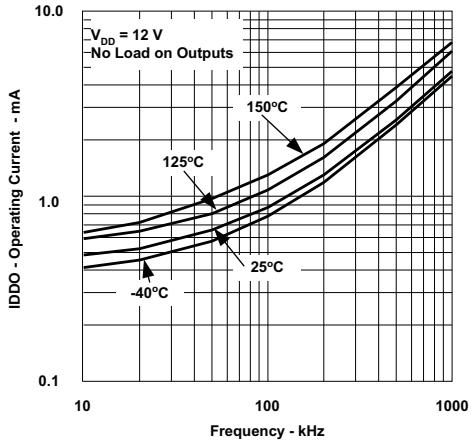


Figure 2. UCC27200A IDD Operating Current vs Frequency

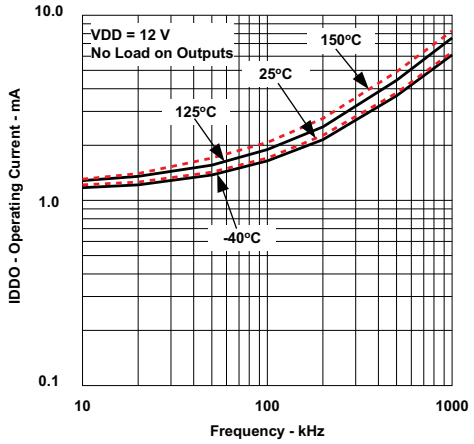


Figure 3. UCC27201A IDD Operating Current vs Frequency

Typical Characteristics (continued)

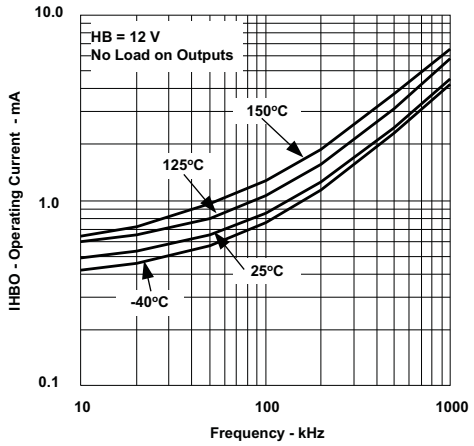


Figure 4. Boot Voltage Operating Current vs Frequency

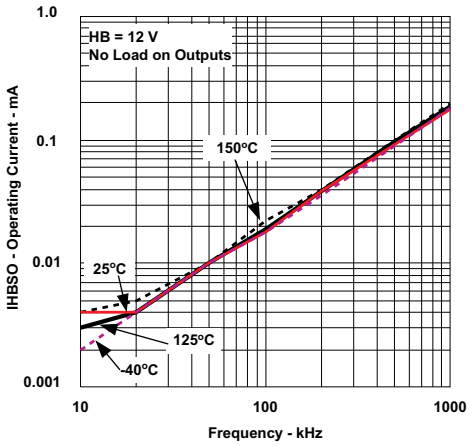


Figure 5. HB to VSS Operating Current vs Frequency

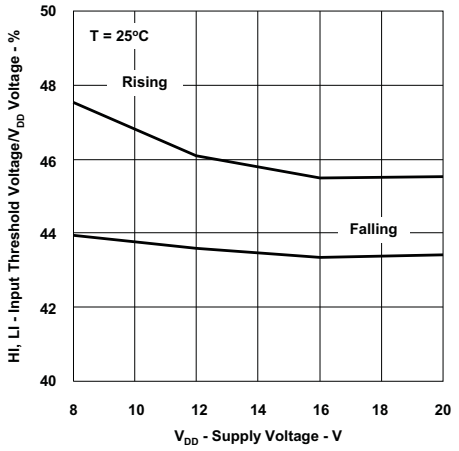


Figure 6. UCC27200A Input Threshold vs Supply Voltage

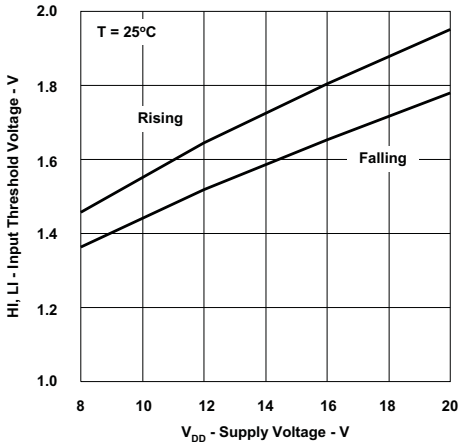


Figure 7. UCC27201A Input Threshold vs Supply Voltage

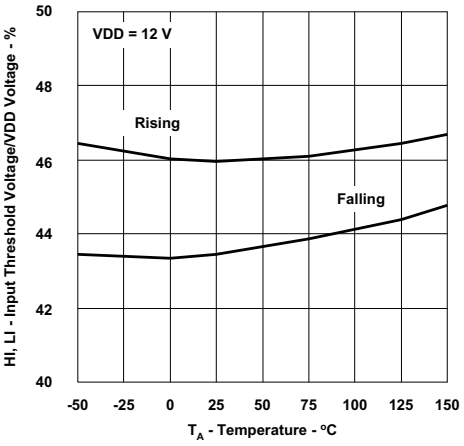


Figure 8. UCC27200A Input Threshold vs Temperature

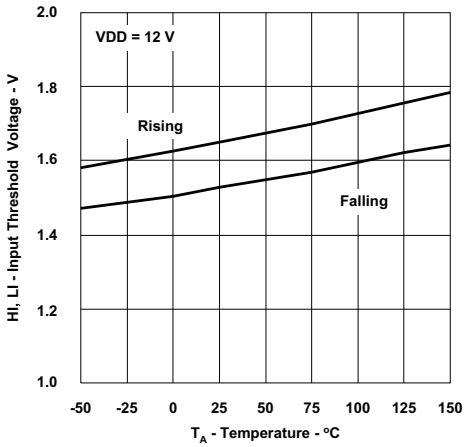


Figure 9. UCC27201A Input Threshold vs Temperature

Typical Characteristics (continued)

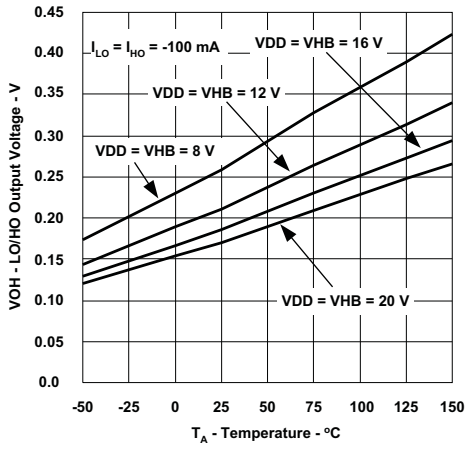


Figure 10. Lo and Ho High Level Output Voltage vs Temperature

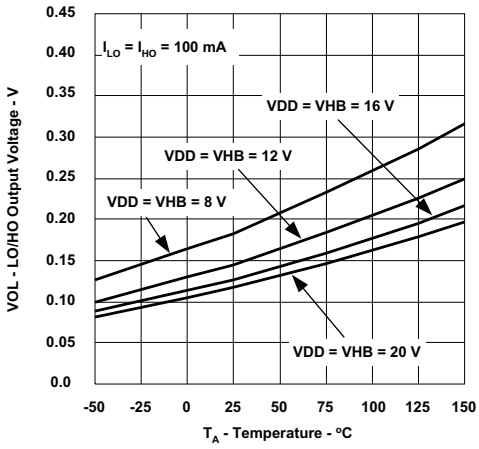


Figure 11. Lo and Ho Low Level Output Voltage vs Temperature

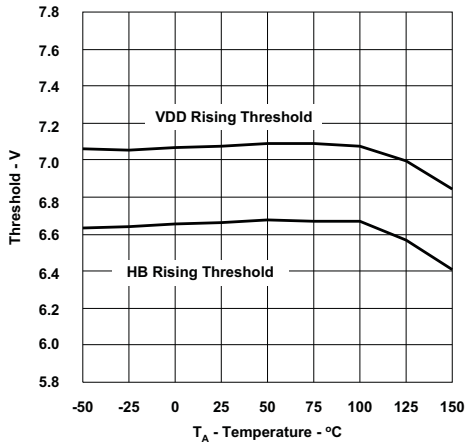


Figure 12. Undervoltage Lockout Threshold vs Temperature

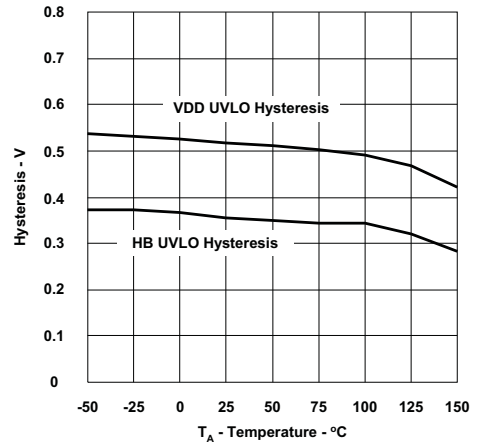


Figure 13. Undervoltage Lockout Threshold Hysteresis vs Temperature

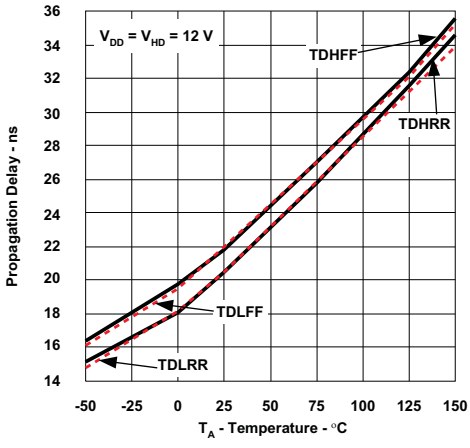


Figure 14. UCC27200A Propagation Delays vs Temperature

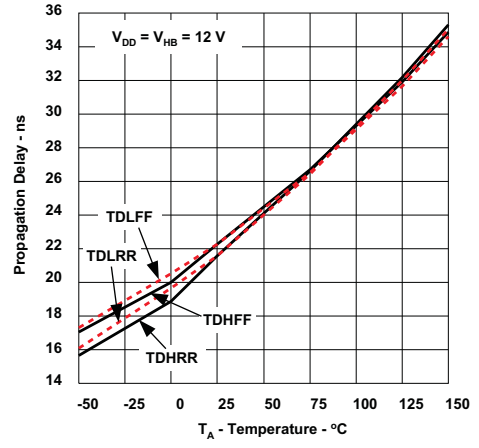


Figure 15. UCC27201A Propagation Delays vs Temperature

Typical Characteristics (continued)

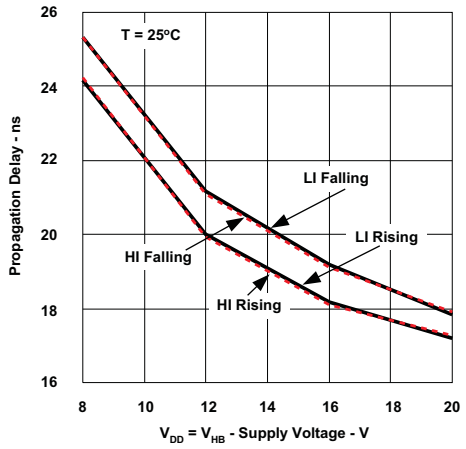


Figure 16. UCC27200A Propagation Delay vs Supply Voltage

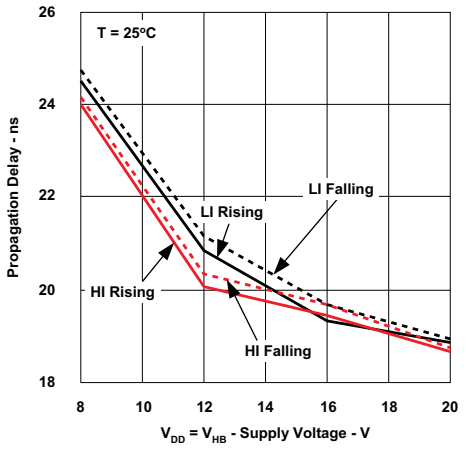


Figure 17. UCC27201A Propagation Delay vs Supply Voltage

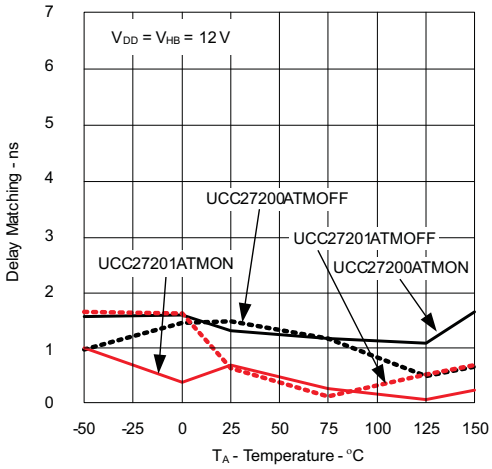


Figure 18. Delay Matching vs Temperature

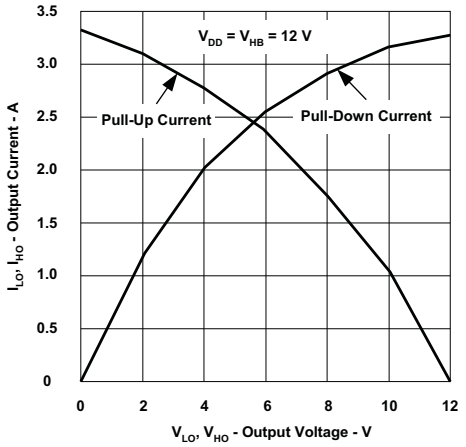


Figure 19. Output Current vs Output Voltage

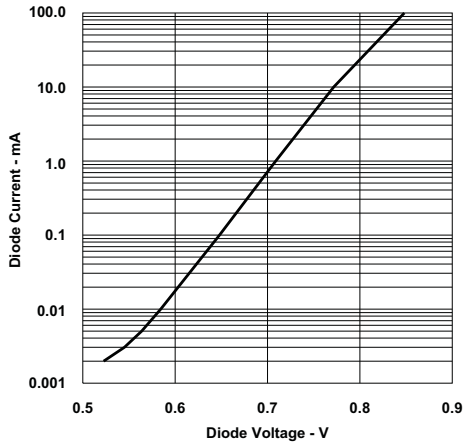


Figure 20. Diode Current vs Diode Voltage

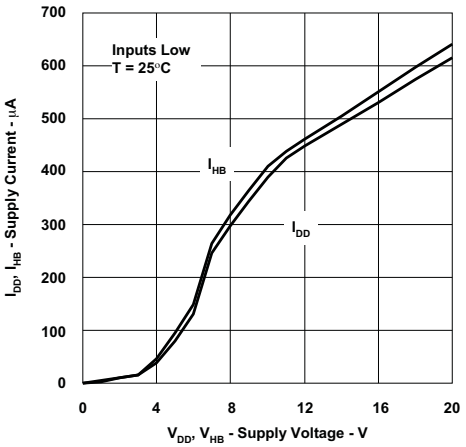


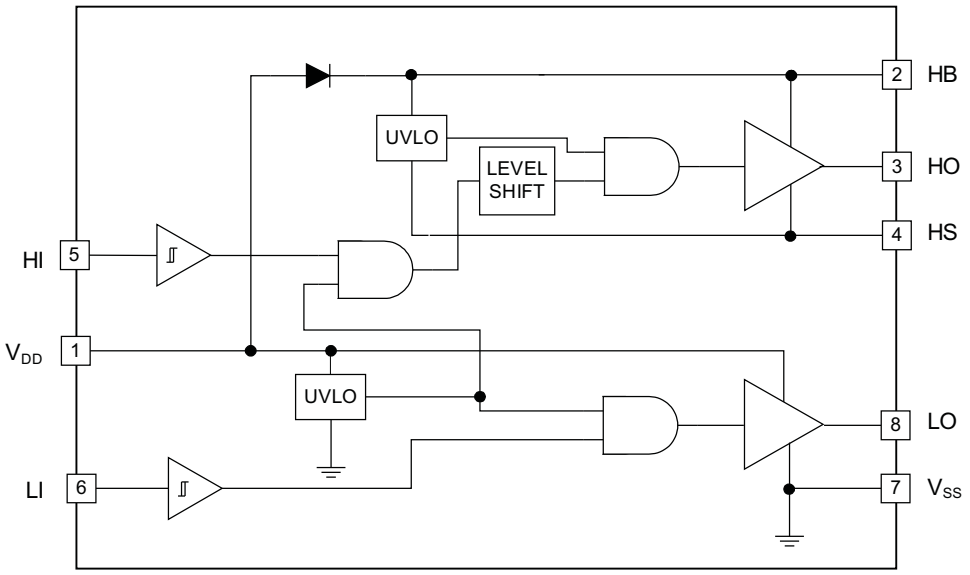
Figure 21. Quiescent Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The UCC27200A and UCC27201A are high-side and low-side drivers. The high-side and low-side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27200A and UCC27201A. The UCC27200A is the CMOS compatible input version and the UCC27201A is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to VSS which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27200A is 200 kΩ nominal and input capacitance is approximately 2 pF. The 200 kΩ is a pulldown resistance to Vss (ground). The CMOS-compatible input of the UCC27200A provides a rising threshold of 48% of VDD and falling threshold of 45% of VDD. The inputs of the UCC27200A are intended to be driven from 0 to VDD levels.

The input stages of the UCC27201A incorporate an open-drain configuration to provide the lower input thresholds. The input impedance is 200 kΩ nominal and input capacitance is approximately 4 pF. The 200 kΩ is a pulldown resistance to VSS (ground). The logic level compatible input provides a rising threshold of 1.7 V and a falling threshold of 1.6 V.

7.3.1.1 UVLO (Undervoltage Lockout)

The bias supplies for the high-side and low-side drivers have UVLO protection. VDD as well as VHB to VHS differential voltages are monitored. The VDD UVLO disables both drivers when VDD is below the specified threshold. The rising VDD threshold is 7.1 V with 0.5-V hysteresis. The VHB UVLO disables only the high-side driver when the VHB to VHS differential voltage is below the specified threshold. The VHB UVLO rising threshold is 6.7 V with 0.4-V hysteresis.

Feature Description (continued)

7.3.1.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

7.3.1.3 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC2720x family of drivers. The diode anode is connected to VDD and cathode connected to VHB. With the VHB capacitor connected to HB and the HS pins, the VHB capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

7.3.1.4 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from VDD to VSS and the high-side is referenced from VHB to VHS.

7.4 Device Functional Modes

The device operates in normal mode and VULO mode. See UVLO (Undervoltage Lockout) for more information on UVLO operation mode. In normal mode, the output stage is dependent on the sates of the HI and LI pins.

Table 1. Device Logic Table

HI PIN	LI PIN	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to the HS.
(2) LO is measured with respect to the VSS.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

8.2 Typical Application

An open loop half-bridge converter was used to calculate performance in an actual application.

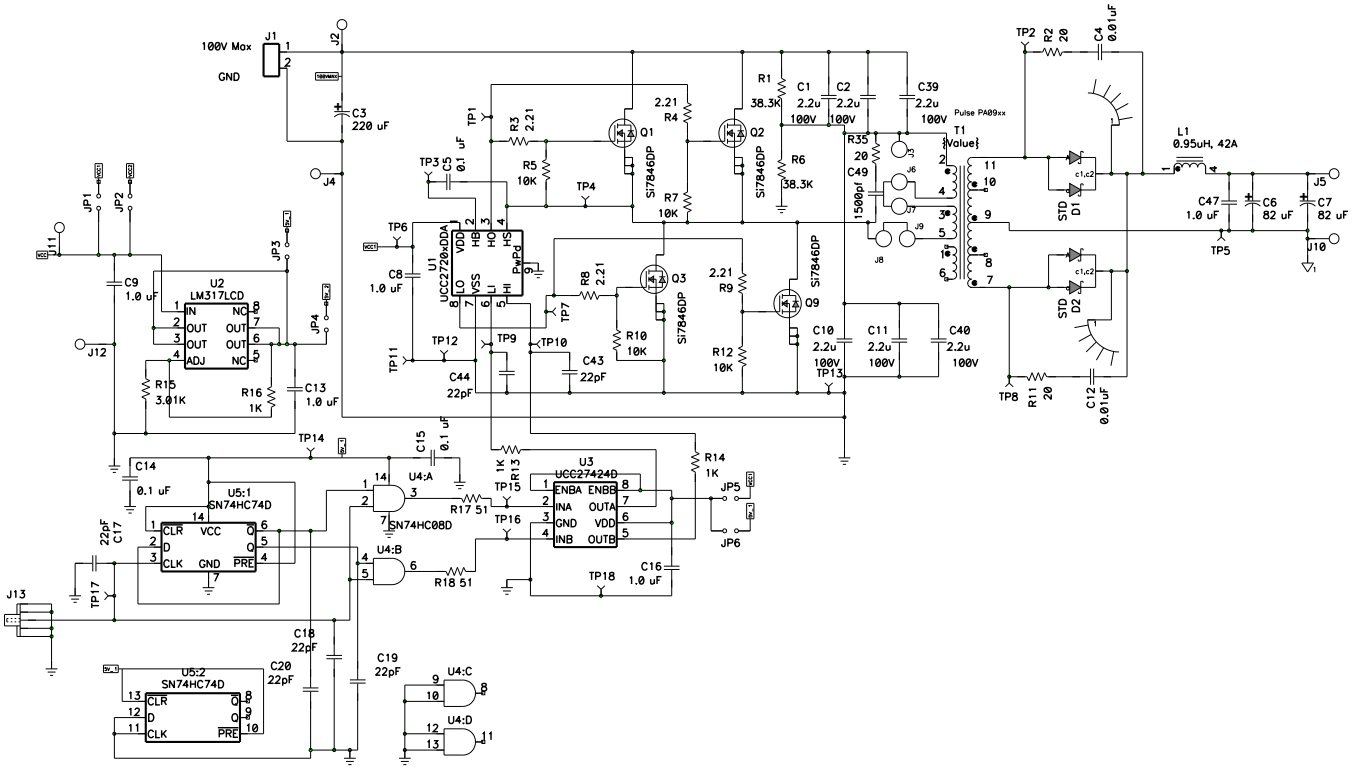


Figure 22. Open Loop Half-Bridge Converter

Typical Application (continued)

8.2.1 Design Requirements

UCC27201A Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Supply Voltage, VDD	12 V
Voltage on HS, VHS	0 V to 100 V
Voltage on HB, VHB	12 V to 112 V
Output	4 V, 20 A
Frequency	200 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Switching the MOSFETs

Achieving optimum drive performance at high frequency efficiently requires special attention to layout and minimizing parasitic inductances. Take care at the driver die and package level as well as the PCB layout to reduce parasitic inductances as much as possible. Figure 23 shows the main parasitic inductance elements and current flow paths during the turnon and turnoff of the MOSFET by charging and discharging its CGS capacitance.

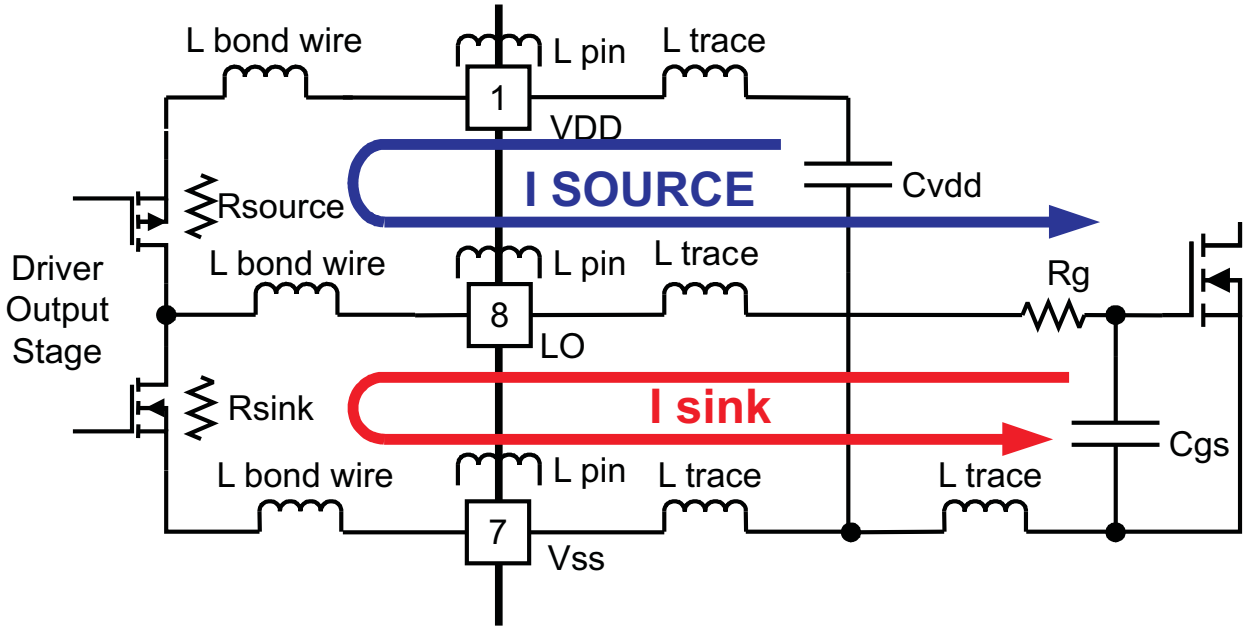


Figure 23. MOSFET Drive Paths and Circuit Parasitics

The I_{SOURCE} current charges the C_{GS} gate capacitor and the I_{SINK} current discharges it. The rise and fall time of the voltage across the gate to source defines how quickly the MOSFET can be switched. Based on actual measurements, the analytical curves in Figure 24 and Figure 25 indicate the output voltage and current of the drivers during the discharge of the load capacitor. Figure 24 shows voltage and current as a function of time. Figure 25 indicates the relationship of voltage and current during fast switching. These figures demonstrate the actual switching process and limitations due to parasitic inductances.

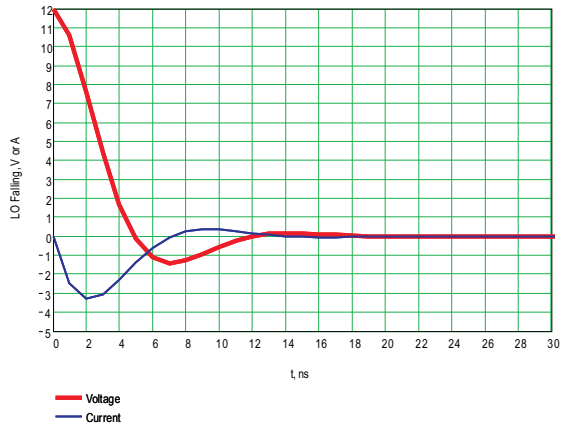


Figure 24. Turnoff Voltage and Current vs Time

Figure 25. Turnoff Voltage and Current Switching Diagram

Turning off the MOSFET needs to be achieved as fast as possible to minimize switching losses. For this reason the UCC2720x drivers are designed for high peak currents and low output resistance. The sink capability is specified as 0.18 V at 100-mA dc current implying 1.8-Ω $R_{DS(on)}$. With 12-V drive voltage, no parasitic inductance and a linear resistance, one would expect initial sink current amplitude of 6.7 A for both high-side and low-side drivers. Assuming a pure R-C discharge circuit of the gate capacitor, one would expect the voltage and current waveforms to be exponential. Due to the parasitic inductances and non-linear resistance of the driver MOSFET'S, the actual waveforms have some ringing and the peak-sink current of the drivers is approximately 3.3 A as shown in Figure 19. The overall parasitic inductance of the drive circuit is estimated at 4 nH. The internal parasitic inductance of the SOIC-8 package is estimated to be 2 nH including bond wires and leads. The SON-8 package reduces the internal parasitic inductances by more than 50%.

Actual measured waveforms are shown in Figure 26 and Figure 27. As shown, the typical rise time of 8 ns and fall time of 7 ns is conservatively rated.

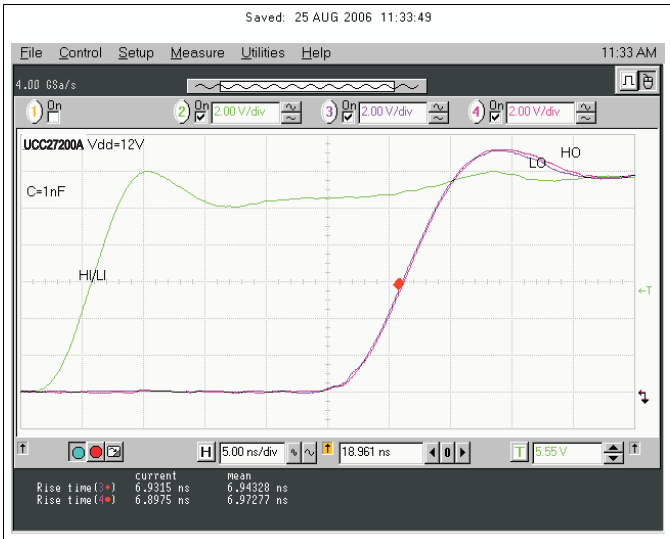


Figure 26. V_{LO} and V_{HO} Rise Time, 1-nf Load, 5 ns/div

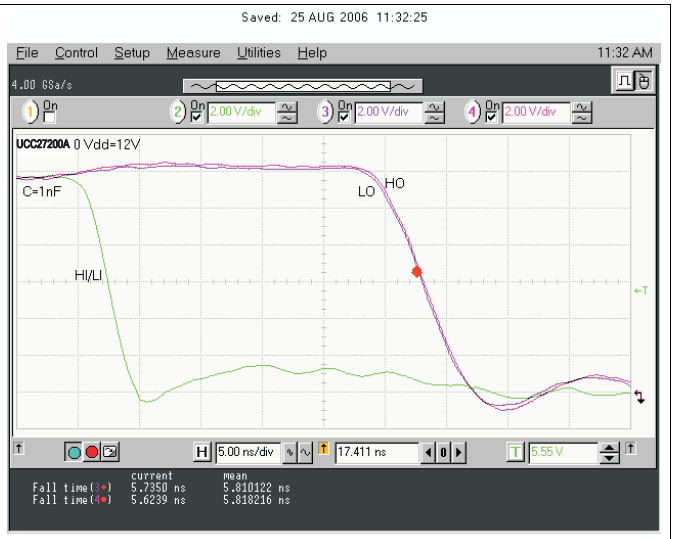


Figure 27. V_{LO} and V_{HO} Fall Time, 1-nf Load, 5-ns/div

8.2.2.2 Dynamic Switching of the MOSFETs

The true behavior of MOSFETS presents a dynamic capacitive load primarily at the gate to source threshold voltage. Using the turnoff case as the example, when the gate to source threshold voltage is reached the drain voltage starts rising, the drain to gate parasitic capacitance couples charge into the gate resulting in the turn off plateau. The relatively low threshold voltages of many MOSFETS and the increased charge that has to be removed (Miller charge) makes good driver performance necessary for efficient switching. An open-loop, half-bridge power converter was utilized to evaluate performance in actual applications. The schematic of the half-bridge converter is shown in . The turn off waveforms of the UCC27200A driving two MOSFETs in parallel is shown in Figure 28 and Figure 29.

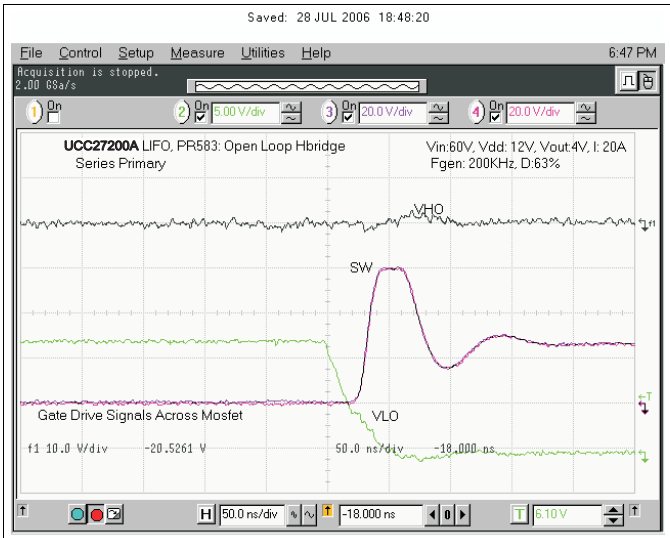


Figure 28. V_{LO} Fall Time in Half-Bridge Converter

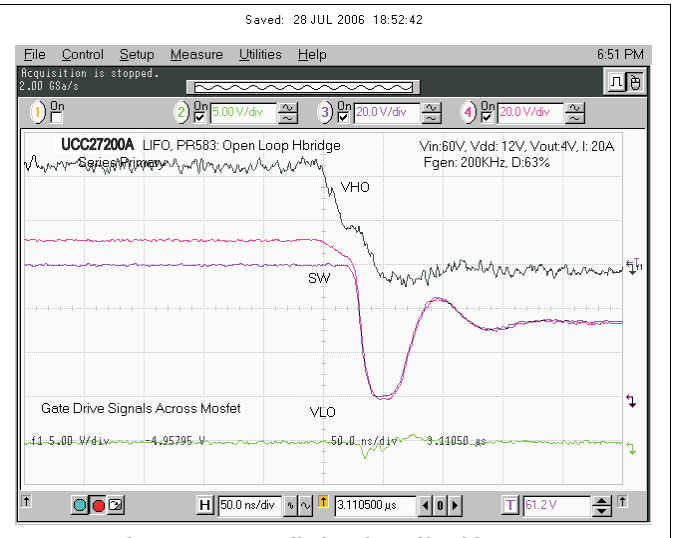


Figure 29. V_{HO} Fall Time in Half-Bridge Converter

8.2.2.3 Delay Matching and Narrow Pulse Widths

The total delays encountered in the PWM, driver and power stage need to be considered for a number of reasons, primarily delay in current limit response. Also to be considered are differences in delays between the drivers which can lead to various concerns depending on the topology. The sync-buck topology switching requires careful selection of dead-time between the high- and low-side switches to avoid 1) cross conduction and 2) excessive body diode conduction. Bridge topologies can be affected by a resulting volt-sec imbalance on the transformer if there is imbalance in the high and low side pulse widths in a steady-state condition.

Narrow pulse width performance is an important consideration when transient and short circuit conditions are encountered. Although there may be relatively long steady state PWM output-driver-MOSFET signals, very narrow pulses may be encountered in 1) soft start, 2) large load transients, and 3) short circuit conditions.

The UCC2720x driver family offers excellent performance regarding high and low-side driver delay matching and narrow pulse width performance. The delay matching waveforms are shown in Figure 30 and Figure 31. The UCC2720x driver narrow pulse performance is shown in Figure 32 and Figure 33.

Figure 30. V_{LO} and V_{HO} Rising Edge Delay Matching

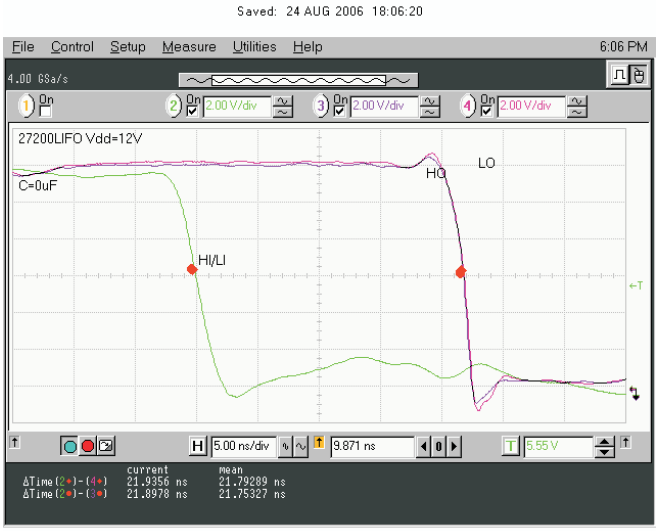


Figure 31. V_{LO} and V_{HO} Falling Edge Delay Matching

Figure 32. 20-ns Input Pulse Delay Matching

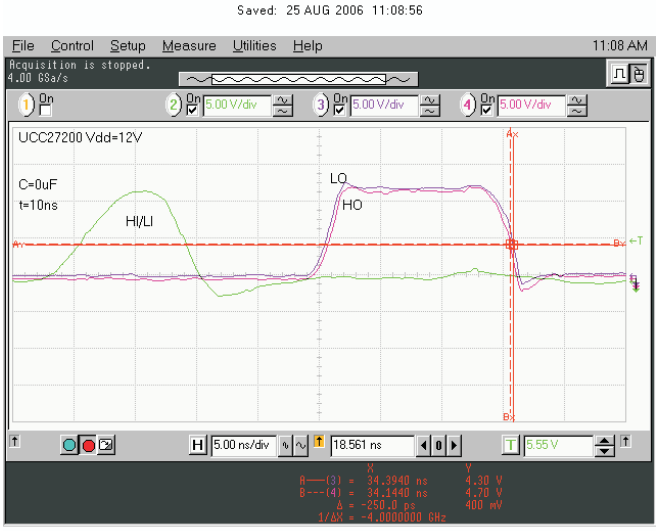


Figure 33. 10-ns Input Pulse Delay Matching

8.2.2.4 Boot Diode Performance

The UCC2720x family of drivers incorporates the bootstrap diode necessary to generate the high-side bias internally. The characteristics of this diode are important to achieve efficient, reliable operation. The dc characteristics to consider are V_F and dynamic resistance. A low V_F and high dynamic resistance results in a high forward voltage during charging of the bootstrap capacitor. The UCC2720x has a boot diode rated at 0.65-V V_F and dynamic resistance of 0.6 Ω for reliable charge transfer to the bootstrap capacitor. The dynamic characteristics to consider are diode recovery time and stored charge. Diode recovery times that are specified with no conditions can be misleading. Diode recovery times at no forward current (I_F) can be noticeably less than with forward current applied. The UCC2720x boot diode recovery is specified at 20ns at I_F = 20 mA, I_{REV} = 0.5 A. At 0 mA I_F the reverse recovery time is 15 ns.

Another less obvious consideration is how the stored charge of the diode is affected by applied voltage. On every switching transition when the HS node transitions from low to high, charge is removed from the boot capacitor to charge the capacitance of the reverse biased diode. This is a portion of the driver power losses and reduces the voltage on the HB capacitor. At higher applied voltages, the stored charge of the UCC2720x PN diode is often less than a comparable Schottky diode.

8.2.3 Application Curves

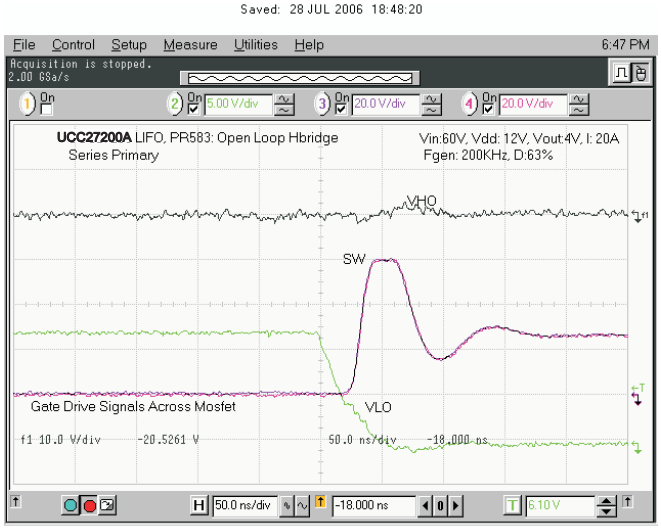


Figure 34. V_{LO} Fall Time in Half-Bridge Converter

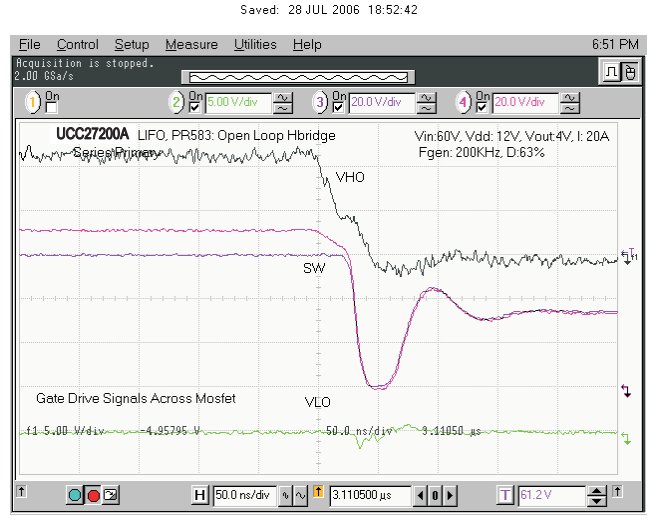


Figure 35. V_{HO} Fall Time in Half-Bridge Converter

9 Power Supply Recommendations

The bias supply voltage range for which the device is rated to operate is from 8 V to 17 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 17 V. The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD(hys).Therefore, ensuring that, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the V(OFF) threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the VDD pin voltage has exceeded above the V(ON) threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the HO pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the HO pin a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that a local bypass capacitor is provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends using a capacitor in the range 0.22 uF to 4.7 uF between VDD and GND. In a similar manner, the current pulses delivered by the LO pin are sourced from the HB pin. Therefore a 0.022-uF to 0.1-uF local decoupling capacitor is recommended between the HB and HS pins.

10 Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and V_{HB} (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA and DRM package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.
- Use similar rules for the HS node as for GND for the high side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. 60 mil to 100 mil width is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node needs to be routed from one layer to another. For GND the number of vias needs to be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid L_I and H_I (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.
- Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

These references and links to additional information may be found at www.ti.com.

1. Additional layout guidelines for PCB land patterns may be found in Application Brief SLUA271
2. Additional thermal performance guidelines may be found in Application Reports SLMA002 and SLMA004

10.2 Layout Example

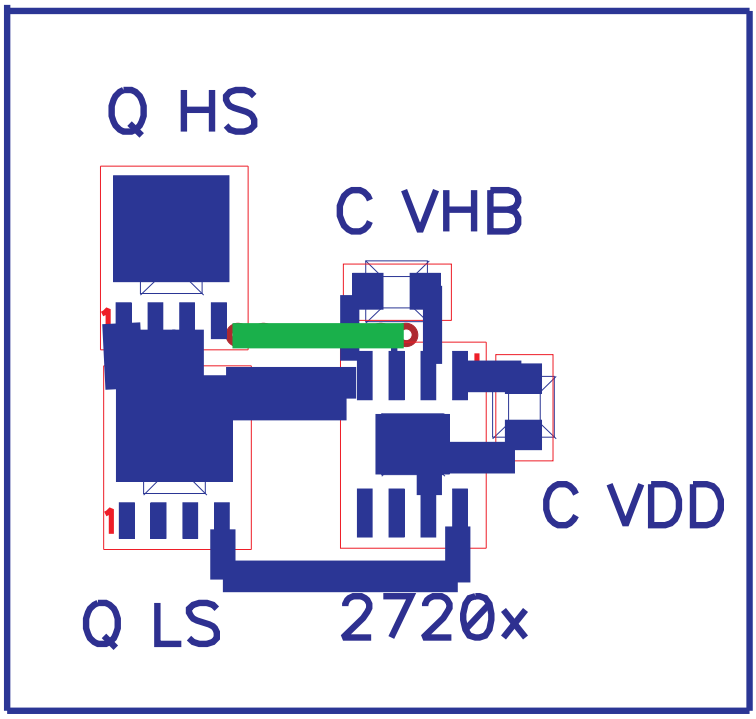


Figure 36. Example Component Placement

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *QFN/SON PCB Attachment*, SLUA271
- *PowerPAD Thermally Enhanced Package*, SLMA002
- *PowerPAD Made Easy*, SLMA004

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27200A	Click here	Click here	Click here	Click here	Click here
UCC27201A	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27200AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADRCR	ACTIVE	VSON	DRC	9	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	200A	Samples
UCC27200ADRCT	ACTIVE	VSON	DRC	9	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	200A	Samples
UCC27200ADRMR	ACTIVE	VSON	DRM	8	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADRMT	ACTIVE	VSON	DRM	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27201AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADPRR	ACTIVE	WSON	DPR	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	UCC 27201A	Samples
UCC27201ADPRT	ACTIVE	WSON	DPR	10	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	UCC 27201A	Samples
UCC27201ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADRCR	ACTIVE	VSON	DRC	9	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	201A	Samples
UCC27201ADRCT	ACTIVE	VSON	DRC	9	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	201A	Samples
UCC27201ADRMR	ACTIVE	VSON	DRM	8	3000	Green (RoHS & no Sb/Br)	Call TI | NIPDAUAG | NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27201ADRMT	ACTIVE	VSON	DRM	8	250	Green (RoHS & no Sb/Br)	Call TI | NIPDAUAG | NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27201A :

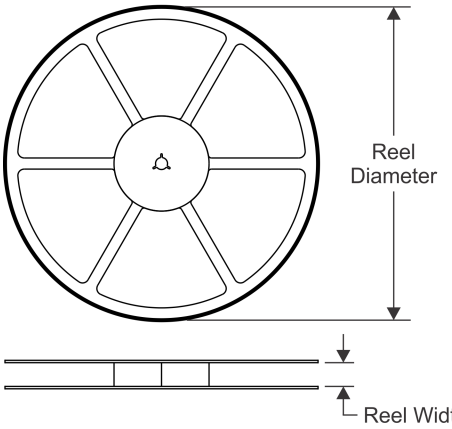
- Automotive: UCC27201A-Q1

NOTE: Qualified Version Definitions:

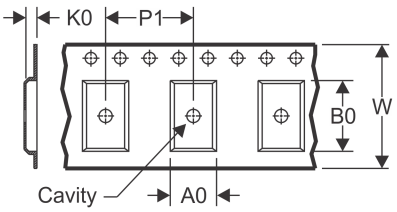
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

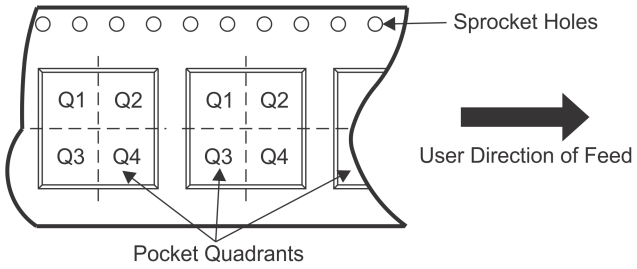


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

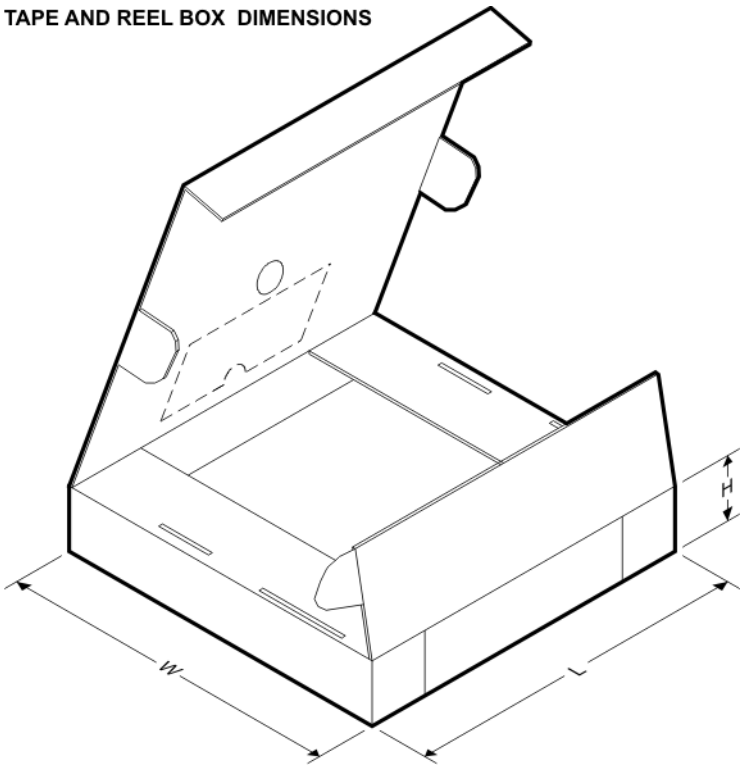
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27200ADDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27200ADR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
UCC27200ADRCR	VSON	DRC	9	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27200ADRCT	VSON	DRC	9	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27200ADRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27200ADRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201ADDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UCC27201ADPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201ADPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201ADR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
UCC27201ADRCR	VSON	DRC	9	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27201ADRCT	VSON	DRC	9	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27201ADRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201ADRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

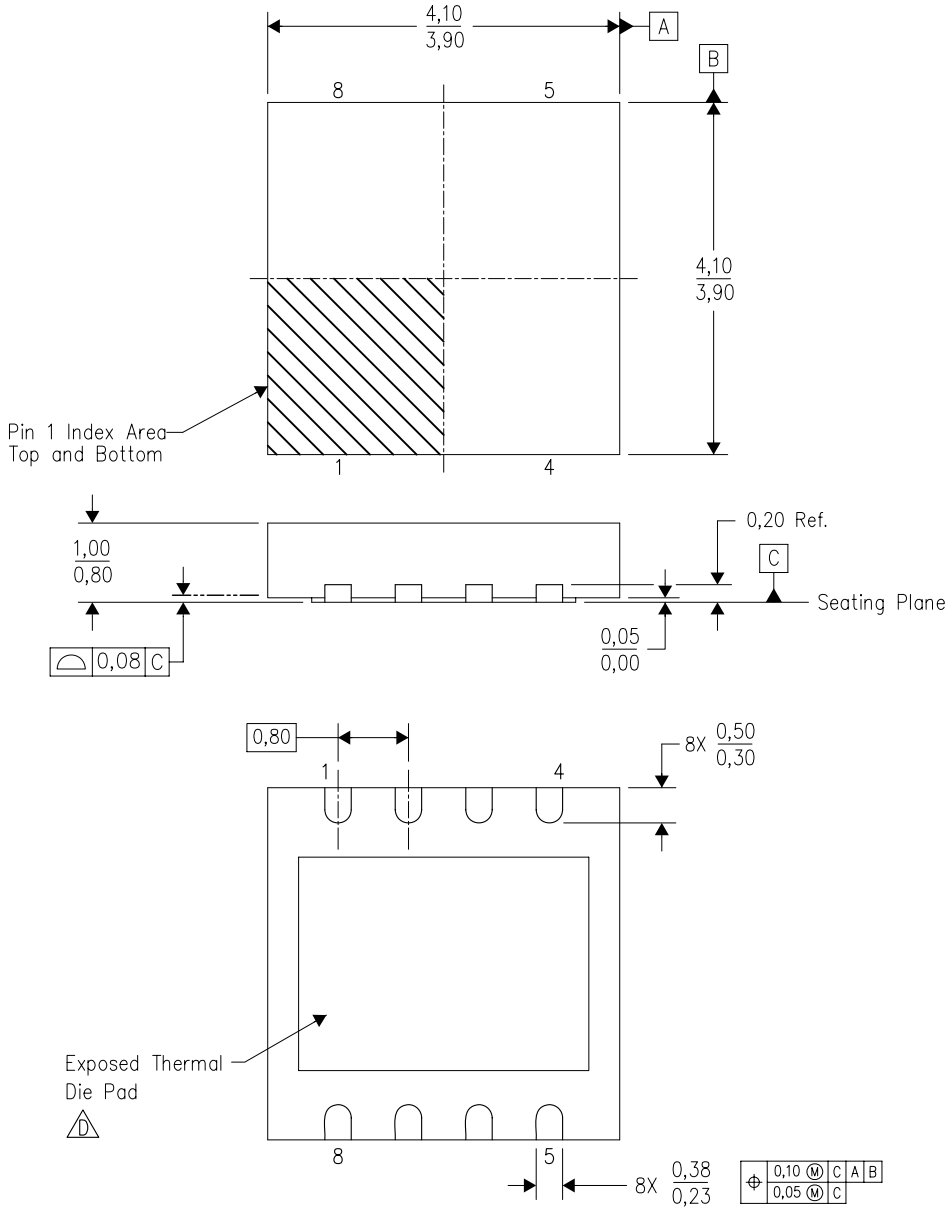
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27200ADDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
UCC27200ADR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27200ADRCR	VSON	DRC	9	3000	367.0	367.0	35.0
UCC27200ADRCT	VSON	DRC	9	250	210.0	185.0	35.0
UCC27200ADRMR	VSON	DRM	8	3000	367.0	367.0	35.0
UCC27200ADRMT	VSON	DRM	8	250	210.0	185.0	35.0
UCC27201ADDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0
UCC27201ADPRR	WSON	DPR	10	3000	367.0	367.0	35.0
UCC27201ADPRT	WSON	DPR	10	250	210.0	185.0	35.0
UCC27201ADR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27201ADRCR	VSON	DRC	9	3000	367.0	367.0	35.0
UCC27201ADRCT	VSON	DRC	9	250	210.0	185.0	35.0
UCC27201ADRMR	VSON	DRM	8	3000	367.0	367.0	35.0
UCC27201ADRMT	VSON	DRM	8	250	210.0	185.0	35.0

DRM (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

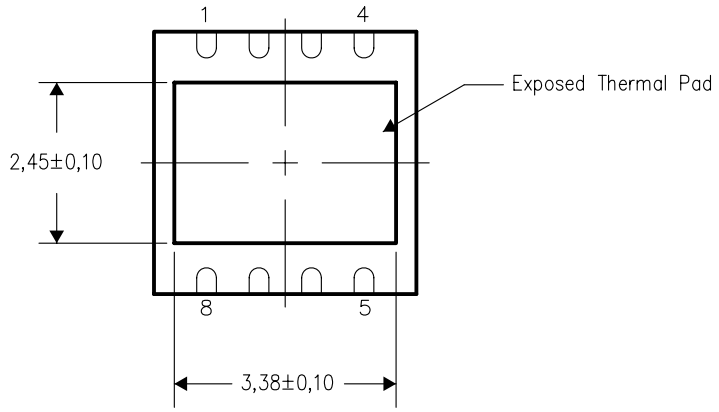
DRM (S–PDSO–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

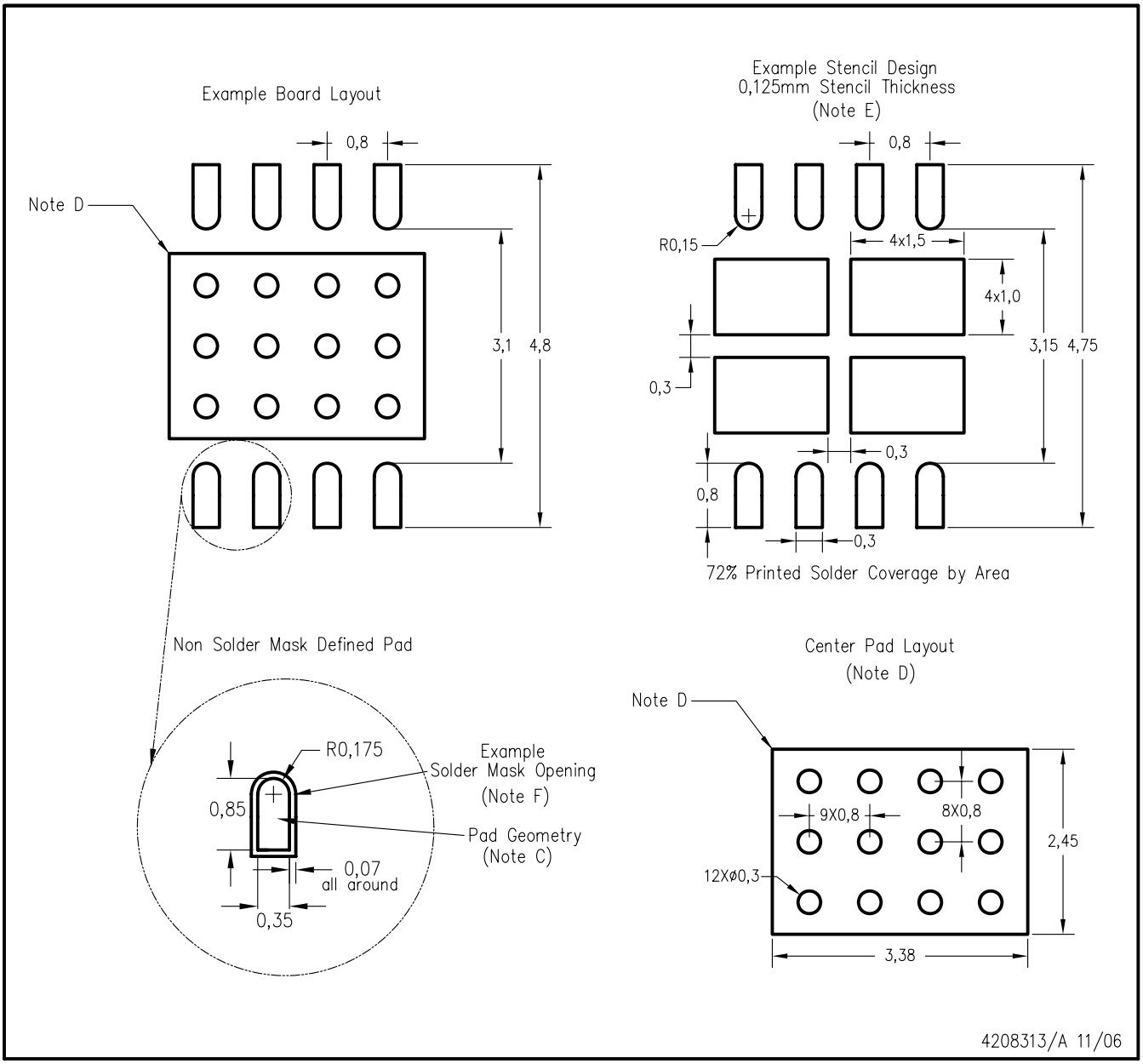


Bottom View

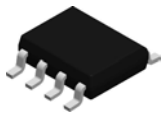
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRM (S–PDSO–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

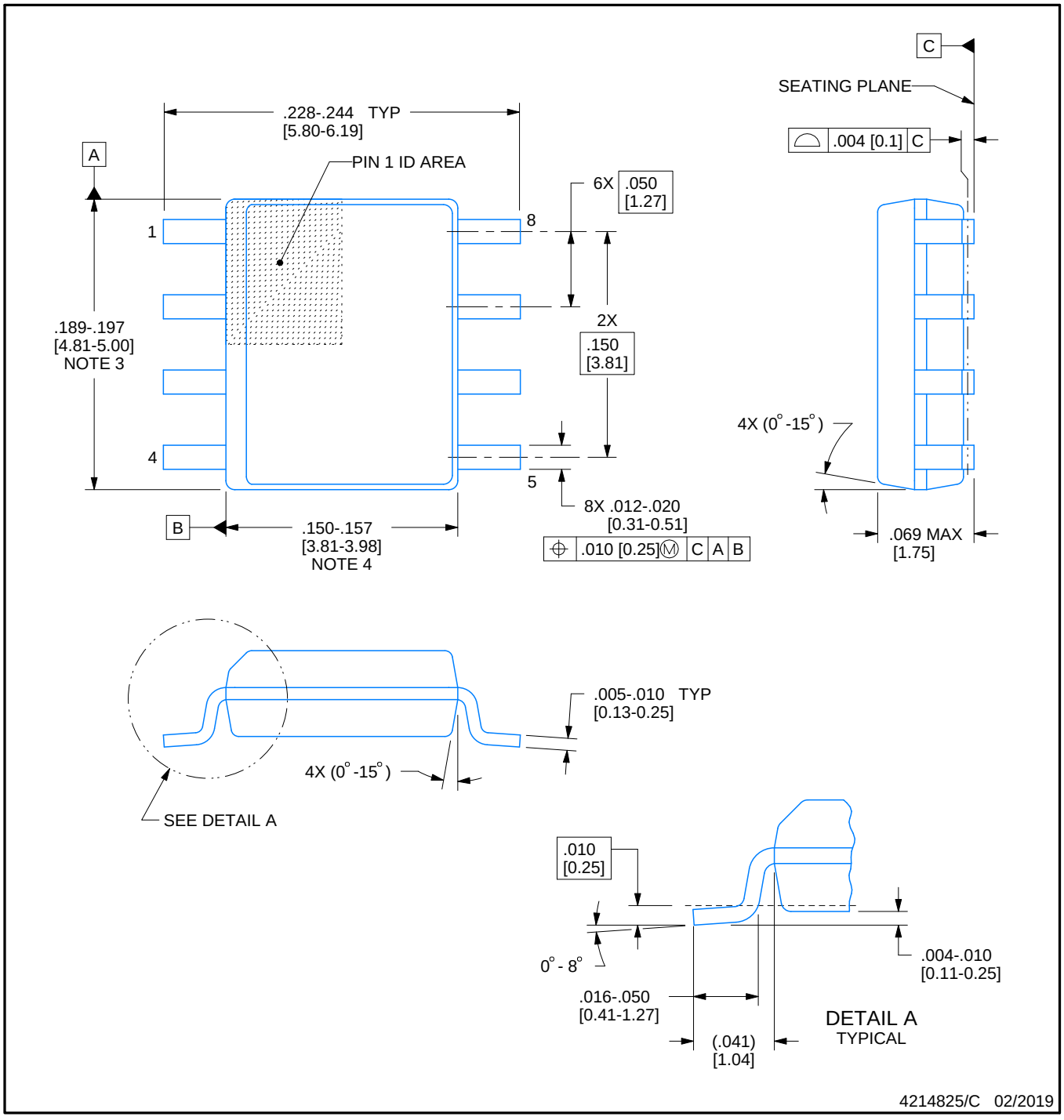


PACKAGE OUTLINE

D0008A

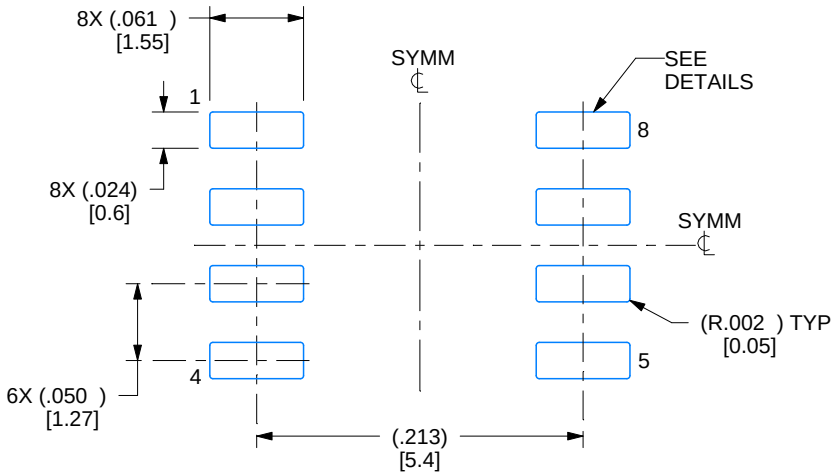
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

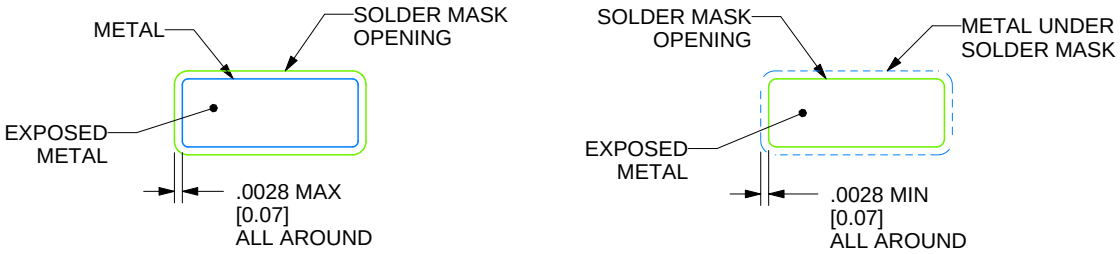


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

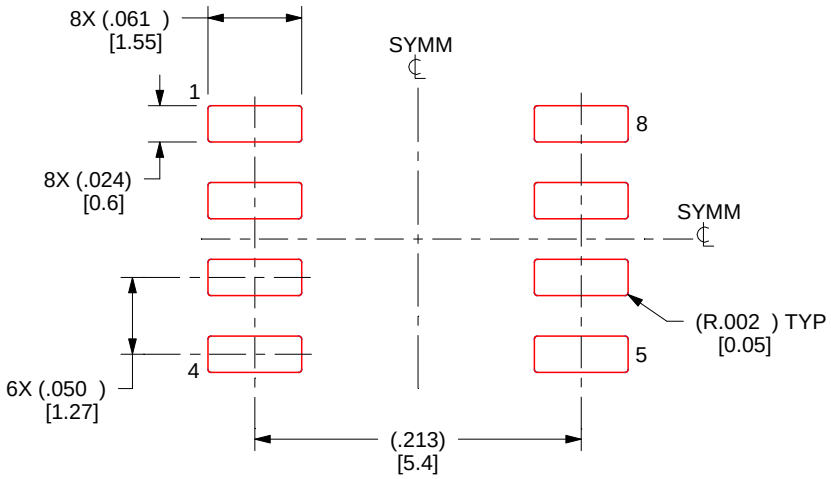
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



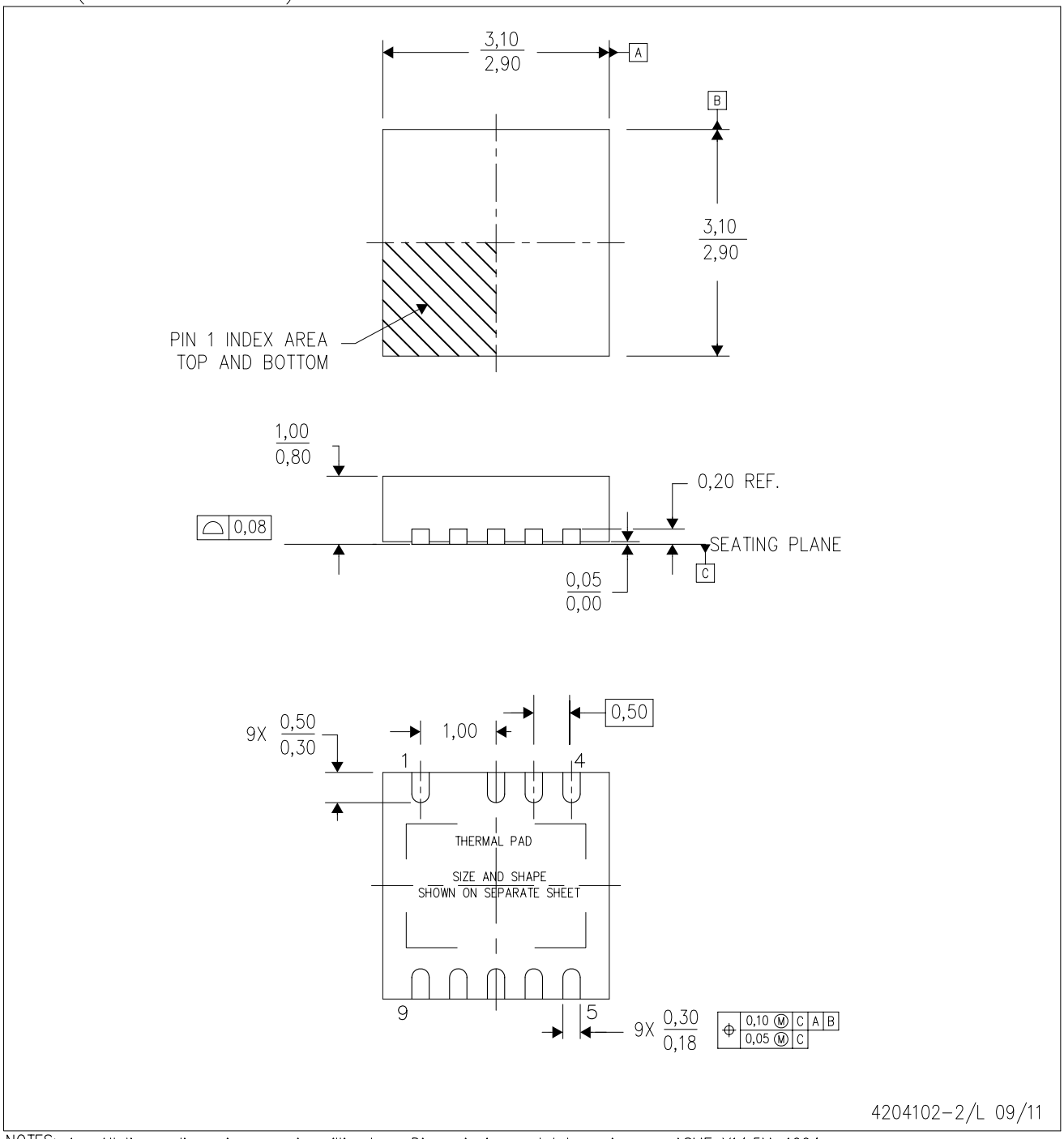
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRC (S–PVSON–N9) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

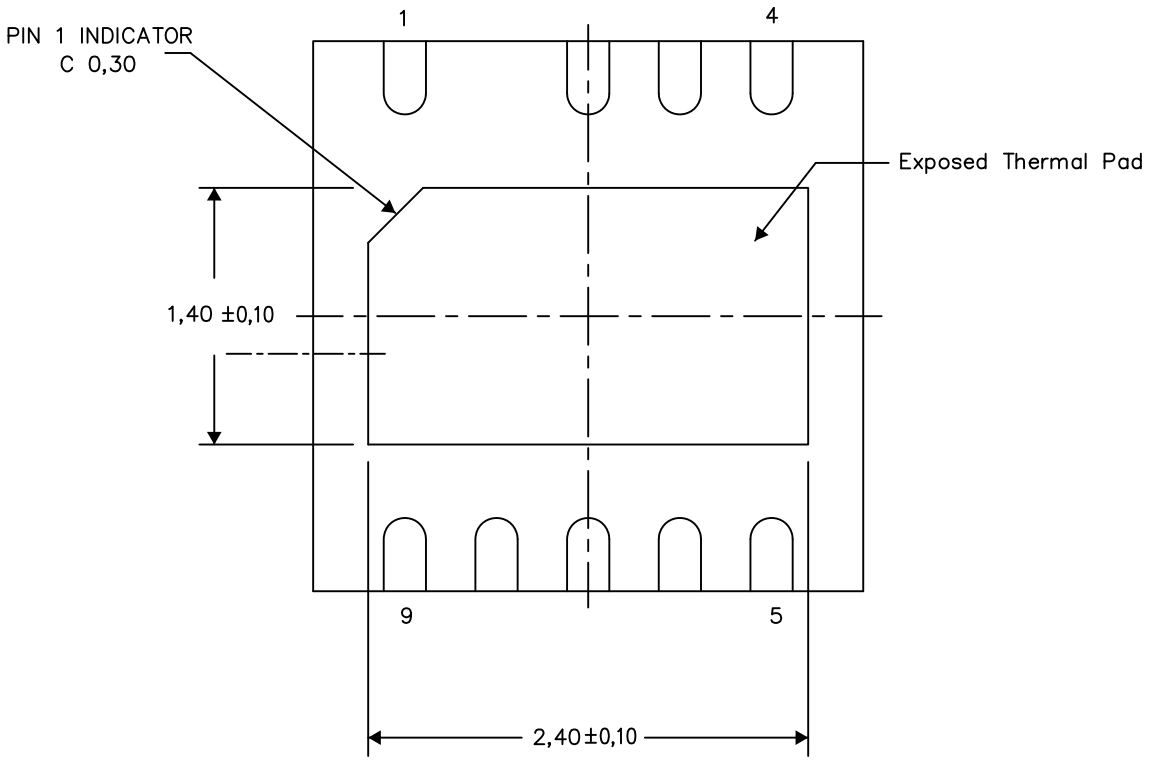
DRC (S–PVSON–N9) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



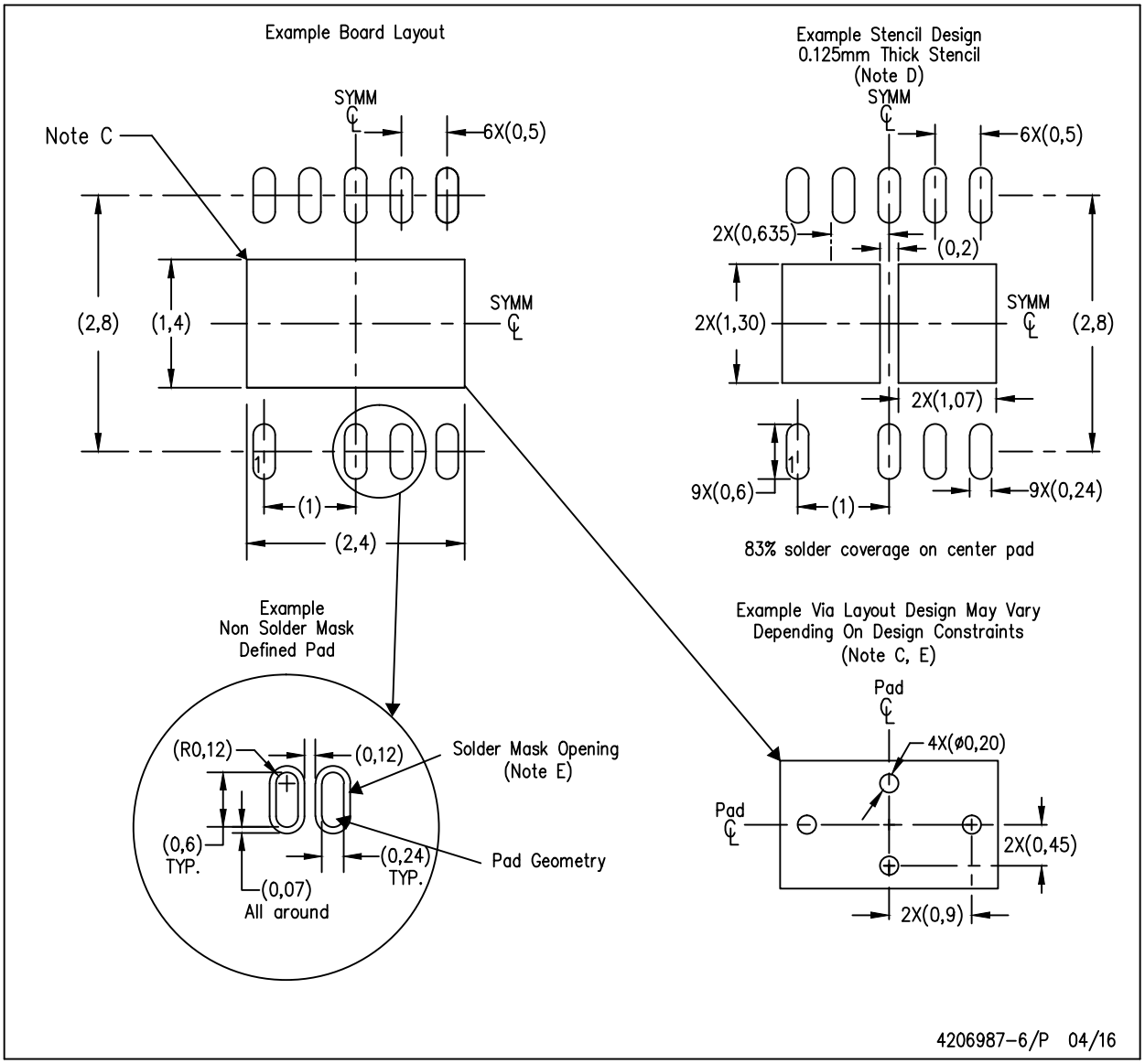
Bottom View

Exposed Thermal Pad Dimensions

4206565–2/Y 08/15

NOTE: A. All linear dimensions are in millimeters

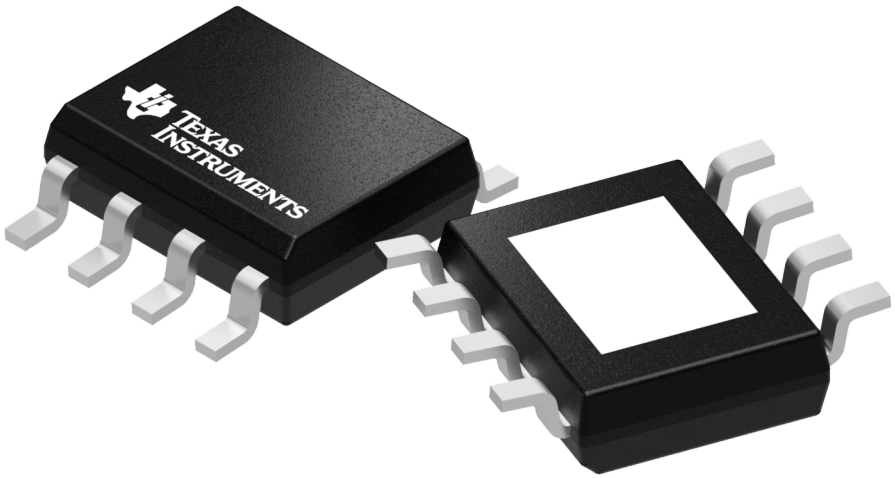
DRC (S–PVSON–N9) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads and via tenting recommendations for any larger diameter vias placed in the thermal pad.

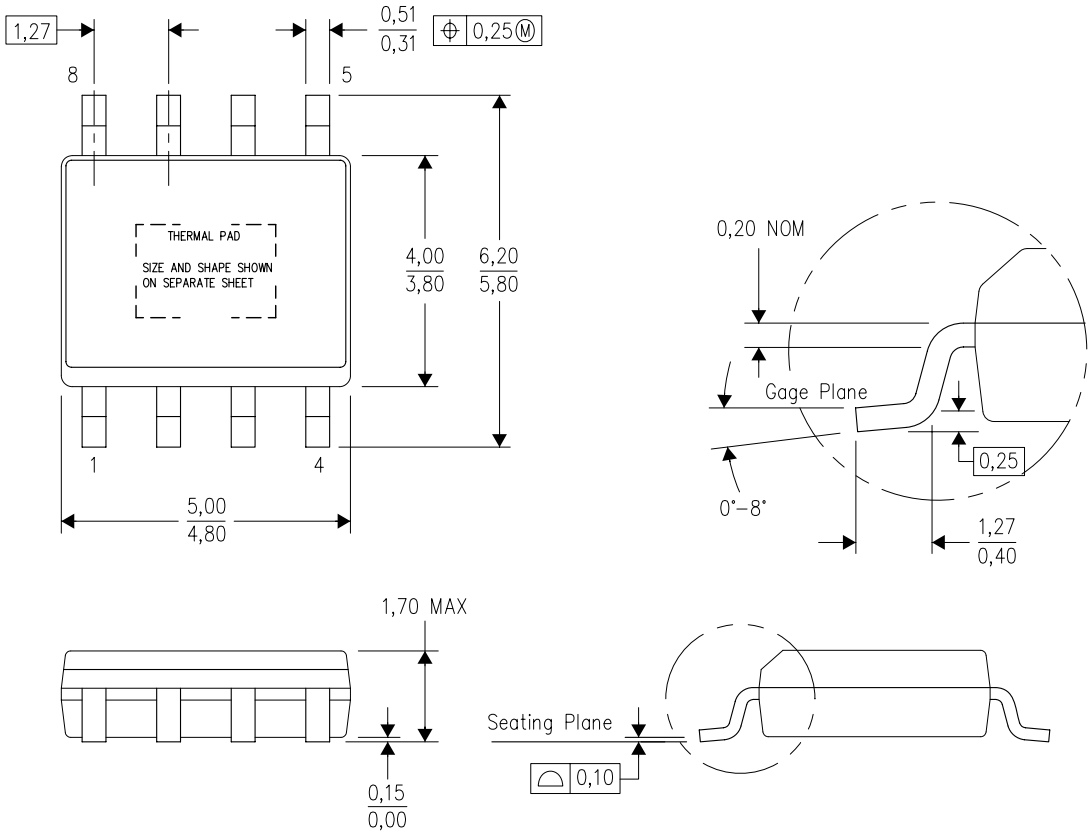
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

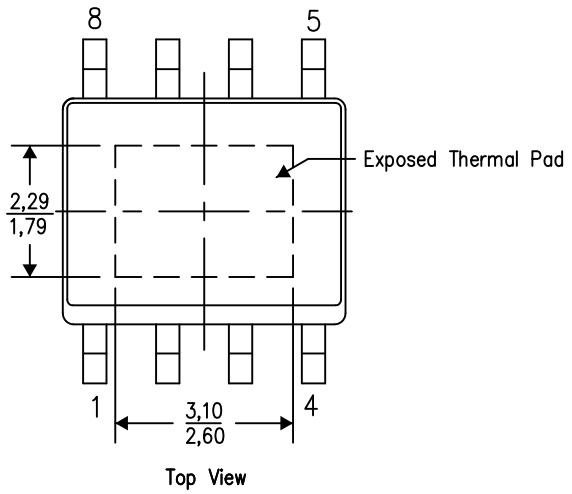
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



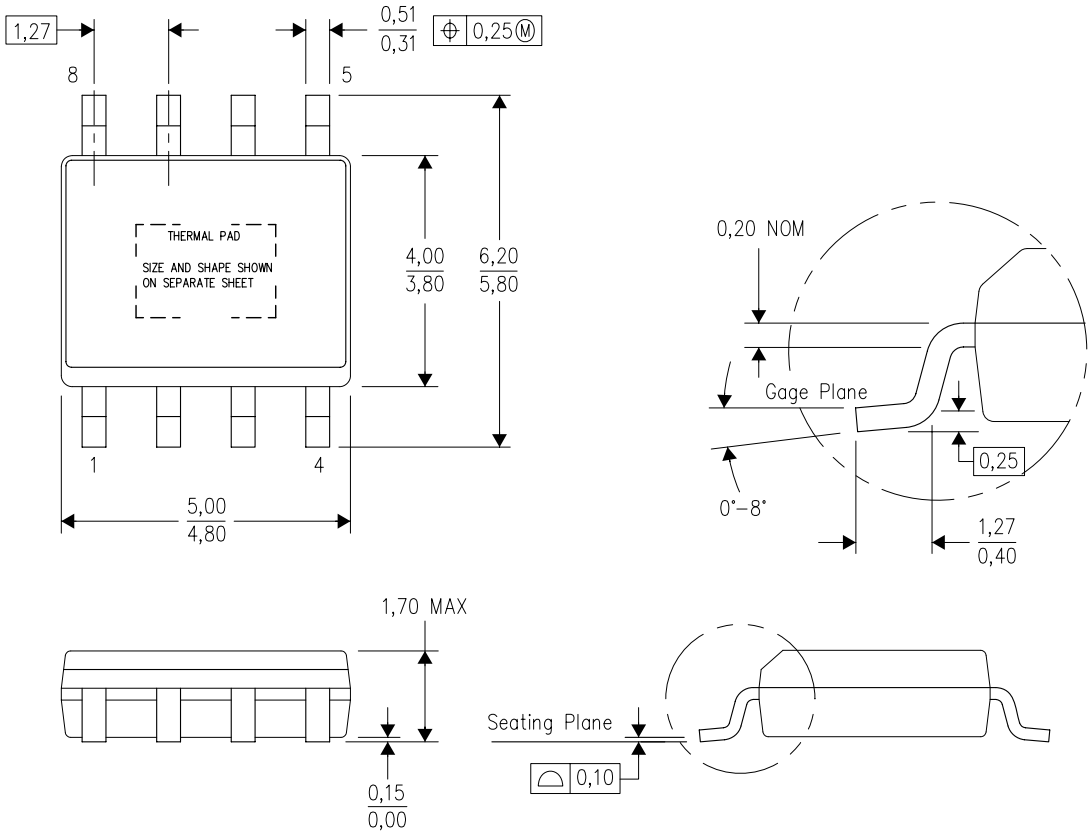
Exposed Thermal Pad Dimensions

4206322–8/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

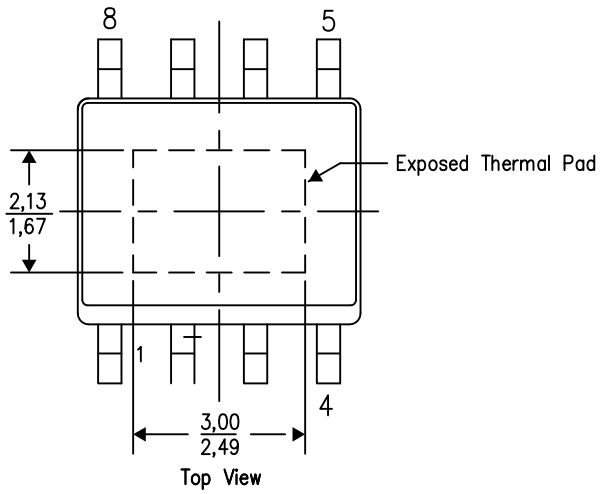
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



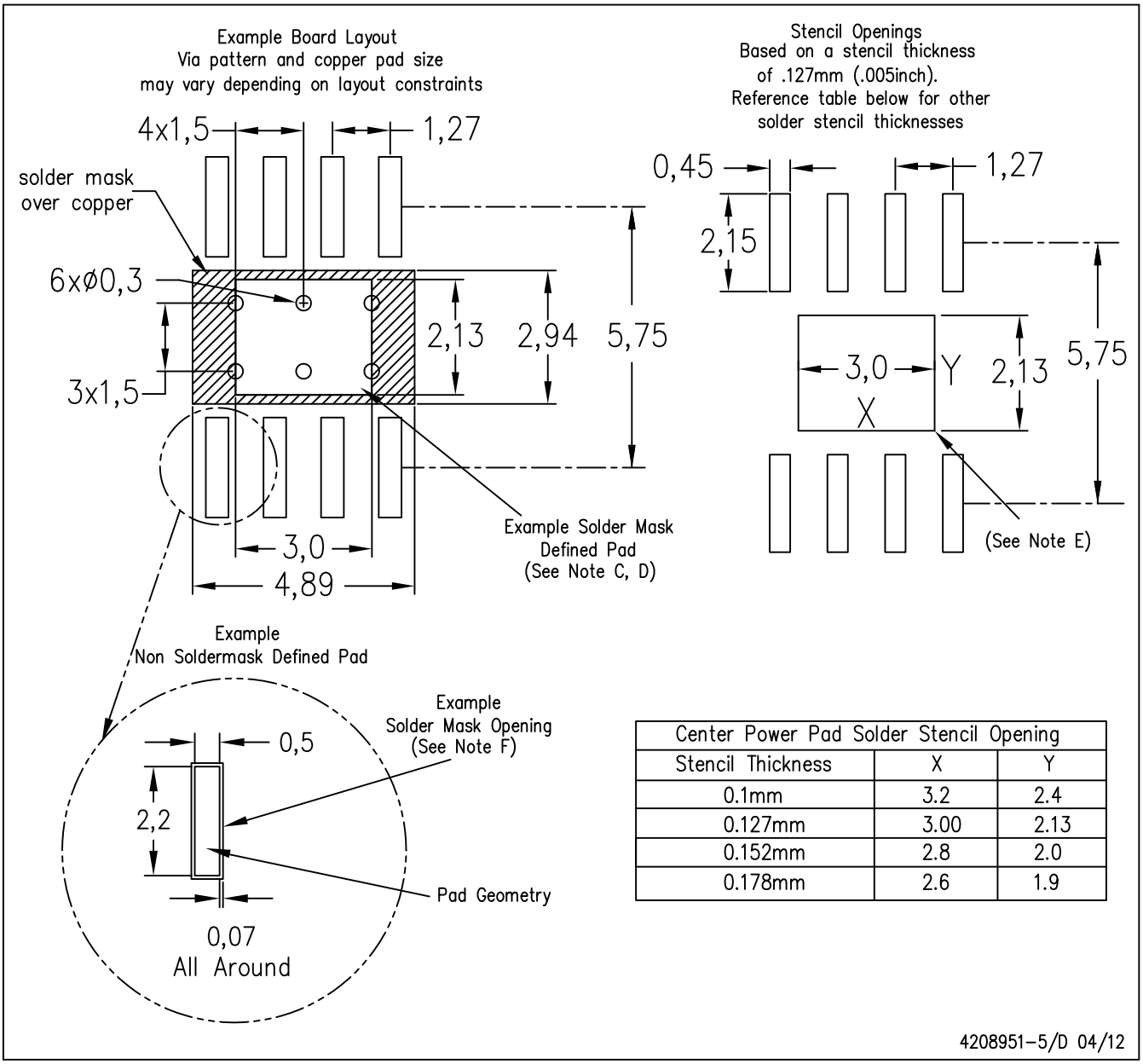
Exposed Thermal Pad Dimensions

4206322–5/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

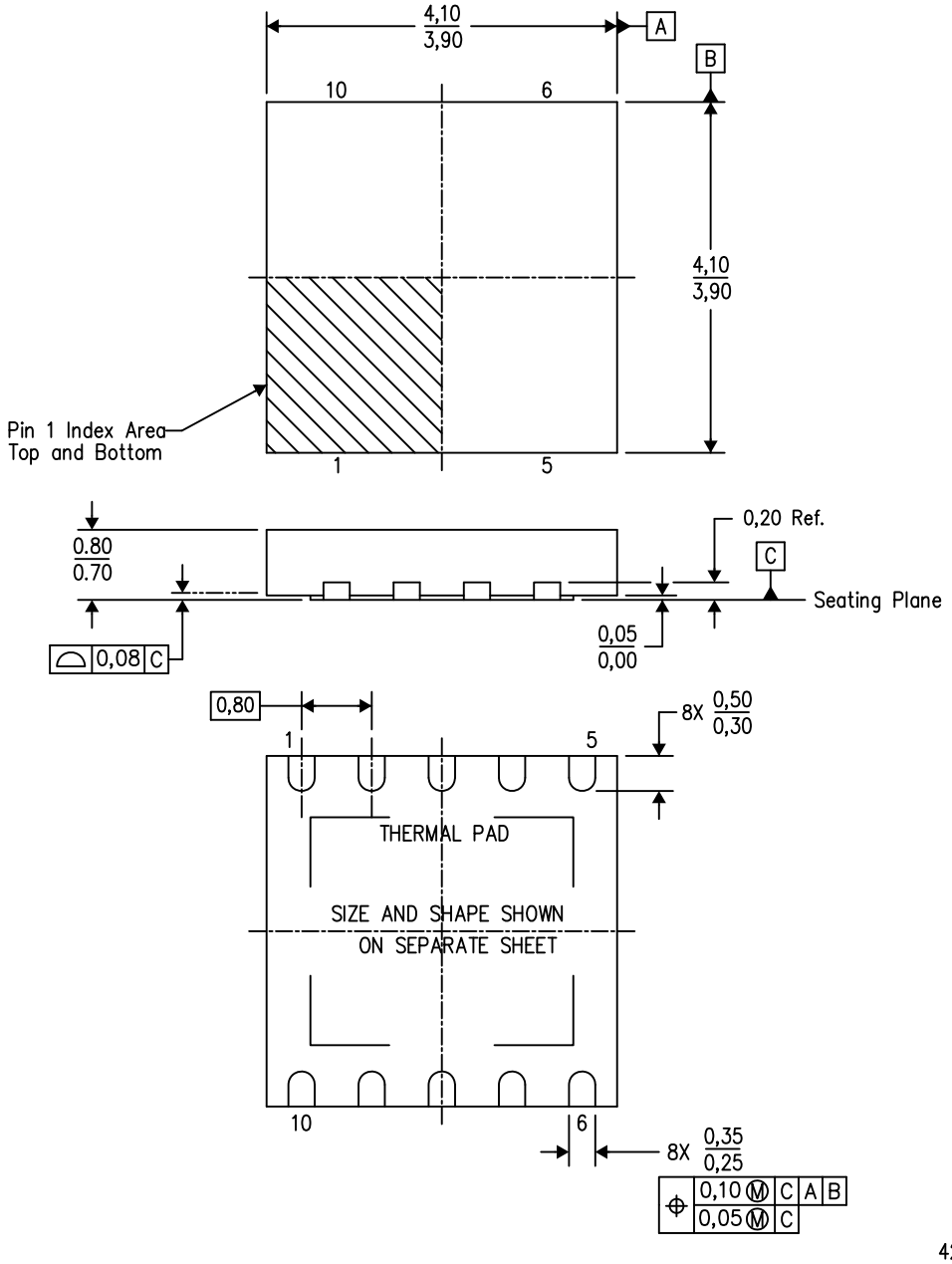


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.2	2.4
0.127mm	3.00	2.13
0.152mm	2.8	2.0
0.178mm	2.6	1.9

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

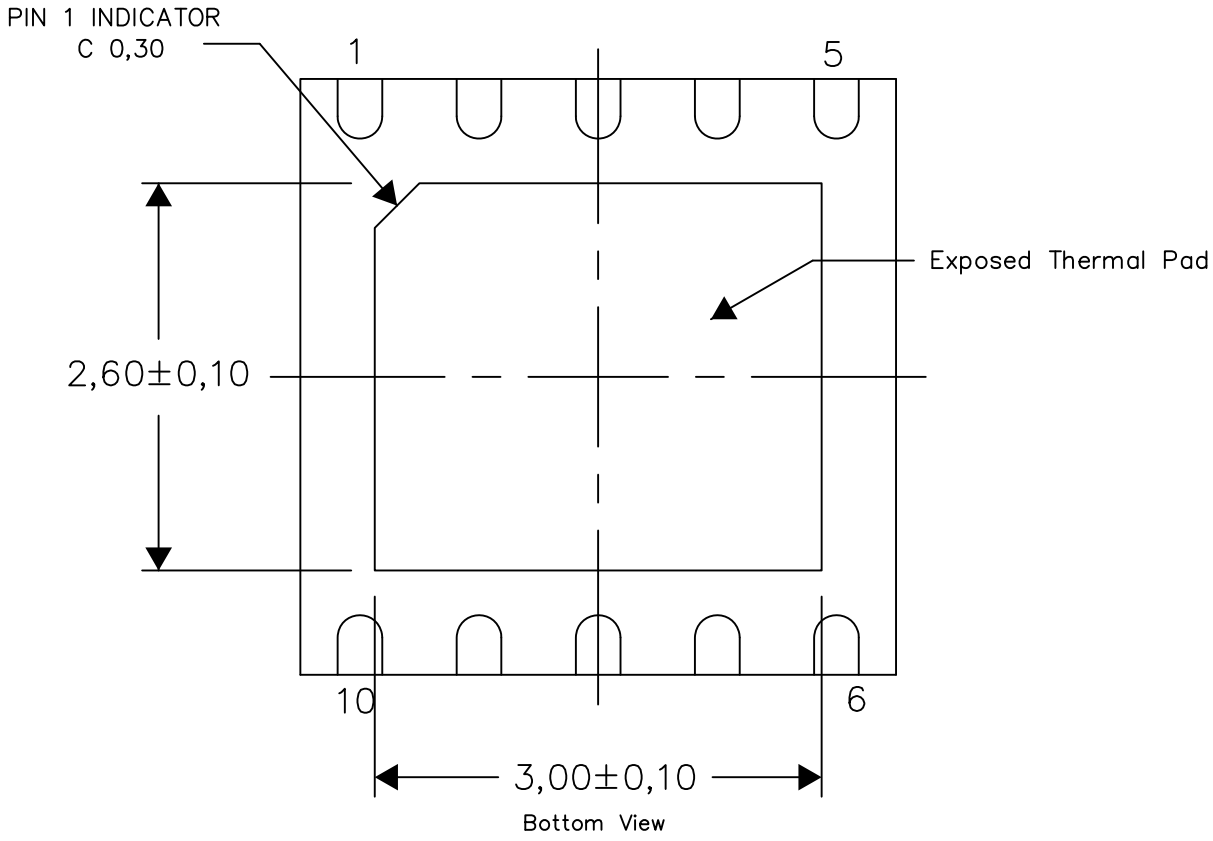
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4211551/C 12/13

NOTES: All linear dimensions are in millimeters

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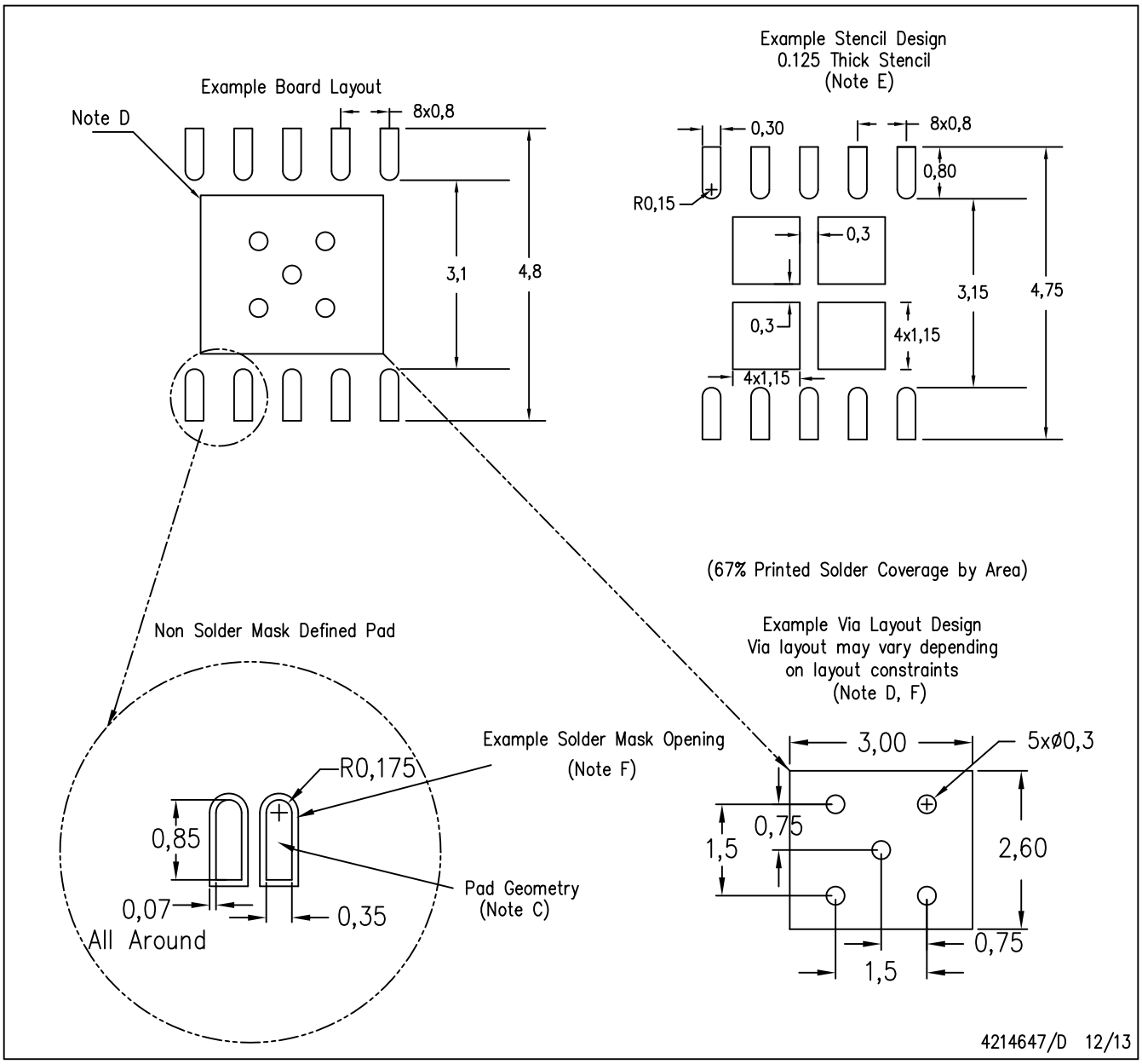

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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