UCC21540EVM

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1 Introduction

The UCC21540EVM device is designed for evaluation of the UCC21540 family of devices, with a 4-A source and 6-A sink peak current for driving Si MOSFETs, IGBTs, and GaN FETs. Developed for high voltage applications where isolation and reliability are required, the UCC21540 device delivers reinforced isolation of 5.7-kV_{RMS} and a surge immunity tested up to 7.8-kV, with a common mode transient immunity (CMTI) greater than 100 V/ns. The device has an impressive propagation delay of 25 ns and the tightest channel-to-channel delay matching in the industry of less than 5 ns, which enables high-switching frequency, high-power density, and efficiency.

The flexible, universal capability of the UCC21540 device, with up to 5-V VCCI and 18-V VDDA and VDDB, allows it to be used as a low-side, high-side, high-side/low-side, or half-bridge driver with dual independent PWM inputs. With its integrated functions, advanced protection features (UVLO, Enable/Disable, and resistor-programmable dead time), and optimized switching performances, the UCC21540 device enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications, allowing for faster time to market.

The UCC21540EVM can also be used for evaluation of pin-to-pin compatible drivers with or without dead time control, including devices from the UCC21520 family.

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2 Description

The UCC21540EVM kit has independent connection points for VCCI, VDDA, and VDDB supplies, including separate ground points. Three-position headers with jumpers for all the key input signals, such as PWM inputs (INA, INB, or PWM) and the disable function (DIS), let designers easily evaluate different protection functions. A variety of testing points support most of the key-feature probing of the UCC21540 device. Moreover, the PCB layout is not only optimized with minimized loop area in each gate driver loop and power supply loop with bypassing capacitors, but it also supports high voltage testing between the primary side and secondary side. The EVM comes equipped with the option to install an SMA bootstrap diode, bootstrap resistor, and extra capacitor of the user's choice, which facilitates high-voltage, half-bridge testing for a wide variety of power converter topologies. For detailed device information, see the UCC21540 4-A/6-A, 5.7-kVRMS Isolated Dual-Channel Gate Driver with Dead Time data sheet and Isolated Gate Driver Solutions, from TI.

2.1 Features

- Evaluation module for UCC21540 and other pin-to-pin compatible drivers in SOIC-16 wide body (DW) package
- 3-V to 5-V VCCI power supply range, with up to 18-V VDDA/VDDB power supply range
- 4-A source and 6-A sink current capability
- 5.7-kV_{RMS} isolation for 1 minute per UL 1577
- TTL/CMOS compatible inputs
- 3-position header for INA, INB, and DIS pins
- Optional footprints for dead time resistor and potentiometer, capacitor, and 3-position header
- PCB layout optimized for power supply bypassing capacitors, gate driver loop
- Maximized creepage distance between two output channels
- Support half-bridge test with MOSFETs and IGBTs, with connection to external power stage
- Testing points allow probing all the key pins of the UCC21540 device and other SOIC-16 wide body isolated driver parts

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2.2 I/O Description

Table 1 lists the test points and jumpers.

Table 1. Test Points and Jumpers

Pins	Pin Label	Description
TP1	VCCIN	Primary supply positive input
TP2	GND	Primary supply negative input
TP3	INA	INA positive input
TP4	GND	INA negative input (primary GND)
TP5	INB	INB positive input
TP6	GND	INB negative input (primary GND)
TP7	DIS	Disable pin input/measurement point
TP8	GND	Primary GND
TP9	DT	Dead time programming pin input/measurement point
TP10	GND	Primary GND
TP11	VDDA	A-channel supply positive input
TP12	OUTA	A-channel output, measured after gate drive resistor
TP13	VSSA	A-channel supply negative input
TP14	VDDB	B-channel supply positive input
TP15	OUTB	B-channel output, measured after gate drive resistor
TP16	VSSB	B-channel supply negative input
J1-1	-	Connected to GND
J1-2	-	Connected to INA
J1-3	-	Connected to VCCI
J2-1	-	Connected to GND
J2-2	-	Connected to INB
J2-3	-	Connected to VCCI
J3-3	-	Connected to GND
J3-2	-	Connected to disable pin
J3-3	-	Connected to VCCI
J4-1	-	Connected to dead time programming potentiometer
J4-2	-	Connected to dead time programming pin
J4-3	-	Connected to VCCI

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2.3 Jumpers (Shunt) Setting

Table 2 lists the jumper settings.

Table 2. Jumpers Setting

Header	Jumper Setting Options		Factory Setting
J1	Option A	Jumper not installed, INA provided by external signal and this pin is low by default if left open.	Option A
	Option B	Jumper on J1-2 and J1-1 sets INA low.	
	Option C	Jumper on J1-2 and J1-3 sets INA high.	
J2	Option A	Jumper not installed, INB provided by external signal, and this pin is low by default if left open.	Option A
	Option B	Jumper on J2-2 and J2-1 sets INB low.	
	Option C	Jumper on J2-2 and J2-3 sets INB high.	
J3	Option A	Jumper not installed.	Option B
	Option B	Jumper on J3-2 and J3-1 sets DIS low (part is enabled).	
	Option C	Jumper on J3-2 and J3-3 sets DIS high (part is disabled).	
J4	Option A	Jumper not installed. DT pin is programmed by R10.	Option B
	Option B	Jumper on J4-2 and J4-3 sets DT pin to VCCI, bypassing the dead time circuit.	
	Option C	Jumper on J4-2 and J4-1 connects pin 6 to the optional trimmer potentiometer.	

3 Electrical Specifications

Table 3 lists the UCC21540EVM electrical specifications.

Table 3. UCC21540EVM Electrical Specifications

Description		MIN	TYP	MAX	UNIT
V_{CCI}	Primary-side power supply	3		5.5	V
V_{DDA}, V_{DDB}	Driver output power supply for UCC21540	9.2		18	V
DT	Programmable dead time range	5		10000	ns
T_J	Operating junction temperature range	–40		150	°C

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4 Test Summary

In this section, the default factory configuration for the jumper settings must be confirmed with the reference image in Figure 1. Different jumper settings, PWM signal input options, and voltage source settings are described in Section 2 and Section 3.

4.1 Equipment

4.1.1 Power Supplies

Three DC power supplies with voltage/current above 18 V and 1 A, respectively are required, for example: Agilent E3634A.

4.1.2 Function Generators

One 2-channel function generator over 20 MHz is required, for example: Tektronix AFG3252.

4.2 Equipment Setup

4.2.1 DC Power Supply Settings

- DC power supply 1
  - Voltage setting: 5 V
  - Current limit: 0.05 A
- DC power supply 2
  - Voltage setting: 12 V
  - Current limit: 0.1 A
- DC power supply 3
  - Voltage setting: 12 V
  - Current limit: 0.1 A

4.2.2 Digital Multi-Meter (DMM) Settings

- Digital multi-meter 1:
  - DC current measurement, auto-range.
- Digital multi-meter 2:
  - DC current measurement, auto-range.

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4.2.3 Two-Channel Function Generator Settings

Table 4 lists the 2-channel function generator settings.

Table 4. Two-Channel Function Generator Settings

	Mode	Frequency	Duty	Delay	High	Low	Output Impedance
Channel 1	Pulse	200 kHz	50%	0 µs	3.3 V	0 V	High Z
Channel 2				2.5 µs			

4.2.4 Oscilloscope Setting

Table 5 lists the oscilloscope setting.

Table 5. Oscilloscope Settings

	Bandwidth	Coupling	Termination	Scale Settings	Inverting
Channel 1	500 MHz or above	DC	1 MΩ or automatic	10× or automatic	Off
Channel 2					

4.2.5 Jumper (Shunt) Settings

The jumper on header J3 should be installed between pins J3-2 and J3-1 to enable the part for testing. The jumper on header J4 may be installed between pins J4-2 and J4-3 to bypass dead time functionality, installed between pins J4-2 and J4-1 to program the dead time using on-board potentiometer R2, or removed to program dead time using SMT resistor R10 (see Figure 1). Note that R10 is not populated by default; if the J4 jumper is removed and R10 is not populated, the UCC21540 dead time function is bypassed by default. Other SOIC-16 wide body dual channel isolated gate drivers may behave differently. Refer to the component datasheet for more dead time programming information.

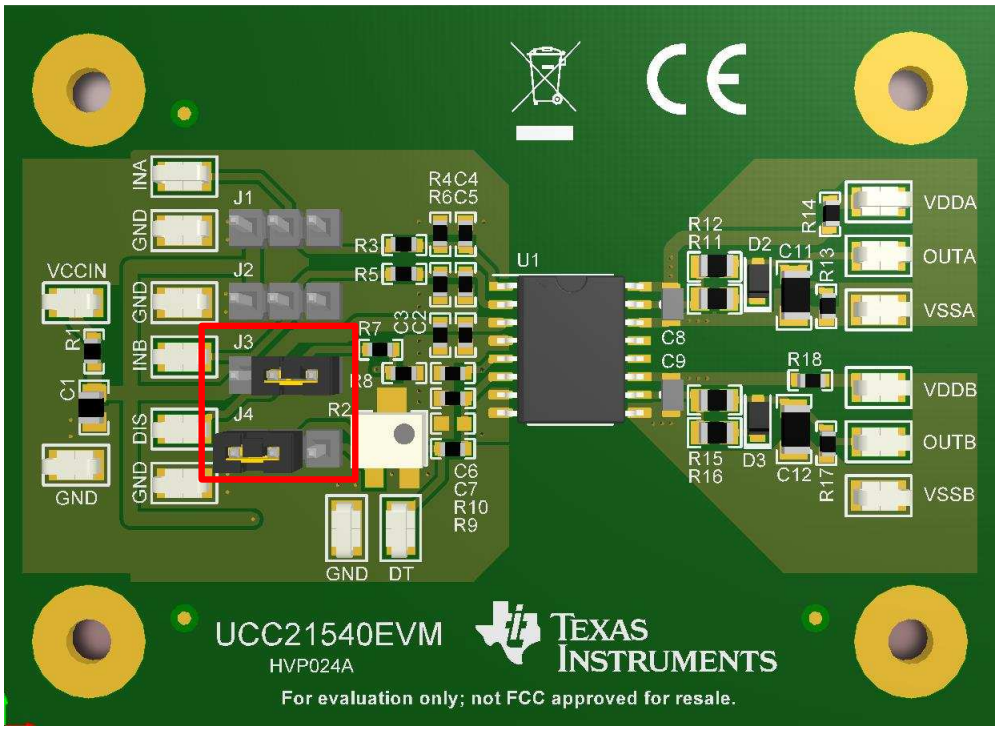


Figure 1. Jumpers Installation Position

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4.2.6 Bench Setup Diagram

The current bench setup diagram includes the function generator and oscilloscope connections.

Follow this connection procedure, Figure 2 can be used as a reference.

1. Ensure the output of the function generator and voltage sources are disabled before connection.
2. Connect the function generator channel 1 to TP3 (INA) and TP4 (GND), see Figure 2.
3. Connect the function generator channel 2 to TP5 (INB) and TP6 (GND), see Figure 2.
4. Power supply 1: Connect the positive lead to TP1 (VCCIN). Connect the negative lead to TP2 (GND).
5. Power supply 2: Connect the positive lead to the current meter input of DMM1, and connect the current meter output of DMM1 to TP11 (VDDA). Connect the negative lead directly to TP13 (VSSA).
6. Power supply 3: Connect the positive lead to the current meter input of DMM2, and connect the current meter output of DMM2 to TP14 (VDDB). Connect the negative lead directly to TP16 (VSSB).
7. Connect the oscilloscope channel 1 probe to TP12 (OUTA) and TP13 (VSSA). The probe loop area should be minimized.
8. Connect the oscilloscope channel 2 probe to TP15 (OUTB) and TP16 (VSSB). The probe loop area should be minimized.

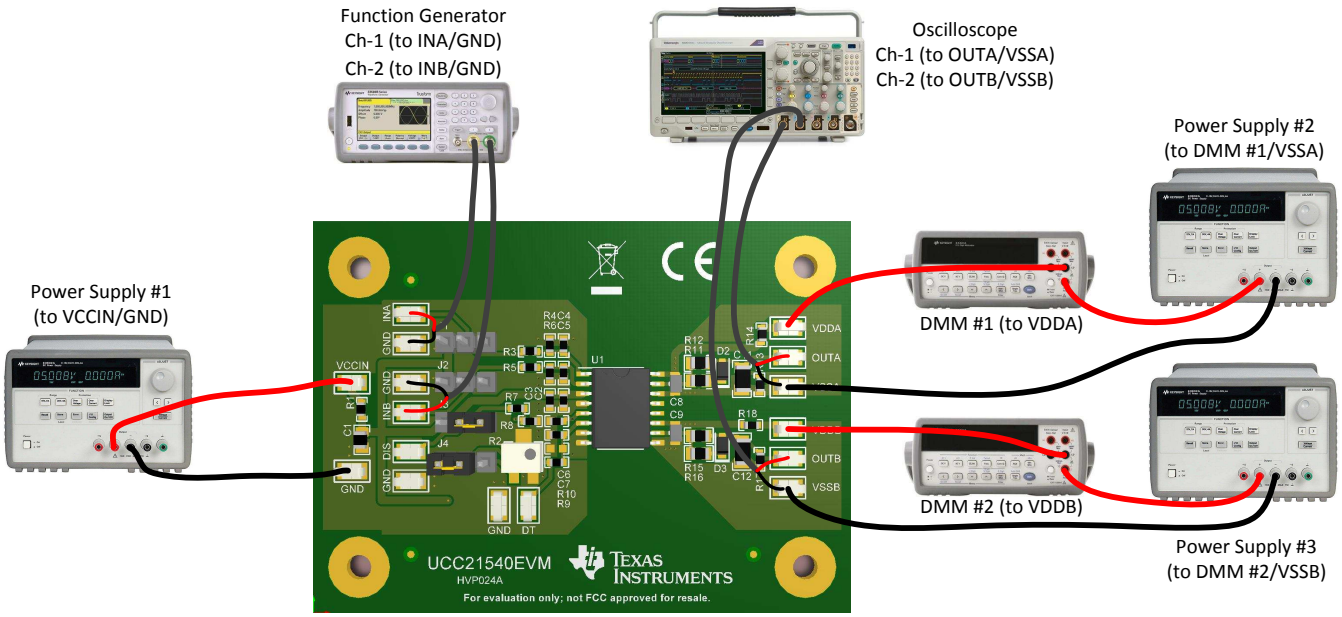


Figure 2. Bench Setup Diagram and Configuration

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5 Power Up and Power Down Procedure

5.1 Power Up

1. Before proceeding with the power up test procedure, ensure that the steps in Section 4.2.6 are complete. Then, Figure 3 can be used as a reference for the expected behavior of the EVM. Figure 3 assumes J4 is left in the default position, bypassing the dead time feature.
2. Enable power supply 1.
3. Enable power supplies 2 and 3. The quiescent current on DMM1 and DMM2 should be approximately 1 mA to 3 mA if everything is set correctly.
4. Enable the function generator outputs.
5. Verify that the following occurs:
    1. Stable pulse output appears on channel 1 and channel 2 in the oscilloscope, see Figure 3.
    2. Oscilloscope frequency measurement matches programmed function generator frequency.
    3. DMM1 and DMM2 currents should read 3.4 ± 0.5 mA with the default 1-nF load installed. For more information about the operating current, see the applications section of the UCC21540 data sheet.

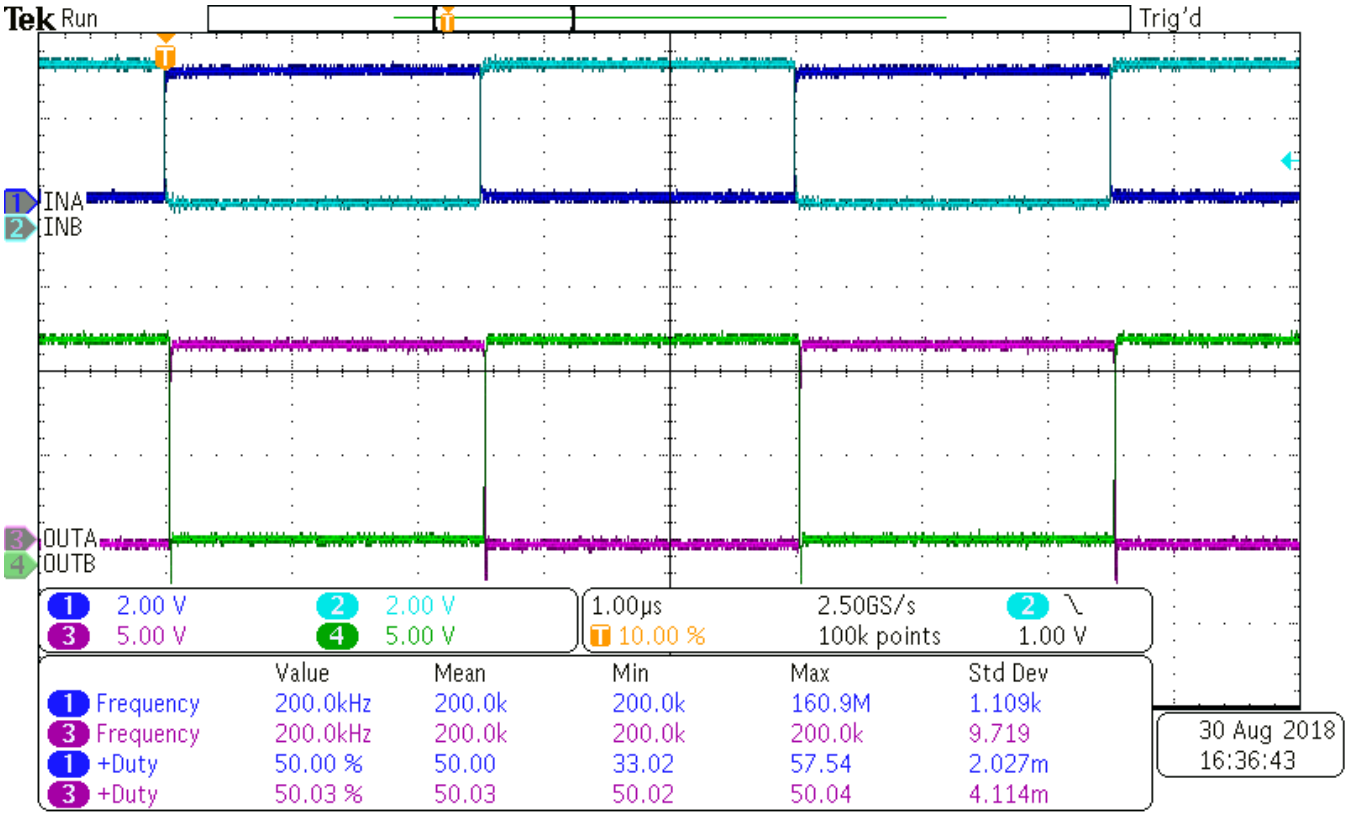


Figure 3. Example Input and Output Waveforms (Inputs: CH1 and CH2, Outputs: CH3 and CH4)

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Figure 4 shows a zoomed-in view of the example input and output waveforms.

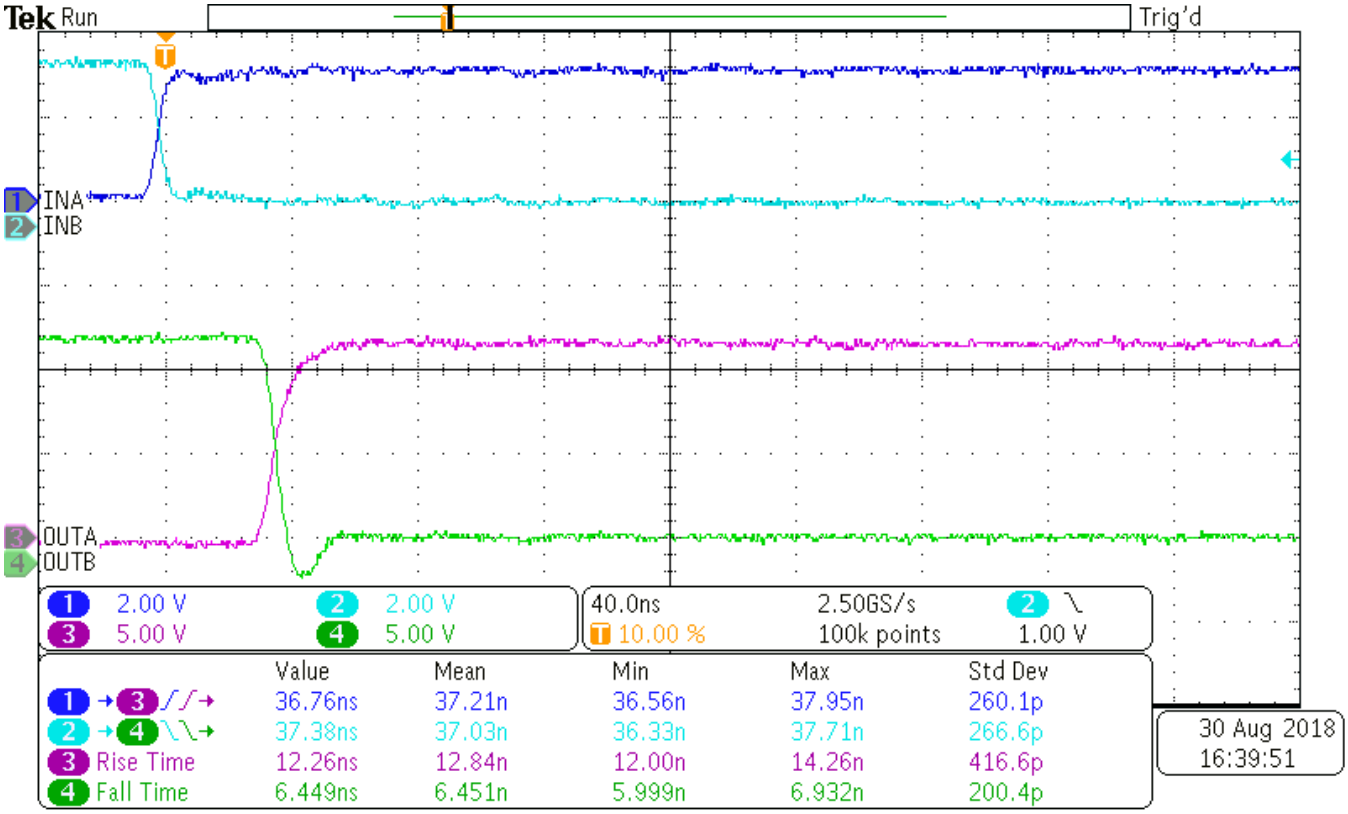


Figure 4. Example Input and Output Waveforms, Zoom In (Inputs: CH1 and CH2, Outputs: CH3 and CH4)

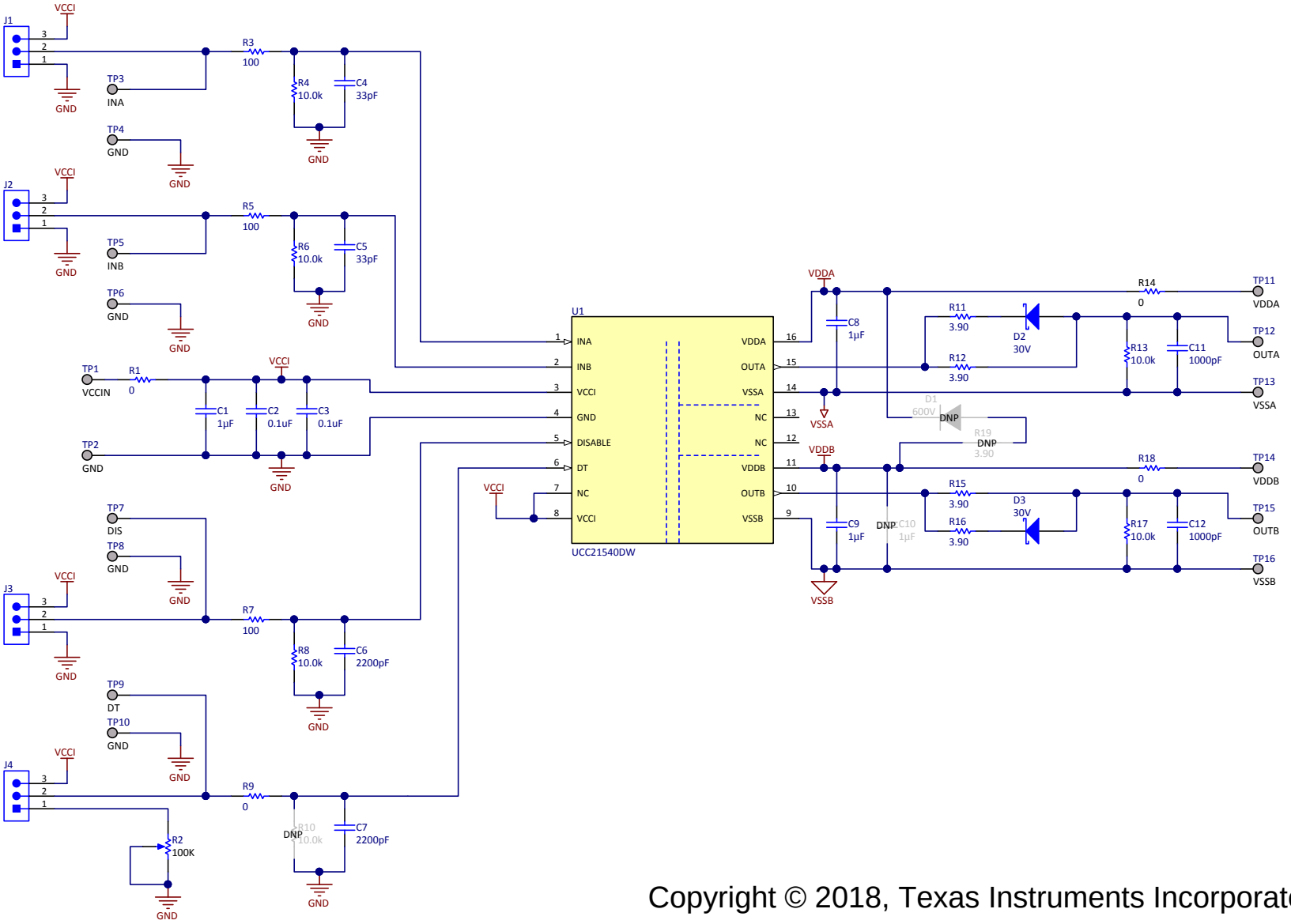
5.2 Power Down

The following list describes the procedure to power down the EVM.

1. Disable the function generator.
2. Disable power supplies 2 and 3.
3. Disable power supply 1.
4. Disconnect the cables and probes.

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6 Schematic



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Figure 5. UCC21540EVM Schematic

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7 Layout Diagrams

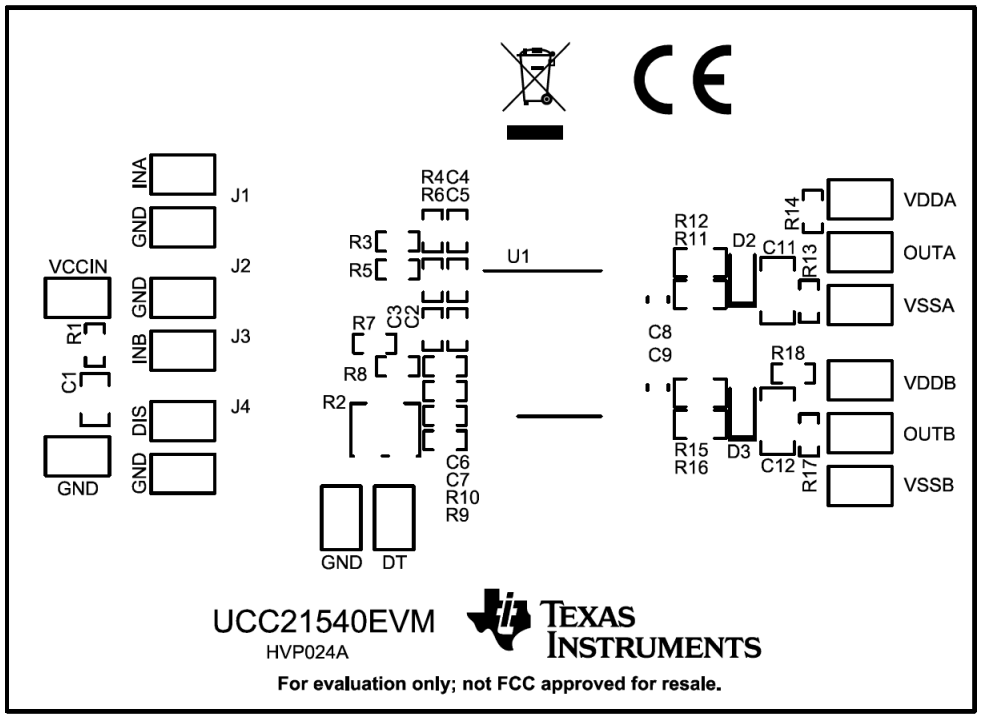


Figure 6. Top Overlay

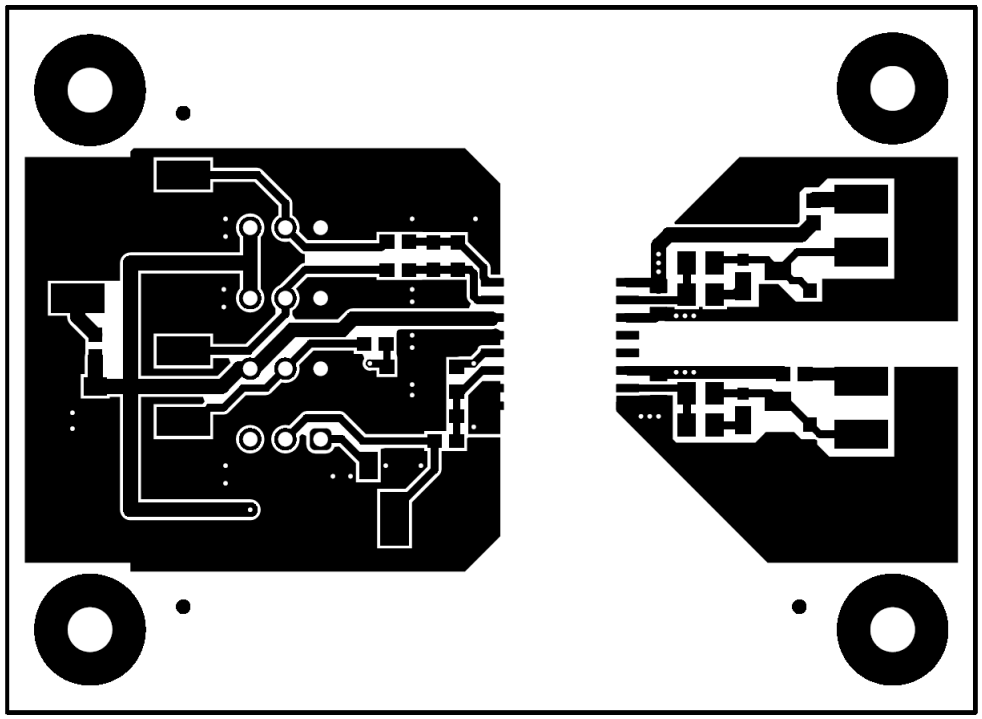


Figure 7. Top Layer

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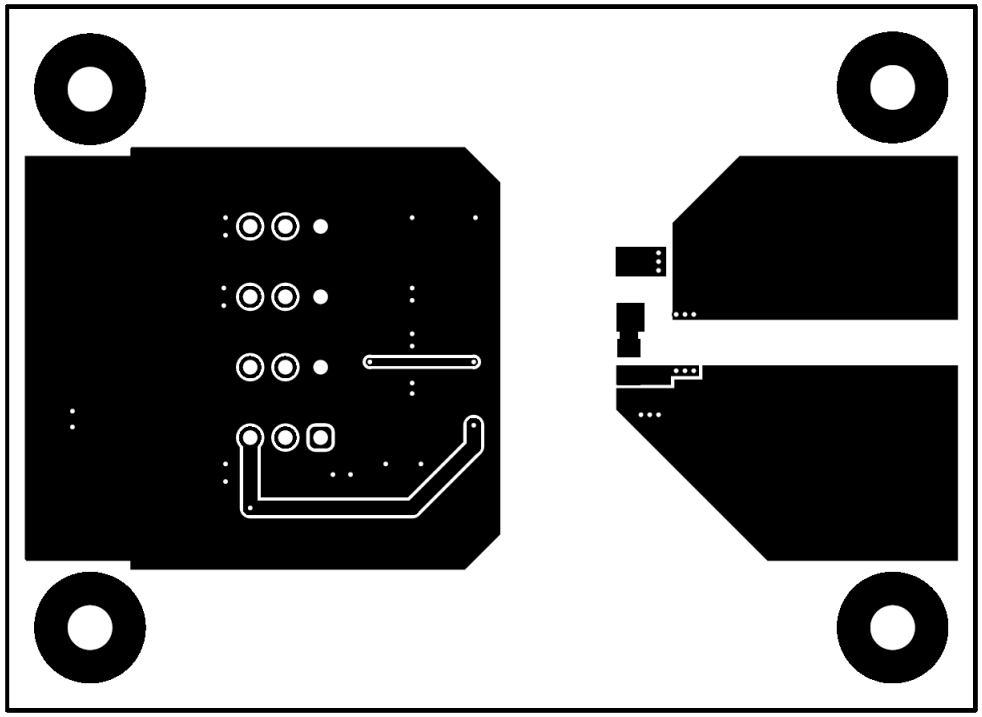


Figure 8. Bottom Layer

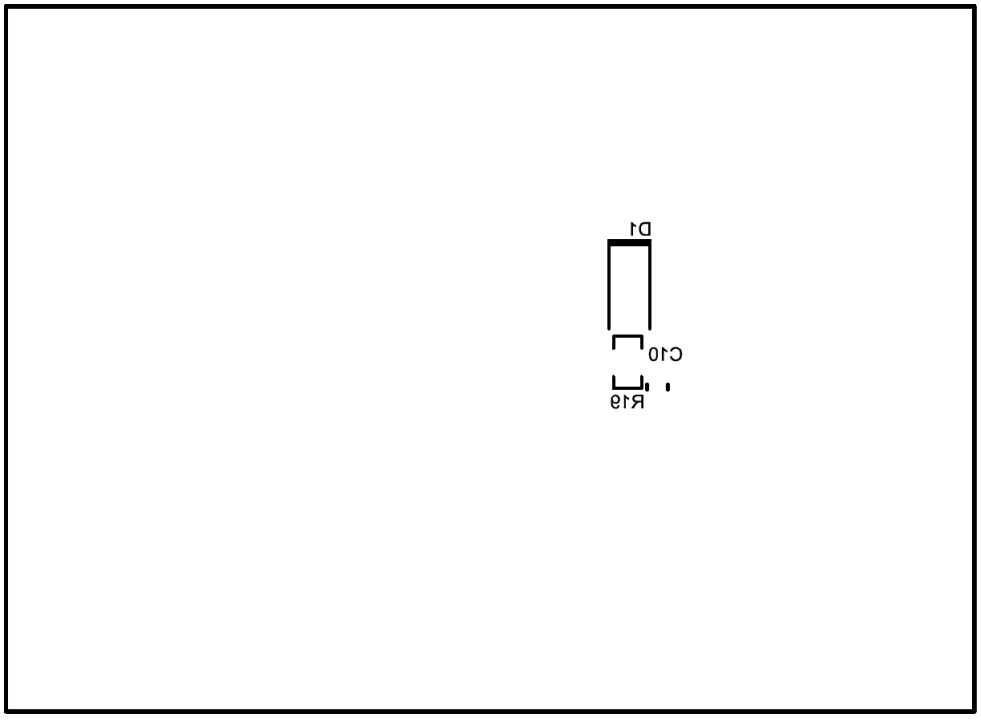


Figure 9. Bottom Overlay

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8 Bill of Materials

Table 6. UCC21540EVM List of Materials

QTY	Designator	Description
3	C1, C8, C9	Capacitor, ceramic, 1 μF, 50 V, ± 10%, X7R, 0805
2	C2, C3	Capacitor, ceramic, 0.1 μF, 25 V, ± 10%, X7R, 0603
2	C4, C5	Capacitor, ceramic, 33 pF, 50 V, ± 5%, C0G/NP0, 0603
2	C6, C7	Capacitor, ceramic, 2200 pF, 50 V, ± 10%, C0G/NP0, 0603
2	C11, C12	Capacitor, ceramic, 1000pF, 50 V, ± 5%, C0G/NP0, 1206
2	D2, D3	Diode, Schottky, 30 V, 1 A, MicroSMP
4	J1, J2, J3, J4	Header, 100 mil, 3 × 1, TH
4	R1, R9, R14, R18	Resistor, 0 Ω, 0%, 0.25 W, 0603
1	R2	Trimmer, 100 kΩ, 0.25W, SMD
3	R3, R5, R7	Resistor, 100 Ω, 1%, 0.1 W, 0603
5	R4, R6, R8, R13, R17	Resistor, 10.0 kΩ, 1%, 0.1 W, 0603
4	R11, R12, R15, R16	Resistor, 3.90 Ω, 1%, 0.125 W, 0805
2	SH-J3, SH-J4	Shunt, 100 mil, Gold plated, Black
16	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	Test point, miniature, SMT
1	U1	4-A, 6-A, 5.7-kV_{RMS} isolated dual-channel gate driver with dead time, DW0016A (SOIC-16 Wide Body)
0	C10	Capacitor, ceramic, 1 μF, 50 V, ± 10%, X7R, 0805
0	D1	Diode, Ultrafast, 600 V, 1 A, SMA
0	H1, H2, H3, H4	Standoff, Hex, 0.5"L #4-40 Nylon
0	H5, H6, H7, H8	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead
0	R10	Resistor, 10.0 kΩ, 1%, 0.1 W, 0603
0	R19	Resistor, 3.90 Ω, 1%, 0.125 W, 0805

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