Using the UCC21225AEVM-365

User's Guide



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Using the UCC21225AEVM-365

1 Introduction

UCC21225AEVM-365 evaluation module is designed for evaluation of UCC21225A, a member of TI's isolated dual-channel gate driver family with 4-A source and 6-A sink peak current for driving Si MOSFETs, IGBTs and wide-bandgap devices, i.e. SiC and GaN transistors. Developed for applications where isolation and reliability are required and board space is at a premium, the UCC21225A delivers reinforced isolation of 2.5 kV_{RMS} and a surge immunity tested up to 3535 V along with a common mode transient immunity (CMTI) greater than 100 V/ns. It has the industry's fastest propagation delay of 19 ns and the tightest channel-to-channel delay matching of less than 5 ns which enables high-switching frequency, high-power density and efficiency. The UCC21225A is available in a 5-mm x 5-mm LGA, offering more than 3x reduction in footprint size compared to industry-standard 16-SOIC drivers.

The flexible, universal capability of the UCC21225A with up to 18-V VCCI and 25-V VDDA/VDDB allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver with dual PWM input. UCC21225AEVM-365 demonstrates the integrated components, advanced protection features (UVLO, dead time and disable) and optimized switching performance of the UCC21225A, enabling designers to build smaller, more robust designs for enterprise, telecom, automotive and industrial applications and allowing for faster time to market. To evaluate other Iso-Drivers, it is recommended to read the datasheet thoroughly before switching the part in the EVM covered by this user guide.

2 Description

The UCC21225AEVM-365 evaluation board uses surface mount test points to expose VCCI, VDDA and VDDB. 3-position headers with jumpers are available for easy access to the dead time (DT) programming and disable function (DIS), allowing designers to easily evaluate different protection functions. A variety of testing points support key feature probing of the UCC21225A. Moreover, the PCB layout is optimized with minimized loop area in each gate driver loop and power supply loop with bypassing capacitors. For detailed device information, please refer to the UCC21225A datasheet and TI's Isolated gate driver solutions.

2.1 Features

- Evaluation module for the low-voltage features of UCC21225A in 5mm x 5mm LGA-13 (NPL) package
- 3-V to 18-V VCCI power supply range, and up to 25-V VDDA/VDDB power supply range
- 4-A and 6-A source/sink current capability
- TTL/CMOS compatible inputs
- On-board resistor for dead-time programming
- 3-position header for DT and disable
- PCB layout optimized for power supply bypassing cap, gate driver loop
- Optional capacitive load and external gate drive resistor/diode for power/thermal testing
- Test points allow probing all the key pins of the UCC21225AEVM-365

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2.2 I/O Description

Table 1. Test Points and Jumper Pins

PINS	DESCRIPTION
VIN	VCCI positive input
GND	VCCI negative input, PWMINx negative input, and primary ground at U1
VINA	VDDA positive input
GNDA	VSSA negative input
VINB	VDDB positive input
GNDB	VSSB negative input
PWMINA	Channel A PWM signal input
PWMINB	Channel B PWM signal input
INA	Filtered input to Channel A
INB	Filtered input to Channel B
DIS	Disable pin measurement
DT	Deadtime pin measurement
J1-1	Primary ground
J1-2	Disable signal input
J1-3	Primary VCC
J2-1	Connects to deadtime resistor
J2-2	Deadtime programming pin
J2-3	Primary VCC
VCC	Primary VCC
VDDA	VDDA at U1
VSSA	VSSA at U1
VDDB	VDDB at U1
VSSB	VSSB at U1
OUTA	Channel A output at U1
OUTB	Channel B output at U1
LDA	Output at optional capacitive load CLDA
LDB	Output at optional capacitive load CLDB

2.3 Jumper Settings

Table 2. Jumper Settings

Header	JUMPER SETTING OPTIONS		FACTORY SETTING
J1	Option A:	Jumper not installed. The device under test is enabled when left open on disable pin.	Option C
	Option B:	Jumper on J1-2 and J1-3, connecting DIS to VCCI. The device under test is disabled.	
	Option C:	Jumper on J1-2 and J1-1, connecting DIS to GND. The device under test is enabled.	
J2	Option A:	Jumper not installed. Dead time is internally set to <15ns.	Option B
	Option B:	Jumper on J2-2 and J2-3 allows driver output overlap. Dead time is set by the input source for PWMINA and PWMINB.	
	Option C:	Jumper on J2-1 and J2-2 sets dead time by DT (in ns) = R_{DT} (in kΩ) × 10. By default a 20-kΩ resistor RDT programs a 200 ns dead time. For better noise immunity and dead time matching, a 10 nF bypass capacitor C4 is included from the DT pin to GND.	

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3 Electrical Specifications

Table 3. UCC21225AEVM-365 Electrical Specifications

DESCRIPTION		MIN	TYP	MAX	UNIT
V_{CCI}	Primary-side power supply	3		18	V
V_{DDA}, V_{DDB}	Driver output power supply	9.2		25	V
F_S	Switching frequency	0		5	MHz
T_J	Operating junction temperature range	–40		125	°C

NOTE: The UCC21225AEVM-365 is designed for low voltage evaluation only, and is not certified for evaluation with voltages beyond the absolute maximums listed in the electrical specifications. **Do not evaluate high voltage parameters with this board.**

4 Test Summary

Different jumper settings, PWM signal input options and voltage source settings can be found in Section 2 and Section 3.

4.1 Definitions

This procedure details how to configure the UCC21225AEVM-365 evaluation board. Within this test procedure the following naming conventions are followed. Refer to the UCC21225AEVM-365 Bench Setup and Test Diagram, Figure 2, for details.

V_{xx}: External voltage supply name.

DMM: Digital multi-meters.

DUT: Device under test

EVM: Evaluation module assembly.

4.2 Equipment

4.2.1 Power Supplies

Three DC power supplies with voltage/current above 25 V/1 A, for example: Agilent E3634A

4.2.2 Function Generators

One two-channel function generator over 20 MHz, for example, Tektronics AFG3252

4.3 Equipment Setup

4.3.1 DC Power Supply Settings

- DC power supply #1
  - Voltage setting: 5 V
  - Current limit: 0.05 A
- DC power supply #2
  - Voltage setting: 15 V
  - Current limit: 0.1 A
- DC power supply #3
  - Voltage setting: 15 V
  - Current limit: 0.1 A

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4.3.2 Digital Multi-Meter Settings

- Digital multi-meter #1
  - DC current measurement, auto-range
- Digital multi-meter #2
  - DC current measurement, auto-range

4.3.3 Two-Channel Function Generator Settings

Table 4. Two-Channel Function Generator Settings

	MODE	FREQUENCY	DUTY	DELAY	HIGH	LOW	OUTPUT IMPEDANCE
Channel A	Pulse	DC ~ 5 MHz	50%	0 ns	3.3 V	0 V	High Z
Channel B				100 ns			

4.3.4 Oscilloscope Settings

Table 5. Oscilloscope Settings

	BANDWIDTH	COUPLING	TERMINATION	SCALE SETTINGS	INVERTING
Channel A	500 MHz or above	DC	1 MΩ or automatic	10× or automatic	OFF
Channel B					

4.3.5 Jumper Settings

Ensure that the two shunts are installed on the jumpers as follows:

1. Shunt #1 on header *J1* on pin 1-2 as shown in Figure 1.
2. Shunt #2 on header *J2* on pin 2-3 as shown in Figure 1.

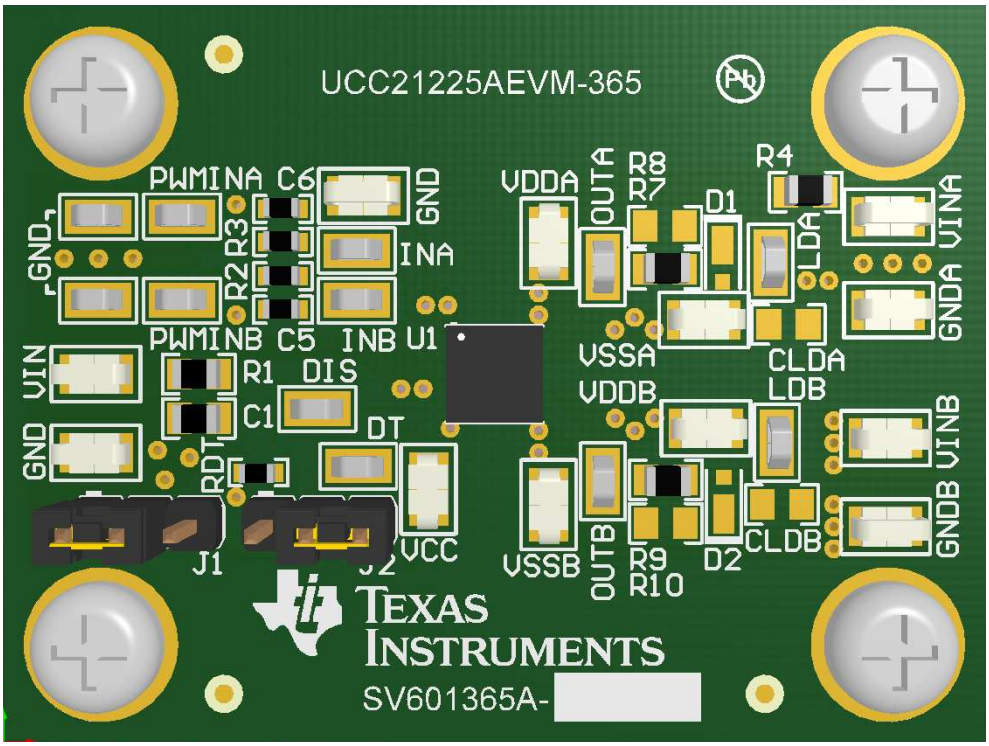


Figure 1. Jumpers Installation Position

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4.3.6 Bench Setup Diagram

The bench setup diagram includes the function generator and oscilloscope connections.

Please follow the connection procedure below, and Figure 2 can be used as a reference.

- Make sure the output of the function generator and power supplies are disabled before connection.
- Apply function generator channel-A on PWMINA/GND.
- Apply function generator channel-B on PWMINB/GND.
- Power supply #1: apply positive lead to test point VIN, and negative lead to nearby test point GND.
- Power supply #2: apply positive lead to current input of DMM #1 and current output of DMM #1 to test point VINA; apply negative lead to test point GNDA.
- Power supply #3: apply positive lead to current input of DMM #2 and current output of DMM #2 to test point VINB; apply negative lead to test point GNDB.
- Apply oscilloscope channel-A probes on OUTA/VSSA, minimizing the loop area as much as possible.
- Apply oscilloscope channel-B probes on OUTB/VSSB, minimizing the loop area as much as possible.

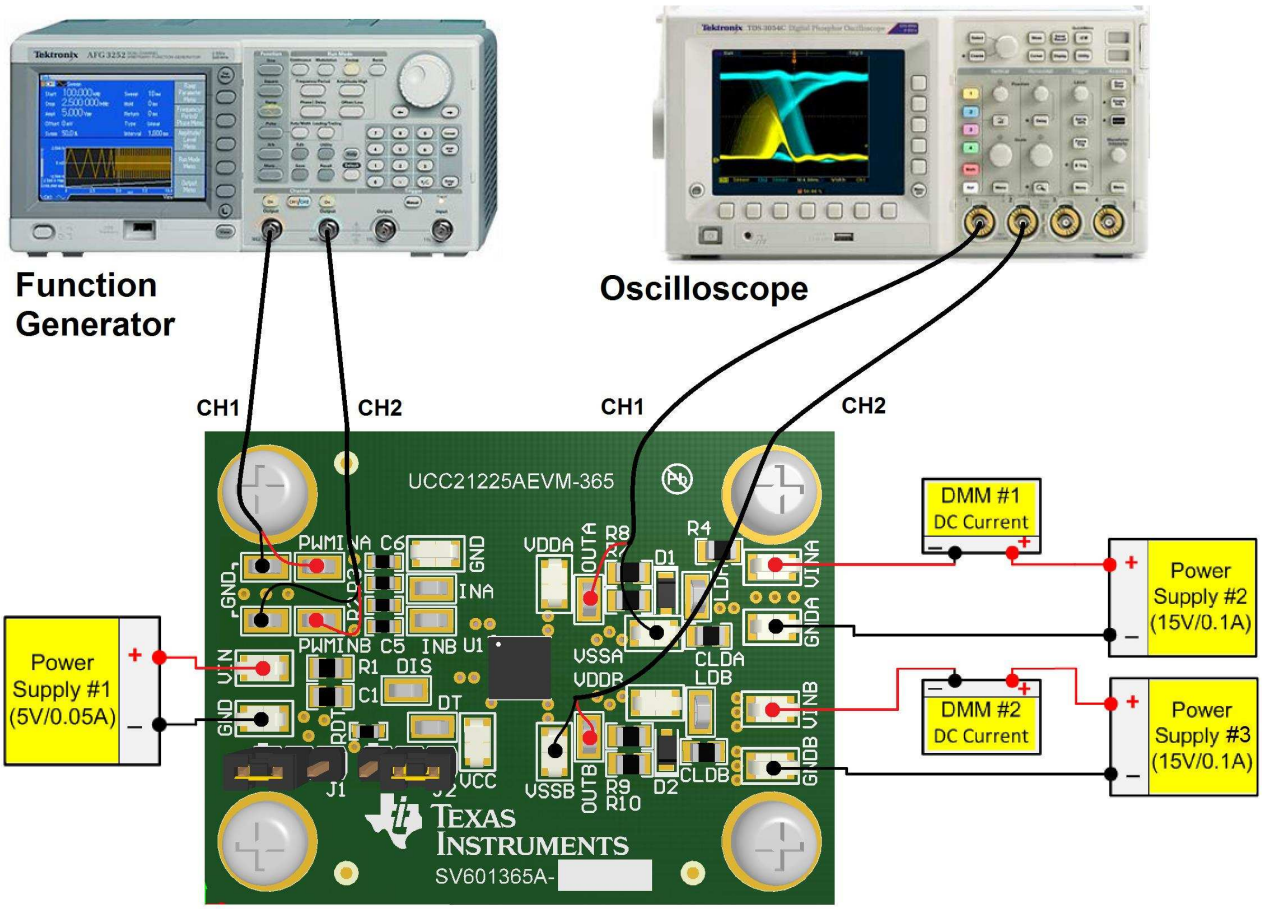


Figure 2. Bench Setup Diagram and Configuration

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5 Power Up, Disable Function, and Power Down Procedure

5.1 Power Up

1. Before beginning the power up test procedure, verify the connections with the Section 4.3.6.
2. Enable supply #1.
3. Enable supply #2 and #3, the quiescent current on DMM1 and DMM2 ranges in 2 mA ± 1 mA if everything is set correctly.
4. Enable function generator outputs channel-A and channel-B.
5. There will be:
   (a) Stable pulse output on the channel-A and channel-B in the oscilloscope, refer to Figure 3;
   (b) Scope frequency measurement is equal to the programmed function generator frequency;
   (c) DMM #1 and #2 should display around 10 mA, ±2 mA under no load conditions. For more information about operating current, please refer to UCC21225A Datasheet.

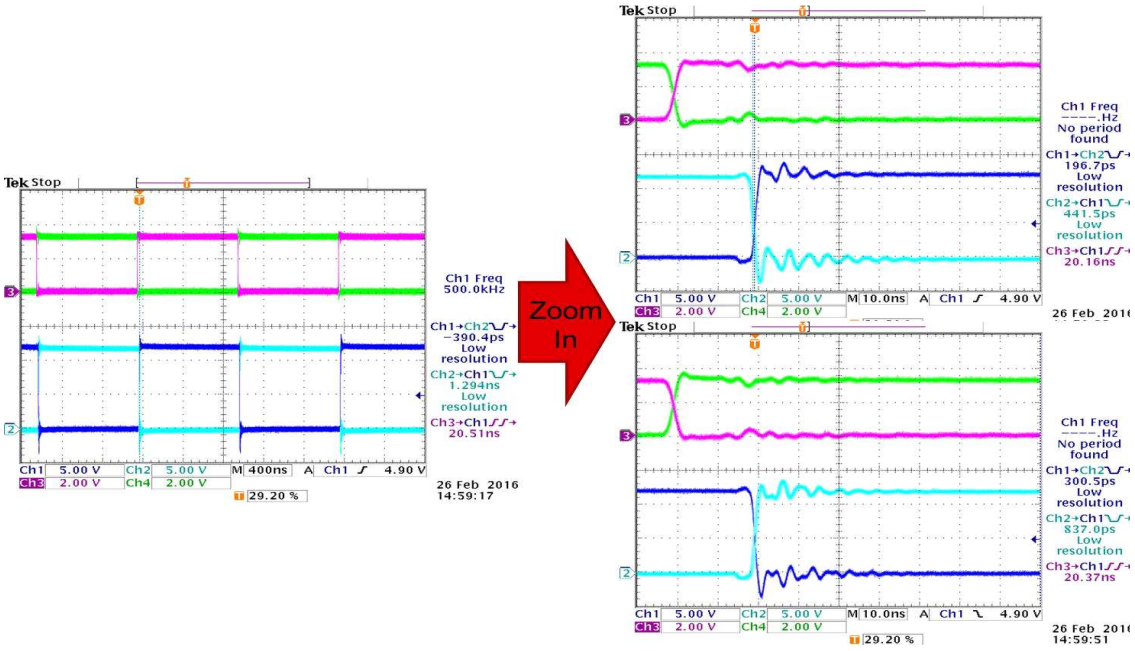


Figure 3. Example Input and Output Waveforms
(Green/Magenta are PWM Inputs, Blue/Cyan are Driver Outputs)

5.2 Disable Function

Carefully remove the jumper connecting J1-1 and J1-2, and replace it to connect J1-2 and J1-3. There should no longer be an output present on the oscilloscope, and the DMMs should read 2 mA ± 1 mA. To continue evaluation, return J1 jumper to original setting.

5.3 Power Down

1. Disable function generator.
2. Disable power supply #2 and #3.
3. Disable power supply #1.
4. Disconnect cables and probes.

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6 Test Waveforms (C_L = 0 pF) with Different DT Configurations

6.1 DT Pin Floating or Left Open (J2 Option A in Table 2)

The dead time between two channels' output is around 8 ns, which is preset for interlock protections, see Figure 4.

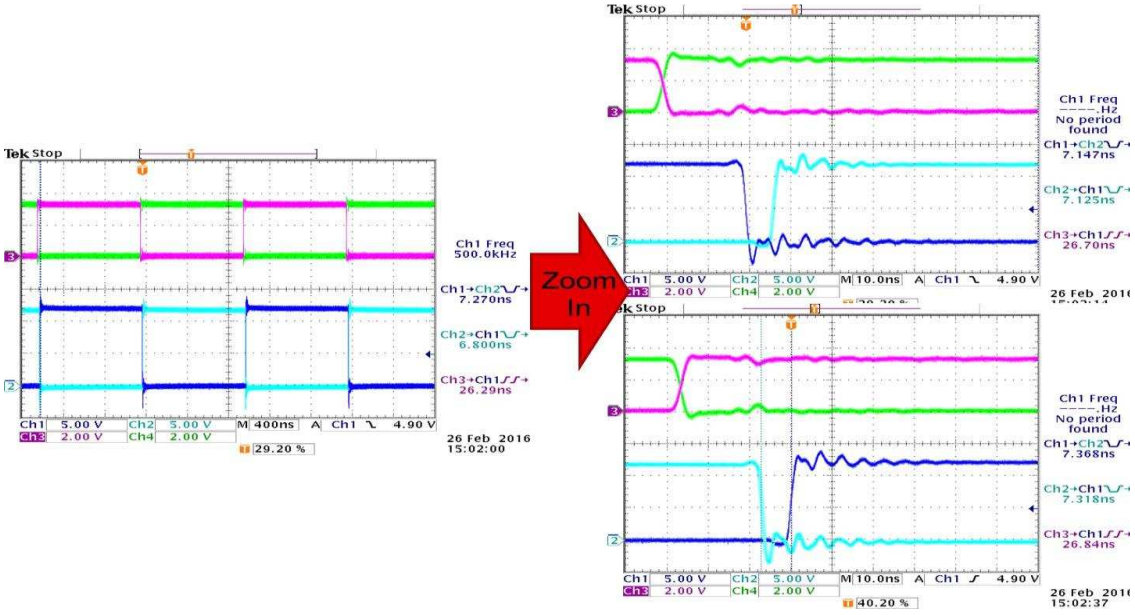


Figure 4. Test Waveforms if DT is Left Open
(Green/Magenta are PWM Inputs, Blue/Cyan are Driver Outputs)

6.2 DT Connected to VCCI (J2 Option B in Table 2)

The dead time between two channels' output is decided by inputs, see Figure 5. Overlap between two output channels is allowed. Figure 5 shows a waveform with overlapped operations.

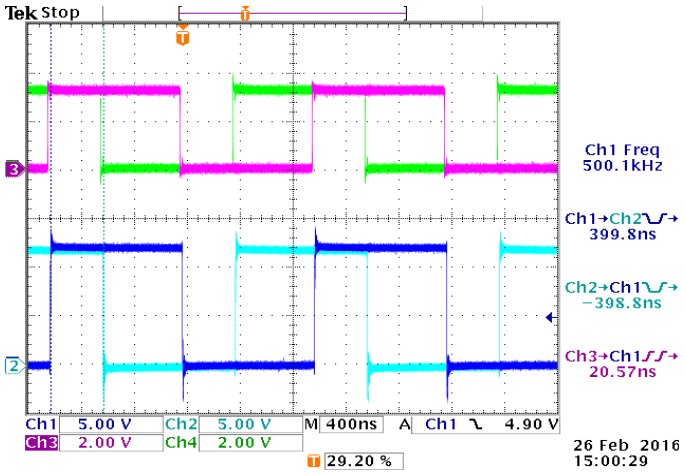


Figure 5. Overlap is Allowed when DT Connected to VCCI
(Green/Magenta are PWM Inputs, Blue/Cyan are Driver Outputs)

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6.3 DT Pin Connected to RDT (J2 Option C in Table 2)

The dead time between two channels' output is set according to: DT (in ns) = 10 × RDT (in kΩ). By default, the onboard dead time resistor programs 200 ns dead time.

The steady state voltage at DT pin is around 0.8 V, and the DT pin current will be less than 10 µA when R_{DT} ≥ 100 kΩ. Consequently, as R_{DT} increases, the steady state DT pin current will be susceptible to noise, which can degrade dead time accuracy. It is recommended that a ceramic bypass capacitor, 2.2 nF or above, is placed in parallel with R_{DT} to achieve better noise immunity and better dead time matching between two channels, especially when the dead time is larger than 300 ns. For added convenience, a 10nF bypass capacitor C4 is already present on the EVM, immediately next to J2 on the underside of the board.

Figure 6 shows a waveform with a 40.2 kΩ resistor used for R_{DT}, corresponding to 400 ns dead time.

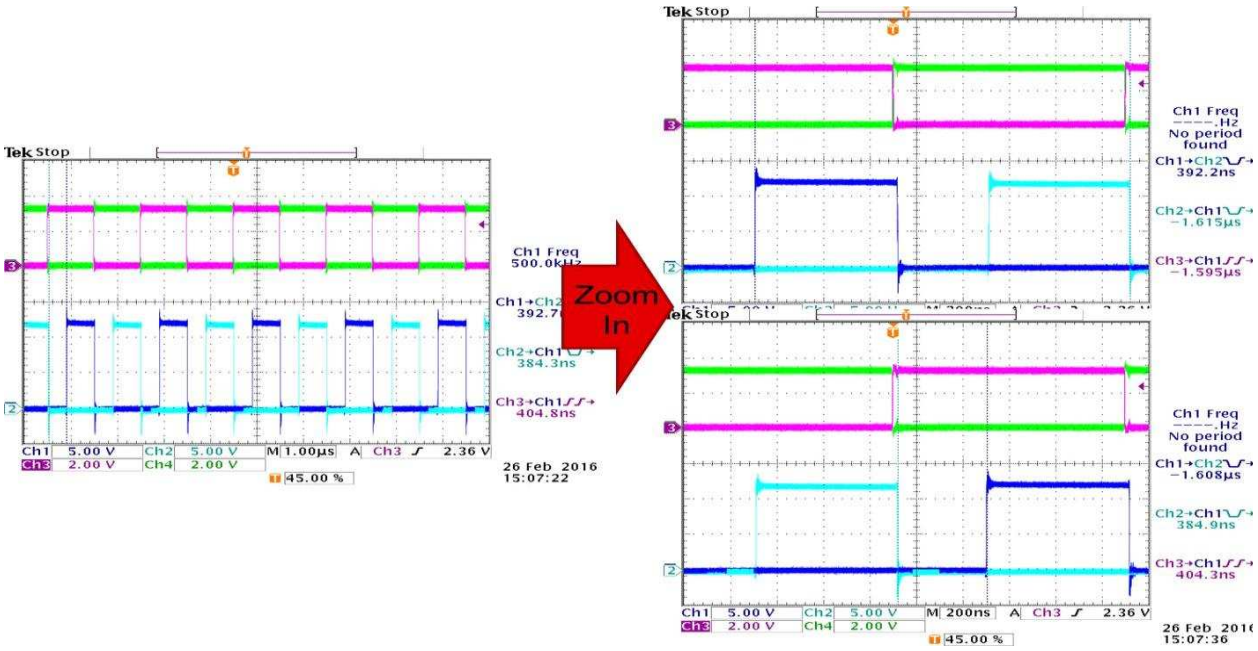


Figure 6. Test Waveforms if DT Connected to R_{DT} (Green/Magenta are PWM Inputs, Blue/Cyan are Driver Outputs)

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7 Schematic

Figure 7 shows the schematic diagram for the UCC21225AEVM-365.

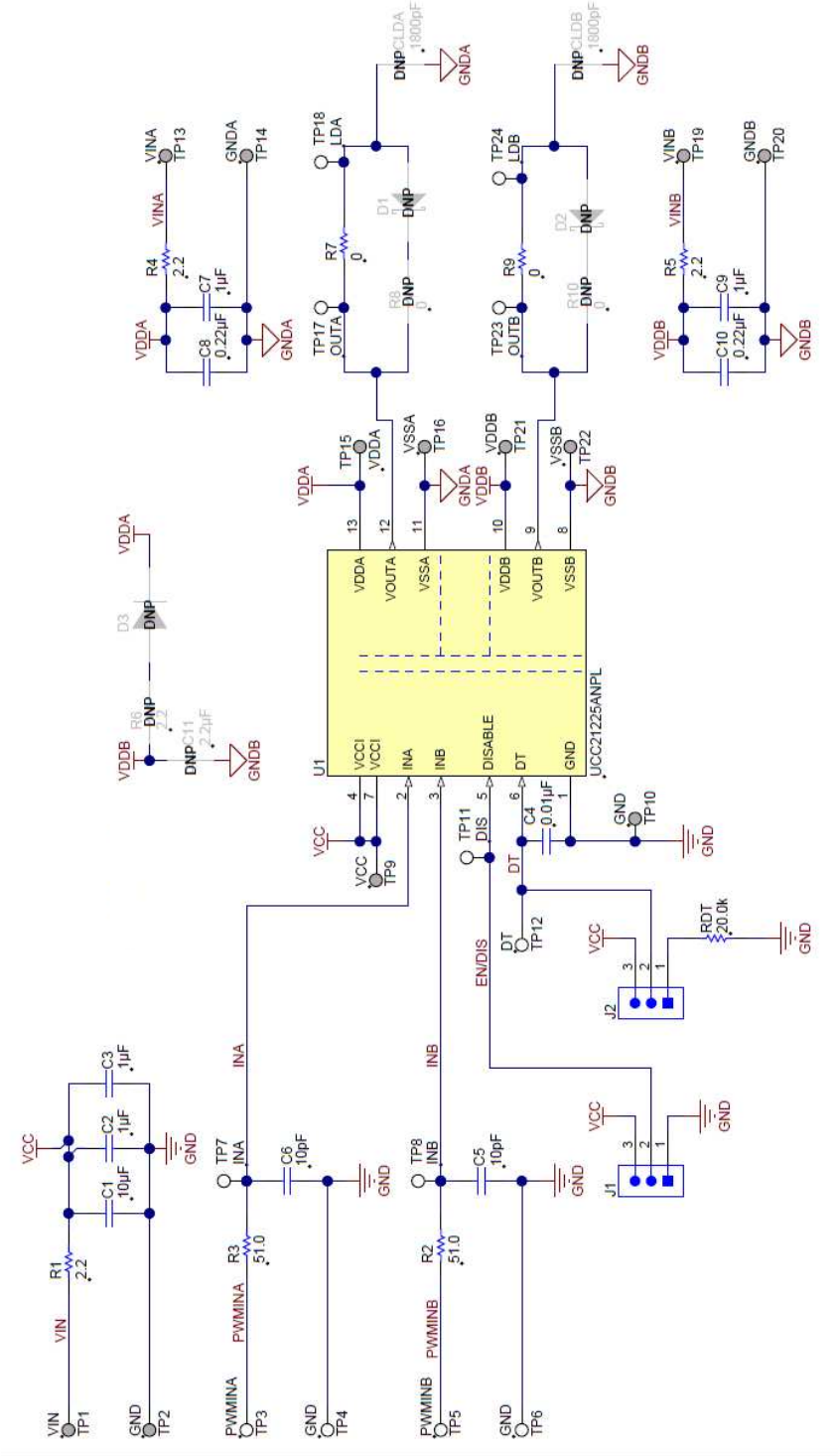


Figure 7. UCC21225AEVM-365 Schematic

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8 Layout Diagrams

The PCB layout information for UCC21225AEVM-365 is shown in Figure 8, Figure 9, Figure 10 and Figure 11.

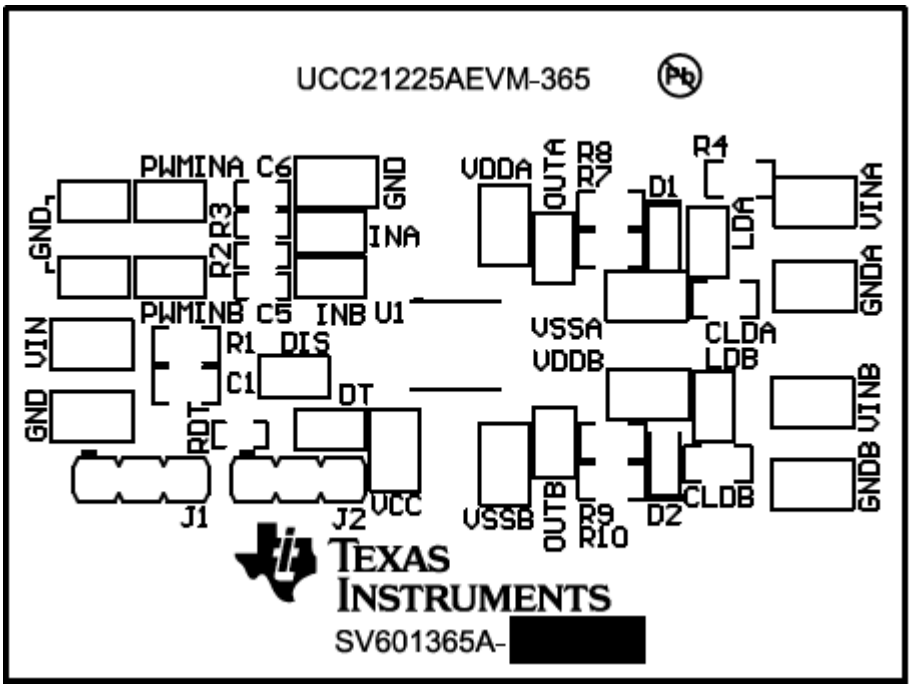


Figure 8. Top Overlay

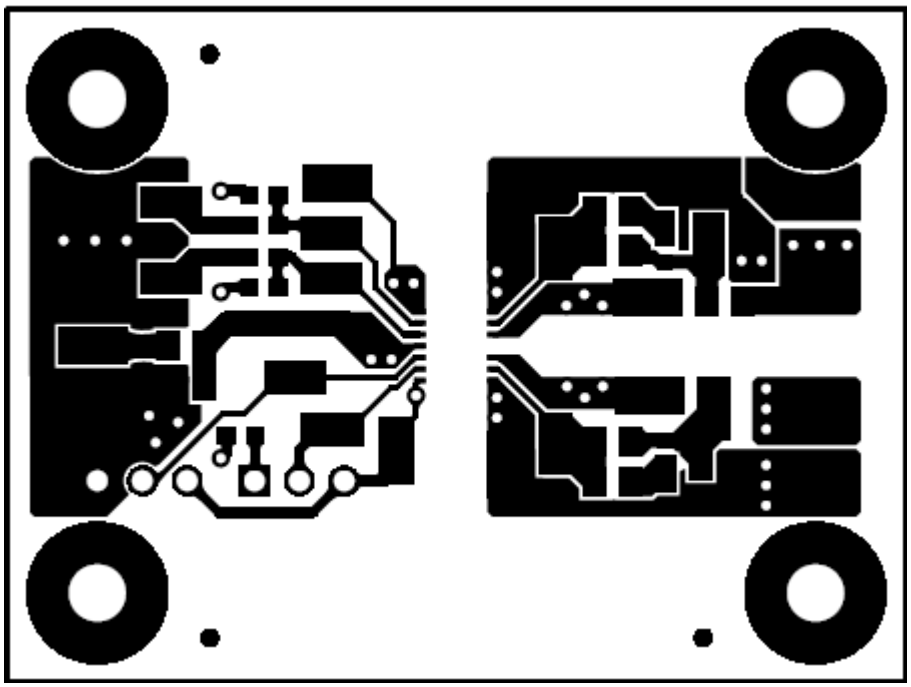


Figure 9. Top Layer

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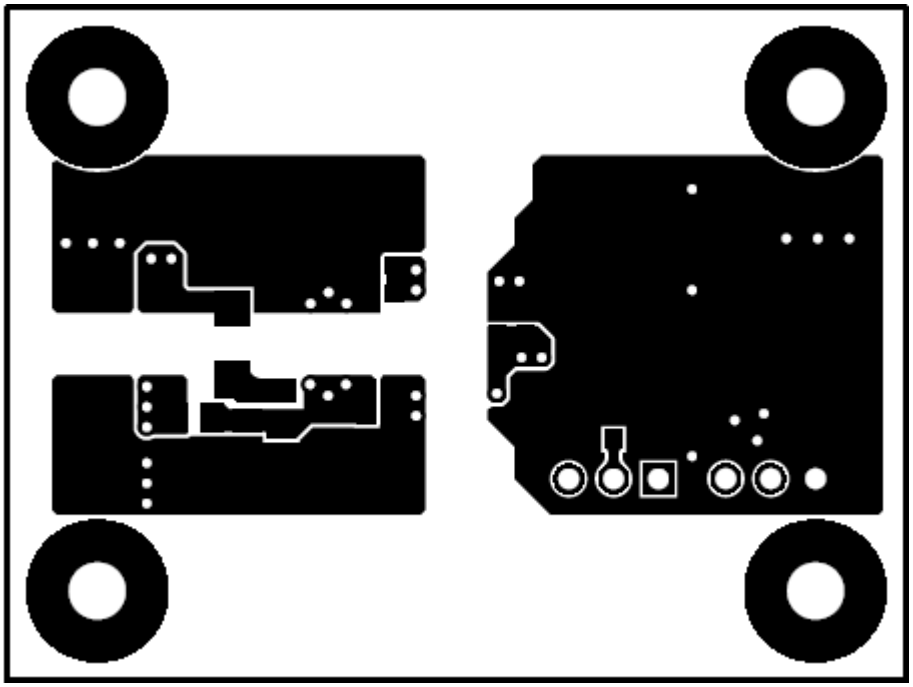


Figure 10. Bottom Layer (Flipped)

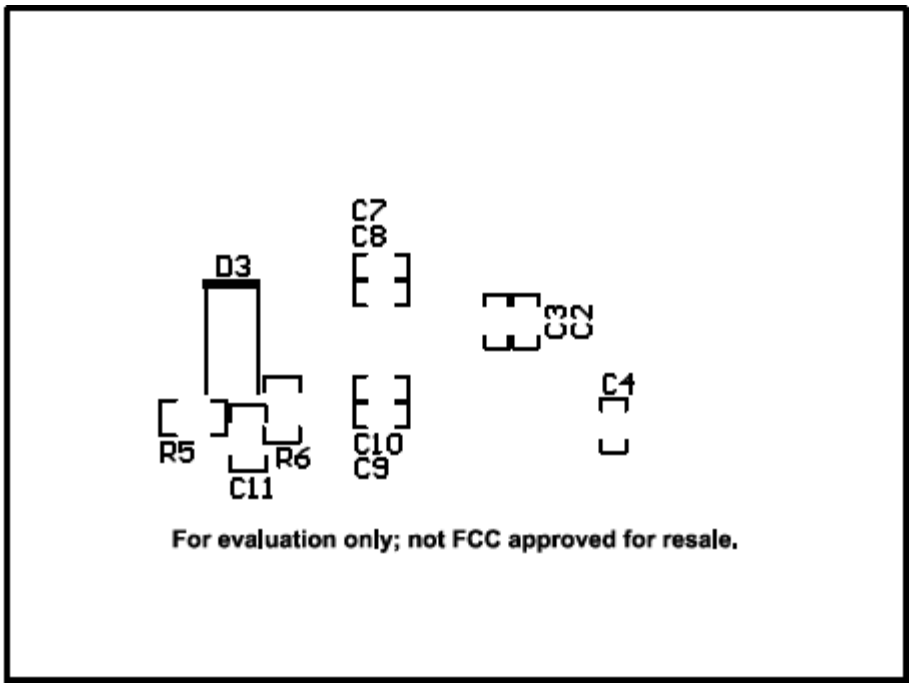


Figure 11. Bottom Overlay (Flipped)

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9 List of Materials

Table 6. UCC21225AEVM-365 List of Materials

QTY	DES	DESCRIPTION	MANUFACTURE	PART NUMBER
1	C1	Capacitor, ceramic, 10 µF, 35 V, ±10%, X5R, 0805	TDK	C2012X5R1V106K 085AC
4	C2, C3, C7, C9	Capacitor, ceramic, 1 µF, 50 V, ±10%, X5R, 0603	TDK	C1608X5R1H105K 080AB
1	C4	Capacitor, ceramic, 0.01 µF, 50 V, ±10%, X7R, 0603	Samsung Electro-Mechanics	CL10B103KB8NC NC
2	C5, C6	Capacitor, ceramic, 10 pF, 50 V, ±5%, C0G/NP0, 0603	Kemet	C0603C100J5GAC TU
2	C8, C10	Capacitor, ceramic, 0.22 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCM188R71H224 KA64D
4	H1, H2, H3, H4	Machine screw, round, #4-40 x 1/4, nylon, philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH
4	H5, H6, H7, H8	Standoff, hex, 0.5"L #4-40 nylon	Keystone	1902C
2	J1, J2	Header, 2.54 mm, 3x1, Gold, TH	Wurth Elektronik	61300311121
3	R1, R4, R5	Resistor, 2.2 Ω, 5%, 0.125 W, 0805	Yageo America	RC0805JR-072R2L
2	R2, R3	Resistor, 51.0 Ω, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0751RL
2	R7, R9	Resistor, 0 Ω, 5%, 0.125 W, 0805	Yageo America	RC0805JR-070RL
1	RDT	Resistor, 20.0 kΩ, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0720KL
2	SH-J1, SH-J2	Shunt, 100mil, gold plated, black	Samtec	SNT-100-BK-G
12	TP1, TP2, TP9, TP10, TP13, TP14, TP15, TP16, TP19, TP20, TP21, TP22	Test point, miniature, SMT	Keystone	5019
12	TP3, TP4, TP5, TP6, TP7, TP8, TP11, TP12, TP17, TP18, TP23, TP24	Test point, miniature, SMT	Keystone	5015
1	U1	4A/6A Isolated Dual-Channel Gate Driver, NPL0013A (VLGA-13)	Texas Instruments	UCC21225ANPL
DNP	CLDA, CLDB	Capacitor, ceramic, 1800 pF, 50V, ±5%, C0G/NP0, 0805	MuRata	GRM2165C1H182J A01D
DNP	D1, D2	Diode, Schottky, 30 V, 1 A, AEC-Q101, MicroSMP	Vishay-Semiconductor	MSS1P3L-M3/89A
DNP	D3	Diode, Ultrafast, 600 V, 1 A, AEC-Q101, SMA	ON Semiconductor	MURA160T3G
DNP	R6	Resistor, 2.2 Ω, 5%, 0.125 W, 0805	Yageo America	RC0805JR-072R2L
DNP	R8, R10	Resistor, 0 Ω, 5%, 0.125 W, 0805	Yageo America	RC0805JR-070RL

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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