UNITRODE

UC1637
UC2637
UC3637

Switched Mode Controller for DC Motor Drive

FEATURES

- Single or Dual Supply Operation
- ±2.5V to ±20V Input Supply Range
- ±5% Initial Oscillator Accuracy; ± 10% Over Temperature
- Pulse-by-Pulse Current Limiting
- Under-Voltage Lockout
- Shutdown Input with Temperature Compensated 2.5V Threshold
- Uncommitted PWM Comparators for Design Flexibility
- Dual 100mA, Source/Sink Output Drivers

DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with ±100mA output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

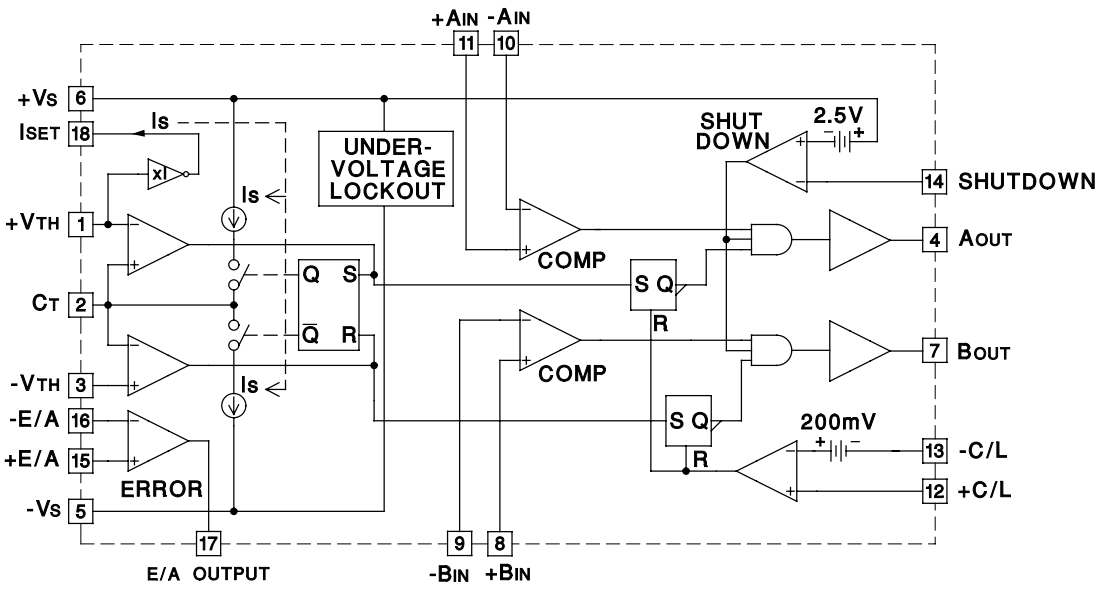
The UC1637 is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC2637 and UC3637 are characterized for -25°C to +85°C and 0°C to +70°C, respectively.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (±Vs)	±20V
Output Current, Source/Sink (Pins 4, 7)	500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11 12, 13, 14, 15, 16)	±Vs
Error Amplifier Output Current (Pin 17)	±20mA
Oscillator Charging Current (Pin 18)	-2mA
Power Dissipation at T_A = 25°C (Note 2)	1000mW
Power Dissipation at T_C = 25°C (Note 2)	2000mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	+300°C

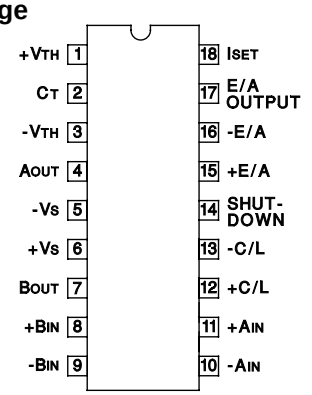
Note 1: Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

BLOCK DIAGRAM

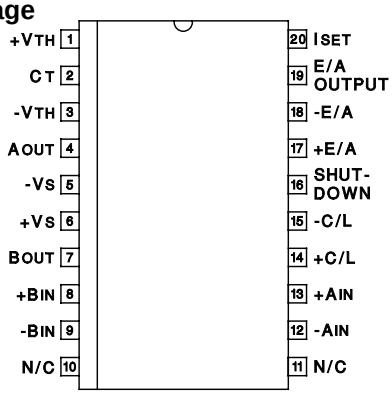


CONNECTION DIAGRAM

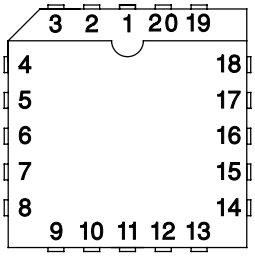
DIL-18 (TOP VIEW)
J or N Package



SOIC-20 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
+VTH	1
CT	2
-VTH	3
AOUT	4
-VS	5
N/C	6
+VS	7
BOUT	8
+BIN	9
-BIN	10
-AIN	11
+AIN	12
+C/L	13
-C/L	14
SHUTDOWN	15
N/C	16
+E/A	17
-E/A	18
E/A OUTPUT	19
ISET	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; $+V_S$ = +15V, $-V_S$ = - 15V, $+V_{TH}$ = 5V, $-V_{TH}$ = -5V, R_T = 16.7kΩ, C_T = 1500pF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator								
Initial Accuracy	T_J = 25°C (Note 6)	9.4	10	10.6	9	10	11	kHz
Voltage Stability	V_S = ±5V to ±20V, $V_{PIN\ 1}$ = 3V, $V_{PIN\ 3}$ = -3V		5	7		5	7	%
Temperature Stability	Over Operating Range (Note 3)		0.5	2		0.5	2	%
$+V_{TH}$ Input Bias Current	$V_{PIN\ 2}$ = 6V	-10	0.1	10	-10	0.1	10	µA
$-V_{TH}$ Input Bias Current	$V_{PIN\ 2}$ = 0V	-10	-0.5		-10	-0.5		µA
$+V_{TH}$, $-V_{TH}$ Input Range		$+V_S$-2		$-V_S$+2	$+V_S$-2		$-V_S$+2	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 0V		1.5	5		1.5	10	mV
Input Bias Current	V_{CM} = 0V		0.5	5		0.5	5	µA
Input Offset Current	V_{CM} = 0V		0.1	1		0.1	1	µA
Common Mode Range	V_S = ±2.5 to 20V	$-V_S$+2		$+V_S$	$-V_S$+2		$+V_S$	V
Open Loop Voltage Gain	R_L = 10k	75	100		80	100		dB
Slew Rate			15			15		V/µS
Unity Gain Bandwidth			2			2		MHz
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	V_S = ±2.5 to ±20V	75	110		75	110		dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637: V_S = +15V, $-V_S$ = - 15V, $+V_{TH}$ = 5V, $-V_{TH}$ = -5V, R_T = 16.7kΩ, C_T = 1500pF, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier (Continued)								
Output Sink Current	$V_{PIN\ 17}$ = 0V		-50	-20		-50	-20	mA
Output Source Current	$V_{PIN\ 17}$ = 0V	5	11		5	11		mA
High Level Output Voltage		13	13.6		13	13.6		V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	V_{CM} = 0V		20			20		mV
Input Bias Current	V_{CM} = 0V		2	10		2	10	µA
Input Hysteresis	V_{CM} = 0V		10			10		mV
Common Mode range	V_S = ±5V to ±20V	$-V_S$+1		$+V_S$-2	$-V_S$+1		$+V_S$-2	V
Current Limit								
Input Offset Voltage	V_{CM} = 0V, T_J = 25°C	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			-0.2			-0.2		mV/°C
Input Bias Current		-10	-1.5		-10	-1.5		µA
Common Mode Range	V_S = ±2.5V to ±20V	$-V_S$		$+V_S$-3	$-V_S$		$+V_S$-3	V
Shutdown								
Shutdown Threshold	(Note 4)	-2.3	-2.5	-2.7	-2.3	-2.5	-2.7	V
Hysteresis			40			40		mV
Input Bias Current	$V_{PIN\ 14}$ = +V_S to -V_S	-10	-0.5		-10	-0.5		µA
Under-Voltage Lockout								
Start Threshold	(Note 5)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	I_{SINK} = 20mA		-14.9	-13		-14.9	-13	V
	I_{SINK} = 100mA		-14.5	-13		-14.5	-13	
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		
Rise Time	(Note 3) C_L = Inf, T_J = 25°C		100	600		100	600	ns
Fall Time	(Note 3) C_L = Inf, T_J = 25°C		100	300		100	300	ns

Note 3: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 4: Parameter measured with respect to +Vs (Pin 6).
Note 5: Parameter measured at +Vs (Pin 6) with respect to -Vs (Pin 5).
Note 6: R_T and C_T referenced to Ground.

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, I_{SET} and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins $+V_{TH}$ and $-V_{TH}$ respectively. The $+V_{TH}$ terminal voltage is buffered internally and also applied to the I_{SET} terminal to develop the capacitor charging current through R_T. If R_T is referenced to $-V_S$ as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.

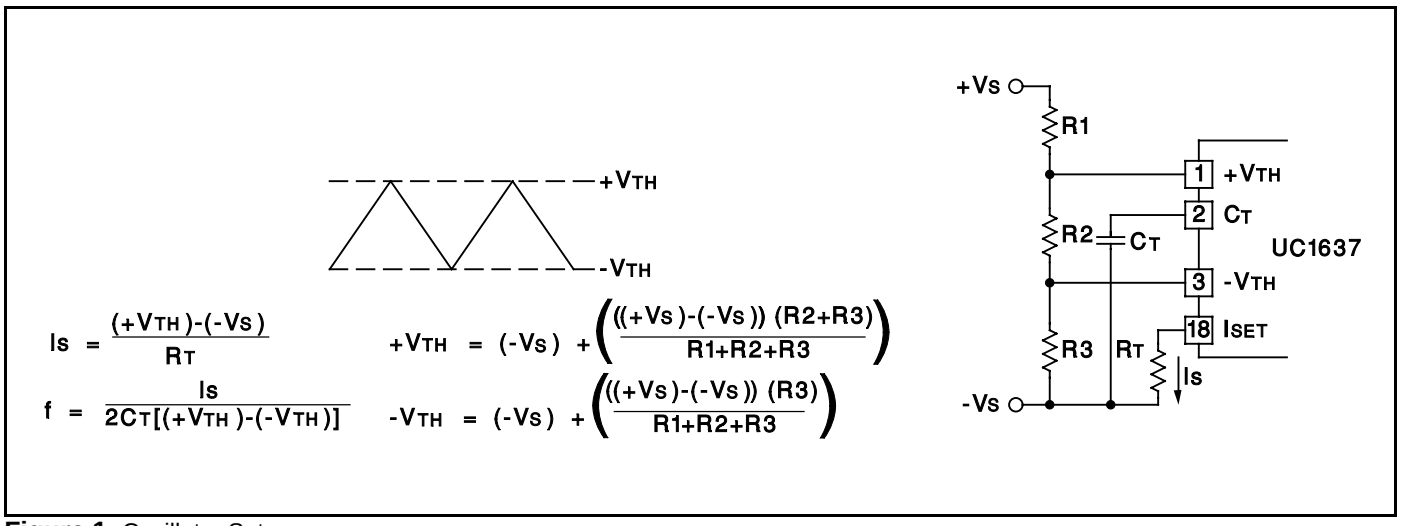


Figure 1. Oscillator Setup

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexibility. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high state of output A and shorten the high state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on Pin 9 and 11.

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 9 and Pin 11)
In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 9 > Pin 11)
A small differential voltage between Pin 9 and 11 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode
(Voltage on Pin 9 > Pin 11)
With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

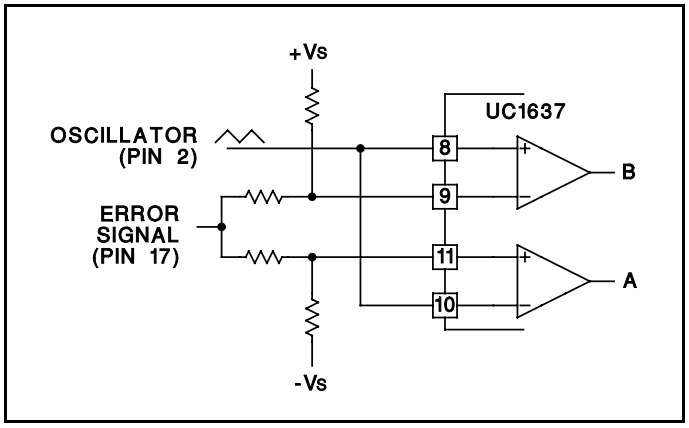


Figure 2. Comparator Biasing

Output Drivers

Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically -VS + 0.2V @50mA low level and +VS - 2.0V @50mA high level.

Error Amplifier

The error amplifier consists of a high slew rate (15V/µs) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the ±VS supply voltage, the common mode input range and the voltage output swing is within 2V of the VS supply.

Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

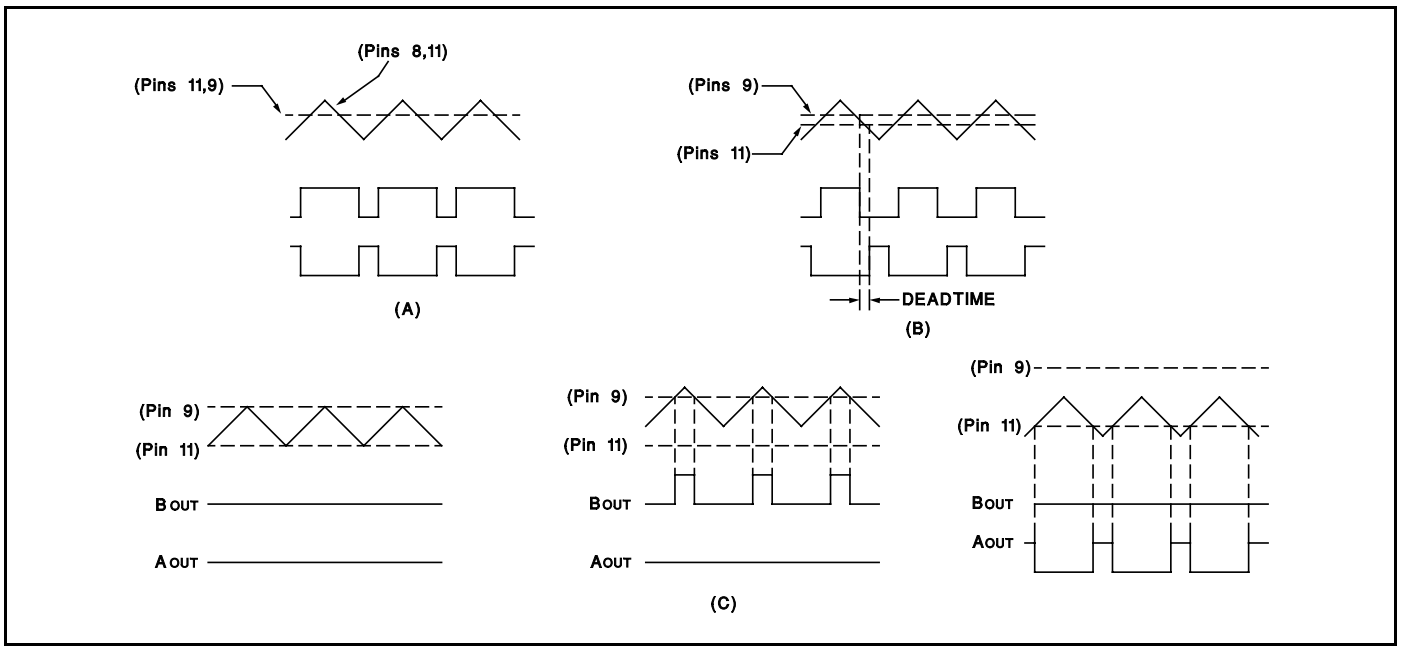


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below VIN, the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

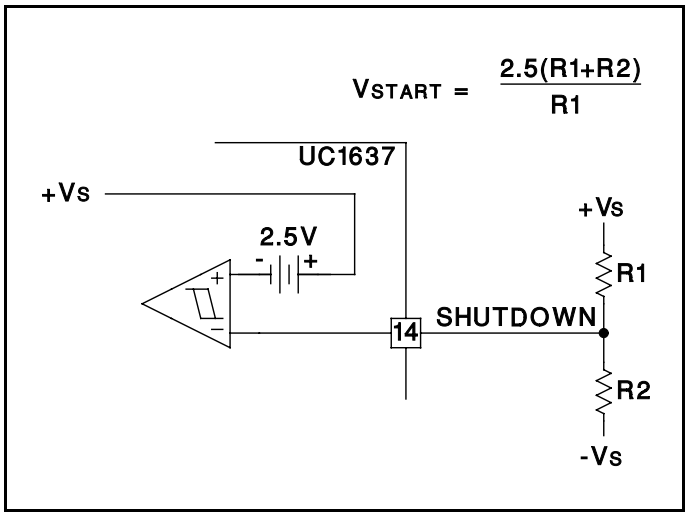


Figure 4. External Under-Voltage Lockout

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from -Vs to within 3V of the +Vs supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

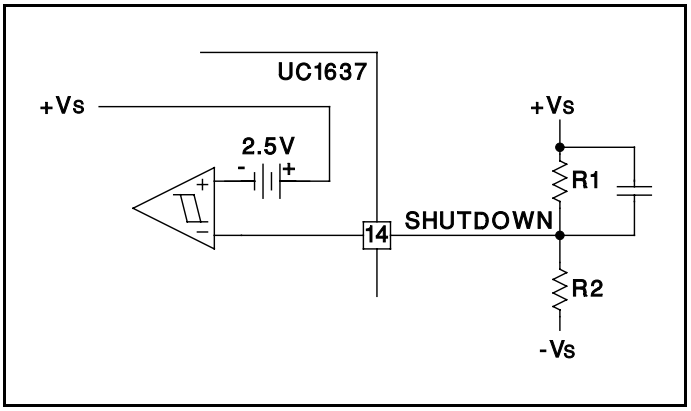


Figure 5. Delayed Start-Up

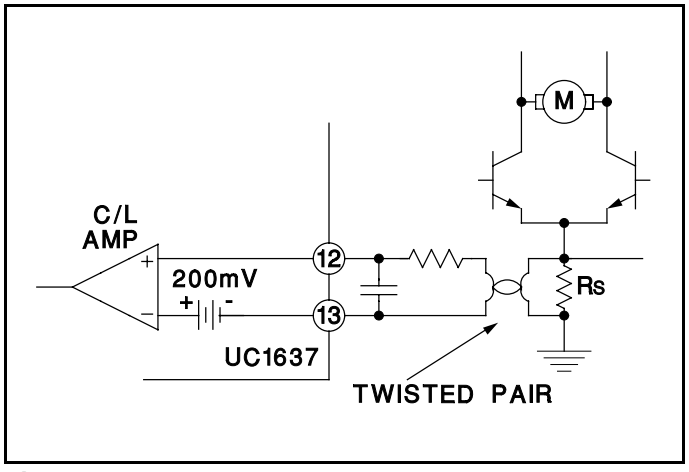


Figure 6. Current Limit Sensing

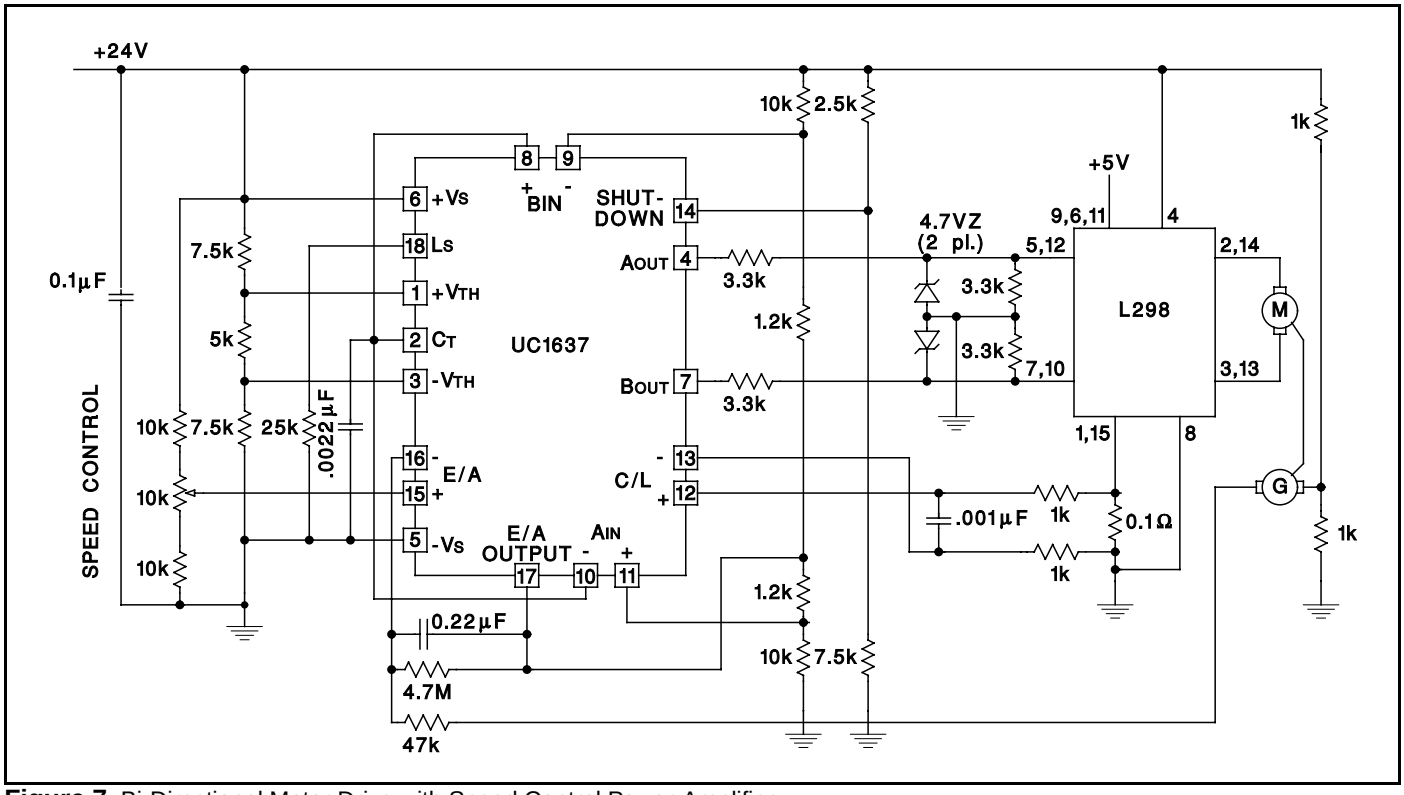


Figure 7. Bi-Directional Motor Drive with Speed Control Power-Amplifier

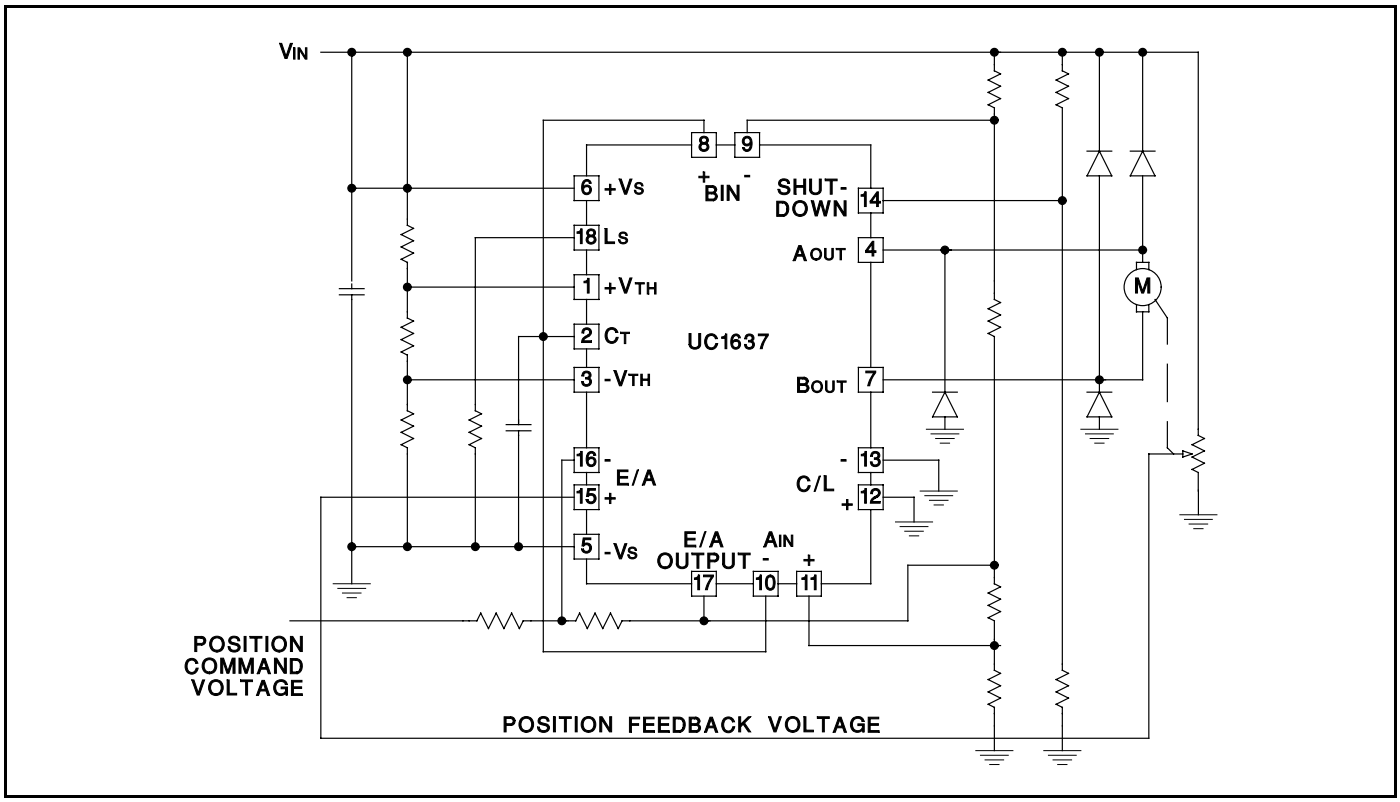


Figure 8. Single Supply Position Servo Motor Drive

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89957012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89957012A UC1637L/ 883B	Samples
5962-8995701VA	ACTIVE	CDIP	J	18	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8995701VA UC1637J/883B	Samples
UC1637J	ACTIVE	CDIP	J	18	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	UC1637J	Samples
UC1637J883B	ACTIVE	CDIP	J	18	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8995701VA UC1637J/883B	Samples
UC1637L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1637L	Samples
UC1637L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89957012A UC1637L/ 883B	Samples
UC2637DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2637DW	Samples
UC2637DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2637DW	Samples
UC2637DWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2637DW	Samples
UC2637J	ACTIVE	CDIP	J	18	1	TBD	Call TI	N / A for Pkg Type	0 to 0	UC2637J	Samples
UC2637N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-25 to 85	UC2637N	Samples
UC2637NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-25 to 85	UC2637N	Samples
UC3637DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3637DW	Samples
UC3637DWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3637DW	Samples
UC3637J	ACTIVE	CDIP	J	18	1	TBD	Call TI	N / A for Pkg Type	0 to 70	UC3637J	Samples
UC3637N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3637N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1637, UC3637, UC3637M :

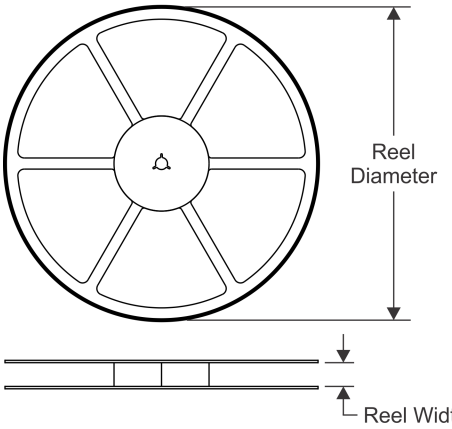
- Catalog: UC3637, UC3637M, UC3637
- Military: UC1637, UC1637
- Space: UC1637-SP

NOTE: Qualified Version Definitions:

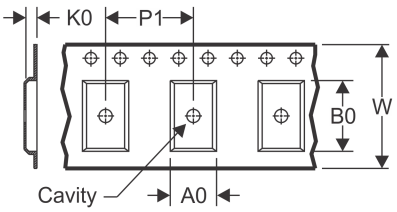
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

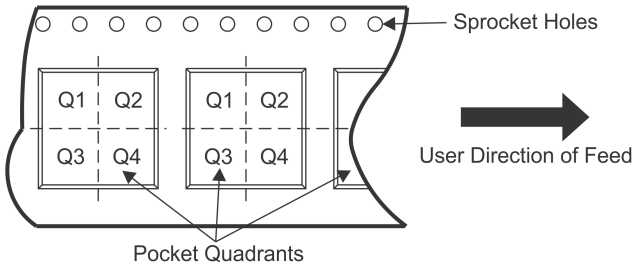


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

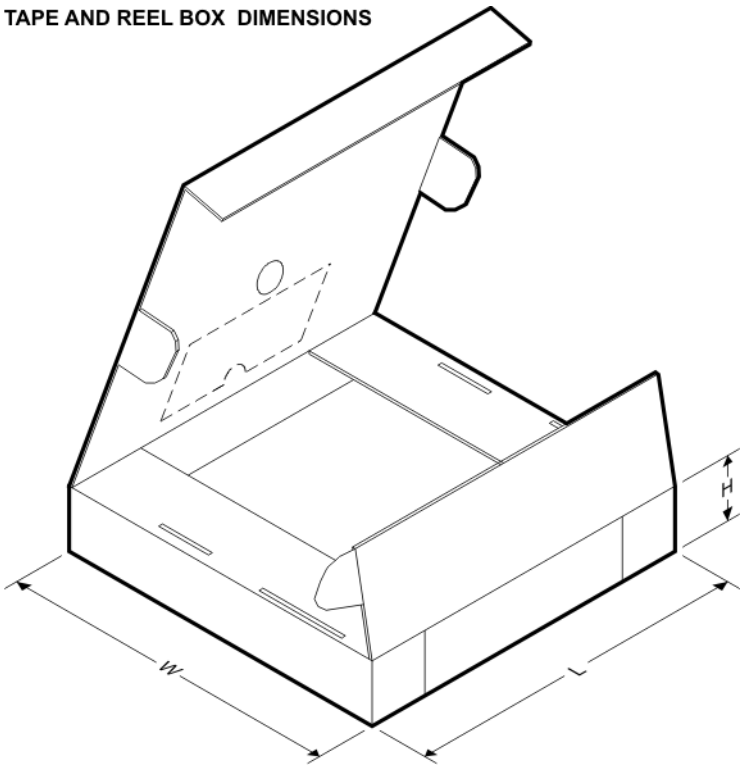
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2637DWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
UC3637DWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



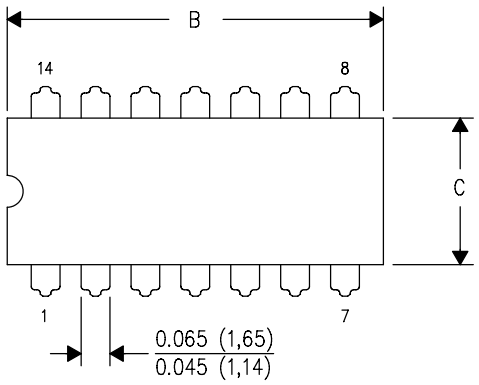
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2637DWTR	SOIC	DW	20	2000	367.0	367.0	45.0
UC3637DWTR	SOIC	DW	20	2000	367.0	367.0	45.0

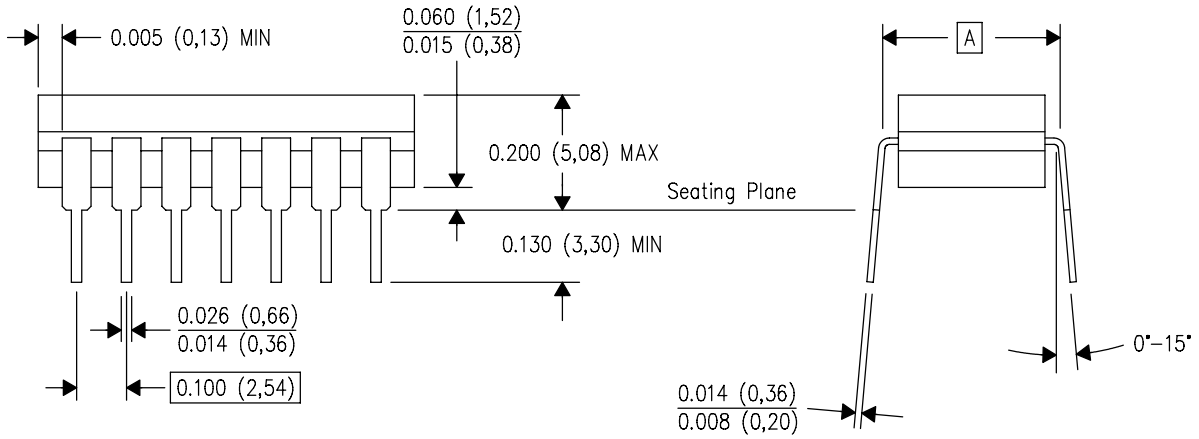
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

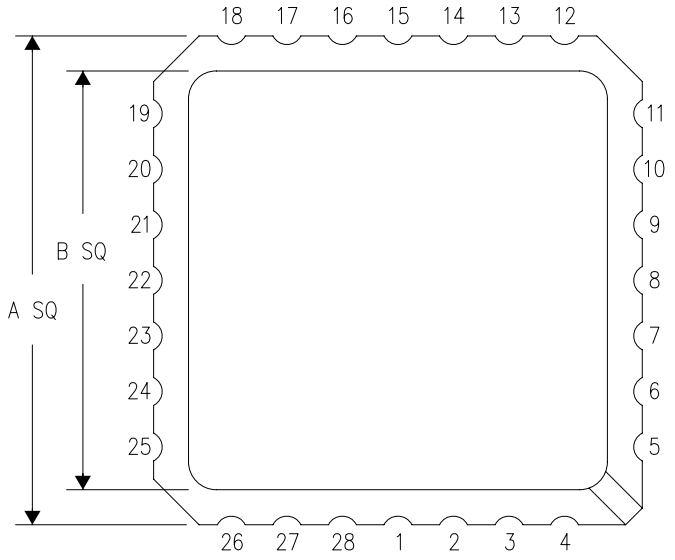


4040083/F 03/03

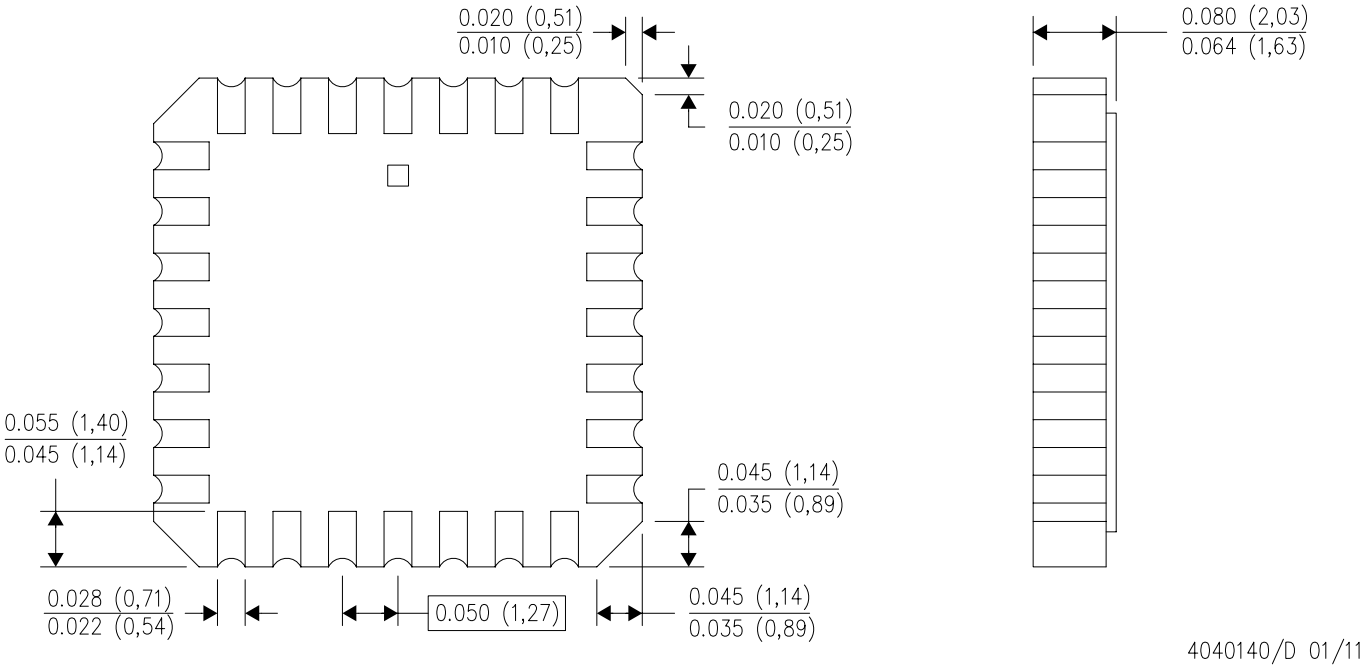
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



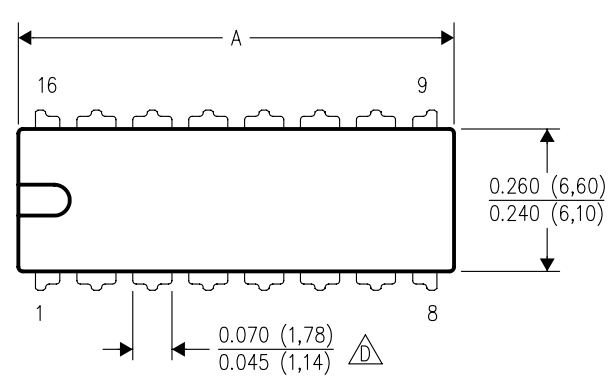
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

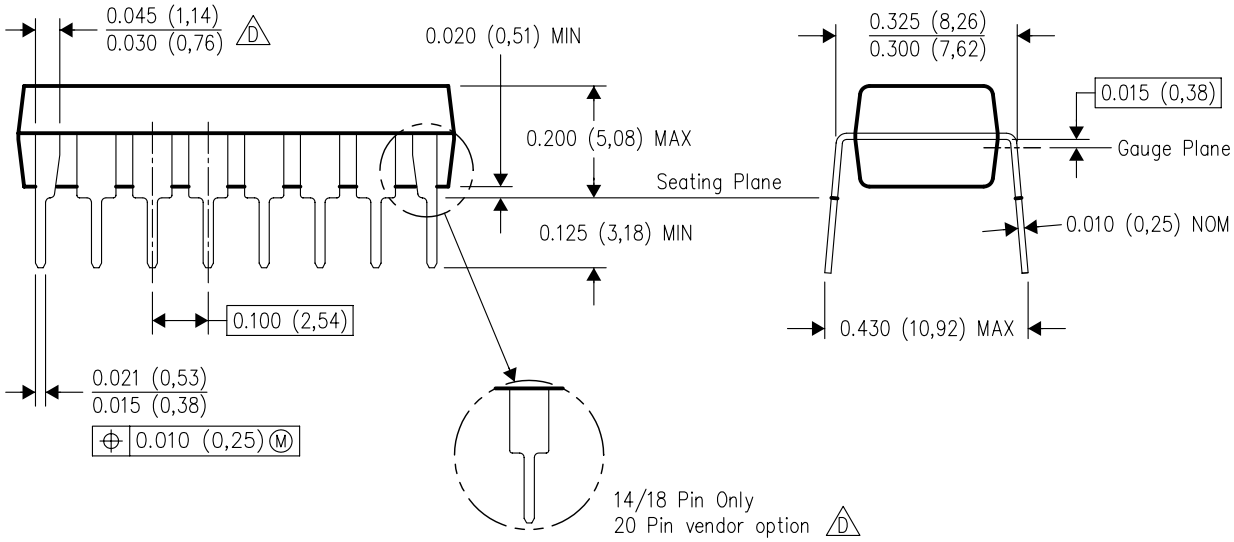
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

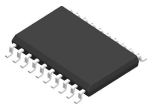


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

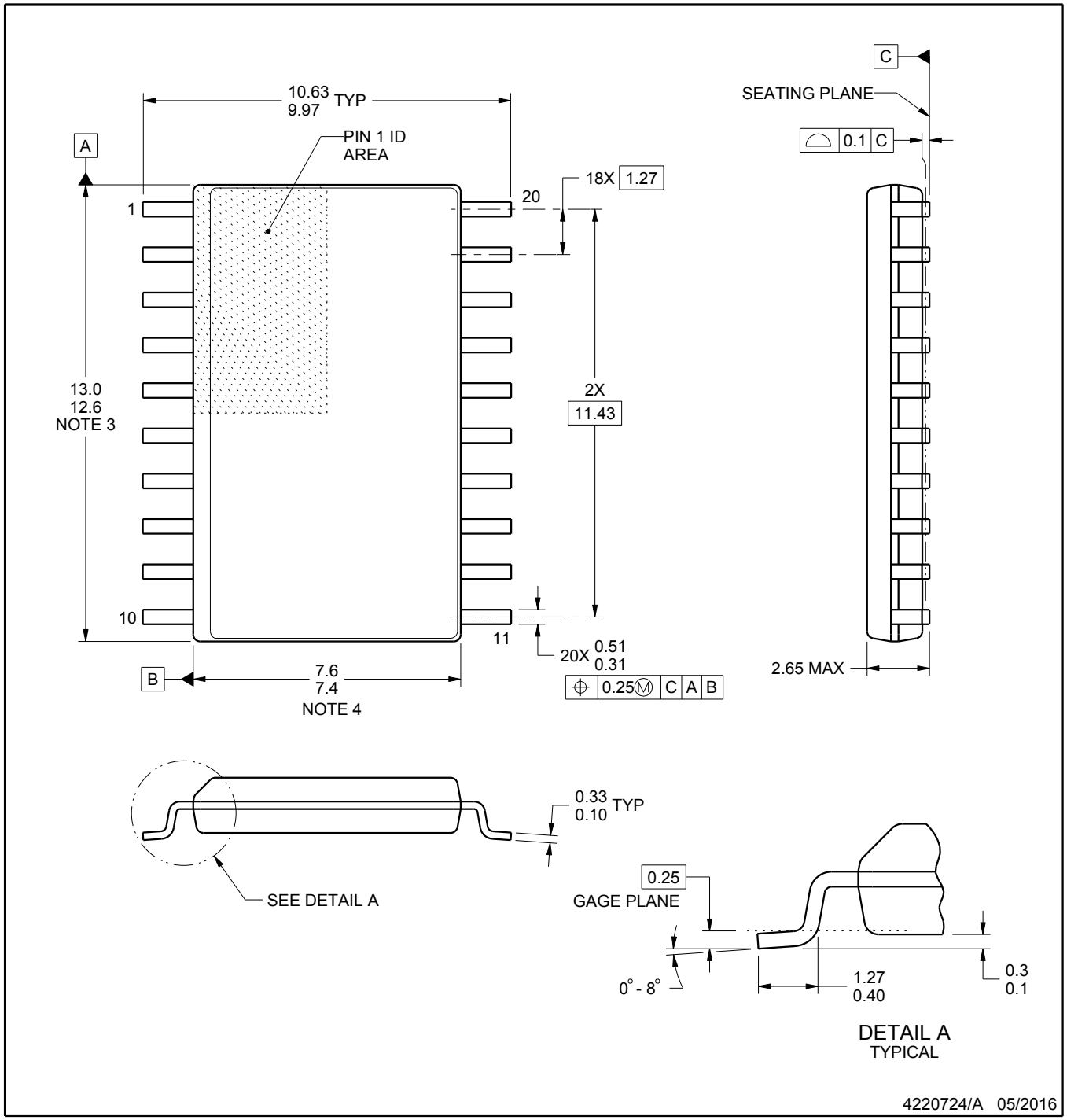


PACKAGE OUTLINE

DW0020A

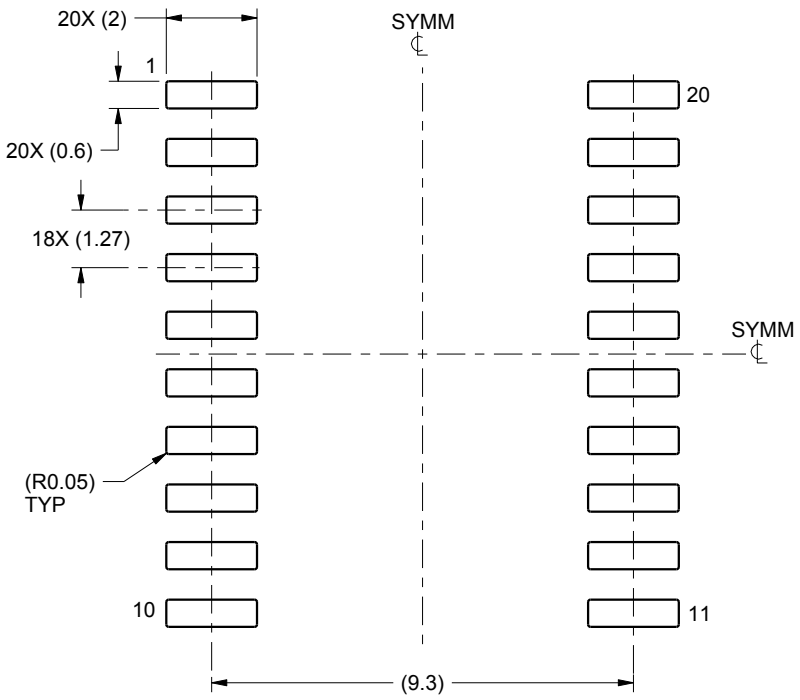
SOIC - 2.65 mm max height

SOIC

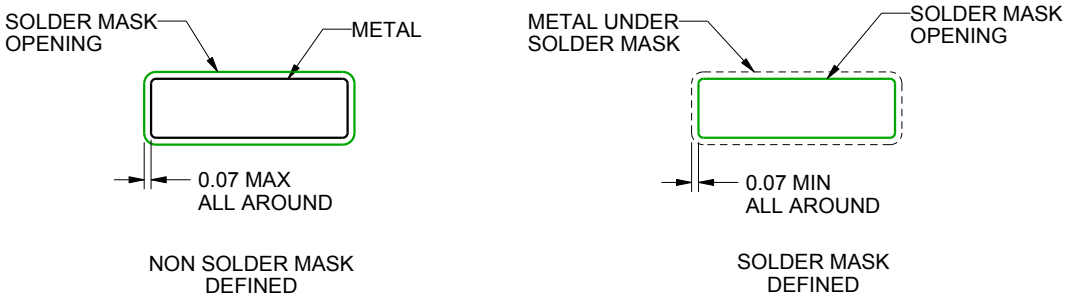


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

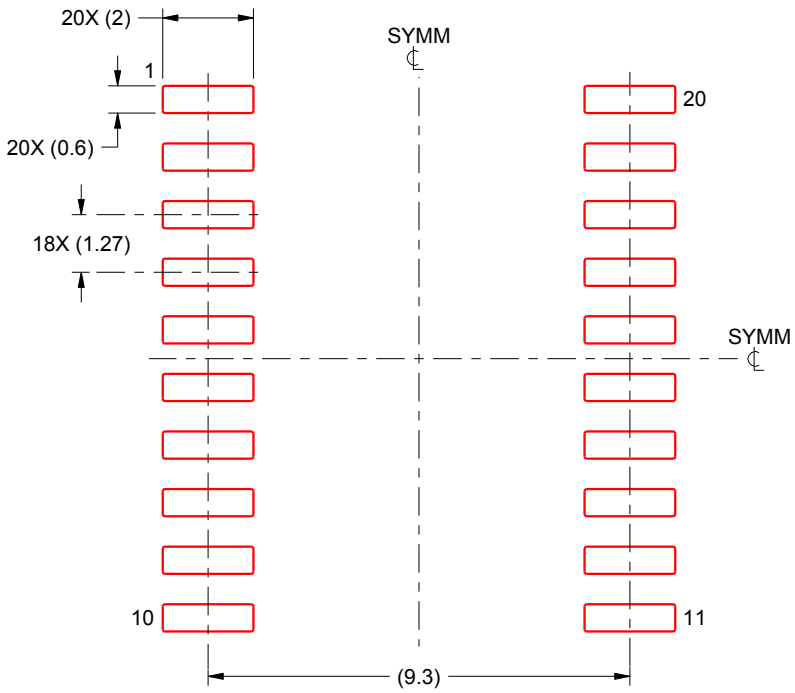


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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