Advanced Regulating Pulse Width Modulators

FEATURES

- Fully Interchangeable with Standard UC1524 Family
- Precision Reference Internally Trimmed to ±1%
- High-Performance Current Limit Function
- Under-Voltage Lockout with Hysteretic Turn-on
- Start-Up Supply Current Less Than 4mA
- Output Current to 200mA
- 60V Output Capability
- Wide Common-Mode Input Range for both Error and Current Limit Amplifiers
- PWM Latch Insures Single Pulse per Period
- Double Pulse Suppression Logic
- 200ns Shutdown through PWM Latch
- Ensured Frequency Accuracy
- Thermal Shutdown Protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

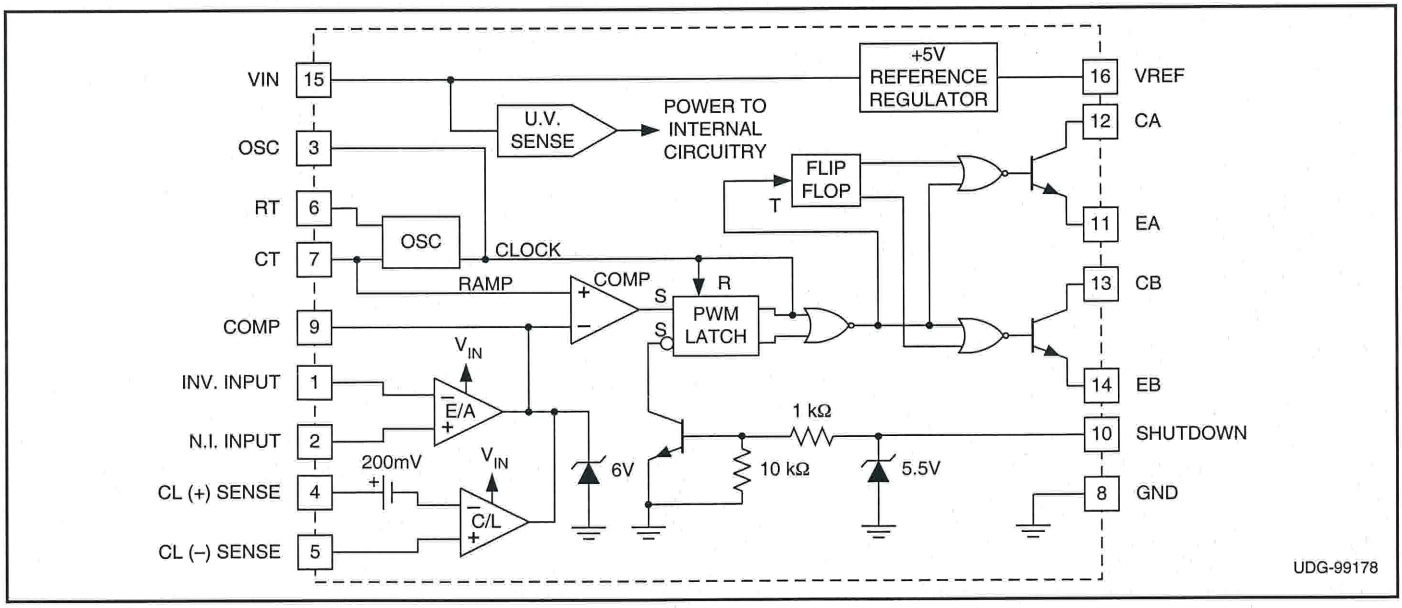
The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from -55°C to +125°C. The UC2524A and 3524A are available in either ceramic or plastic packages and are rated for operation from -40°C to +85°C and 0°C to 70°C, respectively. Surface mount devices are also available.

BLOCK DIAGRAM

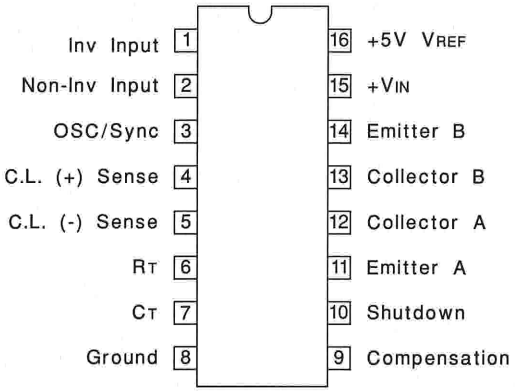


ABSOLUTE MAXIMUM RATINGS

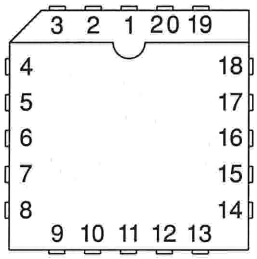
Supply Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 60V
Output Current (each Output) 200mA
Maximum Forced Voltage (Pin 9, 10) . . . . . -3 to +5V
Maximum Forced Current (Pin 9, 10) . . . . . ±10mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C 1000mW
Power Dissipation at T_C = +25°C 2000mW
Operating Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature, (Soldering, 10 seconds) . . . . . +300°C
Note: Consult packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q or L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
Non-Inv. Input	3
OSC/SYNC	4
C.L. (+) sense	5
N/C	6
C.L. (-) sense	7
R_T	8
C_T	9
Ground	10
N/C	11
Compensation	12
Shutdown	13
Emitter A	14
Collector A	15
N/C	16
Collector B	17
Emitter B	18
+V_{IN}	19
+5V V_{REF}	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -40° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		6.5	7.5	8.5	6.5	7.5	8.5	V
Turn-on Current	V_{IN} = 6V		2.5	4		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.5			0.5		V
Reference Section								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
	Over Operating Range	4.9		5.1	4.85		5.15	V
Line Regulation	V_{IN} = 10 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20 mA		20	25		20	35	mV
Temperature Stability*	Over Operating Range*		20	25		20	35	mV
Short Circuit Current	V_{REF} = 0, 25°C ≤ T_J ≤ 125°C		80	100		80	100	mA
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz, T_J =25°C		40			40		μVrms
Long Term Stability*	T_J =125°C, 1000 Hrs.		20	50		20	50	mV

** These parameters are ensured by design but not 100% tested in production.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -40° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_J = 25°C	41	43	45	39	43	47	kHz
	Over Operating Range	40.2		45.9	38.2		47.9	kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1mfd			140			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470pF	500			500			kHz
Output Amplitude*		3	3.5		3	3.5		V
Output Pulse Width*		0.29	0.5	1.0	0.3	0.5	1.0	µs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	T_J = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			-1.0			-1.0		mV/°C
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	µA
Input Offset Current			.05	1		0.5	1	µA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	70	80		70	80		dB
Output Swing (Note 1)		5.0		0.5	5.0		0.5	V
Open Loop Voltage Gain	ΔV_O= 1 to 4V, $R_L \geq$ 10MΩ	72	80		64	80		dB
Gain-Bandwidth*	T_J = 25°C, A_V = 0dB	1	3		1	3		MHz
DC Transconductance*§	T_J = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.7	2.3		1.7	2.3		mS
P.W.M. Comparator (R_T = 2kΩ, C_T = 0.01mfd)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.8V	45			45			%
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	T_J = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	µA
Common Mode Rejection Ratio	$V_{(pin\ 5)}$ = -0.3V to + 5.5V	50	60		50	60		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing (Note 1)	Minimum Total Range	5.0		0.5	5.0		0.5	V
Open-Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10MΩ	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100µA	60	80		60	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	µA

** These parameters are ensured by design but not 100% tested in production.*

§ DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to the common mode voltage.

The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

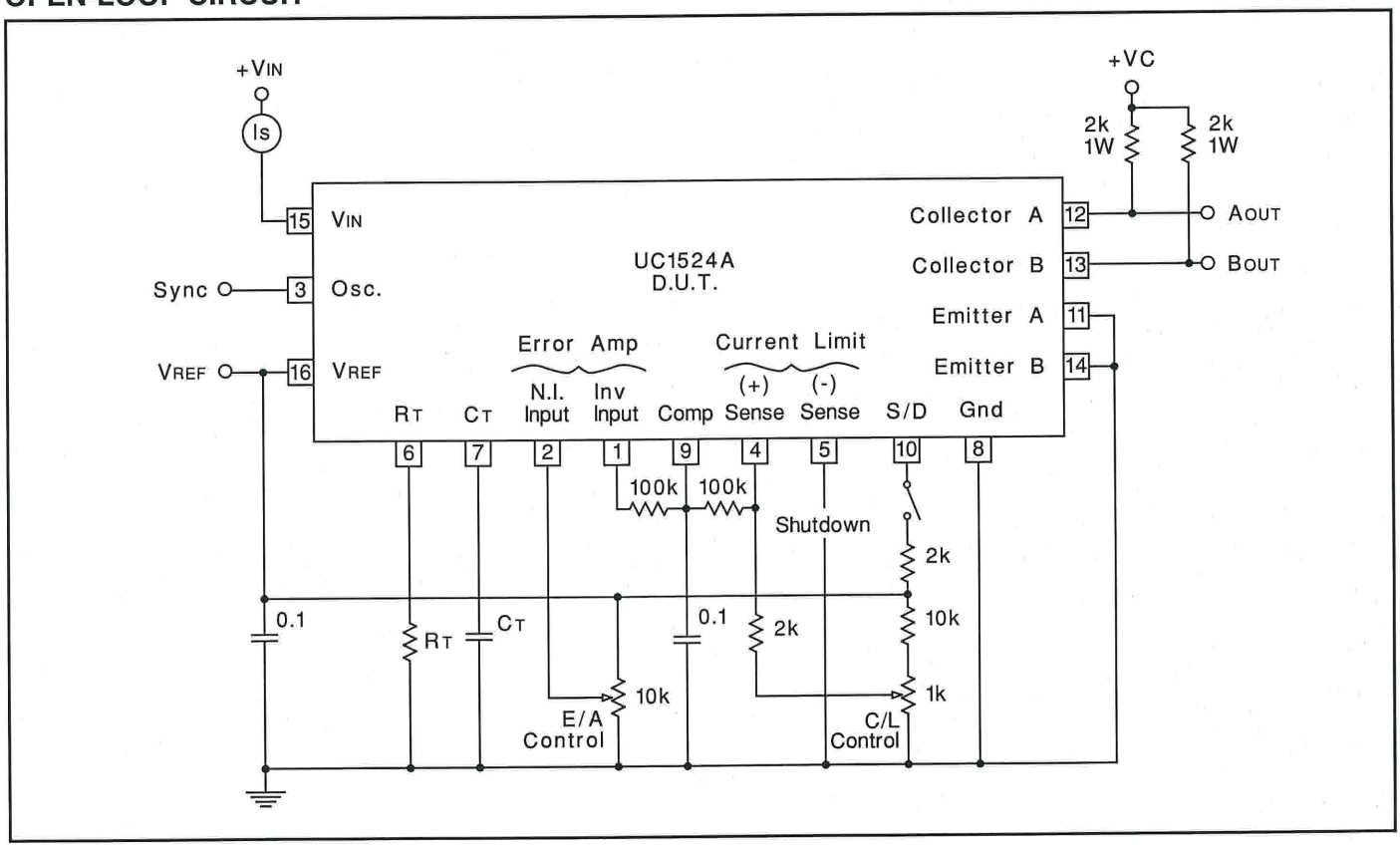
Note 1: Min Limit applies to output high level, max limit applies to output low level.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -40° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V. T_A = T_J.

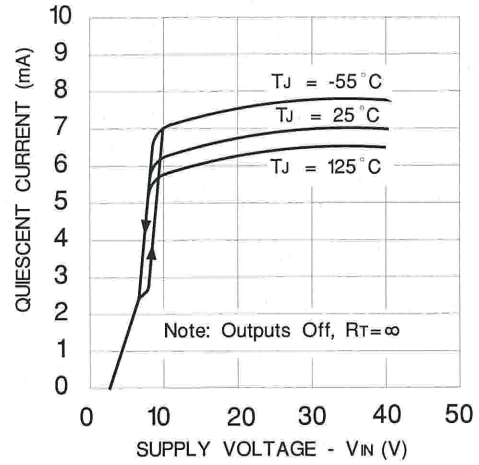
PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section (cont.) (Each Output)								
Saturation Voltage	I_C = 20mA I_C = 200mA		.2 1	.4 2.2		.2 1	.4 2.2	V V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_J = 25°C, R = 2kΩ		120	400		120	400	ns
Fall Time*	T_J = 25°C, R = 2kΩ		25	200		25	200	ns
Comparator Delay*	T_J = 25°C, Pin 9 to output		300			300		ns
Shutdown Delay*	T_J = 25°C, Pin 10 to output		200			200		ns
Shutdown Threshold	T_J = 25°C, R_C = 2kΩ	0.6	.7	1.0	0.6	.7	1.0	V
S/D Threshold Over Temp.	Over Operating Temperature Range	0.4		1.2	0.4		1.0	V
Thermal Shutdown*			165			165		°C

** These parameters are ensured by design but not 100% tested in production.*

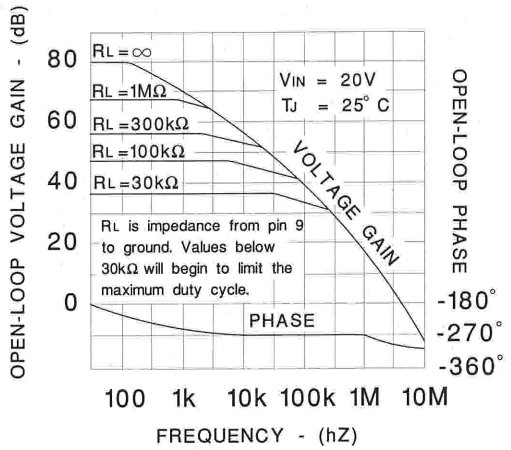
OPEN-LOOP CIRCUIT



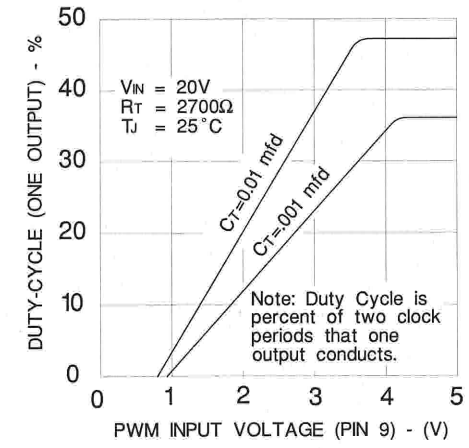
Supply Current vs Voltage



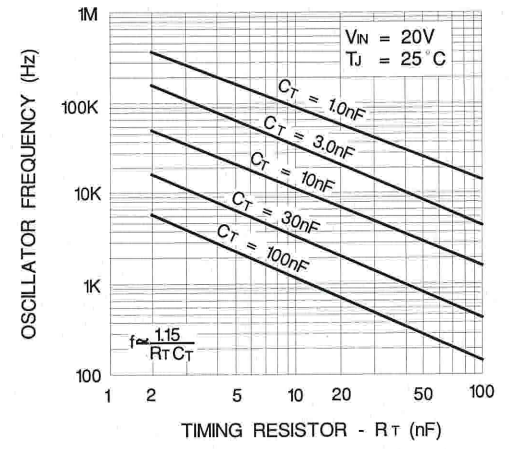
Error Amplifier Voltage Gain and Phase vs Frequency



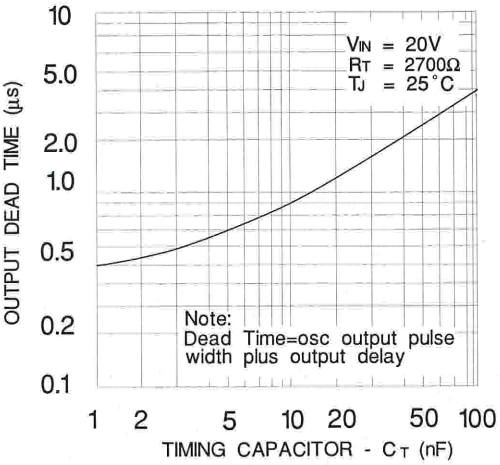
Pulse Width Modulator Transfer Function



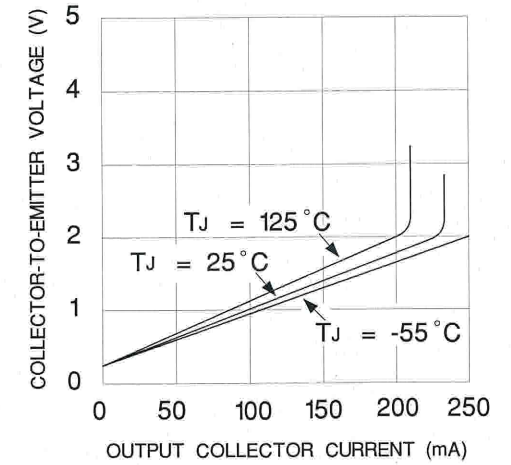
Oscillator Frequency vs Timing Components



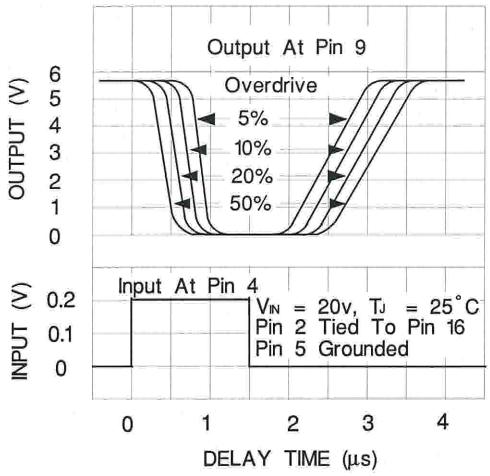
Output Dead Time vs Timing Capacitor Value



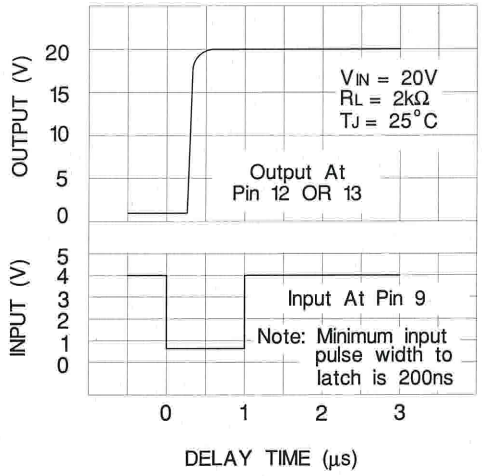
Output Saturation Voltage



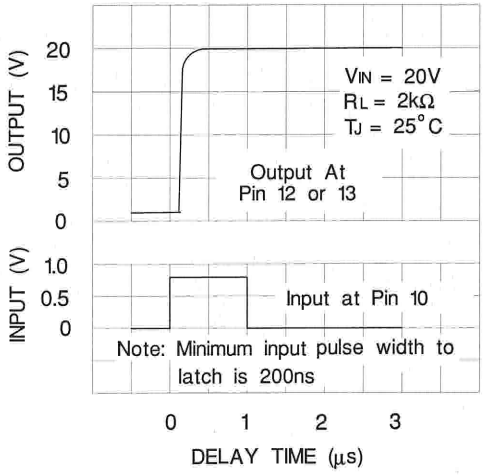
Current Limit Amplifier Delay



Shutdown Delay From PWM Comparator - Pin 9



Turn-Off Delay From Shutdown - Pin 10



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8764502EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8764502EA	Samples
UC1524AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	UC1524AJ	Samples
UC1524AJ883B	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	UC1524AJ/883B	Samples
UC1524AL	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1524AL	Samples
UC1524AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1524AL/ 883B	Samples
UC2524ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2524ADW	Samples
UC2524ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2524ADW	Samples
UC2524ADWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2524ADW	Samples
UC2524AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-40 to 85	UC2524AJ	Samples
UC2524AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2524AN	Samples
UC3524ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524ADW	Samples
UC3524ADWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3524ADW	Samples
UC3524AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	0 to 70	UC3524AJ	Samples
UC3524AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3524AN	Samples
UC3524ANG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3524AN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1524A, UC2524A, UC2524AM, UC3524A, UC3524AM :

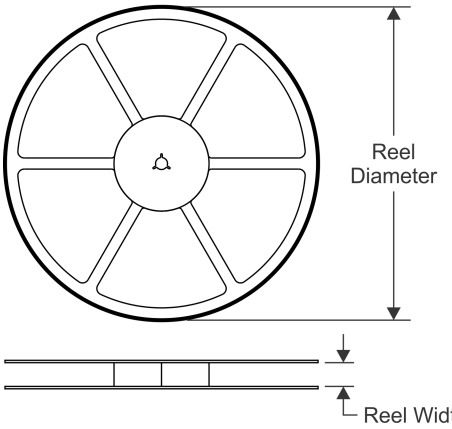
- Catalog: UC3524A, UC2524A, UC3524AM, UC3524A
- Military: UC2524AM, UC1524A, UC1524A

NOTE: Qualified Version Definitions:

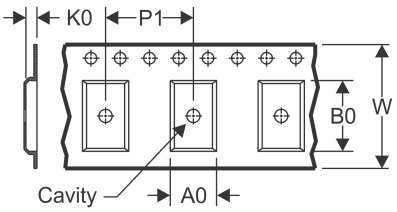
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

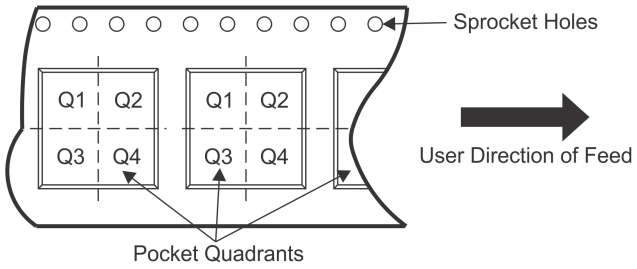


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

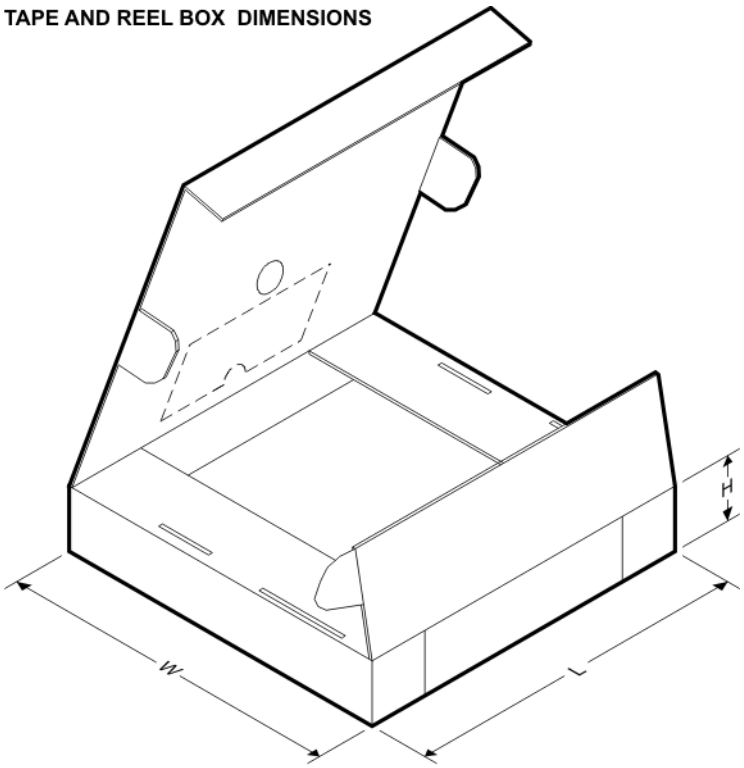
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2524ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3524ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

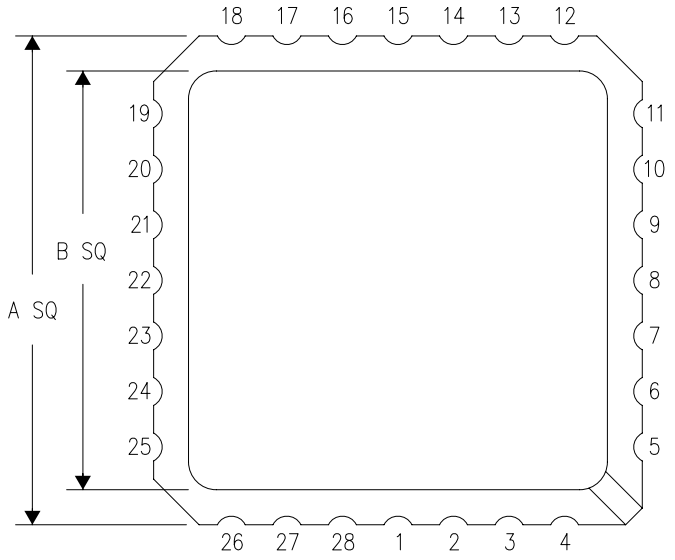


*All dimensions are nominal

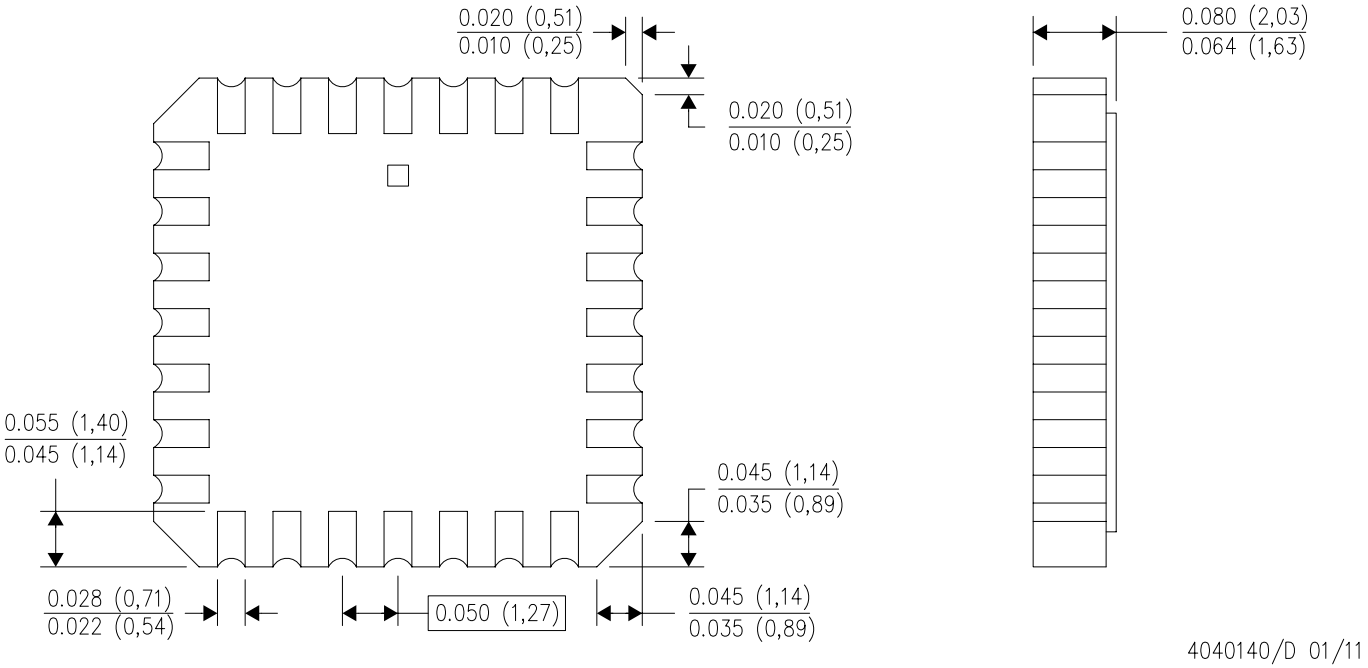
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2524ADWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3524ADWTR	SOIC	DW	16	2000	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

GENERIC PACKAGE VIEW

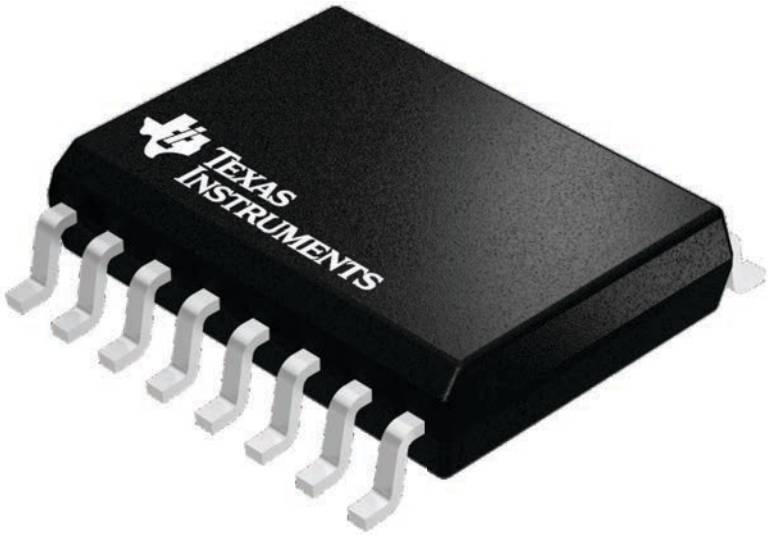
DW 16

SOIC - 2.65 mm max height

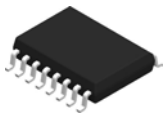
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

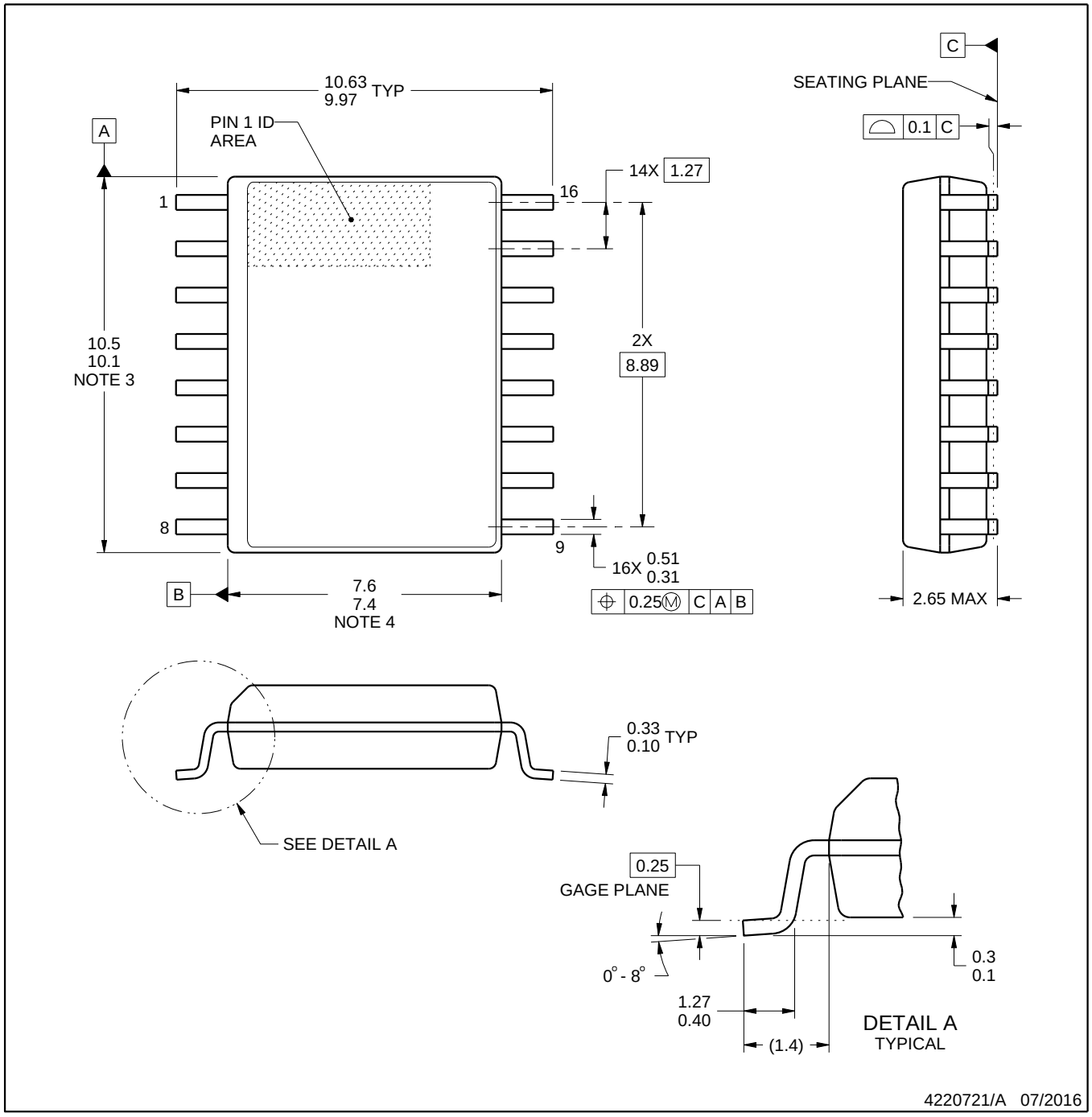


PACKAGE OUTLINE

DW0016A

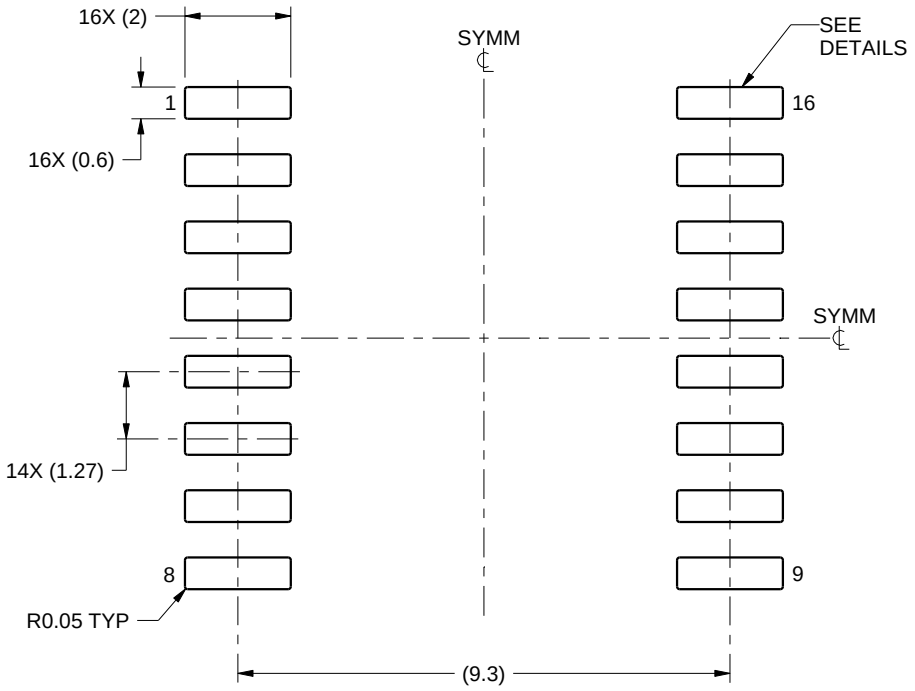
SOIC - 2.65 mm max height

SOIC

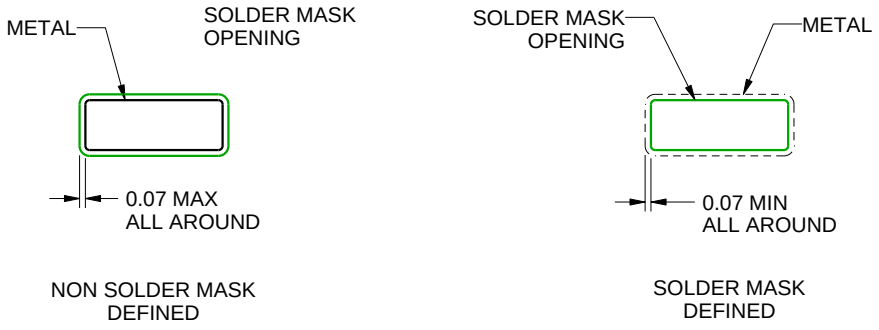


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

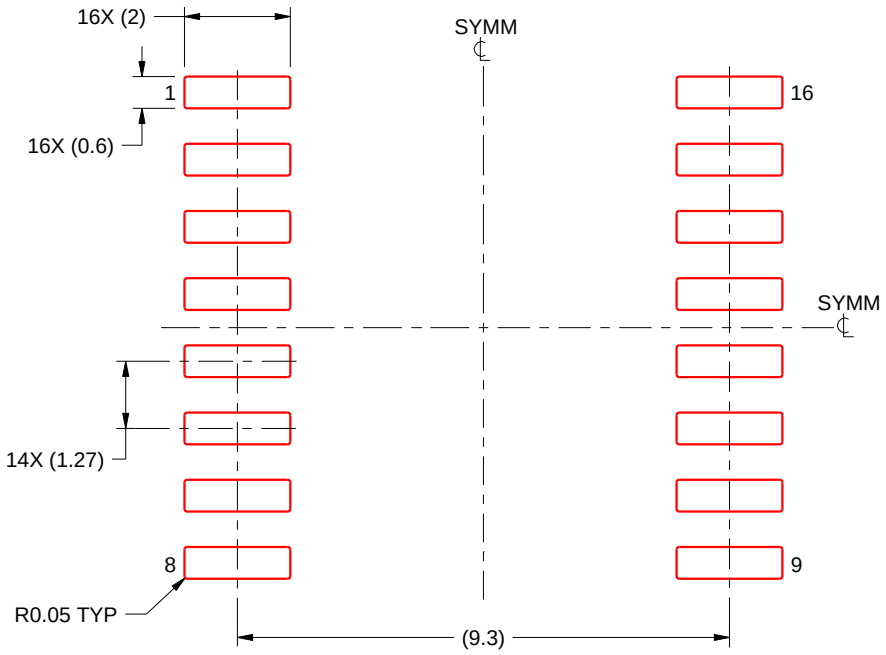


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

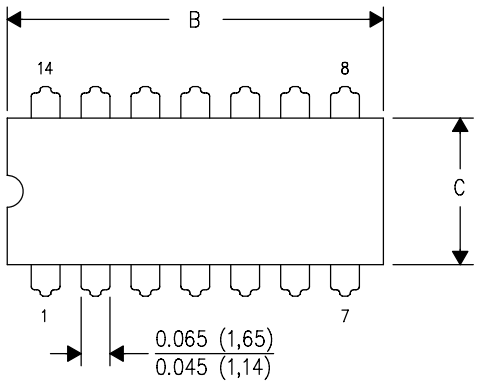
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

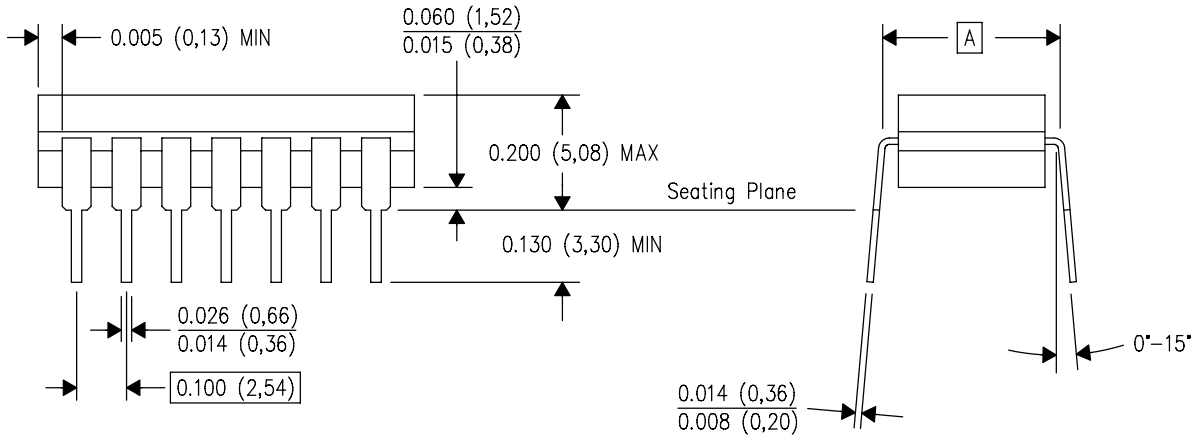
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



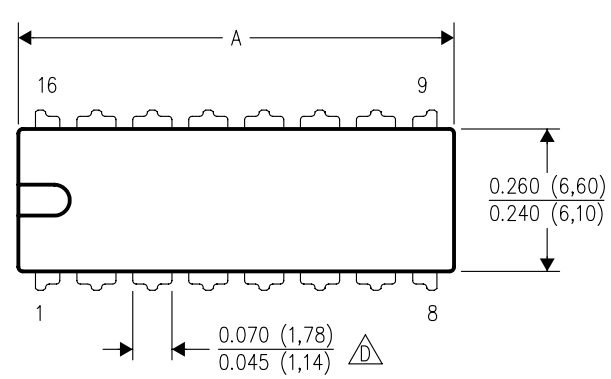
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

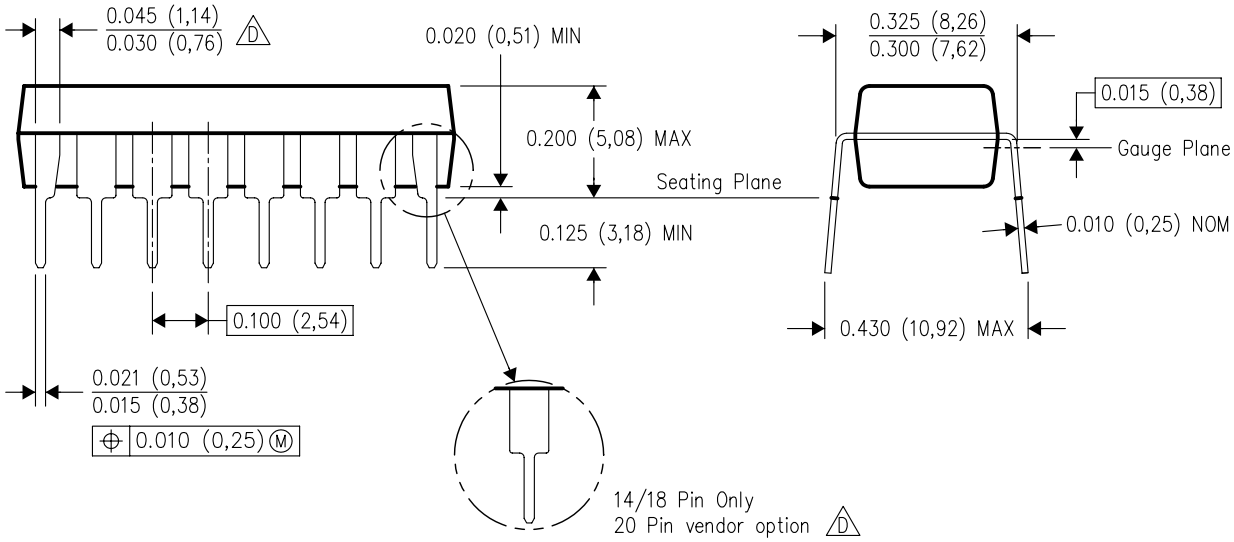
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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