UBA2016A/15/15A

600 V fluorescent lamp driver with PFC, linear dimming and boost function

Rev. 1 — 20 May 2011 **Objective data sheet**

1. General description

The UBA2016A/15/15A are high voltage Integrated Circuits (IC) intended to drive fluorescent lamps with filaments such as Tube Lamps (TL) and Compact Fluorescent Lamps (CFL) in general lighting applications. The IC comprises a fluorescent lamp control module, half-bridge driver, built-in critical conduction mode Power Factor Correction (PFC) controller/driver and several protection mechanisms. The IC drives fluorescent lamp(s) using a half-bridge circuit made of two MOSFETs with a supply voltage of up to 600 V.

The UBA2016A/15/15A are designed to be supplied by a start-up bleeder resistor and a dV/dt supply from the half-bridge circuit, or any other auxiliary supply derived from the half-bridge or the PFC. The supply current of the IC is low. An internal clamp limits the supply voltage.

2. Features and benefits

- Power factor correction features:
  - Integrated 4-pin critical conduction mode PFC controller/driver
  - Open and short pin-short protection on PFC feedback pin
  - Overcurrent protection
  - Overvoltage protection
- Half-bridge driver features:
  - Integrated level-shifter for the high-side driver of the half-bridge
  - Integrated bootstrap diode for the high-side driver supply of the half-bridge
  - Independent non-overlap time
- Fluorescent lamp controller features:
  - Linear dimming (UBA2016A and UBA2015A only)
  - EOL (End-Of-Life) detection (both symmetrical and asymmetrical)
  - Adjustable preheat time
  - Adjustable preheat current
  - Adjustable fixed frequency preheat (UBA2015 and UBA2015A only)
  - Lamp ignition failure detection
  - Ignition detection of all lamps fat multiple lamps with separate resonant tanks
  - Second ignition attempt if first failed
  - Constant output power independent of mains voltage variations
  - Automatic restart after changing lamps
  - Adjustable lamp current boost at start-up (UBA2016A only)
  - Lamp current control

- Enable input (UBA2015 and UBA2015A only)

- Protection
  - Hard switching/capacitive mode protection
  - Half-bridge overcurrent (coil saturation) protection
  - Lamp overvoltage (lamp removal) protection
  - Temperature protection

3. Applications

- Intended for fluorescent lamp ballasts with either a dimmable (UBA2016A and UBA2015A) or a fixed (UBA2015) output and PFC for AC mains voltages of up to 390 V.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UBA2016AT/N1	SO20	plastic small package outline package; 20 leads; body width 7.5 mm	SOT163-1
UBA2015T/N1	SO20	plastic small package outline package; 20 leads; body width 7.5 mm	SOT163-1
UBA2015AT/N1	SO20	plastic small package outline package; 20 leads; body width 7.5 mm	SOT163-1
UBA2016AP/N1	DIP20	plastic dual in-line package; 20 leads; (300 mil)	SOT146-1
UBA2015P/N1	DIP20	plastic dual in-line package; 20 leads; (300 mil)	SOT146-1
UBA2015AP/N1	DIP20	plastic dual in-line package; 20 leads; (300 mil)	SOT146-1

Table 2. Functional selection

Type	PFC	dim	Boost	fixed frequency preheat
UBA2016A	yes	yes	yes	no
UBA2015	yes	no	no	yes
UBA2015A	yes	yes	no	yes

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5. Block diagram

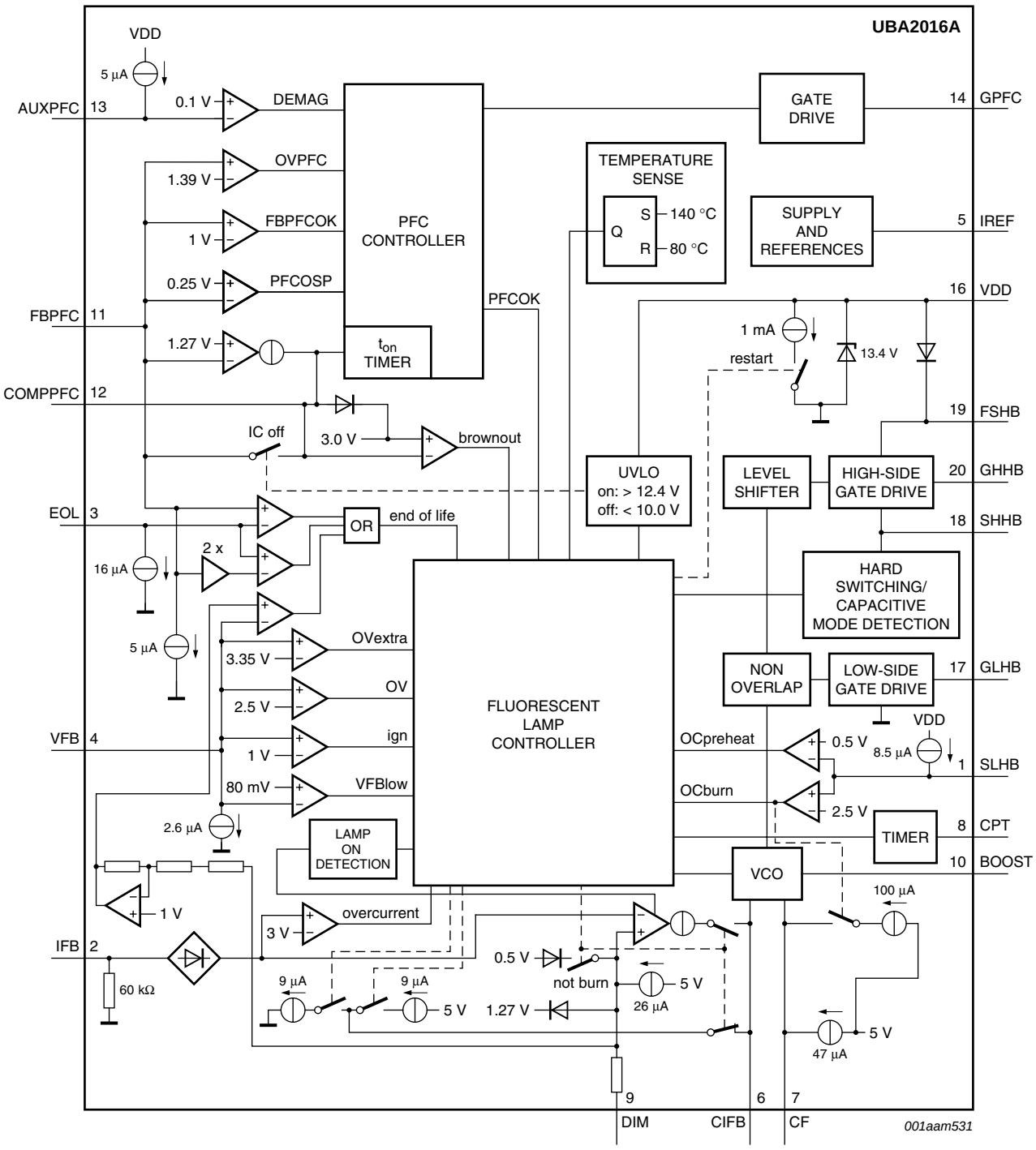
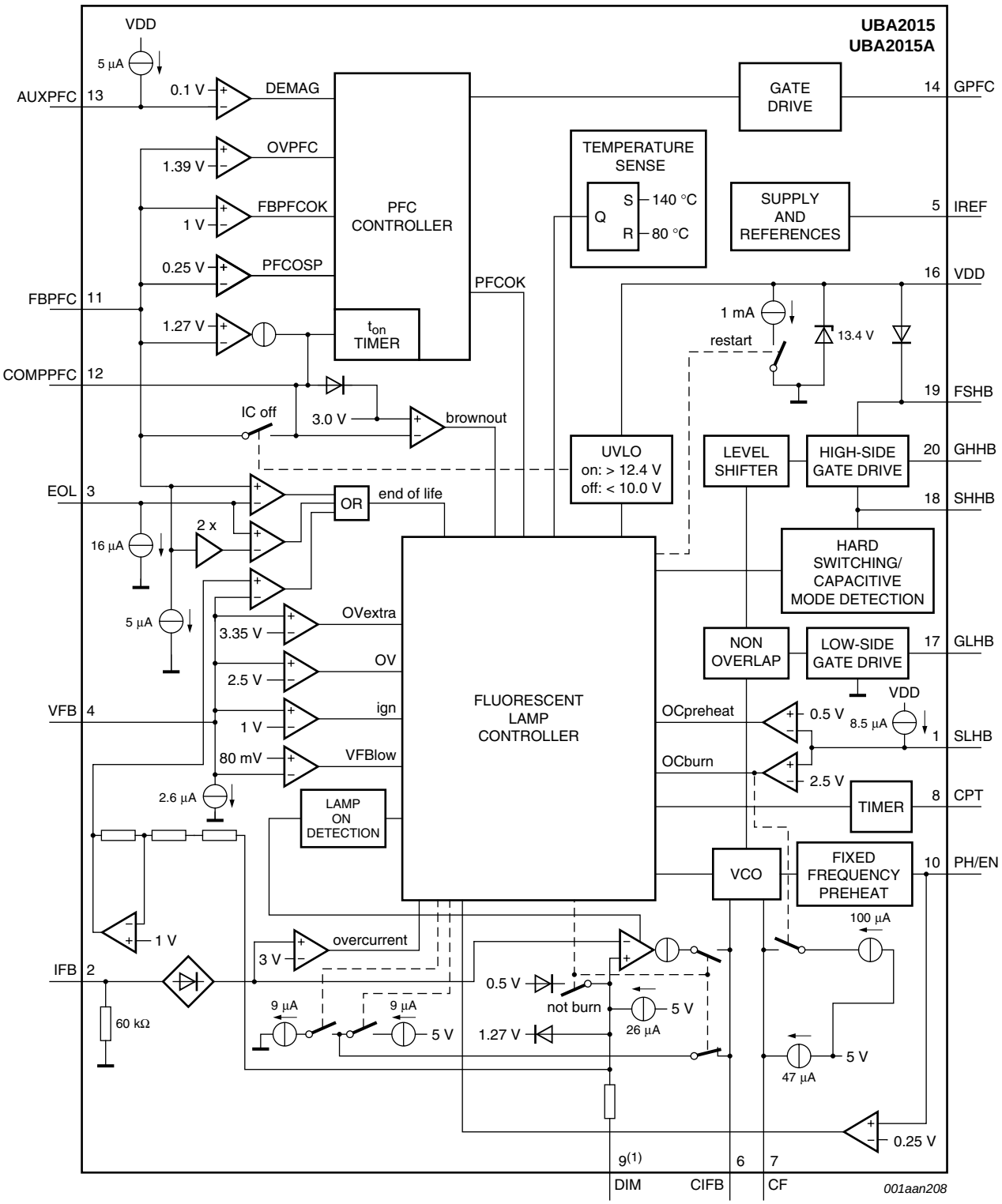


Fig 1. Block diagram UBA2016A

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(1) Pin 9 is not connected in the UBA2015.

Fig 2. Block diagram UBA2015A and UBA2015

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6. Pinning information

6.1 Pinning

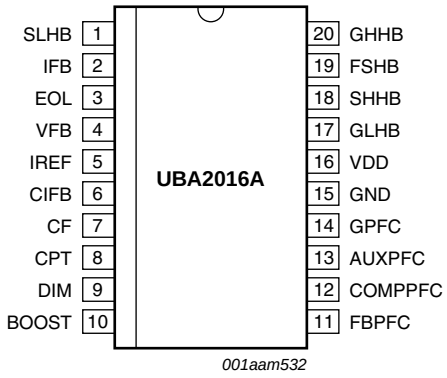


Fig 3. Pin configuration UBA2016A

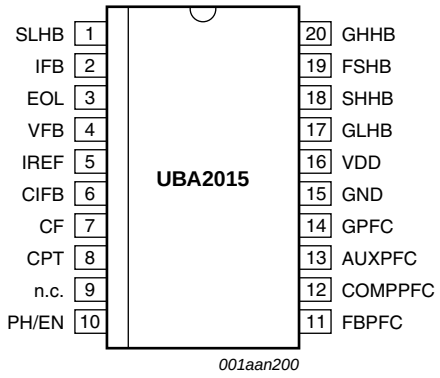


Fig 4. Pin configuration UBA2015

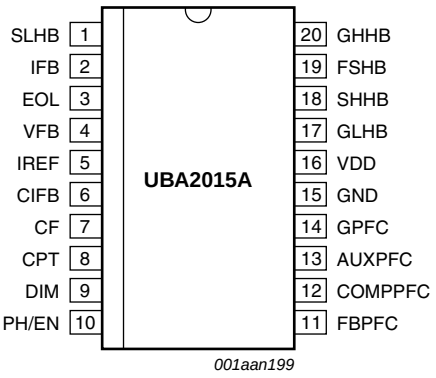


Fig 5. Pin configuration UBA2015A

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SLHB	1	half-bridge (HB) low-side switch current sense input
IFB	2	lamp current feedback input
EOL	3	end-of-life sensing input
VFB	4	lamp voltage feedback input
IREF	5	reference current setting
CIFB	6	lamp current feedback compensation
CF	7	high frequency (HF) oscillator timing capacitor
CPT	8	preheat and fault timing capacitor
DIM	9	dimming function input UBA2016A and UBA2015A
n.c.	9	UBA2015

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Table 3. Pin description *...continued*

Symbol	Pin	Description
BOOST	10	boost function input UBA2016A
PH/EN	10	preheat frequency setting combined with enable UBA2015 and UBA2015A
FBPFC	11	PFC feedback input
COMPPFC	12	PFC output voltage feedback compensation
AUXPFC	13	PFC auxiliary winding input
GPFC	14	PFC gate driver output
GND	15	ground
VDD	16	supply
GLHB	17	HB low-side switch gate driver output
SHHB	18	HB high-side source connection
FSHB	19	HB floating supply connection
GHHB	20	HB high-side switch gate driver output

7. Functional description

7.1 Introduction

The UBA2016A/15/15A is an integrated circuit for electronically ballasted fluorescent lamps. It provides a critical conduction mode Power Factor Correction (PFC) controller/driver and a half-bridge controller/driver with all the necessary functions for correct preheat, ignition and on-state operation of the lamp. Several protection mechanisms are incorporated to ensure the safe operation of the fluorescent lamp or a shut down of the complete ballast under any abnormal operating conditions or lamp failure.

7.2 Power Factor Correction (PFC)

The PFC is a boundary conduction mode, on-time controlled system. The basic application diagram can be found in Figure 6. This type of PFC operates at the boundary between continuous and discontinuous mode. Energy is stored in the inductor L_{PFC} each period that switch Q_{PFC} is on. When the input current $I_{i(PFC)}$ is zero at the moment that Q_{PFC} is switched on, the amplitude of the current build up in L_{PFC} will be proportional to $V_{i(PFC)}$ and the time $t_{on(PFC)}$ that Q_{PFC} is on. This current continues to flow as output current $I_{o(PFC)}$ via D_{PFC} into C_{BUS} after Q_{PFC} is switched off. In this phase $I_{o(PFC)}$ is equal to $I_{i(PFC)}$. A new cycle is started when $I_{o(PFC)}$ reaches zero. $I_{i(PFC)}$ consists of a sequence of triangular pulses, each having an amplitude proportional to the input voltage and $t_{on(PFC)}$. If $t_{on(PFC)}$ is kept constant, the first harmonic of the input current is proportional to the input voltage. The PFC output voltage $V_{o(PFC)}$ is controlled by $t_{on(PFC)}$. As $t_{on(PFC)}$ is more slowly regulated than the mains frequency it will not disturb the power factor.

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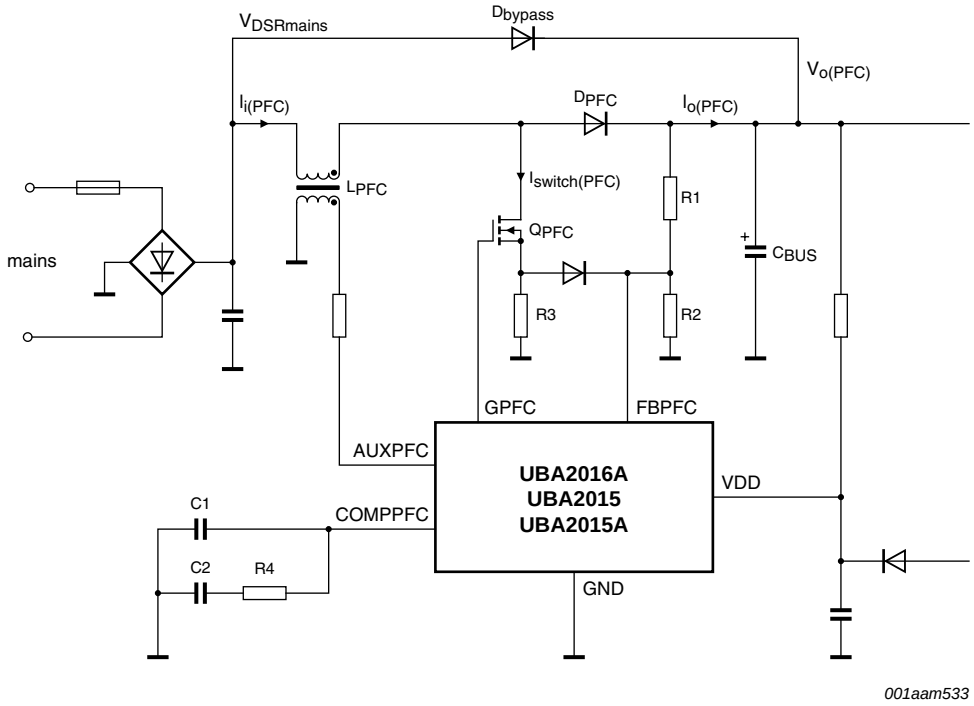


Fig 6. Basic PFC application diagram

7.2.1 Regulation loop

The control loop senses the PFC output voltage via resistors R1, R2 and the feedback input FBPFC. The frequency compensation network C1, C2 and R4 sets the response time and stability of the loop. The voltage at pin FBPFC is regulated to $V_{reg(FBPFC)}$. When voltage on pin FBPFC is above the regulation voltage, pin COMPPFC is charged and when voltage on pin FBPFC is lower, pin COMPPFC is discharged. Current flow through pin COMPPFC is controlled by the PFC Operational Transconductance Amplifier (OTA) and its transconductance $g_{m(PFC)}$. The voltage on pin COMPPFC controls the PFC on-time, $t_{on(PFC)}$. So when the voltage at pin FBPFC is too high, $t_{on(PFC)}$ is reduced and less energy is transferred. When voltage at pin FBPFC is too low, $t_{on(PFC)}$ is increased and more energy is transferred.

The voltage on pin FBPFC is sampled at the rising edge of pin GPFC and held internally during the leading edge blanking time $t_{leb(FBPPC)}$ before going to the OTA to prevent disturbance of the regulation level due to transition effects when the PFC external power switch is turned on

The maximum $t_{on(PFC)}$ is set when the voltage at pin COMPPFC is clamped to $V_{clamp(COMPPFC)}$ to limit the dead time in recovering regulation after a regulation range overshoot. The $t_{on(PFC)}$ time can be regulated down to zero. The moment at which the gate is turned on is determined by pin AUXPFC. When this pin is below demagnetization detection voltage $V_{det(demag)AUXPFC}$ and the low PFC off-time $t_{off(PFC)low}$ timer is finished, the next cycle starts.

During start-up, the capacitor connected to pin COMPPFC is connected by an internal switch to pin FBPFC which allows it to partially charge before the PFC starts. This reduces the start-up time.

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7.2.2 Protection

The PFC incorporates the following protection mechanisms:

- When voltage on pin FBPFC drops below open/short protection threshold voltage $V_{th(osp)(FBPFC)}$, the gate is turned off and the start of a new cycle is inhibited. A small internal filter prevents this protection reacting to a negative spike.
- When pin FBPFC is left open, a pull-down bias current $I_{bias(FBPFC)}$ ensures that the pin voltage drops below $V_{th(osp)(FBPFC)}$.
- When voltage at pin FBPFC rises above overvoltage threshold voltage $V_{th(ov)(FBPFC)}$ the gate immediately turns off. A new cycle will not start while V_{FBPFC} remains above $V_{th(ov)(FBPFC)}$. This limits the PFC output voltage. This protection is disabled during the leading edge blanking time $t_{leb(FBPFC)}$ after GPFC goes high.
- When the $t_{off(PFC)low}$ timer sequence has ended with no demagnetization detected (V_{AUXPFC} has not risen above $V_{det(demag)}$) the on-time of the next cycle will be the no demagnetization detected PFC on-time $t_{on(PFC)nodemag}$ to prevent excessive current build up in the coil.
- Bias current $I_{bias(AUXPFC)}$ ensures that pin AUXPFC is HIGH when not connected ensuring pin GPFC stays LOW.

7.3 Half-bridge driver

The IC incorporates drivers for the half-bridge switches and all related circuits such as non-overlap, high voltage level shifter, bootstrap circuit for the floating supply and hard switching and capacitive mode detection.

The UBA2016A/15/15A is designed to drive a half-bridge inverter with an inductive load. The load consists typically of an inductor with a resonant capacitor and a TL or CFL. A basic half-bridge application circuit driving a TL is shown in Figure 7 which also shows a typical IC supply configuration with a start-up bleeder resistor and a dV/dt supply.

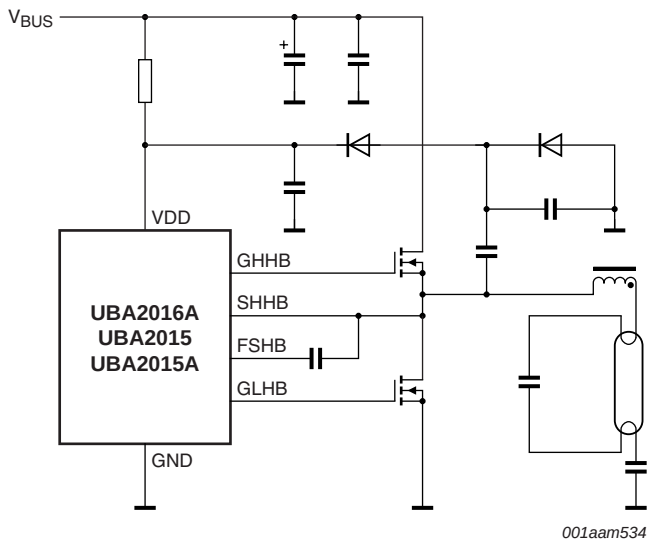


Fig 7. Basic half-bridge and IC supply connection diagram

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7.3.1 VDD supply

The UBA2016A/15/15A is intended to be supplied by a start-up bleeder resistor connected between the bus voltage V_{BUS} and VDD and a dV/dt supply from the half-bridge point at pin SHHB.

The IC starts up when the voltage at pin VDD rises above start-up voltage $V_{startup(VDD)}$ and locks out (stops oscillating) when the voltage at pin VDD drops below stop voltage $V_{stop(VDD)}$. The hysteresis between the start and stop levels allows the IC to be supplied by a buffer capacitor until the dV/dt supply is settled. The UBA2016A/15/15A has an internal VDD clamp. This is an internal active Zener (or shunt regulator) that limits the voltage on the VDD supply pin to clamp voltage $V_{clamp(VDD)}$. No external Zener diode is needed in the dV/dt supply circuit if the maximum current of the dV/dt supply minus the current consumption of the IC (mainly determined by the gate drivers' load) is below $I_{clamp(VDD)}$.

7.3.2 Low- and high-side drivers

The low- and high-side drivers are identical. The output of each driver is connected to the equivalent gate of an external power MOSFET. The high-side driver is supplied by the bootstrap capacitor, which is charged from the VDD supply voltage via an internal diode when the low-side power MOSFET is on. The low-side driver is directly supplied by the VDD supply voltage.

7.3.3 Non-overlap

During each transition between the two states GLHB HIGH/GHHB LOW and GLHB LOW/GHHB HIGH, GLHB and GHHB will both be LOW for a fixed non-overlap time t_{no} to allow the half-bridge point to be charged or discharged by the load current (assuming the load always has an inductive behavior), and enabling zero voltage switching; see Figure 8.

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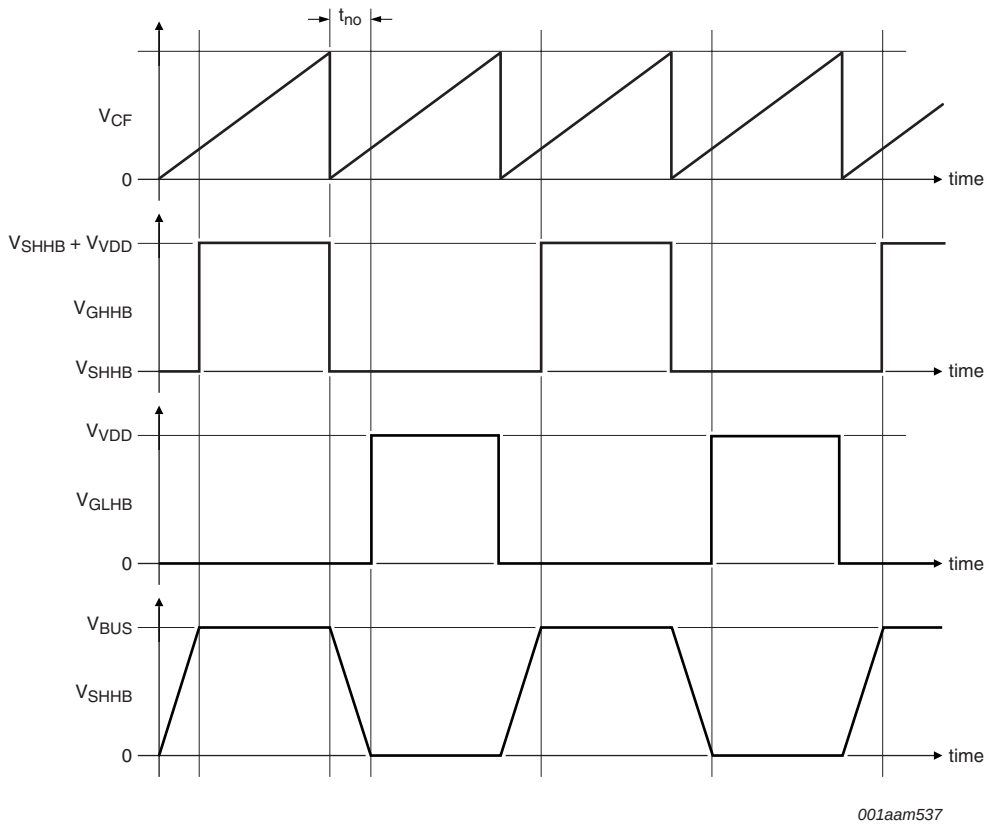


Fig 8. Oscillator, driver and half-bridge voltages

7.4 Fluorescent lamp control

The IC incorporates all the regulation and control needed for the fluorescent lamp(s), such as filament preheat, ignition frequency sweep, lamp voltage limitation, lamp current control, start-up boost, dimming, end-of-life detection, overcurrent protection and hard switching limiting.

In the UBA2016A/15/15A, 7 different operating states can be distinguished. In each state the IC acts in a specific way, as described in the next paragraphs. Figure 9 shows the possible transitions between the states with their conditions.

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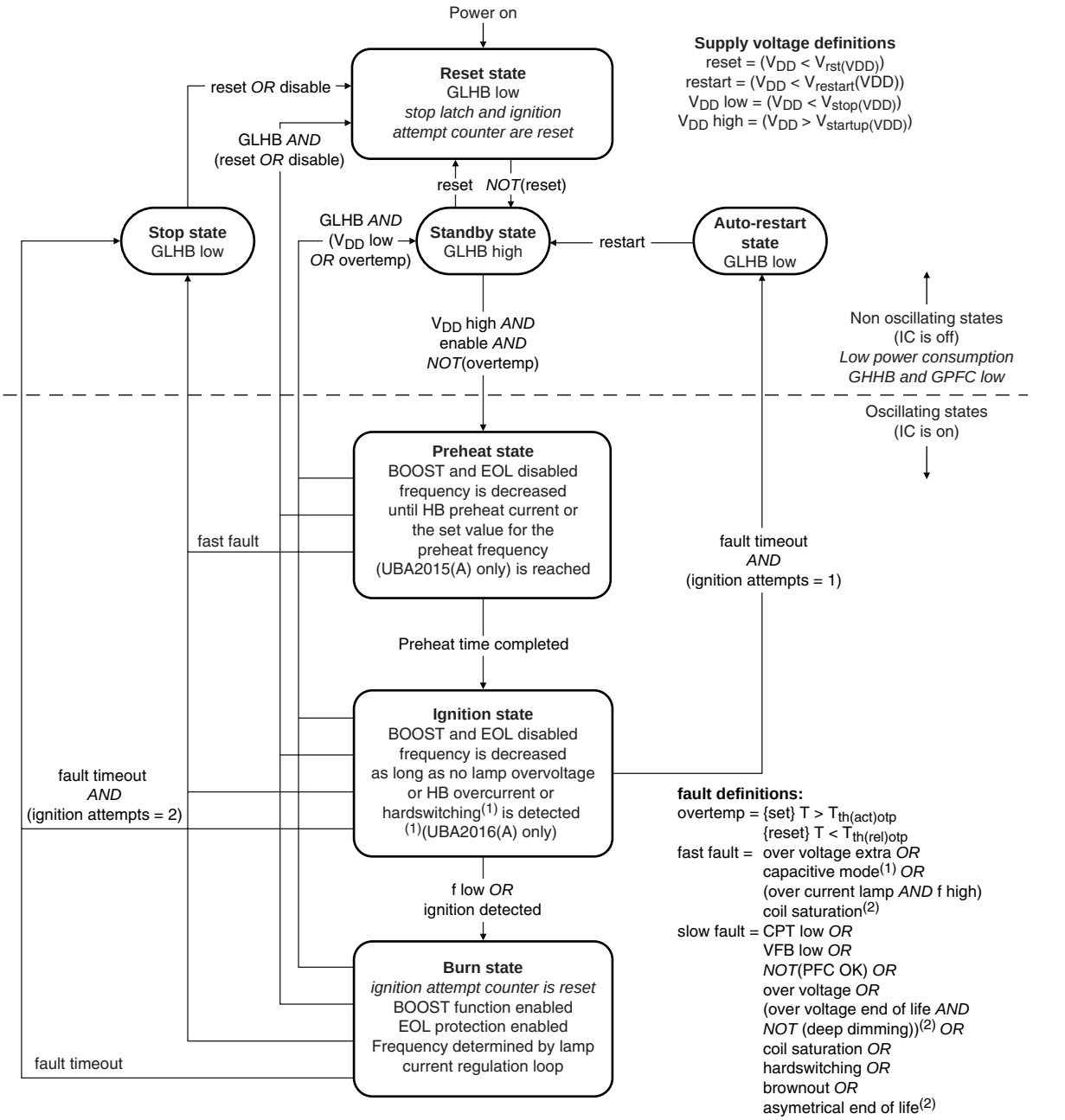


Fig 9. State diagram

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7.4.1 Reset

When voltage on pin VDD is below the reset voltage $V_{rst(VDD)}$, both gates of the half-bridge driver are LOW. All internal latches are reset. When voltage on pin VDD rises above $V_{rst(VDD)}$, the IC will enter STANDBY state.

7.4.2 Standby

In STANDBY state the low-side gate driver is on (GLHB is HIGH).The floating supply capacitor C_{FSHB} is then charged. When the VDD voltage rises above $V_{startup(VDD)}$, the Preheat state is entered.

7.4.3 Oscillating states (Preheat, Ignition and Burn)

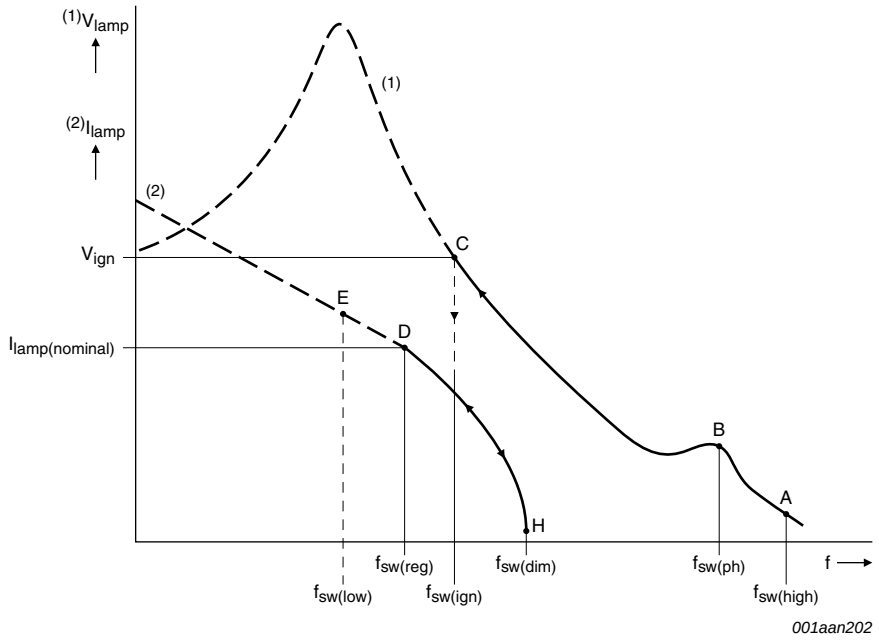
The highest and lowest oscillation frequency can be set with capacitor C_{CF} connected to the CF pin. The oscillator is implemented in such a way that the lowest frequency $f_{sw(low)}$ is the most accurate. In any oscillating state (Preheat, Ignition or Burn), when VDD voltage drops below $V_{stop(VDD)}$ or overtemperature is detected, the half-bridge stops oscillation when GLHB is HIGH and enters the STANDBY state.

7.4.4 Preheat

The oscillating frequency starts at $f_{sw(high)}$ (see Figure 10 “Resonance curve application with UBA2015A” or Figure 11 “Resonance curve application with UBA2016A” point A) and remains at that frequency until the PFC output is sufficient (the voltage at pin FBPFC rises above the PFC voltage OK threshold voltage on pin FBPFC, $V_{th(VPFCok)FBPFC}$) and the voltages at pins CPT and VFB settle above their pin short protection levels ($V_{VFB} > V_{th(osp)(VFB)}$ and $V_{CPT} > V_{th(scp)(CPT)}$). The half-bridge current is regulated when in the Preheat state; see Figure 10 “Resonance curve application with UBA2015A” or Figure 11 “Resonance curve application with UBA2016A” point B. Pin CIFB supplies a current $I_{ch(CIFB)}$ to the externally connected compensation network on this pin and its voltage will rise. This will cause the switching frequency to decrease (pin CIFB is the input for the voltage controlled oscillator). This will cause an increase in half-bridge current (assuming the switching frequency is higher than the load resonance frequency). This current is measured via pin SLHB using a resistor connected between the source of the low-side switch and ground. When the voltage on pin SLHB rises above the preheat current control voltage $V_{crtl(ph)SLHB}$, discharge current $I_{dch(CIFB)}$ to pin CIFB and the frequency is increased. When the voltage drops below $V_{th(ocp)SLHB}$, current $I_{ch(CIFB)}$ from pin CIFB causes the frequency to decrease.

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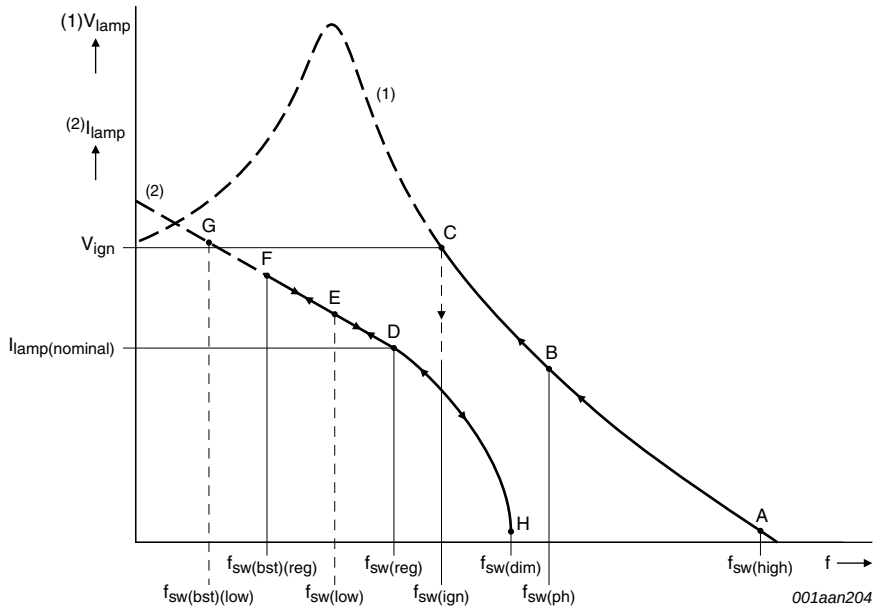
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(1) Lamp voltage when lamp is off (not ignited yet).

(2) Lamp current when lamp is on.

Fig 10. Resonance curve application with UBA2015A



(1) Lamp voltage when lamp is off (not ignited yet).

(2) Lamp current when lamp is on.

Fig 11. Resonance curve application with UBA2016A

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The preheat frequency for UBA2015 and UBA2015A can also be regulated via pin PH/EN. UBA2015 and UBA2015A support current controlled preheat and fixed frequency preheat. During preheat the output voltage of pin PH/EN is $V_{ph(PH/EN)}$. The output current that an external resistor $R_{ext(PH/EN)}$ connected to this pin sinks is compared to $^4/_5$ of the output current of the VCO (the current at pin CF with no fault condition present and the capacitor at that pin being charged minus the same current at $f_{sw(low)}$). As long as the output current of the VCO is bigger the frequency is being decreased (by charging pin CIFB with $I_{ch(CIFB)}$). If the current through the external resistor is bigger the frequency will be increased (by discharging pin CIFB with $I_{dch(CIFB)}$).

Current and fixed frequency control mechanisms are active at the same time. For fixed frequency preheat using pin PH/EN, the half-bridge current sense resistor connected to pin SLHB should be small enough not the activate the current control mechanism. If current controlled preheat is used, pin PH/EN should be left open (except of course for the open collector or open drain that drives the enable function). The preheat time $t_{to(ph)}$ can be set with capacitor C_{CPT} on pin CPT.

7.4.5 Ignition

After the Preheat state the IC enters the Ignition state. During the Ignition state the switching frequency is decreased by charging pin CIFB with $I_{ch(CIFB)}$. This will result in increasing lamp voltage until the lamp ignites (see point C in Figure 10 “Resonance curve application with UBA2015A” or Figure 11 “Resonance curve application with UBA2016A”) and lamp-on or $f_{sw(low)}$ (lowest frequency) is detected. Lamp-on detection occurs when the average absolute voltage on pin IFB is above lamp-on detection threshold $V_{th(lod)(IFB)}$ and the voltage on pin VFB is more then 50 % of each clock cycle below the lamp-on detection threshold $V_{th(lod)(VFB)}$ and after a delay $t_{d(lod)}$.

If either saturation, overvoltage or hard switching regulation (UBA2016A only) is triggered it will overrule the frequency sweep down and hold the frequency at the border where the fault appeared and start the fault timer. When the fault timeout $t_{to(fault)}$ is reached the IC enters Auto-restart state if it was the first ignition attempt, otherwise it will go to the Stop state; see Figure 9 “State diagram”.

7.4.6 Auto-restart

The Auto-restart state is entered after a fault time out in the Ignition state during the first ignition attempt. See Figure 9 “State diagram”. When the IC is in Auto-restart state, it draws supply current $I_{restart(VDD)}$. This will slowly discharge the buffer capacitor on pin VDD until the voltage on this pin drops below $V_{restart(VDD)}$. The IC then enters the Standby state. Here the VDD capacitor will be charged again to start a second ignition attempt. The bleeder current must be between standby current $I_{stb(VDD)}$ and $I_{restart(VDD)}$. A time delay can be set between the two ignition attempts with the capacitor at pin VDD to reduce stress on the HB components.

7.4.7 Burn

In Burn state the lamp current regulation and all protection circuits are active. The boost function (available in UBA2016A only) is also enabled.

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7.4.7.1 Lamp current control and dimming

The AC lamp current is sensed by an external resistor connected to pin IFB. The resulting AC voltage on pin IFB is internally Double-Side Rectified (DSR), and compared to a reference level by an OTA. This reference level is determined by the internal reference regulation level $V_{reg(ref)}$ and the voltage on the DIM input (UBA2015A and UBA2016A only), as shown in Figure 12 “Lamp current control”.

Definition: the regulation voltage on pin IFB ($V_{reg(IFB)}$) is the level seen from outside the IC to which the IC will try to regulate the average absolute voltage on pin IFB.
If the DIM input is not present or not connected or $V_{DIM} > V_{reg(ref)}$ then $V_{reg(IFB)}$ is $V_{reg(ref)}$ + non-idealities from the OTA and the DSR else $V_{reg(IFB)} = V_{DIM}$ + non-idealities from OTA and DSR.

For the UBA2016A $V_{reg(IFB)}$ also depends on the input current on pin BOOST (I_{BOOST}). The boost current is multiplied and added to the OTA output current which translates to an extra voltage being added to $V_{reg(ref)}$. See Section 7.4.7.3 “Boost” for further detail about the boost function. For the remainder of this Section we will assume $I_{BOOST} = 0$.

For the UBA2015A and UBA2016A the DIM input controls the lamp current set point. The DIM input level is internally clamped to $V_{reg(ref)}$. The lowest possible DIM input level is set by the bias current on pin DIM $I_{bias(DIM)}$ and the external resistance on the pin. If no dimming is required, pin DIM can be left open or connected via a capacitor to ground. The internal current source $I_{bias(DIM)}$ will then charge the pin until it is internally clamped to $V_{reg(ref)}$.

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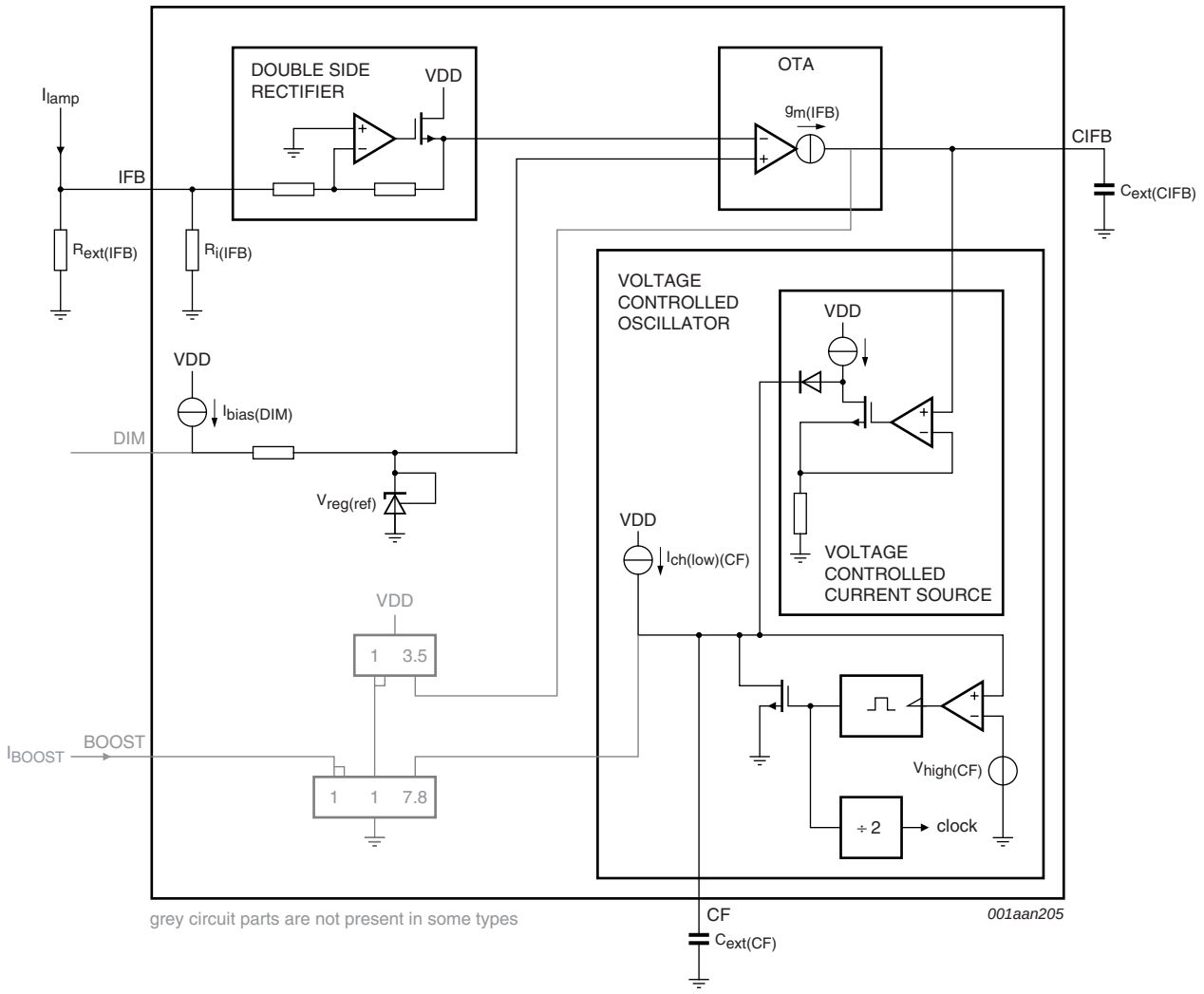


Fig 12. Lamp current control

The output of the OTA is connected to pin CIFB. The external capacitor $C_{ext(CIFB)}$ is charged and discharged according to the voltage on the OTA inputs and the transconductance of the OTA, $g_{m(IFB)}$ according to the formula:
$I_{CIFB} = g_{m(IFB)} \times (V_{IFB} - V_{reg(IFB)})$.
More components can be connected to pin CIFB to improve the response time and stability of the lamp current control loop.

Pin CIFB is connected to the input of the VCO (Voltage Controlled Oscillator) that determines the frequency of the IC. Pin CIFB voltage is inversely proportional to the switching frequency. When the load is inductive, an increase in frequency decreases the lamp current, and a decrease in frequency increases the lamp current. With the closed loop for the lamp current in place, the IC will regulate to the required frequency for the desired lamp current. So when the IC enters Burn state it will go to either point D or H shown in Figure 10 (UBA2015A) or Figure 11 (UBA2016A) depending on the DIM input voltage.

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However, the switching frequency can never go below $f_{sw(low)}$ (unless for UBA2016A when the boost function is active, see Section 7.4.7.3). If the regulation level is not reached at $f_{sw(low)}$ the IC will stay at $f_{sw(low)}$ (point E in Figure 10 and Figure 11).

7.4.7.2 Operation without lamp current control

To operate the lamp without current control the lamp current sense pin IFB must be connected to ground. The lamp now operates at the lowest frequency $f_{sw(low)}$ (point E in Figure 10 or Figure 11). Dimming is not supported in this case.

7.4.7.3 Boost

The boost feature is available only in the UBA2016A to support shorter run up times. The boost function changes the half-bridge switching frequency by lowering the lowest possible switching frequency from $f_{sw(low)}$ to $f_{sw(bst)(low)}$ and increasing the lamp current set point $V_{reg(IFB)}$ by adding a multiple of the boost current to the OTA output current which translates to an extra voltage being added to $V_{reg(ref)}$. During boost time, the frequency is lowered, and as a consequence of the inductive load the lamp current is increased.

The implementation of the boost function is shown in Figure 12 “Lamp current control”. The boost input is a current input with an input range of 0 to $I_{sat(BOOST)}$. The input current is internally clamped at $I_{sat(BOOST)}$. If the input current at the pin is above $I_{sat(BOOST)}$ the effect will not become bigger. The voltage on the pin is determined by the voltage drop across the internal current mirror input and limited by an internal clamp circuit if the input current at the pin rises above $I_{sat(BOOST)}$. For maximum current allowed into the pin; see Table 4. An example of how boost function can be implemented is shown in Figure 13.

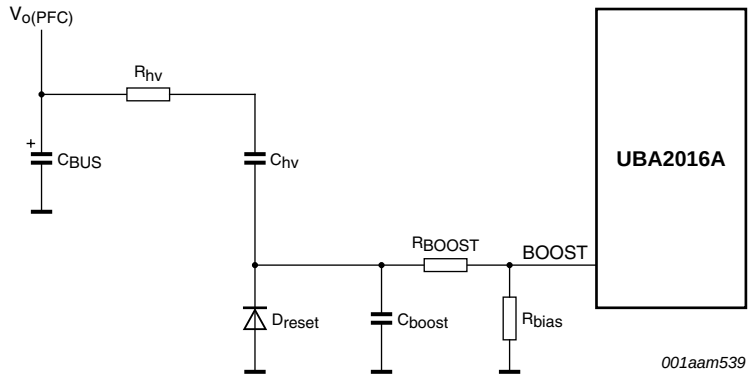


Fig 13. Boost application example; UBA2016A

The boost current is determined by resistor R_{BOOST}. R_{bias} provides a small threshold for the boost function and with capacitor C_{BOOST} keeps the BOOST pin at a defined (inactive) level (0 V) during normal lamp operation (after the boost period). The boost time constant is reflected by the sum of capacitors C_{hv} and C_{BOOST} and R_{BOOST}. Resistor R_{hv} and capacitor C_{BOOST} filter out the ripple on $V_{o(PFC)}$.
An example of component values for $V_{o(PFC)}$ = 430 V is:
R_{hv} = 22 MΩ (500 V); C_{hv} = 100 nF (500 V); D_{reset} = 1N4148; C_{BOOST} = 150 nF (63 V); R_{BOOST} = 10 MΩ and R_{bias} = 10 MΩ.

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The amount of boost depends on the current into the BOOST pin and the lamp current control. If the application does not use lamp current control, the switching frequency will go down to the lowest possible boost switching frequency $f_{sw(bst)(low)}$ (point G in Figure 11 "Resonance curve application with UBA2016A") that is determined by Equation 1 or Equation 2, depending on the value of I_{BOOST}.

$$0 \leq I_{BOOST} \leq I_{sat(BOOST)} \rightarrow f_{sw(bst)(low)} = f_{sw(low)}(1 - I_{BOOST} \cdot N_{f(bst)(low)}) \quad (1)$$

$$I_{BOOST} > I_{sat(BOOST)} \rightarrow f_{sw(bst)(low)} = f_{sw(low)}(1 - I_{sat(BOOST)} \cdot N_{f(bst)(low)}) \quad (2)$$

If the application uses lamp current control, the switching frequency is regulated to boost regulation voltage on pin IFB, $V_{reg(bst)(IFB)}$ (point F in Figure 11 "Resonance curve application with UBA2016A") that can be calculated by Equation 3 or Equation 4, (depending on the value of I_{BOOST}) if the switching frequency remains above $f_{sw(bst)(low)}$, otherwise the switching frequency is $f_{sw(bst)(low)}$; see Equation 1 or Equation 2.

$$0 \leq I_{BOOST} \leq I_{sat(BOOST)} \rightarrow V_{reg(IFB)}(I_{BOOST}) = V_{reg(IFB)}(1 + I_{BOOST} \cdot N_{l(bst)reg}) \quad (3)$$

$$I_{BOOST} > I_{sat(BOOST)} \rightarrow V_{reg(bst)(IFB)} = V_{reg(IFB)} + I_{sat(BOOST)} \cdot N_{Vreg(bst)} \quad (4)$$

7.4.8 Stop state

When in Stop state the IC is off and all driver outputs are low. The IC will remain in Stop state until the voltage on pin VDD drops below $V_{rst(VDD)}$ or it is disabled, in which case it will go to Reset state.

The sequence of events for entering the Stop state are shown in Figure 9 "State diagram".

7.5 Enable and Disable

The enable function is only available in the UBA2015 and UBA2015A and works via pin PH/EN. If this pin is pulled below the enable voltage $V_{en(PH/EN)}$ then the IC goes into the Standby state (immediately if GLHB is high, otherwise it will continue its normal clock cycle until GLHB is high and then go to the Standby state).

The external interface with pin PH/EN for the enable signal should be an open collector or open drain type driver. To enable the IC the open collector or open drain should be open (high ohmic) to not disturb the fixed frequency preheat setting function of pin PH/EN.

In Restart, Standby and Stop states the standby pull-up current source $I_{pu(stb)(PH/EN)}$ will pull the voltage at pin PH/EN above $V_{en(PH/EN)}$. In Preheat, Ignition and Burn states the normal output voltage driver of the IC will pull the pin high. In those cases the external driver must draw a current $I_{clamp(PH/EN)}$ from the pin to disable the IC.

7.6 Protection circuits

7.6.1 End-of-life rectifying lamp detection

If voltage on pin EOL is below low threshold voltage $V_{th(low)EOL}$ or above $V_{th(high)EOL}$ the fault timer will start. These threshold voltage levels are related to pin FBPFC voltage according to the formula: $V_{th(low)EOL} = V_{FBPFC} = V_{th(high)EOL} / 2$. The FBPFC voltage is sampled during GPFC low and hold during GPFC high periods to prevent disturbance of the EOL levels due to the switching of the PFC.

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A programmable end-of-life window is achieved by the internal bias current sink $I_{bias(EOL)}$. The effective relative size of the EOL window will decrease in line with the increasing series resistance connected to pin EOL.

The end-of-life lamp rectifying detection is only active during the Burn state.

7.6.2 End-of-life overvoltage detection

This protection is intended to protect against symmetrical lamp aging. When in Burn state the voltage on pin VFB exceeds the overvoltage end-of-life threshold voltage $V_{th(oveol)(VFB)}$ by more then 50 % of each switching cycle the fault timer will start. $V_{th(oveol)(VFB)}$ is related to the regulation voltage on pin IFB $V_{reg(IFB)}$ that itself is dependent on the voltage on pin DIM (see Section 7.4.7.1 “Lamp current control and dimming”) according to the formula:

$$V_{th(oveol)(VFB)} = a - b \times V_{reg(IFB)}$$

Parameters a and b can be calculated from the $V_{th(oveol)(VFB)}$ values given in Table 6.

The end-of-life overvoltage protection is only active during Burn state and (for UBA2015A and UBA2016A) if the voltage at pin DIM is above the overvoltage end-of-life enable voltage $V_{en(oveol)(DIM)}$.

7.6.3 Capacitive mode detection

Under all normal operating conditions the half-bridge switching frequency should be higher than the load resonance frequency. The load then shows an inductive behavior in that the load current I_{load} lags behind the half-bridge voltage V_{SHHB}. If the amplitude and the phase difference are large enough, the load current will charge any capacitance on pin SHHB during the non-overlap time $t_{no(LH)}$, and discharge it during the other non-overlap time $t_{no(HL)}$. As a result the voltage across the switches is almost zero at the moment they turn on. This is called zero voltage switching; see Figure 14 “Switching”. Zero voltage switching provides the highest switching efficiency and the least Electromagnetic Emission (EME).

Capacitive mode switching can occur when, due to any abnormal condition, the switching frequency is below the load resonance frequency. This can happen when the lamp is removed. The load current will then keep the backgate diode of the switch that is switched off conducting during the non-overlap time, and if the other switch is turned on, a sudden step of the half-bridge voltage to the other supply rail takes place (which causes huge current spikes). Also cross conduction between the switches can occur during the reverse recovery of the backgate diode. These effects put huge stress on the power switches, most of which can only handle capacitive mode switching a few times before they break down.

To protect against capacitive mode switching the IC monitors pin SHHB during the non-overlap time $t_{no(LH)}$ between switching off of the low-side switch and switching on of the high-side switch. If a rise of V_{SHHB} ($dV_{SHHB}/dt > V_{th(cm)(SHHB)}$) during $t_{no(LH)}$ is not detected then the IC will conclude that capacitive mode switching is occurring during the next full cycle. If capacitive mode is detected longer than the fault activation delay time $t_{det(fault)}$ then the IC will enter Stop state.

Capacitive mode detection is active in all oscillating states for all ICs except in the Ignition state of the UBA2016A if zero voltage switching has been observed. In that case the UBA2016A switches to hard switching regulation, see Section 7.6.4 “Hard switching regulation (UBA2016A)”.

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During ignition a situation may occur where the amplitude of the load current is high and the half-bridge is at the boundary of capacitive mode switching; see Figure 14 “Switching”. The load current crosses zero during the non-overlap time. If the amplitude of the load current is large enough, the UBA2015 and UBA2015A might not detect capacitive mode because V_{SHHB} did rise before going down again. The backgate diode of one switch is conducting again when the other switch switches on. Since this can only happen if the load current crosses zero during the non-overlap time, the momentary value of the load current at the end of the non-overlap time will be not so big, and will not necessarily damage the switches.

Depending on the topology used, the DC blocking capacitor might be charged via the lamp(s) at the moment the lamp(s) ignite. This will cause a temporary DC current addition to the load current that might be interpreted by the UBA2015 and UBA2015A as capacitive mode switching. If this happens the DC blocking capacitor must be reduced or pre-charged. The UBA2016A does not have this problem.

7.6.4 Hard switching regulation (UBA2016A)

In Ignition state the UBA2016A capacitive mode detection is disabled and replaced by hard switching regulation. This enables ignition without voltage feedback.

The hard switching regulation measures the voltage step on pin SHHB at the end of the non-overlap time $t_{no(LH)}$ ($V_{step(SHHB)}$ in Figure 14 “Switching”) and increases the switching frequency by discharging pin CIFB with a current according to the formula:

$$I_{dch(hswr)CIFB} = (V_{step(SHHB)} - V_{th(hswr)SHHB}) \times g_{m(hswr)}$$

In this way the IC keeps the switching frequency during ignition at the point where there is still a small phase difference between the load current and the half-bridge voltage, and the switching losses due to hard switching are limited. This is assuming that it is not already held at the higher frequency by the overvoltage protection or coil saturation protection.

As Figure 14 “Switching” shows, hard switching also occurs when the amplitude of the load current is to small. This might happen when the IC enters Ignition state at the end of preheat and the frequency is still relatively high. To prevent the IC from getting stuck at f_{high} the hard switching regulation is disabled until zero voltage switching has been observed, that is if $V_{step(SHHB)} < V_{th(zvs)SHHB}$.

7.6.5 Hard switching protection

The hard switching level $V_{step(SHHB)}$ step is measured via pin SHHB. The hard switching level is determined by measuring the voltage step on pin SHHB on the rising edge of pin GHHB; see Figure 14 “Switching”. When $V_{step(SHHB)}$ is above the hard switching protection threshold voltage on pin SHHB ($V_{th(hswp)SHHB}$) the fault timer is activated.

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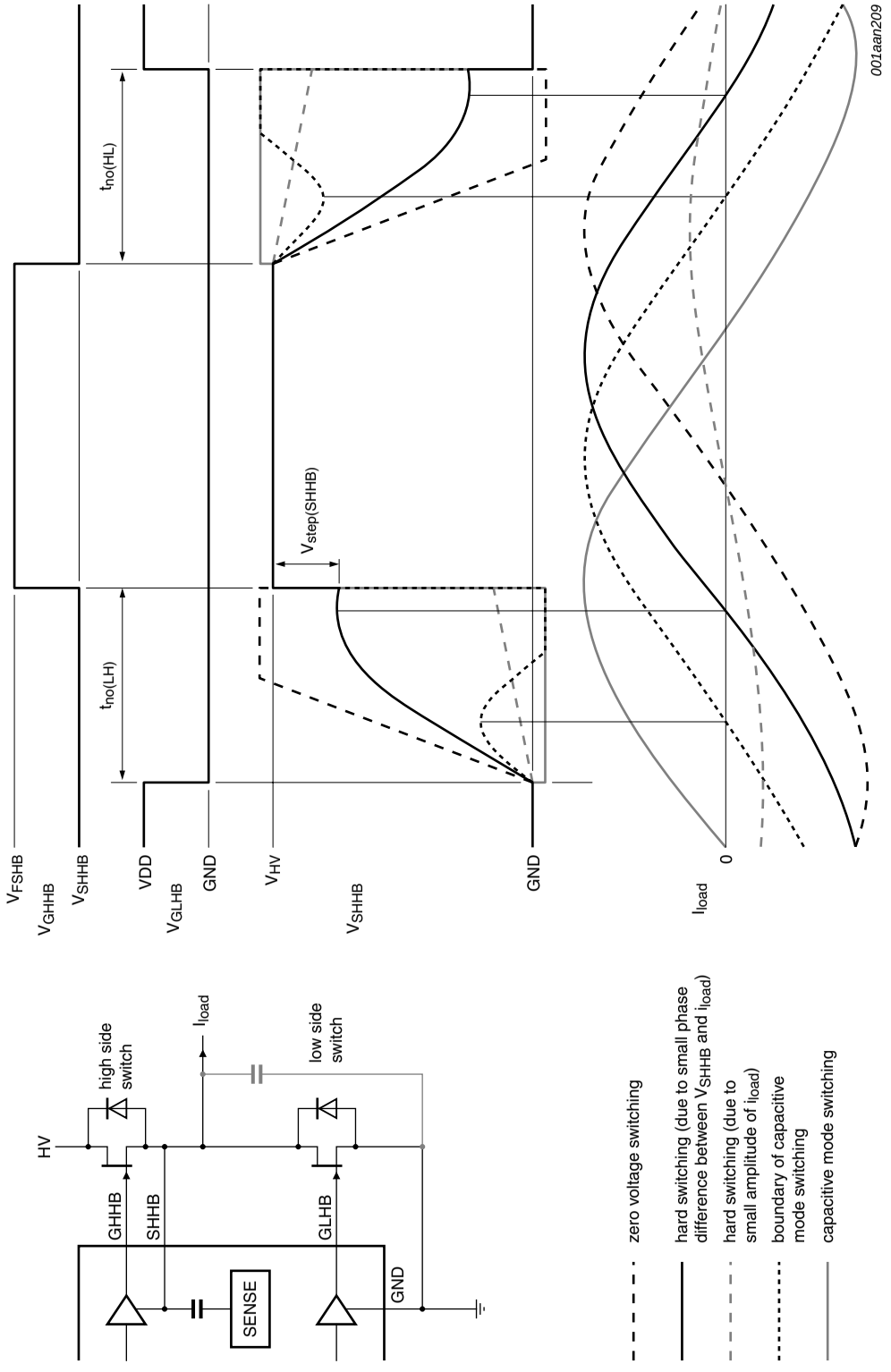


Fig 14. Switching

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7.6.6 Coil saturation protection

When the peak voltage on pin SLHB exceeds saturation threshold voltage $V_{th(sat)SLHB}$, an additional current $I_{add(CF)}$ is sourced to pin CF to shorten the running oscillator cycle. In Ignition state the fault timer is started and a discharge current $I_{dch(CIFB)}$ is drawn from pin CIFB during the next cycle to increase the switching frequency.

In Burn state the IC will go to Stop state if coil saturation is detected longer than the saturation detection delay time $t_{d(det)sat}$.

Current $I_{bias(SLHB)}$ is sourced to pin SLHB which will force the controller into coil saturation protection if pin SLHB is left open.

7.6.7 Lamp overcurrent protection

If voltage on pin IFB exceeds the overcurrent detection threshold voltage $V_{th(ocd)(IFB)}$, and the oscillator is running at $f_{sw(high)}$, an overcurrent is detected and the IC will immediately enter the Stop state.

7.6.8 Lamp overvoltage protection

When the peak voltage on pin VFB exceeds $V_{th(ov)(VFB)}$, the fault timer is started and a discharge current $I_{dch(CIFB)}$ is drawn from pin CIFB during the next cycle to increase the switching frequency.

When $V_{VFB} > V_{th(ovextra)(VFB)}$ for longer than the fault activation delay time $t_{det(fault)}$ then the IC will enter the Stop state.

7.6.9 Lamp removal detection

Removing the lamp from applications that have the resonant capacitor connected via the lamp filaments, will result in hard switching because current cannot flow through the ballast inductor.

If hard switching is detected during Ignition or Burn state the fault timer will be started.

For applications with the resonant capacitor connected directly to the ballast inductor, capacitive mode, coil saturation or over voltage will be detected. Capacitive mode is activated if the switching frequency ends up below the resonance frequency due to removal of the lamp. If the switching frequency is near or above the resonance frequency, the lamp (or rather the lamp socket) voltage and half-bridge current will be very high due to the unloaded resonant circuit (lamp inductor and lamp capacitor) which activates the coil saturation protection or the overvoltage protection.

7.6.10 Temperature protection

When the temperature is above $T_{th(act)otp}$ and GLHB is high, the IC enters Standby state. The IC cannot exit the Standby state until the temperature drops below $T_{th(rel)otp}$.

7.6.11 Fault timer

Any fault that starts the fault timer must be detected for longer than the fault activation delay time $t_{d(act)fault}$ to actually start the timer. When the timer is started, the capacitor at pin CPT is alternately being charged and discharged. After 8 charging and 7 discharging cycles the fault time-out period $t_{to(fault)}$ is reached and the IC enters either the Stop state or the Auto-restart state, depending on the fault detected, the current state of the timer and the number of ignition attempts; see Figure 9 “State diagram”. If the fault that started the

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timer is no longer detected for a period longer than the fault release delay time $t_{d(rel)fault}$, the fault timer will be reset and at any new occurance of the fault, the timer will start from zero.

Faults which activate the fault timer are shown as SlowFault in Figure 9 “State diagram”.

The fault timer uses the same pin (CPT) to set the time with an external capacitor $C_{ext(CPT)}$ as the preheat timer. The ratio between the preheat time-out time $t_{to(ph)}$ and the fault time-out time $t_{to(fault)}$ can be changed by adding an external series resistor $R_{s(ext)(CPT)}$ or an external parallel resistor $R_{p(ext)(CPT)}$ to the external capacitor $C_{ext(CPT)}$; see Figure 15 “CPT connections”.

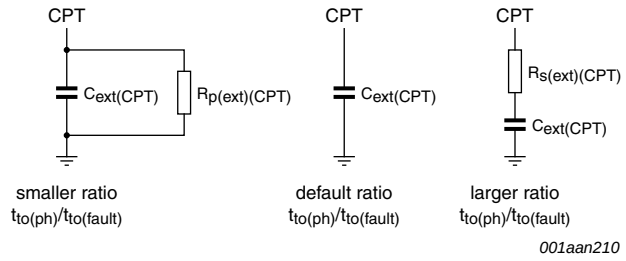


Fig 15. CPT connections

The fault timer incorporates a protection that ensures safe operation conditions if the CPT pin voltage is below $V_{th(scp)(CPT)}$ (shorted to GND) by holding the oscillation frequency at $f_{sw(high)}$.

7.6.12 Brownout protection

Brownout protection is designed to maintain stable and safe lamp operation during dips in mains supply. Without this protection the current demand from the bus voltage to maintain constant lamp power would increase upon a drop in bus voltage. This creates an unstable situation with the mains input voltage dropping and the PFC reaching its regulation range limit.

Brownout protection reduces the lamp power when the PFC is out of regulation. This situation is only allowed for a limited time to prevent excessive component stress.

When the PFC is outside its regulation range and the bus voltage is still too low ($V_{COMPPFC} = V_{clamp(COMPPFC)}$ and $V_{FBPFC} < V_{reg(FBPFC)}$), a brownout current $I_{bo(CF)}$ is added to the charge current at pin CF, thus increasing the $f_{sw(low)}$. A discharge brownout current $I_{dch(bo)(CIFB)}$ is also drawn from pin CIFB. Both $I_{bo(CF)}$ and $I_{dch(bo)(CIFB)}$ are proportional to the difference between V_{FBPFC} and $V_{reg(FBPFC)}$. If $V_{FBPFC} < V_{th(bo)(FBPFC)}$ the fault timer will start.

The start-up bleeder resistor and the regulation range of the PFC should be dimensioned in such a way that if the fault timer times out on brownout protection and the IC enters Stop state, the input mains voltage is too low to support the standby current of the IC via the bleeder resistor. The IC will then automatically reset and start-up in normal mode (and reignite the lamps) when the mains voltage has returned to normal.

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8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages referenced to signal ground (GND pin 15); current flow into the IC is positive.

Symbol	Parameter	Conditions	Min	Max	Unit
General					
$R_{ref(IREF)}$	reference resistance on pin IREF		30	36	kΩ
SR	slew rate	pins FSHB, GHHB and SHHB	–4	+4	V/ns
T_{amb}	ambient temperature		–40	+125	°C
T_j	junction temperature		–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
Voltage					
V_{FSHB}	voltage on pin FSHB	continuous	0	570	V
		t < 0.5 s	0	630	V
		with respect to V_{SHHB}	–0.3	+14	V
V_{GHHB}	voltage on pin GHHB	with respect to V_{SHHB}	–0.3	+14	V
V_{GLHB}	voltage on pin GLHB		–0.3	+14	V
V_{GPFC}	voltage on pin GPFC		–0.3	+14	V
V_{VDD}	voltage on pin VDD		–0.3	+14	V
V_{AUXPFC}	voltage on pin AUXPFC		–9	+9	V
V_{EOL}	voltage on pin EOL		–9	+9	V
V_{SLHB}	voltage on pin SLHB		–9	+9	V
V_{IFB}	voltage on pin IFB		–5	+5	V
V_{DIM}	voltage on pin DIM		–0.1	+5	V
V_{FBPFC}	voltage on pin FBPFC		–0.1	+5	V
V_{BOOST}	voltage on pin BOOST		–0.3	+2.2	V
$V_{PH/EN}$	voltage on pin PH/EN		–0.1	+5	V
V_{VFB}	voltage on pin VFB		–0.1	+5	V
Current					
I_{VDD}	current on pin VDD		-	50	mA
I_{EOL}	current on pin EOL		–1	+1	mA
I_{SLHB}	current on pin SLHB		–1	+1	mA
I_{BOOST}	current on pin BOOST		–50	+50	μA
I_{AUXPFC}	current on pin AUXPFC		–1	+1	mA

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Table 4. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages referenced to signal ground (GND pin 15); current flow into the IC is positive.

Symbol	Parameter	Conditions	Min	Max	Unit
ElectroStatic Discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM)			
		JEDEC Class 2 for pins: SLHB, IFB, EOL, CIFB, CPT, IREF, VFB, CF, DIM, BOOST, PH/EN, FBPFC, COMPPFC, AUXPFC, GPFC, VDD and GLHB	–2	+2	kV
		JEDEC Class 1C for pins: GHHB, FSHB and SHHB	–1	+1	kV
		Charge Device Model (CDM)			
		JEDEC Class 2 for pins: SHHB, FSHB, GHHB	–200	+200	V
		JEDEC Class 3 for pins: SLHB, IFB, EOL, VFB, IREF, CIFB, CF, CPT, DIM, BOOST, PH/EN, FBPFC, COMPPFC, AUXPFC, GPFC, VDD, GLHB	–500	+500	V
Latch-up					
I_{lu}		latch-up current [1]	–100	+100	mA

[1] Positive and negative latch-up currents tested at T_j = 150 °C by discharging a 22 μF capacitor though a 50 Ω series resistor with a 350 μH series inductor. Latch-up current values are in accordance with the general quality specification.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; mounted on a single-sided PCB; SO20 package	100	K/W
		in free air; mounted on a single-sided PCB; DIP20 package	90	K/W

10. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High voltage						
I_{leak}	leakage current	V_{FSHB} = 630 V; V_{GHHB} = 630 V; V_{SHHB} = 630 V; V_{VDD} = 0 V	-	-	2	μA
Start-up						
$V_{startup(VDD)}$	start-up voltage on pin VDD		11.9	12.4	12.9	V
$V_{stop(VDD)}$	stop voltage on pin VDD		9.6	10.0	10.4	V
$V_{hys(VDD)}$	hysteresis voltage on pin VDD		2.1	2.4	2.7	V
$I_{stb(VDD)}$	standby current on pin VDD	V_{VDD} = 11.5 V	0.20	0.24	0.28	mA
$I_{pu(stb)(PH/EN)}$	standby pull-up current on pin PH/EN	Standby or Stop state; $V_{PH/EN}$ = 0.25 V	7.7	9	10.3	μA
$V_{rst(VDD)}$	reset voltage on pin VDD		3.6	4.2	4.8	V

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Table 6. Characteristics *…continued*

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{restart(VDD)}$	restart voltage on pin VDD		6.2	6.5	6.8	V
$I_{restart(VDD)}$	restart current on pin VDD	V_{VDD} = 9 V	0.85	1.10	1.35	mA
$V_{clamp(VDD)}$	clamp voltage on pin VDD	IC off; I_{VDD} = 0.33 mA	13.0	13.4	13.8	V
$I_{clamp(VDD)}$	clamp current on pin VDD	IC off; V_{VDD} = 14.0 V	25	45	-	mA
I_{VDD}	current on pin VDD	V_{FBPFC} = 1.2 V; $V_{COMPPFC}$ = 1 V	1.2	1.7	2.2	mA
PFC normal operation						
$t_{on(PFC)}$	PFC on-time	$V_{COMPPFC}$ = 350 mV	0.70	1.05	1.40	µs
$t_{on(PFC)high}$	high PFC on-time	$V_{COMPPFC}$ = $V_{high(COMPPFC)}$	24	28	32	µs
$t_{off(PFC)low}$	low PFC off-time		1.7	2.0	2.3	µs
$t_{leb(FBPFC)}$	leading edge blanking time on pin FBPFC	from the start of rising edge on pin GPFC	260	330	400	ns
$V_{reg(FBPFC)}$	regulation voltage on pin FBPFC	$V_{COMPPFC}$ = 1.6 V	1.23	1.27	1.31	V
		$V_{COMPPFC}$ = 200 mV	1.23	1.28	1.33	V
$I_{bias(FBPFC)}$	bias current on pin FBPFC	V_{FBPFC} = 1.27 V	4.5	5.0	5.5	µA
$g_{m(PFC)}$	PFC transconductance	$V_{COMPPFC}$ = 1.5 V; 1.2 V < V_{FBPFC} < 1.34 V	25	30	35	µA/V
$V_{th(VPFCok)FBPFC}$	PFC voltage OK threshold voltage on pin FBPFC		0.95	1.00	1.05	V
$V_{det(demag)}$	demagnetization detection voltage	on pin AUXPFC	50	100	150	mV
$V_{clamp(COMPPFC)}$	clamp voltage on pin COMPPFC	V_{FBPFC} = 1 V	2.85	3.00	3.15	V
PFC protection						
$t_{on(PFC)nodemag}$	no demagnetization detected PFC on-time		1.0	1.3	1.6	µs
$V_{th(osp)(FBPFC)}$	open/short protection threshold voltage on pin FBPFC		0.20	0.25	0.30	V
$V_{th(ov)(FBPFC)}$	overvoltage threshold voltage on pin FBPFC		1.34	1.39	1.43	V
$I_{bias(AUXPFC)}$	bias current on pin AUXPFC	V_{AUXPFC} = 0.1 V	–6	–5	–4	µA
PFC driver						
$I_{source(GPFC)}$	source current on pin GPFC	V_{GPFC} = 4 V; V_{VDD} = 12 V	–105	–90	–75	mA
$R_{sink(GPFC)}$	sink resistance on pin GPFC	V_{GPFC} = 2 V; V_{VDD} = 12 V	13.5	16.0	18.5	Ω
HB preheat						
$R_{ext(PH/EN)}$	external resistor on pin PH/EN		38.6	-	-	kΩ
$t_{to(ph)}$	preheat time-out time	C_{CPT} = 100 nF	0.80	0.94	1.08	s
$V_{O(ph)(PH/EN)}$	preheat output voltage on pin PH/EN	Preheat or Ignition state	1.78	1.84	1.90	V
$V_{ctrl(ph)SLHB}$	overcurrent protection threshold voltage on pin SLHB	preheat	0.44	0.48	0.52	V
$I_{ch(CIFB)}$	charge current on pin CIFB	no fault detected; Preheat and Ignition states only; V_{CIFB} = 1.5 V	–10.3	–9.0	–7.7	µA

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Table 6. Characteristics *…continued*

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{dch(CIFB)}$	discharge current on pin CIFB	preheat overcurrent detected; V_{CIFB} = 1.5 V	7.7	9.0	10.3	µA
$f_{sw(ph)}$	preheat switching frequency	UBA2015; UBA2015A				
		$R_{ext(PH/EN)}$ = 40 kΩ; $C_{ext(CF)}$ = 200 pF	93	97.7	102.4	kHz
		$R_{ext(PH/EN)}$ = 100 kΩ; $C_{ext(CF)}$ = 200 pF	62	66	70	kHz
HB lamp ignition						
$f_{sw(high)}/f_{sw(low)}$	high switching frequency to low switching frequency ratio		2.2	2.4	2.6	
$V_{fsw(low)(CIFB)}$	low switching frequency voltage on pin CIFB		-	3.0	-	V
$V_{th(lod)(IFB)}$	lamp on detection threshold voltage on pin IFB		1.00	1.11	1.22	V
$V_{th(lod)(VFB)}$	lamp on detection threshold voltage on pin VFB		0.9	1.0	1.1	V
$V_{(Vreg-Vth(lod))}$	regulation voltage to lamp-on-detect threshold voltage difference	pin IFB	40	160	220	mV
$t_{d(lod)}$	lamp on detection delay time		2	3	4	ms
HB normal operation						
$f_{sw(low)}$	low switching frequency	C_{CF} = 200 pF	41	43	45	kHz
			20	-	80	kHz
$V_{high(CF)}$	high voltage on pin CF		-	2.5	-	V
$V_{reg(IFB)}$	regulation voltage on pin IFB	V_{CIFB} = 2 V; V_{IFB} > 0 V	1.22	1.27	1.32	V
		V_{CIFB} = 2 V; V_{DIM} = 127 mV; V_{IFB} > 0 V	77	127	177	mV
		V_{CIFB} = 2 V; V_{IFB} < 0 V	−1.34	−1.27	−1.2	V
		V_{CIFB} = 2 V; V_{DIM} = 127 mV; V_{IFB} < 0 V	−197	−127	−57	mV
$I_{ch(low)(CF)}$	low charge current on pin CF		-	47	-	µA
$V_{i(IFB)}$	input voltage range on pin IFB	V_{CIFB} = 2 V	−3.1	-	+3.1	V
$R_{i(IFB)}$	input resistance on pin IFB	V_{IFB} = 1 V	-	60	-	kΩ
		V_{IFB} = −1 V	-	30	-	kΩ
$V_{en(PH/EN)}$	enable voltage on pin PH/EN		0.21	0.25	0.29	V
$V_{O(burn)(PH/EN)}$	burn state output voltage on pin PH/EN	Burn state	1.21	1.27	1.33	V
$g_{m(IFB)}$	IFB transconductance	V_{CIFB} = 2 V	14	16.5	19	µA/V
$I_{O(clamp)(PH/EN)}$	output current clamp on pin PH/EN	Preheat, Ignition or Burn states; $V_{PH/EN}$ = 0.2 V	-	-	0.16	mA
HB driver						
$I_{source(GLHB)}$	source current on pin GLHB	V_{GLHB} = 4 V	−105	−90	−75	mA
$R_{sink(GLHB)}$	sink resistance on pin GLHB	V_{GLHB} = 2 V	13.5	16	18.5	Ω
$I_{source(GHHB)}$	source current on pin GHHB	V_{SHHB} = 0 V; V_{GHHB} = 4 V	−105	−90	−75	mA

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Table 6. Characteristics *...continued*

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{sink(GHHB)}$	sink resistance on pin GHHB	V_{SHHB} = 0 V; V_{GHHB} = 2 V	13.5	16	18.5	Ω
t_{no}	non-overlap time		1.25	1.50	1.75	µs
$V_{Fd(bs)}$	bootstrap diode forward voltage	I_{FS} = 5 mA	1.0	1.5	2.0	V
Dimming						
$I_{bias(DIM)}$	bias current on pin DIM	V_{DIM} = 1 V	−28	−26	−24	µA
$R_{i(DIM)}$	input resistance on pin DIM	V_{DIM} = 2.5 V	-	30	-	kΩ
HB protection						
$V_{th(sat)(SLHB)}$	saturation threshold voltage on pin SLHB		2.35	2.50	2.65	V
$t_{d(det)sat}$	saturation detection delay time	Burn state	-	0.3	-	µs
$t_{leb(SLHB)}$	leading edge blanking time on pin SLHB		260	340	420	ns
$I_{add(CF)}$	additional current on pin CF	$V_{SLHB} > V_{th(sat)SLHB}$; V_{CF} = 2 V	−107	−96	−85	µA
$I_{bias(SLHB)}$	bias current on pin SLHB	V_{SLHB} = 2.5 V	−10	−8.5	−7	µA
$V_{th(ocd)(IFB)}$	overcurrent detection threshold voltage on pin IFB		2.8	3.0	3.2	V
$V_{th(osp)(VFB)}$	open/short protection threshold voltage on pin VFB		40	80	120	mV
$V_{th(ov)(VFB)}$	overvoltage threshold voltage on pin VFB		2.4	2.5	2.6	V
$t_{det(fault)}$	fault detection time		-	125	-	µs
		overvoltage extra or capacitive mode during burn state	-	50	-	µs
$t_{rel(fault)}$	fault release time		-	1	-	ms
$V_{th(ovextra)(VFB)}$	overvoltage extra threshold voltage on pin VFB		3.2	3.35	3.5	V
$I_{bias(VFB)}$	bias current on pin VFB		2.3	2.6	2.9	µA
$V_{th(low)EOL}$	low threshold voltage on pin EOL	V_{FBPFC} = 1.27 V	1.21	1.27	1.33	V
$V_{th(high)EOL}$	high threshold voltage on pin EOL	V_{FBPFC} = 1.27 V	2.39	2.54	2.69	V
$I_{bias(EOL)}$	bias current on pin EOL	V_{EOL} = 1.9 V	15.2	16.0	16.8	µA
$V_{th(oveol)(VFB)}$	overvoltage end-of-life threshold voltage on pin VFB	pin DIM open	0.8	0.88	0.96	V
		UBA2015A; UBA2016A				
		V_{DIM} = 1.0 V	0.92	1.0	1.08	V
		UBA2015A; UBA2016A				
		V_{DIM} = 0.5 V	1.15	1.23	1.31	V
$V_{en(oveol)(DIM)}$	overvoltage end-of-life enable voltage on pin DIM	UBA2015A; UBA2016A	0.21	0.25	0.29	V
$V_{th(hswp)SHHB}$	hard switching protection threshold voltage on pin SHHB	f_{sw} = 50 kHz	-	100	-	V
$V_{th(zvs)SHHB}$	zero voltage switching detection threshold voltage on pin SHHB	f_{sw} = 50 kHz	-	30	-	V
$V_{th(hswr)SHHB}$	hard switching regulation threshold voltage on pin SHHB	f_{sw} = 50 kHz	-	100	-	V

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Table 6. Characteristics *...continued*

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(cm)SHHB}$	capacitive mode detection threshold voltage on pin SHHB	$t_{no(LH)}$	-	30	-	V/µs
$g_{m(hswr)}$	hard switching regulation transconductance	UBA2016A; Ignition state				
		hard switching step on pin SHHB above $V_{th(hswr)(SHHB)}$ per extra volt step at f_{sw} = 50 kHz	-	18	-	µA/V
$V_{th(scp)(CPT)}$	short-circuit protection threshold voltage on pin CPT		80	120	160	mV
$R_{par(ext)(CPT)}$	external parallel resistance on pin CPT		700	-	-	kΩ
$R_{s(ext)(CPT)}$	external series resistance on pin CPT		-	-	40	kΩ
$t_{to(fault)}$	fault time-out time	C_{CPT} = 100 nF	0.16	0.19	0.22	s
$t_{to(ph)}/t_{to(fault)}$	ratio between preheat time-out time and fault time-out time	$R_{par(ext)}$ = 700 kΩ; $R_{s(ext)}$ not connected (short)	3	3.4	3.8	
		$R_{par(ext)}$ not connected (open); $R_{s(ext)}$ not connected (short)	4.7	5.2	5.7	
		$R_{par(ext)}$ not connected (open); $R_{s(ext)}$ = 40 kΩ	9	11.5	14	
$I_{bo(CF)}$	brownout current on pin CF	$V_{COMPPFC} = V_{high(COMPPFC)}$; V_{FBPFC} = 1.0 V; V_{CF} = 1.5 V	12	17	22	µA
$V_{(Vreg-Vth(bo))}$	regulation voltage to brownout threshold voltage difference on pin FBPFC	$V_{COMPPFC} = V_{high(COMPPFC)}$ [2]	10	30	50	mV
$I_{dch(bo)CIFB}$	brownout discharge current on pin CIFB	$V_{COMPPFC} = V_{high(COMPPFC)}$; V_{FBPFC} = 1.0 V; V_{CIFB} = 2.0 V	14	18	22	µA
Boost						
$f_{sw(bst)(low)}$	low boost switching frequency	$I_{BOOST} \geq I_{sat(BOOST)}$; $C_{ext(CF)}$ = 200 pF	21	24	27	kHz
$N_{f(bst)low}$	low boost frequency constant		0.14	0.165	0.19	1/µA
$V_{reg(bst)(IFB)}$	boost regulation voltage on pin IFB	$I_{BOOST} \geq I_{sat(BOOST)}$	1.75	1.84	1.93	V
$N_{Vreg(bst)}$	boost regulation voltage constant		0.180	0.21	0.24	V/µA
$I_{sat(BOOST)}$	saturation current on pin BOOST		2.3	2.7	3.1	µA
V_{BOOST}	voltage on pin BOOST	I_{BOOST} = 1 µA	-	1	-	V
		I_{BOOST} = 5 µA	-	1.4	-	V
		I_{BOOST} = 50 µA	-	-	2.2	V
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		120	140	160	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		65	80	95	°C

[1] Default setting; see Table 7.

[2] The threshold for the brownout protection is slightly below the normal regulation level on pin FBPFC. The design guarantees that it will always be below this level because the clamp current from the PFC OTA is used as a signal.

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Table 7. Default settings for characteristics

Pin name	Pin	Application
SLHB	1	connected to ground
IFB	2	connected to ground
EOL	3	connected to a 2 V test supply
VFB	4	connected to a 2 V test supply
IREF	5	connected via a 33 kΩ resistor to ground
CIFB	6	connected via a 100 nF capacitor to ground
CF	7	connected via a 200 pF C0G (NP0) capacitor to ground
CPT	8	connected via a 100 nF capacitor to ground
DIM	9	connected via a 100 pF capacitor to ground
BOOST	10	connected to ground; UBA2016A
PH/EN	10	not connected; UBA2015 and UBA2015A
FBPFC	11	connected to a 1.27 V test supply
COMPPFC	12	connected via a 100 nF capacitor to ground
AUXPFC	13	connected to ground
GPFC	14	not connected (open)
GND	15	connected to ground
VDD	16	connected to a 13 V test supply
GLHB	17	not connected (open)
SHHB	18	connected to ground
FSHB	19	connected to a 13 V test supply
GHHB	20	not connected (open)

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11. Application information

11.1 Connecting the IC in an application

A 33 kΩ resistor must be connected between pin IREF and GND. The tolerance of this resistor adds to any current related tolerances of the IC, including $f_{sw(low)}$. No other components can be connected to pin IREF.

Tolerance and temperature dependency of the capacitor connected between pin CF and GND will add to the tolerance on $f_{sw(low)}$.

Small decoupling capacitors (about 100 pF) are recommended on pins FBPFC and IFB close to the IC.

Normal sized decoupling capacitors (about 10 nF) are recommended on pins DIM and EOL.

The capacitors at pins CF, COMPPFC, CPT, FSHB and VDD should also be placed close to the IC.

A capacitor between pin CIFB and GND of at least 470 pF is needed for stability of the low switching frequency.

A capacitor between pin VDD and GND of at least 10 nF is needed for stability of the internal VDD voltage clamp. However, for reliable operation of the IC a low ESR type of at least 470 nF is recommended.

A capacitor between pin FSHB and SHHB is needed to supply the high-side driver. The recommended value for this capacitor is $\frac{1}{5}$ of the value of the capacitor at VDD.

A series resistor of at least 1 kΩ is recommended on pins AUXPFC and SLHB.

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11.2 Without lamp current regulation or dimming

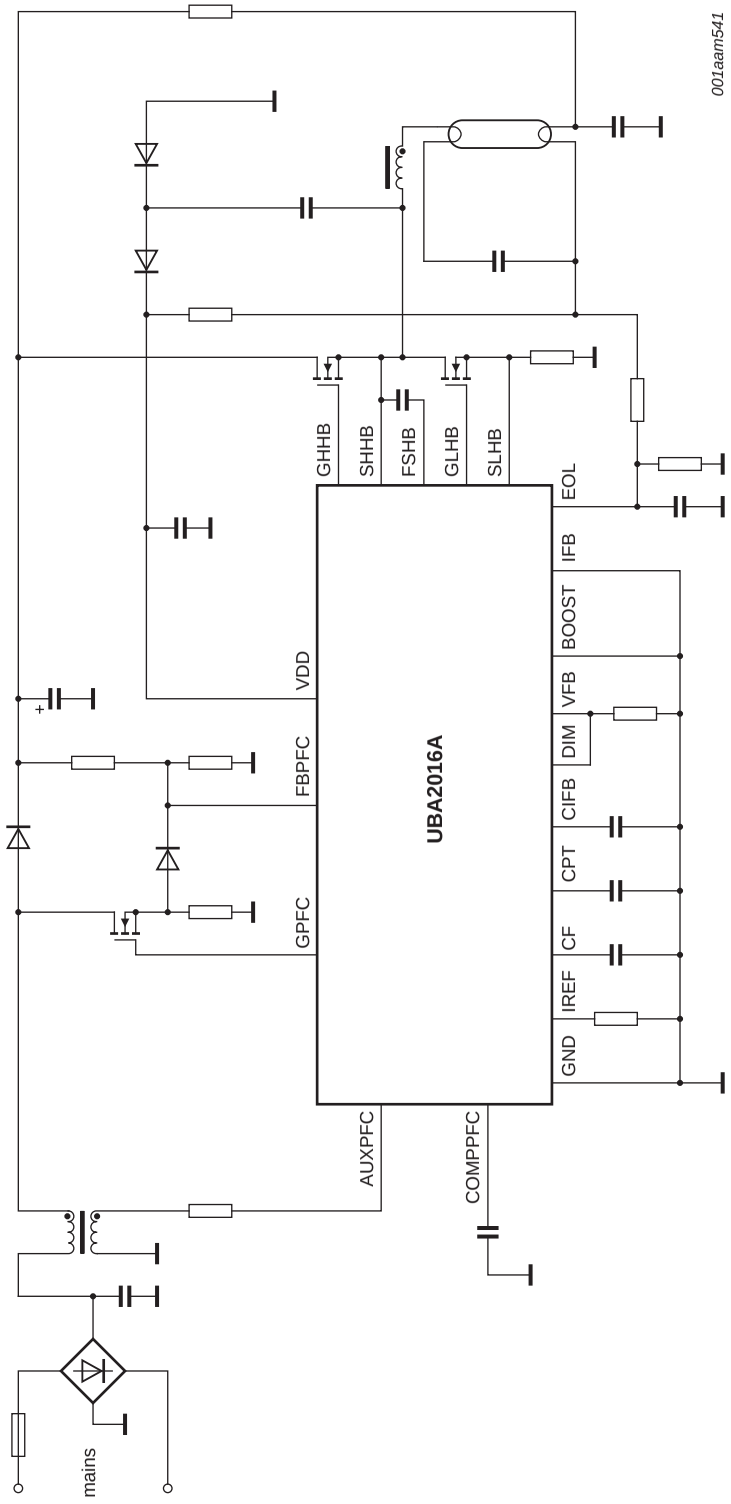


Fig 16. Typical schematic for minimal TL or CFL application with UBA2016A (mains filter not shown)

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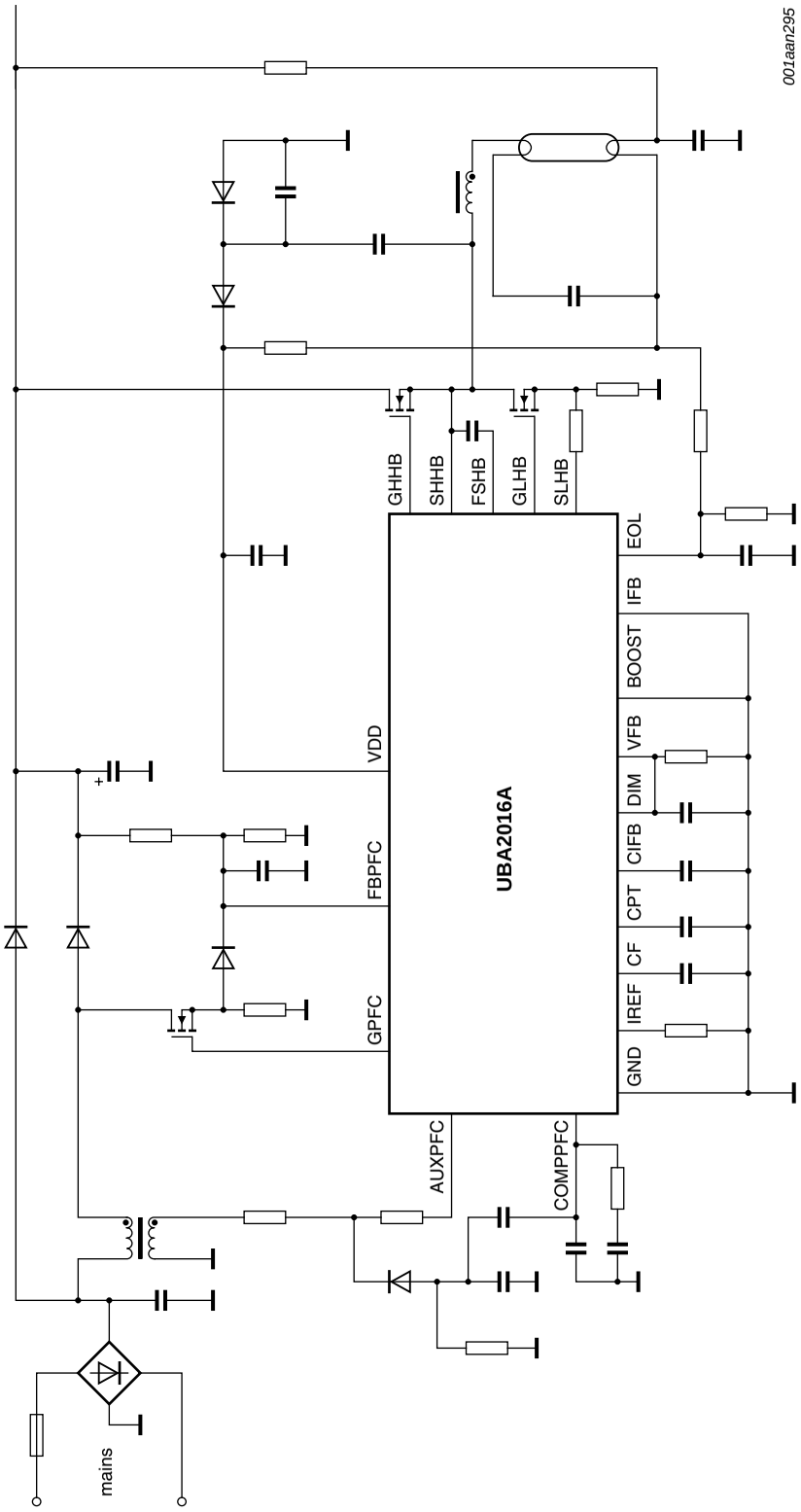


Fig 17. Typical schematic for basic TL or CFL application (better PFC performance than minimal application) (mains filter not shown)

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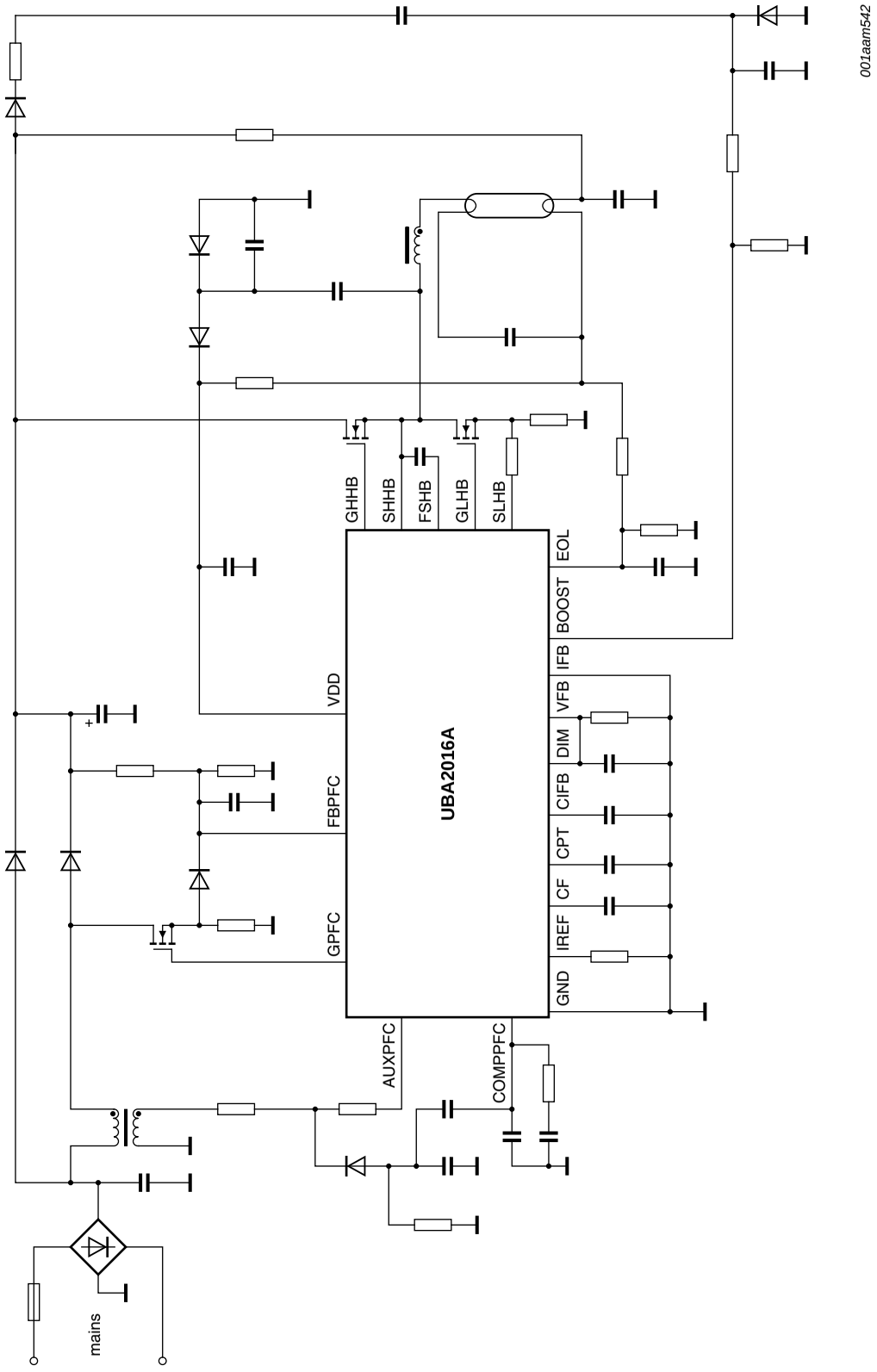


Fig 18. Typical schematic for basic TL or CFL application with UBA2016A with fixed time boost start (mains filter not shown)

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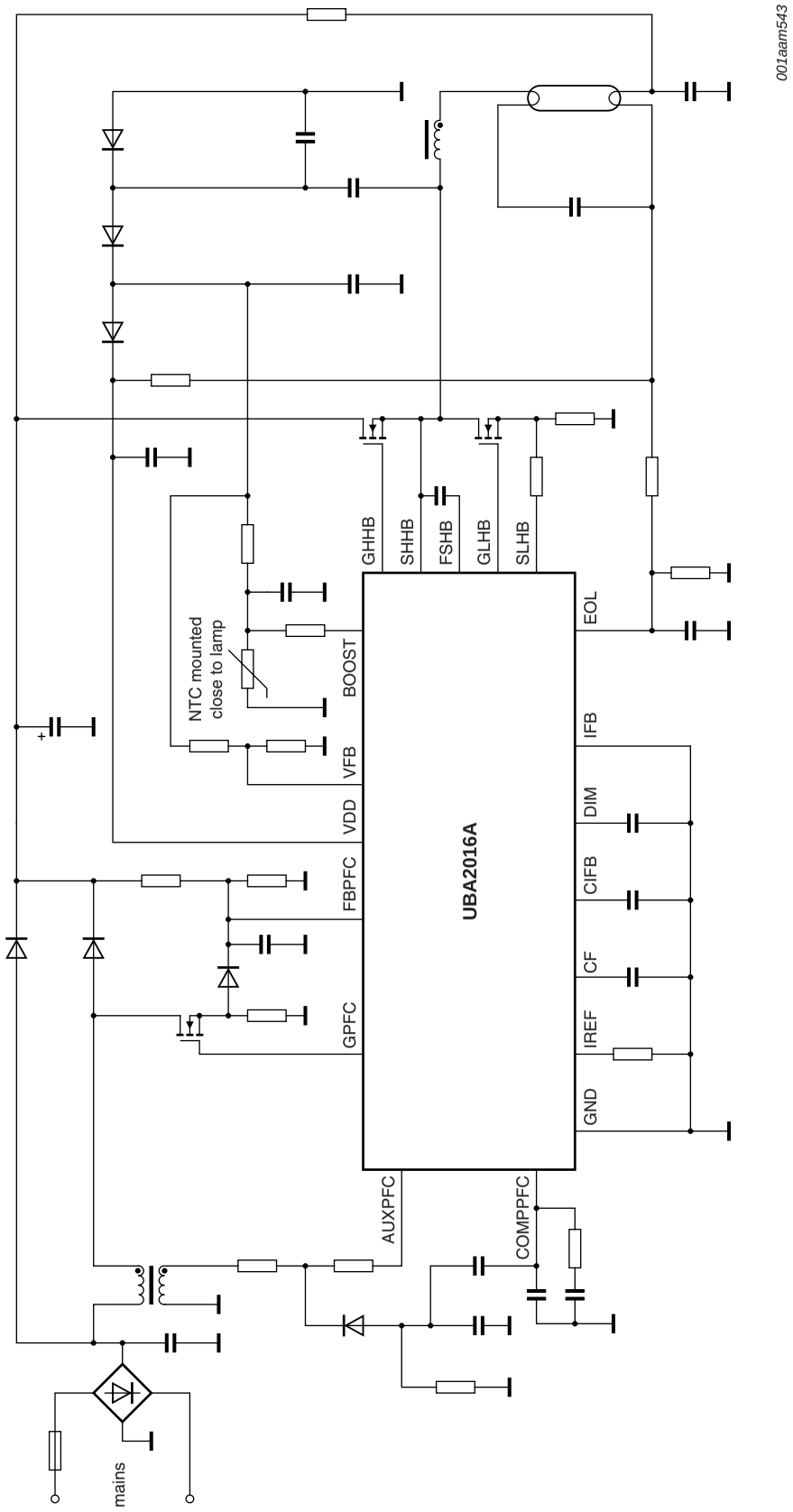


Fig 19. Typical schematic for basic TL or CFL application with UBA2016A, with lamp temperature-dependent boost start (mains filter not shown)

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11.3 With lamp current regulation and dimming

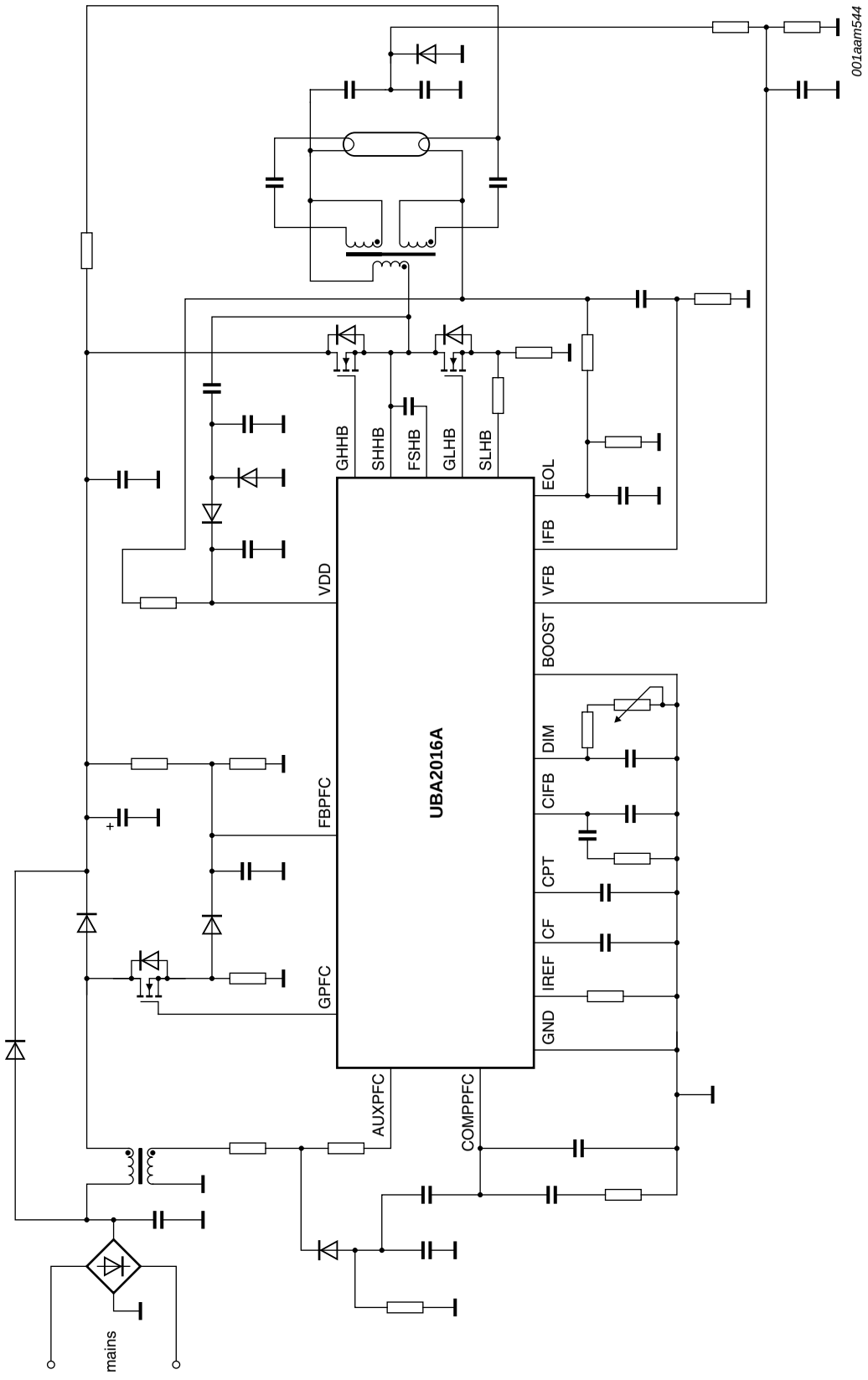


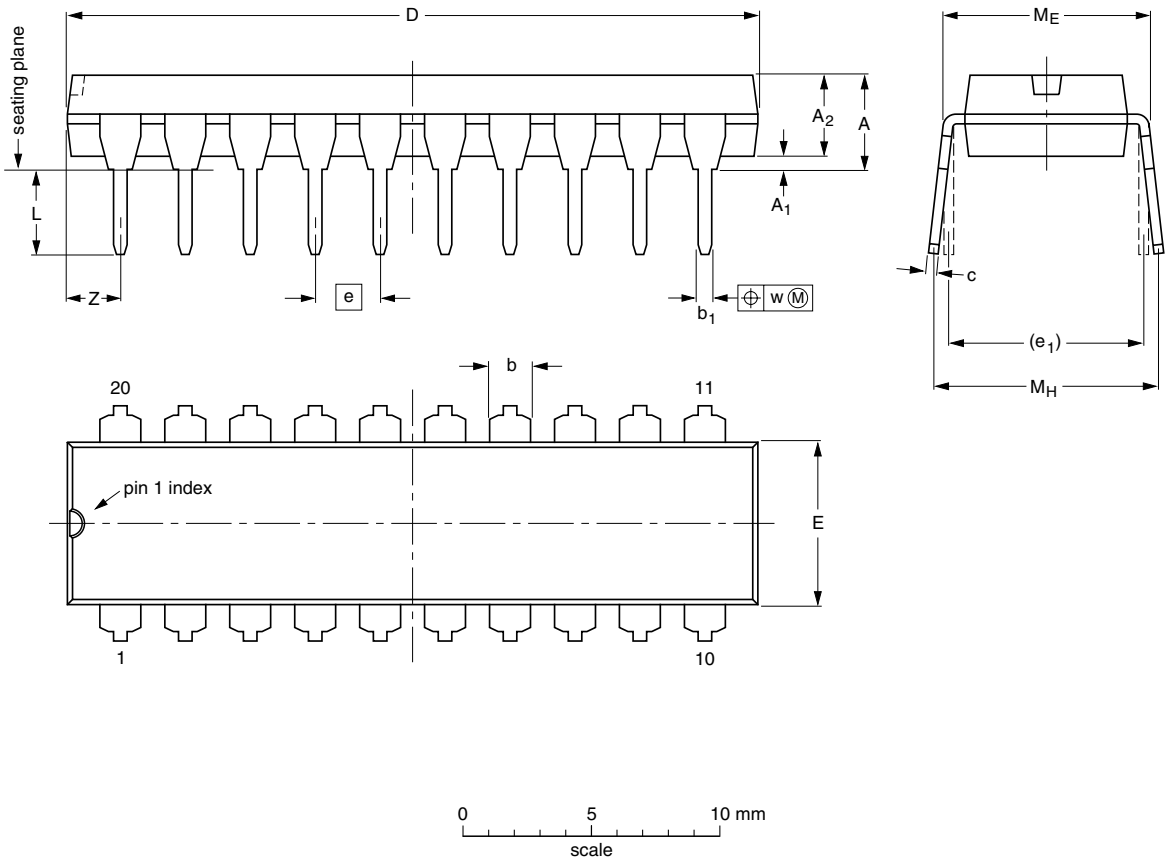
Fig 20. Typical schematic for dimmable TL application with UBA2016A (mains filter not shown)

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12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

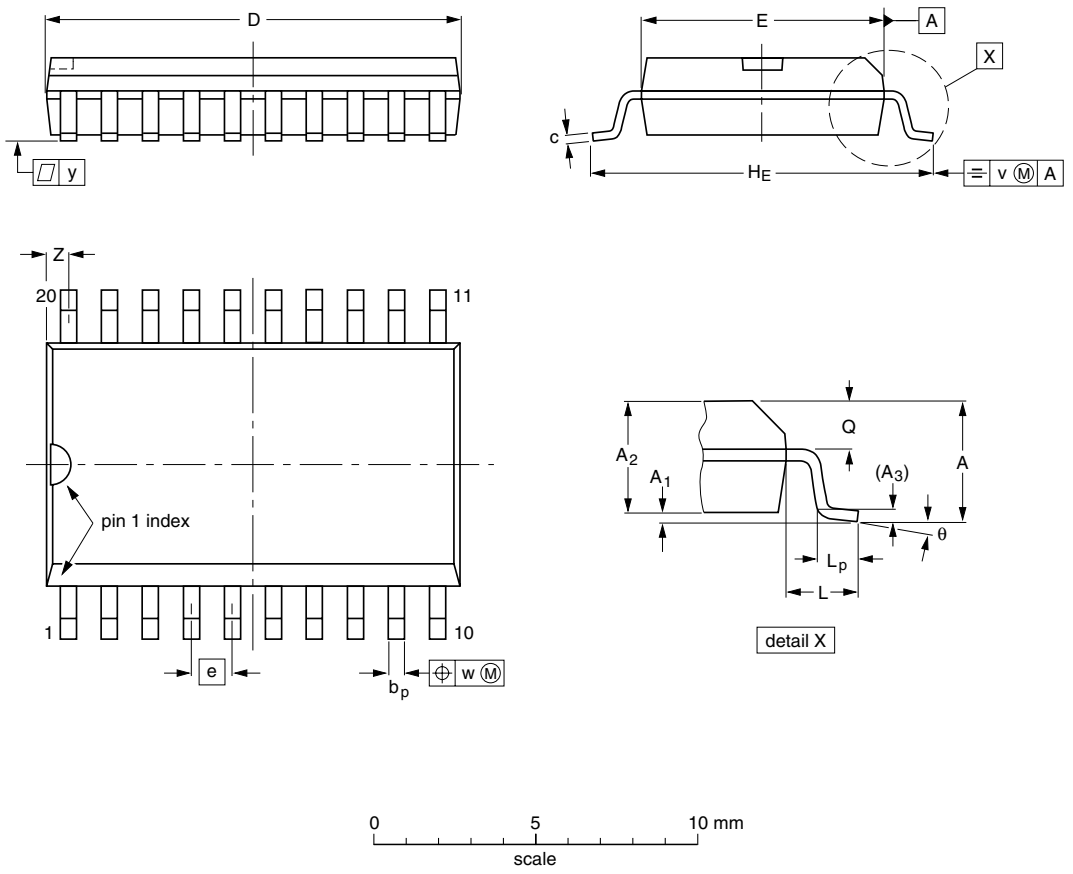
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 21. Package outline SOT146-1 (DIP20)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 22. Package outline SOT163-1 (SO20)

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13. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA2016A_15_15A v.1	20110520	Objective data sheet	-	-

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14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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