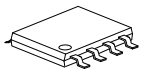
UB209B Preliminary ***CMOS IC***

BATTERY PROTECTION IC WITH CELL-BALANCE FUNCTION



TSSOP-8

■ DESCRIPTION

The UTC **UB209B** Series is a protection IC for lithium-ion/lithium polymer rechargeable batteries, including a high precision voltage detection circuit and a delay circuit.

The UTC **UB209B** Series has a transmission function and two types of cell-balance function so that users are also able to configure a protection circuit with series multi-cell.

■ FEATURES

* Settable delay time by external capacitor for output pin
* High-accuracy voltage detection circuit
* Two types of cell-balance function: charge/discharge
* Control charging, discharging, cell-balance by CTLC, CTLD pins
* Low current consumption: 8.0μA max
* Wide range of operation temperature (-40°C~+85°C)

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UB209BL-P08-R	UB209BG-P08-R	TSSOP-8	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.

UB209BG-xx-P08-R

(1)Packing Type
(2)Package Type
(3)Output Voltage Code
(4)Halogen Free

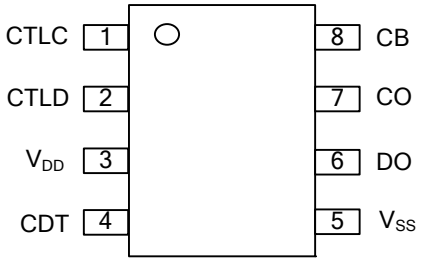
(1) R: Tape Reel
(2) P08: TSSOP-8
(3) xx: Refer to Marking Information
(4) Halogen Free, L: Lead Free

■ SERIAL CODE LIST

Model	Code	Overcharge Detection Voltage [V_{CU}](V)	Overcharge Release Voltage [V_{CL}](V)	Cell-balance Detection Voltage [V_{BU}](V)	Cell-balance Release Voltage [V_{BL}](V)	Overdischarge Detection Voltage [V_{DL}](V)	Overdischarge Release Voltage [V_{DU}](V)	Discharge Cell-balance Function
UB209B	AA	4.100	4.000	4.050	4.000	2.50	2.70	Yes
	AB	3.800	3.750	3.650	3.600	2.00	2.50	Yes
	AC	3.900	3.500	3.550	3.550	2.50	2.70	Yes
	AD	4.250	4.100	4.200	4.100	2.50	3.00	Yes
	AE	4.000	3.900	3.950	3.900	2.50	2.70	Yes
	AF	4.250	4.100	4.100	4.000	2.75	3.05	Yes
	AG	3.900	3.600	3.550	3.500	2.00	2.40	Yes
	AH	3.900	3.700	3.600	3.600	2.50	2.80	No

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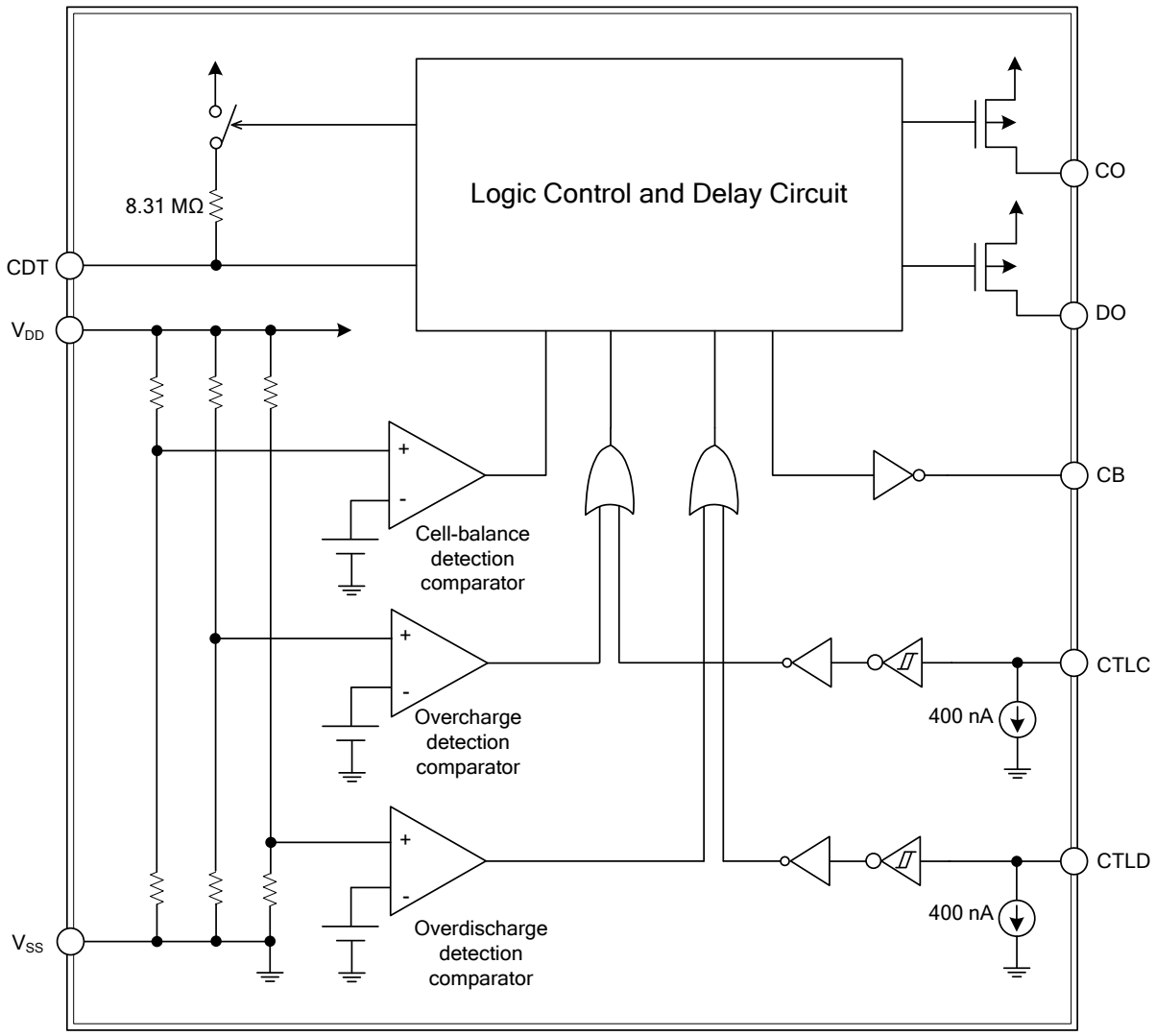
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	CTLC	Pin for charge control
2	CTLD	Pin for discharge control
3	V_{DD}	Connection pin for input positive power supply, for battery's positive voltage
4	CDT	Connection pin to capacitor for overcharge detection delay, for over discharge detection delay
5	V_{SS}	Input pin for negative power supply, Connection pin for battery's negative voltage
6	DO	Output pin for discharge control (Pch open drain output)
7	CO	Output pin for charge control (Pch open drain output)
8	CB	Output pin for cell-balance control (CMOS output)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage Between V_{DD} and V_{SS}	V_{DS}	V_{SS}-0.3~V_{SS}+12	V
CB Pin Output Voltage	V_{CB}	V_{SS}-0.3~V_{DD}+0.3	V
CDT Pin Voltage	V_{CDT}	V_{SS}-0.3~V_{DD}+0.3	V
DO Pin Output Voltage	V_{DO}	V_{DD}-24~V_{DD}+0.3	V
CO Pin Output Voltage	V_{CO}	V_{DD}-24~V_{DD}+0.3	V
CTLC Pin Input Voltage	V_{CTLC}	V_{SS}-0.3~V_{SS}+24	V
CTLD Pin Input Voltage	V_{CTLD}	V_{SS}-0.3~V_{SS}+24	V
Power Dissipation (Note 2)	P_D	700	mW
Operating Ambient Temperature	T_{OPR}	-40~+85	°C
Storage Temperature	T_{STG}	-55~+125	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. When mounted on board: 114.3mm×76.2mm×1.6mm

■ ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test circuit
Overcharge Detection Voltage	V_{CU}		V_{CU} -0.05	V_{CU}	V_{CU} +0.05	V	1
Overcharge Release Voltage	V_{CL}		V_{CL}-0.05	V_{CL}	V_{CL}+0.05	V	1
Cell-balance Detection Voltage	V_{BU}		V_{BU}-0.05	V_{BU}	V_{BU}+0.05	V	1
Cell-balance Release Voltage	V_{BL}		V_{BL}-0.05	V_{BL}	V_{BL}+0.05	V	1
Over Discharge Detection Voltage	V_{DL}		V_{DL}-0.10	V_{DL}	V_{DL}+0.10	V	1
Over Discharge Release Voltage	V_{DU}		V_{DU}-0.10	V_{DU}	V_{DU}+0.10	V	1
CDT Pin Resistance (Note 1)	R_{CDT}	V_{DS}=3.5V, V_{CDT}=0V	4.76	8.31	10.9	MΩ	2
CDT Pin Detection Voltage (Note 1)	V_{CDET}	V_{DS}=3.5V	V_{DS}×0.65	V_{DS}×0.70	V_{DS}×0.75	V	3
Operating Voltage Between VDD and VSS	V_{DSOP}	Output Voltage of CO, DO, CB Fixed	1.5		8.0	V	
CTLC Pin H Voltage	V_{CTLCH}	V_{DS}=3.5V	V_{DS}×0.55		V_{DS}×0.90	V	4
CTLD Pin H Voltage	V_{CTLDH}	V_{DS}=3.5V	V_{DS}×0.55		V_{DS}×0.90	V	4
CTLC Pin L Voltage	V_{CTLCL}	V_{DS}=3.5V	V_{DS}×0.10		V_{DS}×0.45	V	4
CTLD Pin L Voltage	V_{CTLDL}	V_{DS}=3.5V	V_{DS}×0.10		V_{DS}×0.45	V	4
Current Consumption During Operation (Note 2)	I_{OPE}	V_{DS}=3.5V		3.5	8.0	μA	5
Sink Current CTLC (Note 2)	I_{CTLCL}	V_{DS}=3.5V, V_{CTLC}=3.5V	300	400	500	nA	6
Sink Current CTLD (Note 2)	I_{CTLDL}	V_{DS}=3.5V, V_{CTLD}=3.5V	300	400	500	nA	6
Source Current CB	I_{CBH}	V_{CB}=4.0V, V_{DS}=4.5V	30			μA	7
Sink Current CB	I_{CBL}	V_{CB}=0.5V, V_{DS}=3.5V	30			μA	7
Source Current CO	I_{COH}	V_{CO}=3.0V, V_{DS}=3.5V	30			μA	7
Leakage Current CO	I_{COL}	V_{CO}=24V, V_{DS}=4.5V			0.2	μA	8
Source Current DO	I_{DOH}	V_{DO}=3.0V, V_{DS}=3.5V	30			μA	7
Leakage Current DO	I_{DOL}	V_{DO}=24V, V_{DS}=1.8V			0.2	μA	8

Notes:1. In the UTC **UB209B** Series, users are able to set delay time for the output pins. By using the following formula, delay time is calculated with the value of CDT pin's resistance in the IC (R_{CDT}) and the value of capacitor set externally at the CDT pin (C_{CDT}).

t_D [s]=-ln(1-V_{CDET} /V_{DS})×C_{CDT} [μF]×R_{CDT} [MΩ]

=-ln (1-0.7(Typ.))×C_{CDT} [μF]×8.31MΩ(Typ.)

=10.0MΩ(Typ.)×C_{CDT} [μF]

In case of the capacitance of CDT pin C_{CDT}=0.01μF, the output pin delay time t_D is calculated by using the above formula and as follows.

t_D [s]=10.0MΩ (Typ.)×0.01μF=0.1s (Typ.)

Test R_{CDT} and the CDT pin detection voltage (V_{CDET}) by test circuits shown in this datasheet after applying the power supply while pulling-down the CTLC, CTLD pins to the level of V_{DD} pin outside the IC.

2. In case of using CTLC, CTLD pins pulled-down to the level of V_{DD} pin externally, the current flows into the VSS pin (I_{SS}) is calculated by the following formula.

I_{SS}=I_{OPE}+I_{CTLCL}+I_{CTLDL}

■ TEST CIRCUIT

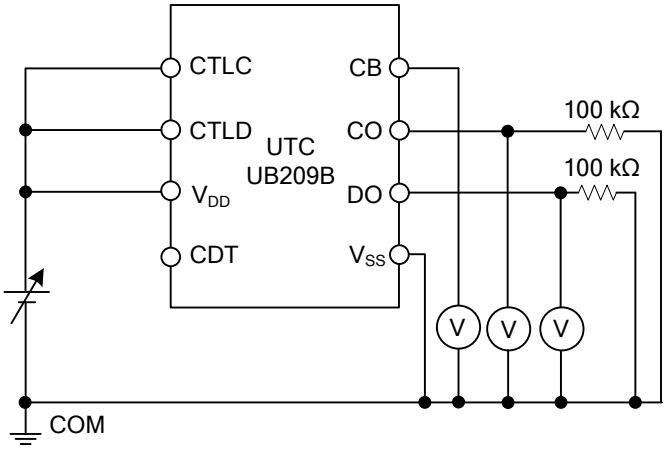


Figure 1. Test Circuit 1

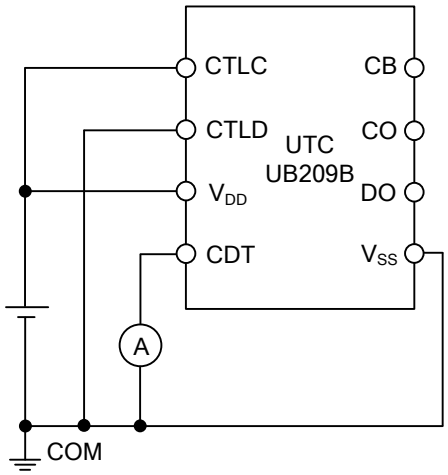


Figure 2. Test Circuit 2

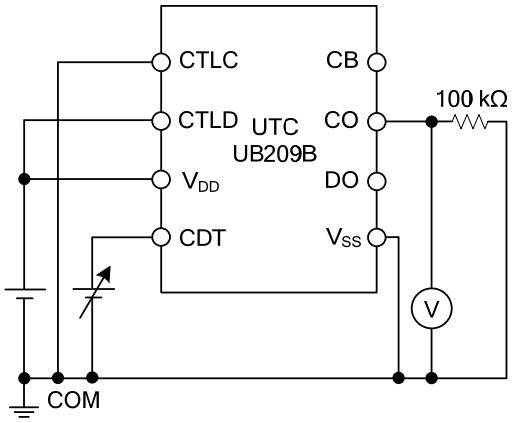


Figure 3. Test Circuit 3

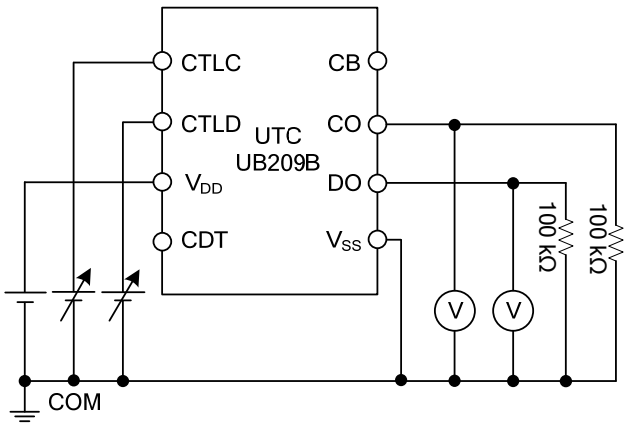


Figure 4. Test Circuit 4

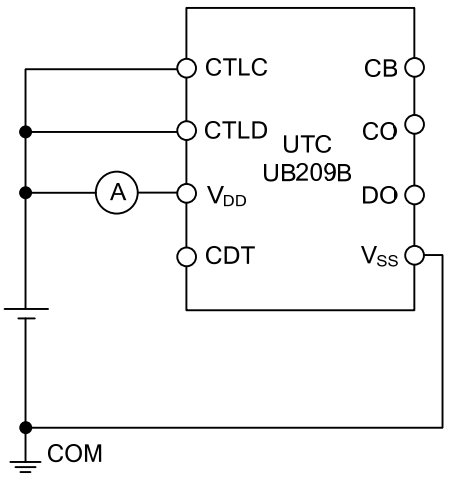


Figure 5. Test Circuit 5

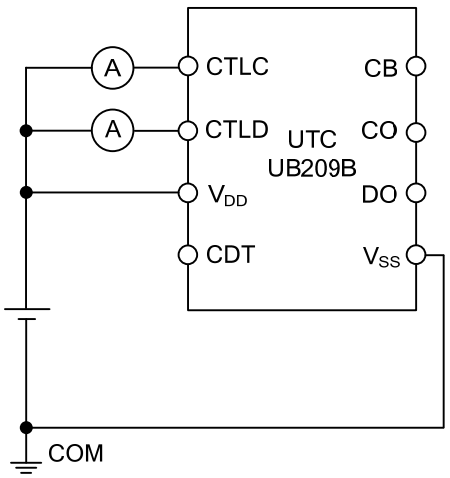


Figure 6. Test Circuit 6

■ TEST CIRCUIT(Cont.)

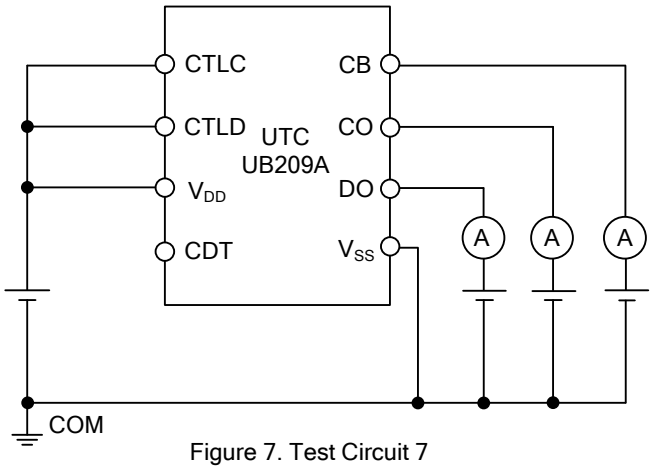


Figure 7. Test Circuit 7

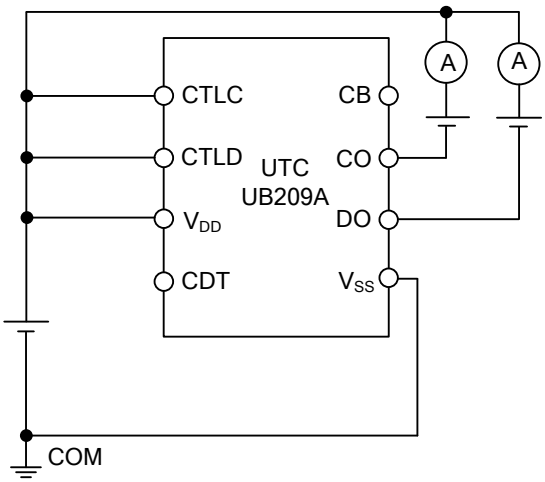


Figure 8. Test Circuit 8

■ OPERATION

Figure 9 shows the operation transition of UTC **UB209B**.

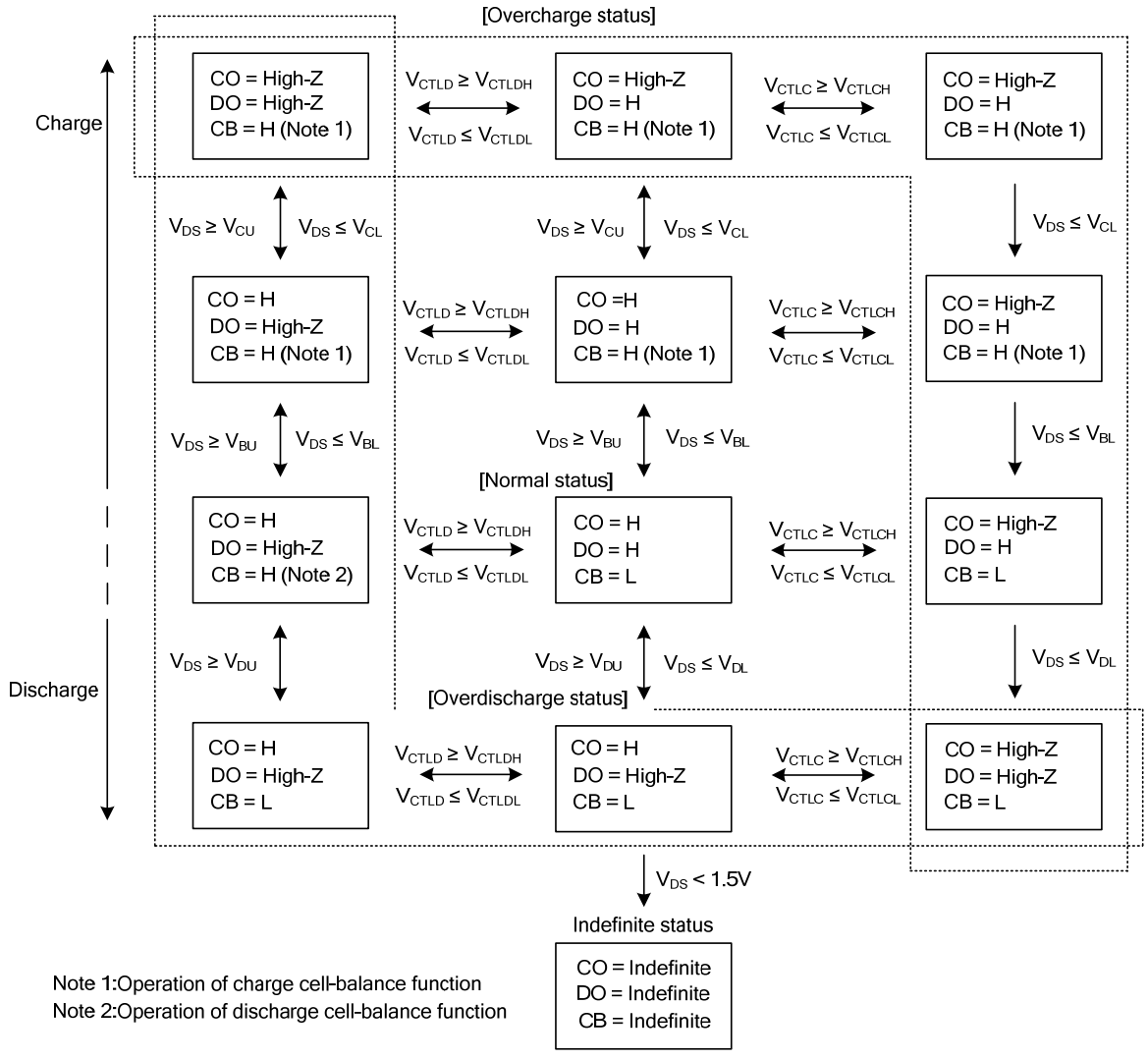


Figure 9. Operation Transition

1. Normal Status

In the UTC **UB209B**, both of CO and DO pin get the V_{DD} level; the voltage between V_{DD} and V_{SS} (V_{DS}) is more than the overdischarge detection voltage (V_{DL}), and is less than the overcharge detection voltage (V_{CU}) and respectively, the CTLC pin input voltage (V_{CTLC}) > the CTLC pin voltage "L" (V_{CTLCL}), the CTLD pin input voltage (V_{CTLD}) > the CTLD pin voltage "L" (V_{CTLDL}). This is the normal status.

2. Overcharge Status

In the UTC **UB209B**, the CO pin is in high impedance; when V_{DS} gets V_{CU} or more, or V_{CTLC} gets V_{CTLCL} or less. This is the overcharge status.

If V_{DS} gets the overcharge release voltage (V_{CL}) or less, and V_{CTLC} gets the CTLC pin voltage "H" (V_{CTLCH}) or more, the UTC **UB209B** releases the overcharge status to return to the normal status.

3. Overdischarge Status

In the UTC **UB209B**, the DO pin is in high impedance; when V_{DS} gets V_{DL} or less, or V_{CTLD} gets V_{CTLDL} or less. This is the overdischarge status.

If V_{DS} gets the overdischarge release voltage (V_{DU}) or more, and V_{CTLD} gets the CTLD pin voltage "H" (V_{CTLDH}) or more, the UTC **UB209B** releases the overdischarge status to return to the normal status.

4. Cell-balance Function

In the UTC **UB209B**, the CB pin gets the level of V_{DD} pin; when V_{DS} gets the cell-balance detection voltage (V_{BU}) or more. This is the charge cell-balance function.

If V_{DS} gets the cell-balance release voltage (V_{BL}) or less again, the UTC **UB209B** sets the CB pin the level of V_{SS} pin.

In addition, the CB pin gets the level of V_{DD} pin; when V_{DS} is more than V_{DL}, and V_{CTLD} is V_{CTLDL} or less. This is the discharge cell-balance function.

If V_{CTLD} gets V_{CTLDH} or more, or V_{DS} is V_{DL} or less again, the UTC **UB209B** sets the CB pin the level of V_{SS}.

5. Delay Circuit

In the UTC **UB209B**, users are able to set delay time which is from detection of changes in V_{DS}, V_{CTLC}, V_{CTLD} to output to the CO, DO, CB pin.

For example in the detection of overcharge status, when V_{DS} exceeds V_{CU}, or V_{CTLC} gets V_{CTLCH} or less, charging to C_{CDT} starts via R_{CDT}. If the voltage between CDT and VSS (V_{CDT}) reaches the CDT pin detection voltage (V_{CDET}), the CO pin is in high impedance. The output pin delay time t_D is calculated by the following formula.

$$t_D\,[s]=10.0M\Omega\ (Typ.)\times C_{CDT}\,[\mu F]$$

The electric charge in C_{CDT} starts to be discharged when the delay time has finished.

The delay time that users have set for the CO pin, as seen above, is settable for each output pin DO, CB.

■ TYPICAL APPLICATION CIRCUIT

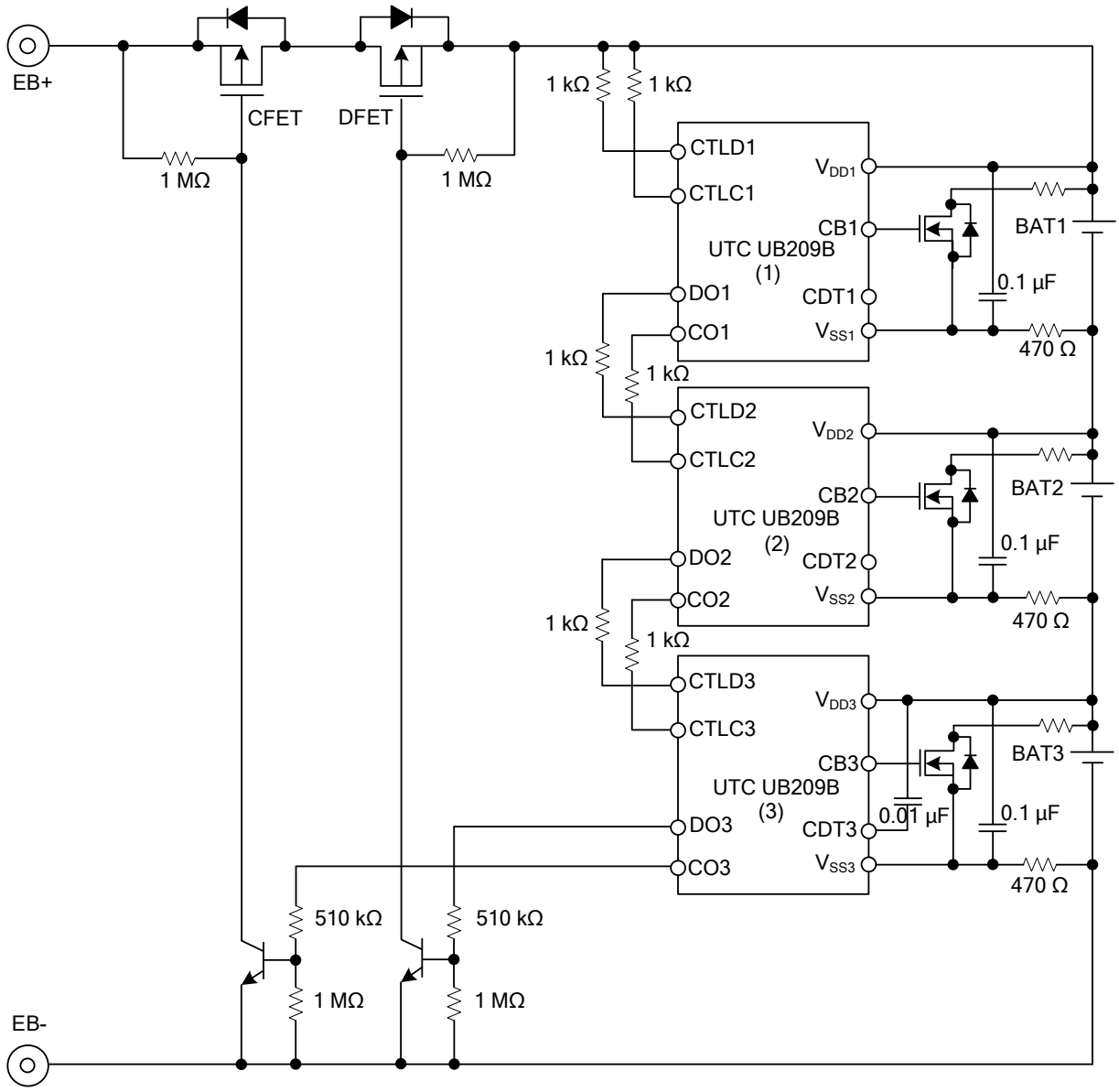


Figure 10

Caution:
1. The above constants may be changed without notice.
2. The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

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