

μ A702QB Wideband DC Amplifier

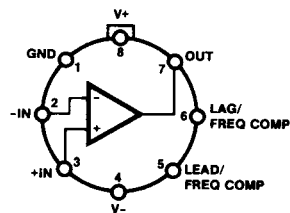
Aerospace and Defense Data Sheet
Linear Products

Description

The μ A702QB is a monolithic DC amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for use as an operational amplifier in analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.⁶

- Low Offset Voltage
- Low Offset Voltage Drift
- Wide Bandwidth
- High Slew Rate

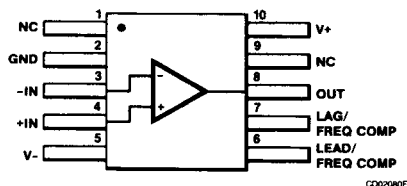
Connection Diagram 8-Lead Can (Top View)



CD002070F

Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



CD002080F

Order Information

Part No.	Case/ Finish	Package Code
μ A702HMQB	GC	Mil-M-38510, Appendix C
μ A702FMQB	HA	A-1 8-Lead Can
μ A702DMQB	CA	F-4 10-Lead Flatpak
		D-1 14-Lead DIP

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation ¹¹	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	21 V
Differential Input Voltage	±5.0 V
Input Voltage ¹²	+1.5 V to -6.0 V
Peak Output Current	50 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_1 is guaranteed by I_{B1} : $Z_1 = 2.0 V_T / I_{B1}$. $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at -55°C.
8. P_{C1} is guaranteed by I_{CC1} : $P_{C1} = (12 V)(I_{CC1}) + (6.0 V)(I_{CC1})$.
9. V_{IR} is guaranteed by the CMR test.
10. P_{C2} is guaranteed by I_{CC2} : $P_{C2} = (6.0 V)(I_{CC2}) + (3.0 V)(I_{CC2})$.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
12. For supply voltage of 21 V.

Transient Response Test Circuits

Figure 1 Unity-Gain Amplifier (Lag Compensation)

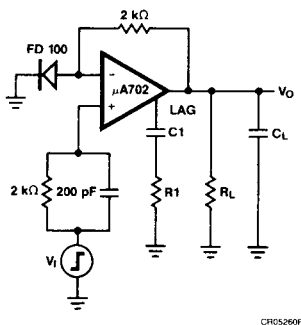
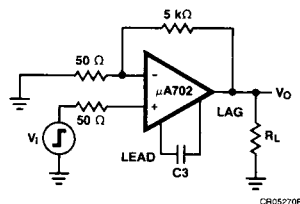


Figure 2 X100 Amplifier (Lead Compensation)



μA702QB

Electrical Characteristics $V_+ = 12\text{ V}$, $V_- = -6.0\text{ V}$, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$		2.0	mV	1	1
					3.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		10	$\mu\text{V}/^\circ\text{C}$	4	2
			$-55^\circ\text{C} \leq T_A \leq +25^\circ\text{C}$		10	$\mu\text{V}/^\circ\text{C}$	4	3
I_{IO}	Input Offset Current		$V_{CM} = 0\text{ V}$		500	nA	1	1,2
					1500	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		5.0	nA/ $^\circ\text{C}$	4	2
			$-55^\circ\text{C} \leq T_A \leq +25^\circ\text{C}$		16	nA/ $^\circ\text{C}$	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0\text{ V}$		3.2	μA	1	1
					10	μA	1	2,3
Z_I	Input Impedance ⁷			16		k Ω	1	1
I_{CC1}	Supply Current		$V_O = 0\text{ V}$		6.7	mA	1	1,2
					7.5	mA	1	3
P_{C1}	Power Consumption ⁸		$V_O = 0\text{ V}$		121	mW	1	1,2
					135	mW	1	3
CMR	Common Mode Rejection		$-4.0\text{ V} \leq V_{CM} \leq 0.5\text{ V}$, $R_S = 2.0\text{ k}\Omega$	80		dB	1	1
				70		dB	1	2,3
V_{IR}	Input Voltage Range ⁹			-4.0	0.5	V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$V_+ = 12\text{ V}$, $V_- = -6.0\text{ V}$ to $V_+ = 6.0\text{ V}$, $V_- = -3.0\text{ V}$, $R_S = 2.0\text{ k}\Omega$		200	$\mu\text{V}/\text{V}$	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$R_L = 100\text{ k}\Omega$, $V_O = \pm 5.0\text{ V}$	2.5	6.0	V/mV	1	4
				2.0	7.0	V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 100\text{ k}\Omega$	± 5.0		V	1	4,5,6
			$R_L = 10\text{ k}\Omega$	± 3.5		V	1	4,5,6
$TR(t_r)$	Transient Response (See Figure 1)	Rise Time	$C_1 = 0.01\ \mu\text{F}$, $R_1 = 20\ \Omega$, $R_L = 100\text{ k}\Omega$, $V_I = 10\text{ mV}$, $C_L = 100\text{ pF}$, $A_V = 1.0$		120	ns	2	9
$TR(o_s)$		Overshoot			50	%	2	9
$TR(t_r)$	Transient Response (See Figure 2)	Rise Time	$C_3 = 50\text{ pF}$, $R_L = 100\text{ k}\Omega$, $V_I = 1.0\text{ mV}$, $A_V = 100$		30	ns	2	9
$TR(o_s)$		Overshoot			40	%	2	9

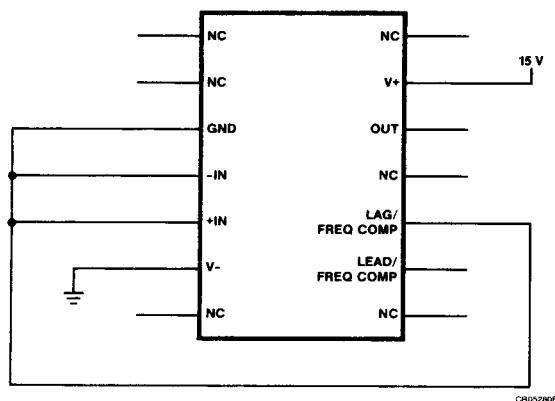
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μA702QB (Cont.)

Electrical Characteristics $V_+ = +6.0\text{ V}$, $V_- = -3.0\text{ V}$, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$		3.0	mV	1	1
				4.0	mV	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$25^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		15	$\mu\text{V}/^\circ\text{C}$	4	2
		$-55^\circ\text{C} \leq T_A \leq +25^\circ\text{C}$		15	$\mu\text{V}/^\circ\text{C}$	4	3
I_{IO}	Input Offset Current	$V_{CM} = 0\text{ V}$		500	nA	1	1,2
				1500	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		4.0	nA/ $^\circ\text{C}$	4	2
		$-55^\circ\text{C} \leq T_A \leq +25^\circ\text{C}$		13	nA/ $^\circ\text{C}$	4	3
I_{IB}	Input Bias Current	$V_{CM} = 0\text{ V}$		2.3	μA	1	1
				7.5	μA	1	2,3
Z_I	Input Impedance ⁷		22		k Ω	1	1
I_{CC2}	Supply Current	$V_O = 0\text{ V}$		3.3	mA	1	1,2
				3.9	mA	1	3
P_{c2}	Power Consumption ¹⁰	$V_O = 0\text{ V}$		30	mW	1	1,2
				35	mW	1	3
CMR	Common Mode Rejection	$-1.5\text{ V} \leq V_{CM} \leq 0.5\text{ V}$, $R_S = 2.0\text{ k}\Omega$	80		dB	1	1
			70		dB	1	2,3
V_{IR}	Input Voltage Range ⁹		-1.5	0.5	V	1	1,2,3
A_{VS}	Large Signal Voltage Gain	$R_L = 100\text{ k}\Omega$, $V_O = \pm 2.5\text{ V}$	0.6	1.5	V/mV	1	4
			0.5	1.75	V/mV	1	5,6
V_{OP}	Output Voltage Swing	$R_L = 100\text{ k}\Omega$	± 2.5		V	1	4,5,6
		$R_L = 10\text{ k}\Omega$	± 1.5		V	1	4,5,6

Primary Burn-In Circuit



Equivalent Circuit

Refer to the Fairchild Linear Data Book Commercial Section